Integrated Device Technology, Inc.

CMOS PARALLEL SyncFIFO™ (CLOCKED FIFO) 2048 x 18-BIT & 4096 x 18-BIT

ADVANCED INFORMATION
IDT72235
IDT72245

FEATURES:

- 2048 x 18-bit and 4096 x 18-bit memory array structures
- 20ns read / write cycle time
- Easily expandable in depth and width
- Read and write clocks can be asynchronous or coincident
- Dual-port zero fall-through time architecture
- Programmable almost-empty and almost-full flags
- Empty and Full flags signal FIFO status
- Half-Full flag capability in a single device configuration
- Output enable puts output data bus in high impedance state
- First device controls all flag logic in depth expansion
- Produced with advanced submicron CEMOS™ technology
- Available in a 68-lead pin grid array (PGA), and plastic leaded chip carrier (PLCC)
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT72235 and IDT72245 are very high speed, low-power first-in, first-out (FIFO) memories with clocked read and write controls. The IDT72235 has a 2048 x 18-bit memory array, while the IDT72245 has a 4096 x 18-bit memory array. These FIFOs are applicable for a wide variety of data buffering needs, such as optical disk controllers, local area networks (LANs), and interprocessor communication.

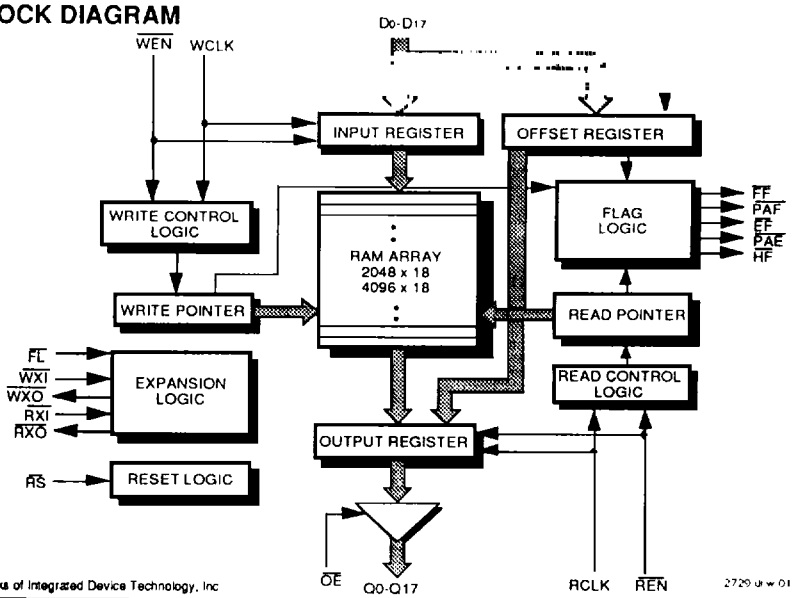
Both FIFOs have 18-bit input and output ports. The input port is controlled by a free-running clock (WCLK), and a data input enable pin ($\overline{WEN}$). Data is read into the synchronous FIFO on every clock when $\overline{WEN}$ is asserted. The output port is controlled by another clock pin (RCLK) and another enable pin ($\overline{REN}$). The read clock can be tied to the write clock for single clock operation or the two clocks can run asynchronous of one another for dual clock operation. An output enable pin ($\overline{OE}$) is provided on the read port for three-state control of the output.

The synchronous FIFOs have two fixed flags, Empty ($\overline{EF}$) and Full ($\overline{FF}$), and two programmable flags, Almost-Empty ($\overline{PAE}$) and Almost-Full ($\overline{PAF}$). The offset loading of the programmable flags is controlled by a simple state machine, and is initiated by asserting the load pin ($\overline{LD}$). A Half-Full flag ($\overline{HF}$) is available when the FIFO is used in a single device configuration.

The IDT72235 and IDT72245 are depth expandable using a daisy-chain technique. The $\overline{XI}$ and $\overline{XO}$ pins are used to expand the FIFOs. To permit programmable flags in depth expansion, the first device, indicated by setting $\overline{FL}$ to low, controls the flags.

The IDT72235/72245 is fabricated using IDT's high speed submicron CEMOS™ technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



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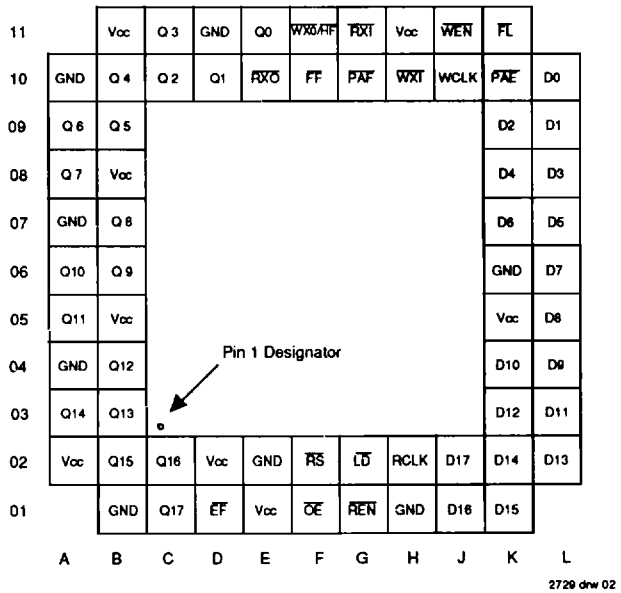
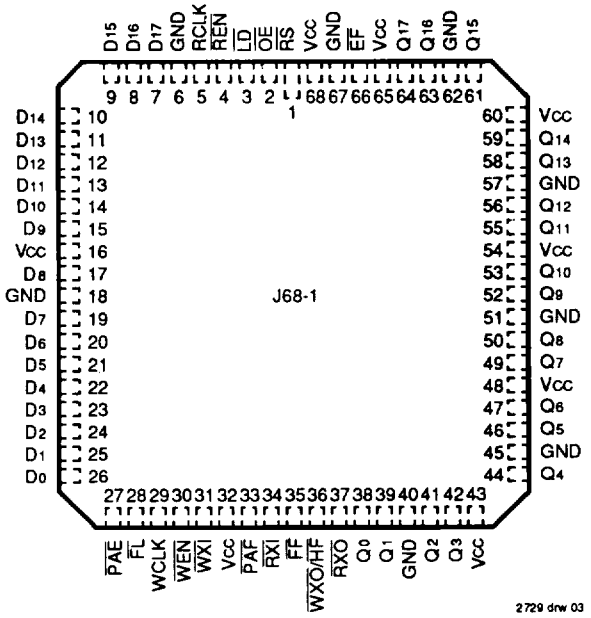
PIN CONFIGURATIONS



PGA
TOP VIEW



PLCC
TOP VIEW

PIN DESCRIPTION

Symbol	Name	I/O	Description
D_0–D_{17}	Data Inputs	I	Data inputs for a 18-bit bus.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set low, internal read and write pointers are set to the first location of the RAM array, $\overline{FF}$ and $\overline{PAF}$ go high, and $\overline{PAE}$ and $\overline{EF}$ go low. A reset is required before an initial WRITE after power-up.
WCLK	Write Clock	I	Data is written into the FIFO on a LOW-to-HIGH transition of WCLK when Write Enable $\overline{WEN}$ is asserted (LOW).
$\overline{WEN}$	Write Enable	I	When $\overline{WEN}$ is LOW, data is written into the FIFO on every LOW-to-HIGH transition of WCLK. When $\overline{WEN}$ is high, the FIFO holds the previous data. Data will not be written into the FIFO if the $\overline{FF}$ is LOW.
RCLK	Read Clock	I	Data is read from the FIFO on a LOW-to-HIGH transition of RCLK when Read Enable $\overline{REN}$ is asserted (LOW).
$\overline{REN}$	Read Enable	I	When $\overline{REN}$ is LOW, data is read from the FIFO on every LOW-to-HIGH transition of RCLK. When $\overline{REN}$ is high, the output register holds the previous data. Data will not be read from the FIFO if the $\overline{EF}$ is LOW.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is LOW, the data output bus is active. If $\overline{OE}$ is HIGH, the output data bus will be in a high impedance state.
$\overline{LD}$	Load	I	When $\overline{LD}$ is LOW, data on the inputs D_0–D_{15} is written to the offset and depth registers on the LOW-to-HIGH transition of the WCLK, when $\overline{WEN}$ is LOW. When $\overline{LD}$ is LOW, data on the outputs Q_0–Q_{15} is read from the offset and depth registers on the LOW-to-HIGH transition of the RCLK, when $\overline{REN}$ is LOW.
$\overline{FL}$	First Load	I	In the single device or width expansion configuration, $\overline{FL}$ is grounded. In the depth expansion configuration, $\overline{FL}$ is grounded on the first device (first load device) and set to high for all other devices in the daisy chain.
$\overline{WXI}$	Write Expansion Input	I	In the single device or width expansion configuration, $\overline{WXI}$ is grounded. In the depth expansion configuration, $\overline{WXI}$ is connected to $\overline{WXO}$ (Write Expansion Out) of the previous device.
$\overline{RXI}$	Read Expansion Input	I	In the single device or width expansion configuration, $\overline{RXI}$ is grounded. In the depth expansion configuration, $\overline{RXI}$ is connected to $\overline{RXO}$ (Read Expansion Out) of the previous device.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ is LOW, the FIFO is empty and further data reads from the output are inhibited. When $\overline{EF}$ is HIGH, the FIFO is not empty. $\overline{EF}$ is synchronized to RCLK.
$\overline{PAE}$	Programmable Almost-Empty Flag	O	When $\overline{PAE}$ is LOW, the FIFO is almost empty based on the offset programmed into the FIFO. The default offset at reset is 1/8 full.
$\overline{PAF}$	Programmable Almost-Full Flag	O	When $\overline{PAF}$ is LOW, the FIFO is almost full based on the offset programmed into the FIFO. The default offset at reset is 7/8 full.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ is LOW, the FIFO is full and further data writes into the input are inhibited. When $\overline{FF}$ is HIGH, the FIFO is not full. $\overline{FF}$ is synchronized to WCLK.
$\overline{WXO/HF}$	Write Expansion Out/Half-Full Flag	O	In the single device or width expansion configuration, the device is more than half full when $\overline{HF}$ is LOW. In the depth expansion configuration, a pulse is sent from $\overline{WXO}$ to $\overline{WXI}$ of the next device when the last location in the FIFO is written.
$\overline{RXO}$	Read Expansion Out	O	In the depth expansion configuration, a pulse is sent from $\overline{RXO}$ to $\overline{RXI}$ of the next device when the last location in the FIFO is read.
Q_0–Q_{17}	Data Outputs	O	Data outputs for a 18-bit bus.
VCC	Power		Eight +5 volt power supply pins.
GND	Ground		Eight 0 volt ground pins.

2729 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2729 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maimum rating conditions for extended periods may affect reliabilty.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CCC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	—	—	V
V_{IH}	Input High Voltage Military	2.2	—	—	V
V_{IL}(1)	Input Low Voltage Commercial & Military	—	—	0.8	V

NOTE: 2729 tbl 03

1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = –55°C to +125°C)

Symbol	Parameter	IDT72235 IDT72235 Commercial t_{CLK} = 20, 25, 50ns			IDT72245 IDT72245 Military t_{CLK} = 25, 30, 50ns			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{LI}(1)	Input Leakage Current (any input)	–1	—	1	–10	—	10	µA
I_{LO}(2)	Output Leakage Current	–10	—	10	–10	—	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OH} = –2 mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage, I_{OL} = 8 mA	—	—	0.4	—	—	0.4	V
I_{CC1}(3)	Active Power Supply Current	—	—	250	—	—	300	mA
I_{CC2}(3)	Average Standby Current (All Input = VCC – 0.2V, except RCLK and WCLK which are free-running)	—	—	60	—	—	75	mA

NOTES: 2729 tbl 04

1. Measurements with 0.4 ≤ V_{IN} ≤ V_{OUT}.
2. $\overline{OE}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. Tested at f = 20 MHz.

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AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = −55°C to +125°C)

Symbol	Parameter	IDT72235L20 IDT72245L20 Com'l.		IDT72235L25 IDT72245L25 Com'l. & Mil.		IDT72235L30 IDT72245L30 Mil.		IDT72235L50 IDT72245L50 Com'l. & Mil.		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
fS	Clock Cycle Frequency	—	50	—	40	—	33	—	20	MHz
tA	Data Access Time	2	14	3	15	3	18	3	25	ns
tCLK	Clock Cycle Time	20	—	25	—	30	—	50	—	ns
tCLKH	Clock High Time	8	—	10	—	12	—	20	—	ns
tCLKL	Clock Low Time	9	—	10	—	12	—	20	—	ns
tDG	Data Set-up Time	5	—	6	—	7	—	10	—	ns
tDH	Data Hold Time	1	—	1	—	1	—	2	—	ns
tENS	Enable Set-up Time	5	—	6	—	7	—	10	—	ns
tENH	Enable Hold Time	1	—	1	—	1	—	2	—	ns
tRS	Reset Pulse Width[1]	20	—	25	—	30	—	50	—	ns
tRSS	Reset Set-up Time[2]	12	—	15	—	18	—	30	—	ns
tRSF	Reset to Flag and Output Time	—	20	—	25	—	30	—	50	ns
tOLZ	Output Enable to Output in Low Z[2]	0	—	0	—	0	—	0	—	ns
tOE	Output Enable to Output Valid	—	9	—	12	—	15	—	20	ns
tOHZ	Output Enable to Output in High Z[2]	1	9	1	12	1	15	1	20	ns
tWFF	Write Clock to Full Flag	—	14	—	16	—	18	—	30	ns
tREF	Read Clock to Empty Flag	—	12	—	15	—	18	—	30	ns
tPAF	Clock to Programmable Almost-Full Flag	—	20	—	22	—	24	—	35	ns
tPAE	Clock to Programmable Almost-Empty Flag	—	20	—	22	—	24	—	35	ns
tHF	Clock to Half-Full Flag	—	22	—	22	—	24	—	35	ns
tXO	Clock to Expansion Out	—	12	—	15	—	18	—	30	ns
tXI	Expansion In Pulse Width	8	—	10	—	12	—	20	—	ns
tXIS	Expansion In Set-Up Time	8	—	10	—	12	—	20	—	ns
tSKEW1	Skew time between Read Clock & Write Clock for Full Flag	14	—	16	—	18	—	20	—	ns
tSKEW2	Skew time between Read Clock & Write Clock for Empty Flag	14	—	16	—	18	—	20	—	ns

2729 tbl 05

NOTES:

1. Pulse widths less than minimum values are not allowed.
2. Values guaranteed by design, not currently tested.