

**Document Title****1Mx8 bit Low Power and Low Voltage CMOS Static RAM****Revision History**

| <b><u>Revision No.</u></b> | <b><u>History</u></b>                                                                                                                                                                                               | <b><u>Draft Date</u></b> | <b><u>Remark</u></b> |
|----------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|----------------------|
| 0.0                        | Initial draft                                                                                                                                                                                                       | June 22, 1999            | Advance              |
| 1.0                        | Finalize<br>- Adopt New Code system.<br>- Improve $V_{IN}$ , $V_{OUT}$ max. on ABSOLUTE MAXIMUM RATINGS from 7.0V to $V_{CC}+0.5V$ .<br>- Change $I_{CC}$ : from 12 to 10mA<br>- Change $I_{CC1}$ : from 10 to 12mA | February 29, 2000        | Final                |

---

The attached datasheets are provided by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications and products. SAMSUNG Electronics will answer to your questions about device. If you have any questions, please contact the SAMSUNG branch offices.

---

## 1Mx8 bit Low Power and Low Voltage CMOS Static RAM

### FEATURES

- Process Technology: TFT
- Organization: 1M x8
- Power Supply Voltage: 4.5~5.5V
- Low Data Retention Voltage: 2.0V(Min)
- Three state output and TTL Compatible
- Package Type: 44-TSOP2-400F/R

### GENERAL DESCRIPTION

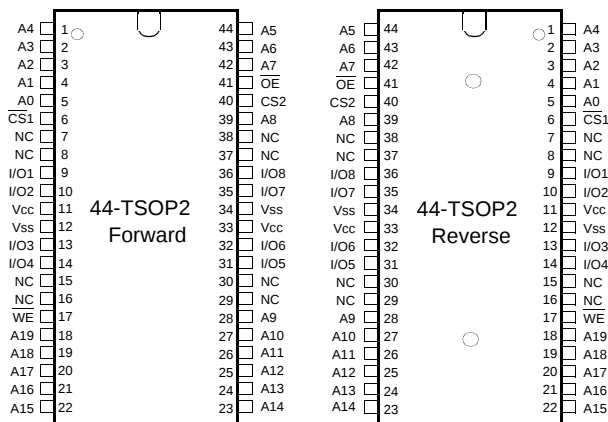
The K6T8008C2M families are fabricated by SAMSUNG's advanced CMOS process technology. The families support industrial operating temperature ranges for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

### PRODUCT FAMILY

| Product Family | Operating Temperature | Vcc Range | Speed                  | Power Dissipation   |                       | PKG Type        |
|----------------|-----------------------|-----------|------------------------|---------------------|-----------------------|-----------------|
|                |                       |           |                        | Standby (Isb1, Max) | Operating (Icc2, Max) |                 |
| K6T8008C2M-B   | Commercial(0~70°C)    | 4.5~5.5V  | 55 <sup>1)</sup> /70ns | 50μA                | 70mA                  | 44-TSOP2-400F/R |
| K6T8008C2M-F   | Industrial(-40~85°C)  |           |                        | 80μA                |                       |                 |

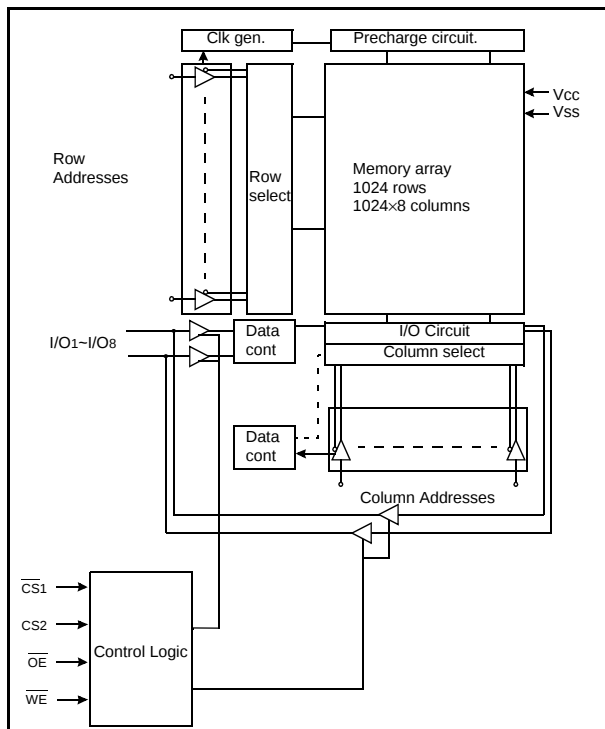
1. The parameter is measured with 50pF test load.

### PIN DESCRIPTION



| Name      | Function            | Name   | Function       |
|-----------|---------------------|--------|----------------|
| CS1, CS2  | Chip Select Inputs  | Vcc    | Power          |
| OE        | Output Enable Input | Vss    | Ground         |
| WE        | Write Enable Input  | A0~A19 | Address Inputs |
| I/O1~I/O8 | Data Inputs/Outputs | NC     | No Connect     |

### FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS CO., LTD. reserves the right to change products and specifications without notice.

## PRODUCT LIST

| Commercial Temperature Products(0~70°C) |                                                          | Industrial Temperature Products(-40~85°C) |                                                          |
|-----------------------------------------|----------------------------------------------------------|-------------------------------------------|----------------------------------------------------------|
| Part Name                               | Function                                                 | Part Name                                 | Function                                                 |
| K6T8008C2M-TB55<br>K6T8008C2M-TB70      | 44-TSOP2-F, 55ns, 5.0V, LL<br>44-TSOP2-F, 70ns, 5.0V, LL | K6T8008C2M-TF55<br>K6T8008C2M-TF70        | 44-TSOP2-F, 55ns, 5.0V, LL<br>44-TSOP2-F, 70ns, 5.0V, LL |
| K6T8008C2M-RB55<br>K6T8008C2M-RB70      | 44-TSOP2-R, 55ns, 5.0V, LL<br>44-TSOP2-R, 70ns, 5.0V, LL | K6T8008C2M-RF55<br>K6T8008C2M-RF70        | 44-TSOP2-R, 55ns, 5.0V, LL<br>44-TSOP2-R, 70ns, 5.0V, LL |

## FUNCTIONAL DESCRIPTION

| $\overline{CS}_1$ | CS <sub>2</sub> | $\overline{OE}$ | $\overline{WE}$ | I/O <sub>1-8</sub> | Mode            | Power   |
|-------------------|-----------------|-----------------|-----------------|--------------------|-----------------|---------|
| H                 | X               | X               | X               | High-Z             | Deselected      | Standby |
| X                 | L               | X               | X               | High-Z             | Deselected      | Standby |
| L                 | H               | H               | H               | High-Z             | Output Disabled | Active  |
| L                 | H               | L               | H               | Dout               | Read            | Active  |
| L                 | H               | X               | L               | Din                | Write           | Active  |

Note: X means don't care. (Must be low or high state)

ABSOLUTE MAXIMUM RATINGS<sup>1)</sup>

| Item                                  | Symbol                             | Ratings                       | Unit | Remark       |
|---------------------------------------|------------------------------------|-------------------------------|------|--------------|
| Voltage on any pin relative to Vss    | V <sub>IN</sub> , V <sub>OUT</sub> | -0.5 to V <sub>CC</sub> +0.5V | V    | -            |
| Voltage on Vcc supply relative to Vss | V <sub>CC</sub>                    | -0.3 to 7.0                   | V    | -            |
| Power Dissipation                     | P <sub>D</sub>                     | 1.0                           | W    | -            |
| Storage temperature                   | T <sub>STG</sub>                   | -65 to 150                    | °C   | -            |
| Operating Temperature                 | T <sub>A</sub>                     | 0 to 70                       | °C   | K6T8008C2M-B |
|                                       |                                    | -40 to 85                     | °C   | K6T8008C2M-F |

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS<sup>1)</sup>

| Item               | Symbol          | Product           | Min                | Typ | Max                                | Unit |
|--------------------|-----------------|-------------------|--------------------|-----|------------------------------------|------|
| Supply voltage     | V <sub>CC</sub> | K6T8008C2M Family | 4.5                | 5.0 | 5.5                                | V    |
| Ground             | V <sub>SS</sub> | All Family        | 0                  | 0   | 0                                  | V    |
| Input high voltage | V <sub>IH</sub> | K6T8008C2M Family | 2.2                | -   | V <sub>CC</sub> +0.5 <sup>2)</sup> | V    |
| Input low voltage  | V <sub>IL</sub> | K6T8008C2M Family | -0.5 <sup>3)</sup> | -   | 0.8                                | V    |

Note:

1. Commercial Product: T<sub>A</sub>=0 to 70°C, otherwise specified.Industrial Product: T<sub>A</sub>=-40 to 85°C, otherwise specified.2. Overshoot: V<sub>CC</sub>+3.0V in case of pulse width ≤30ns.

3. Undershoot: -3.0V in case of pulse width ≤30ns.

4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE<sup>1)</sup> (f=1MHz, T<sub>A</sub>=25°C)

| Item                     | Symbol          | Test Condition      | Min | Max | Unit |
|--------------------------|-----------------|---------------------|-----|-----|------|
| Input capacitance        | C <sub>IN</sub> | V <sub>IN</sub> =0V | -   | 8   | pF   |
| Input/Output capacitance | C <sub>IO</sub> | V <sub>IO</sub> =0V | -   | 10  | pF   |

1. Capacitance is sampled, not 100% tested.

## DC AND OPERATING CHARACTERISTICS

| Item                           | Symbol           | Test Conditions                                                                                                                                                                  | Min          | Typ | Max | Unit |    |
|--------------------------------|------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|-----|-----|------|----|
| Input leakage current          | I <sub>LI</sub>  | V <sub>IN</sub> =V <sub>SS</sub> to V <sub>CC</sub>                                                                                                                              | -1           | -   | 1   | μA   |    |
| Output leakage current         | I <sub>LO</sub>  | $\overline{CS}_1=V_{IH}$ , $\overline{CS}_2=V_{IL}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ , V <sub>IO</sub> =V <sub>SS</sub> to V <sub>CC</sub>                    | -1           | -   | 1   | μA   |    |
| Operating power supply current | I <sub>CC</sub>  | I <sub>IO</sub> =0mA, $\overline{CS}_1=V_{IL}$ , $\overline{CS}_2=V_{IH}$ , $\overline{WE}=V_{IH}$ , V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>                         | -            | -   | 10  | mA   |    |
| Average operating current      | I <sub>CC1</sub> | Cycle time=1μs, 100%duty, I <sub>IO</sub> =0mA, $\overline{CS}_1\leq 0.2V$ , $\overline{CS}_2\geq V_{CC}-0.2V$ , V <sub>IN</sub> ≤0.2V or V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V | -            | -   | 12  | mA   |    |
|                                | I <sub>CC2</sub> | Cycle time=Min, I <sub>IO</sub> =0mA, 100% duty, $\overline{CS}_1=V_{IL}$ , $\overline{CS}_2=V_{IH}$ , V <sub>IN</sub> =V <sub>IL</sub> or V <sub>IH</sub>                       | -            | -   | 70  | mA   |    |
| Output low voltage             | V <sub>OL</sub>  | I <sub>OL</sub> = 2.1mA                                                                                                                                                          | -            | -   | 0.4 | V    |    |
| Output high voltage            | V <sub>OH</sub>  | I <sub>OH</sub> = -1.0mA                                                                                                                                                         | 2.4          | -   | -   | V    |    |
| Standby Current(TTL)           | I <sub>SB</sub>  | $\overline{CS}_1=V_{IH}$ , $\overline{CS}_2=V_{IL}$ , Other inputs=V <sub>IH</sub> or V <sub>IL</sub>                                                                            | -            | -   | 3   | mA   |    |
| Standby Current(CMOS)          | I <sub>SB1</sub> | $\overline{CS}\geq V_{CC}-0.2V$ , Other inputs=0~V <sub>CC</sub>                                                                                                                 | K6T8008C2M-B | -   | -   | 50   | μA |
|                                |                  |                                                                                                                                                                                  | K6T8008C2M-F | -   | -   | 80   |    |

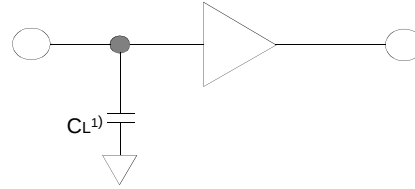
## AC OPERATING CONDITIONS

## TEST CONDITIONS (Test Load and Input/Output Reference)

Input pulse level: 0.4 to 2.2V

Input rising and falling time: 5ns

Input and output reference voltage: 1.5V

Output load (see right):  $C_L = 100\text{pF} + 1\text{TTL}$  $C_L = 50\text{pF} + 1\text{TTL}$ 

1. Including scope and jig capacitance

AC CHARACTERISTICS ( $V_{CC} = 4.5 \sim 5.5\text{V}$ , Commercial product:  $T_A = 0$  to  $70^\circ\text{C}$ , Industrial product:  $T_A = -40$  to  $85^\circ\text{C}$ )

| Parameter List |                                 | Symbol           | Speed Bins |     |      |     | Units |
|----------------|---------------------------------|------------------|------------|-----|------|-----|-------|
|                |                                 |                  | 55ns       |     | 70ns |     |       |
|                |                                 |                  | Min        | Max | Min  | Max |       |
| Read           | Read Cycle Time                 | t <sub>RC</sub>  | 55         | -   | 70   | -   | ns    |
|                | Address Access Time             | t <sub>AA</sub>  | -          | 55  | -    | 70  | ns    |
|                | Chip Select to Output           | t <sub>CO</sub>  | -          | 55  | -    | 70  | ns    |
|                | Output Enable to Valid Output   | t <sub>OE</sub>  | -          | 25  | -    | 35  | ns    |
|                | Chip Select to Low-Z Output     | t <sub>LZ</sub>  | 10         | -   | 10   | -   | ns    |
|                | Output Enable to Low-Z Output   | t <sub>OLZ</sub> | 5          | -   | 5    | -   | ns    |
|                | Chip Disable to High-Z Output   | t <sub>HZ</sub>  | 0          | 20  | 0    | 25  | ns    |
|                | Output Disable to High-Z Output | t <sub>OHZ</sub> | 0          | 20  | 0    | 25  | ns    |
|                | Output Hold from Address Change | t <sub>OH</sub>  | 10         | -   | 10   | -   | ns    |
| Write          | Write Cycle Time                | t <sub>WC</sub>  | 55         | -   | 70   | -   | ns    |
|                | Chip Select to End of Write     | t <sub>CW</sub>  | 45         | -   | 60   | -   | ns    |
|                | Address Set-up Time             | t <sub>AS</sub>  | 0          | -   | 0    | -   | ns    |
|                | Address Valid to End of Write   | t <sub>AW</sub>  | 45         | -   | 60   | -   | ns    |
|                | Write Pulse Width               | t <sub>WP</sub>  | 40         | -   | 50   | -   | ns    |
|                | Write Recovery Time             | t <sub>WR</sub>  | 0          | -   | 0    | -   | ns    |
|                | Write to Output High-Z          | t <sub>WHZ</sub> | 0          | 20  | 0    | 20  | ns    |
|                | Data to Write Time Overlap      | t <sub>DW</sub>  | 25         | -   | 30   | -   | ns    |
|                | Data Hold from Write Time       | t <sub>DH</sub>  | 0          | -   | 0    | -   | ns    |
|                | End Write to Output Low-Z       | t <sub>OW</sub>  | 5          | -   | 5    | -   | ns    |

## DATA RETENTION CHARACTERISTICS

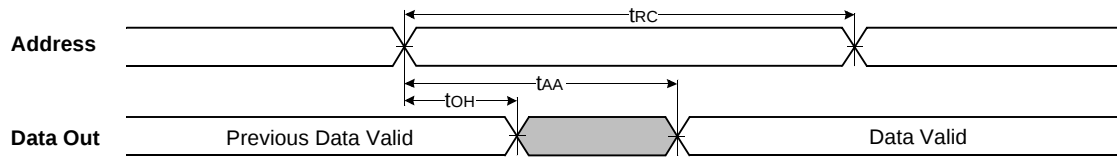
| Item                               | Symbol           | Test Condition                                            | Min | Typ | Max               | Unit |
|------------------------------------|------------------|-----------------------------------------------------------|-----|-----|-------------------|------|
| V <sub>CC</sub> for data retention | V <sub>DR</sub>  | $\overline{CS}_1 \geq V_{CC} - 0.2V^{(1)}$                | 2.0 | -   | 5.5               | V    |
| Data retention current             | I <sub>DR</sub>  | $V_{CC} = 3.0V, \overline{CS}_1 \geq V_{CC} - 0.2V^{(1)}$ | -   | -   | 20 <sup>(2)</sup> | μA   |
| Data retention set-up time         | t <sub>SDR</sub> | See data retention waveform                               | 0   | -   | -                 | ms   |
| Recovery time                      | t <sub>RDR</sub> |                                                           | 5   | -   | -                 |      |

1.  $\overline{CS}_1 \geq V_{CC} - 0.2V, \overline{CS}_2 \geq V_{CC} - 0.2V$  ( $\overline{CS}_1$  controlled) or  $\overline{CS}_2 \geq V_{CC} - 0.2V$  ( $\overline{CS}_2$  controlled).

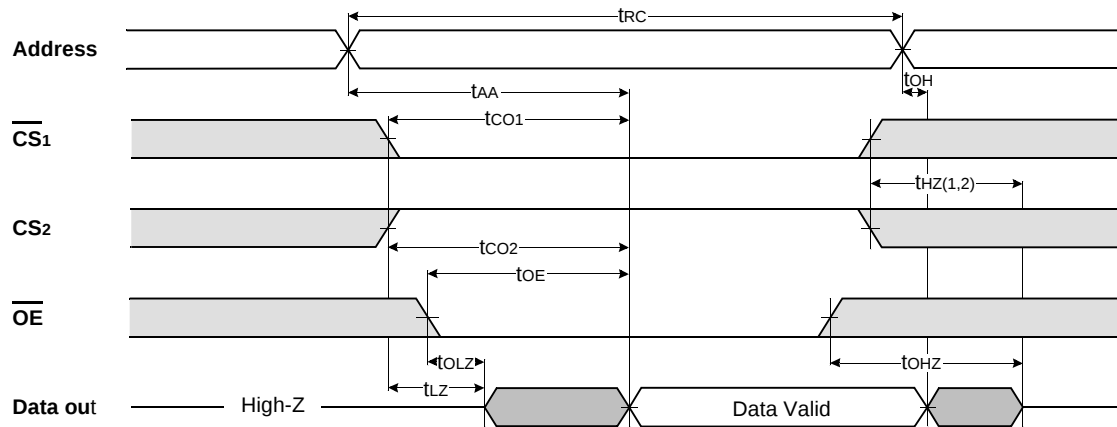
2. Industrial product = 30μA

## TIMMING DIAGRAMS

**TIMING WAVEFORM OF READ CYCLE(1)** (Address Controlled,  $\overline{CS_1}=\overline{OE}=V_{IL}$ ,  $CS_2=\overline{WE}=V_{IH}$ )



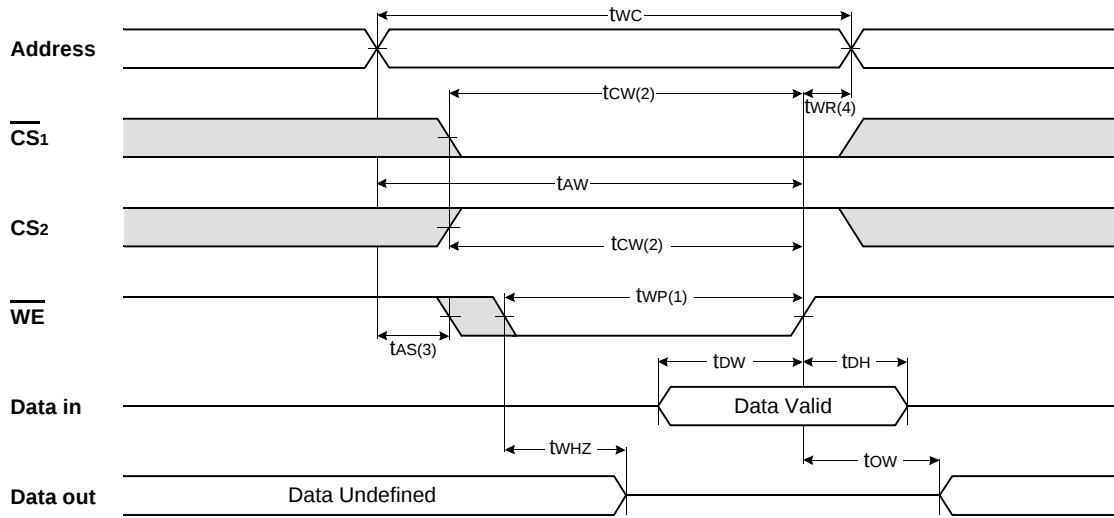
**TIMING WAVEFORM OF READ CYCLE(2)** ( $\overline{WE}=V_{IH}$ )



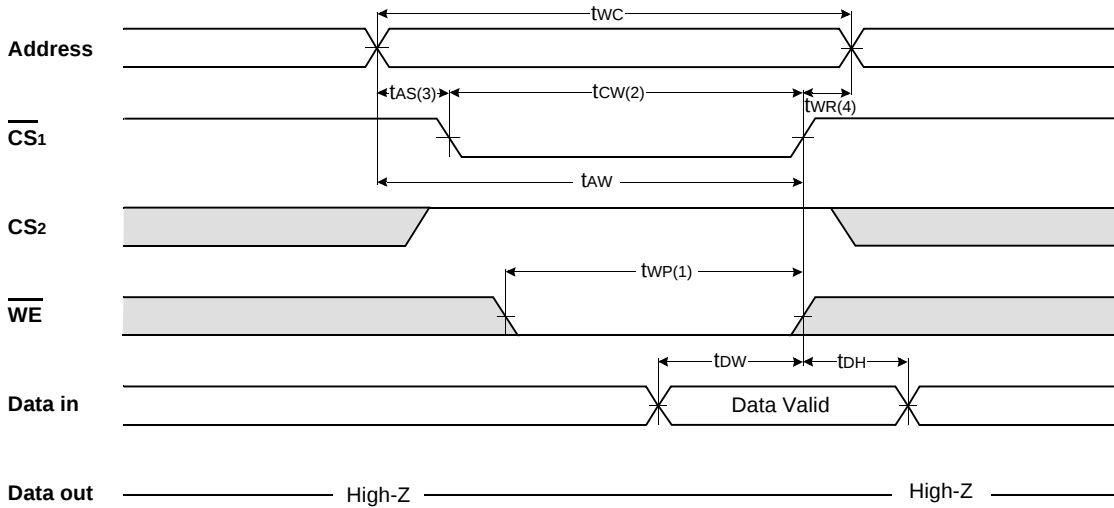
### NOTES (READ CYCLE)

1.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition,  $t_{HZ}(\text{Max.})$  is less than  $t_{LZ}(\text{Min.})$  both for a given device and from device to device interconnection.

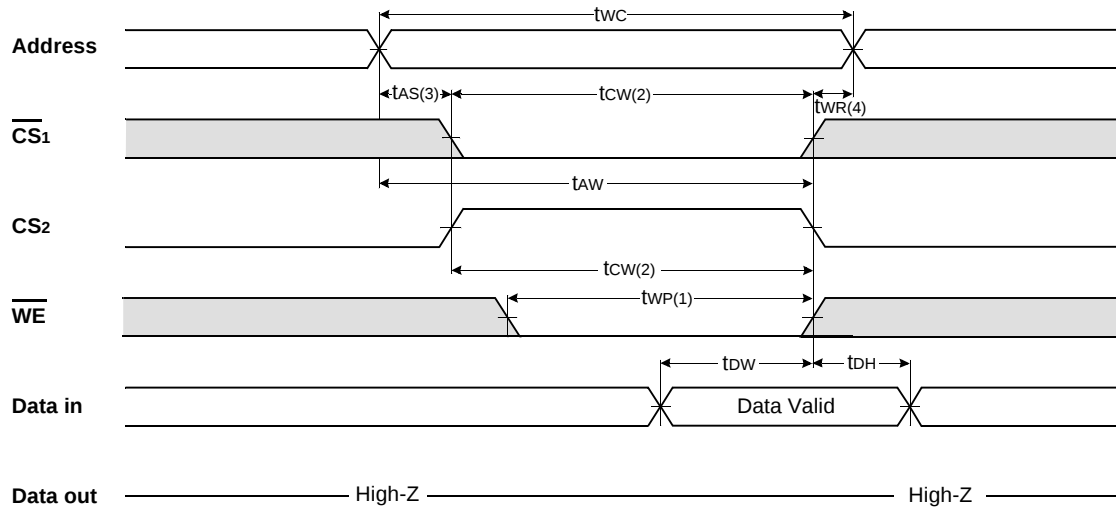
TIMING WAVEFORM OF WRITE CYCLE(1) ( $\overline{\text{WE}}$  Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ( $\overline{\text{CS1}}$  Controlled)



## TIMING WAVEFORM OF WRITE CYCLE(3) (CS<sub>2</sub> Controlled)

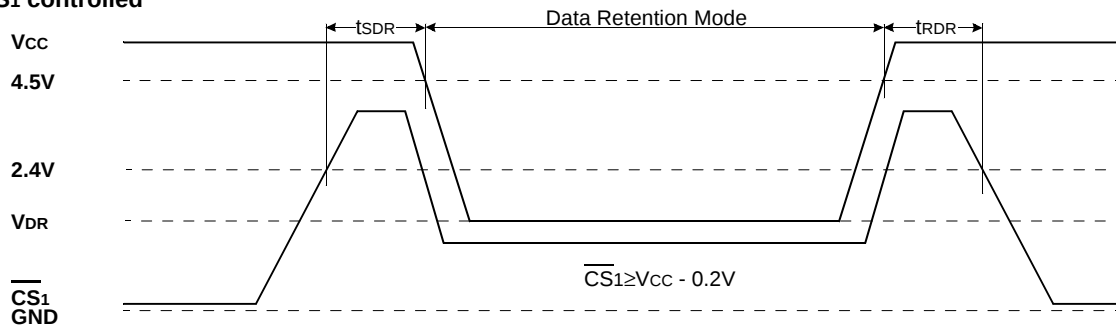


### NOTES (WRITE CYCLE)

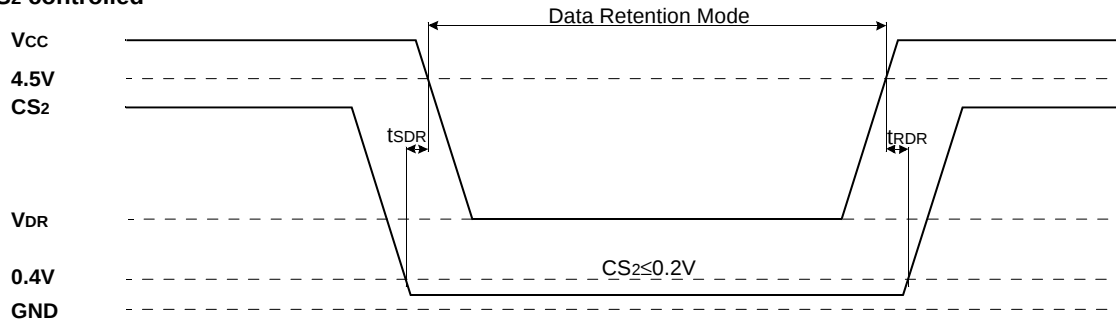
1. A write occurs during the overlap of a low  $\overline{CS_1}$ , a high CS<sub>2</sub> and a low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CS_1}$  goes low, CS<sub>2</sub> going high and WE going low : A write ends at the earliest transition among CS<sub>1</sub> going high, CS<sub>2</sub> going low and WE going high, tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the CS<sub>1</sub> going low or CS<sub>2</sub> going high to the end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR1 applied in case a write ends as  $\overline{CS_1}$  or  $\overline{WE}$  going high tWR2 applied in case a write ends as CS<sub>2</sub> going to low.

## DATA RETENTION WAVE FORM

### CS<sub>1</sub> controlled



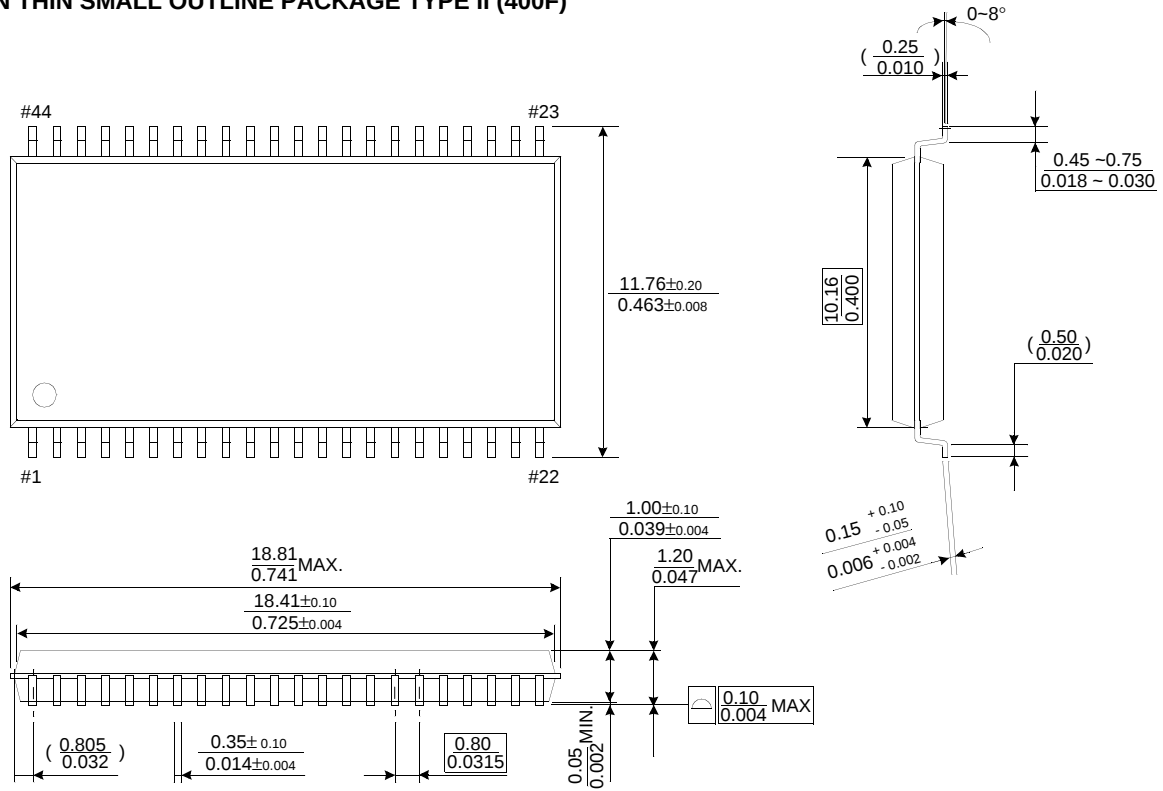
### CS<sub>2</sub> controlled



## PACKAGE DIMENSIONS

Unit: millimeters(inches)

### 44 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400F)



### 44 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400R)

