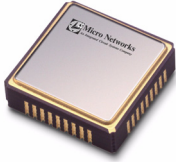




GENERAL DESCRIPTION

The M908-02 is a PLL (Phase Locked Loop) based clock generator that uses an internal VCSO (Voltage Controlled SAW Oscillator) to produce a very low jitter output clock. From the M908-02-155.5200, an output clock frequency of 155.52MHz is provided from eight LVPECL clock output pairs. (Other frequencies are available; consult factory.) The accuracy of the output frequency is assured by the internal PLL that phase-locks the internal VCSO to the reference input frequency (19.44MHz for the M908-02-155.5200). The input reference can either be an external crystal, utilizing the internal crystal oscillator, or a stable external clock source such as a packaged crystal oscillator.



PIN ASSIGNMENT (9 x 9 mm SMT)

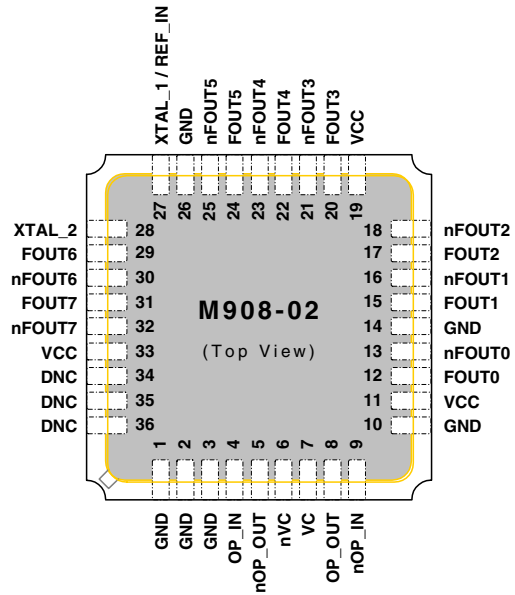


Figure 1: Pin Assignment

FEATURES

- ◆ Output clock frequency range 75MHz to 175MHz (Consult factory for frequency availability)
- ◆ Eight identical LVPECL output pairs
- ◆ Jitter 0.7ps rms (at 155.52MHz, over 12kHz-20MHz), typ.
- ◆ Ideal for OC-48/STM-16 clock reference
- ◆ Output-to-output skew < 100ps
- ◆ External XTAL or LVCMOS reference input
- ◆ Integrated SAW (surface acoustic wave) delay line
- ◆ Single 3.3V power supply
- ◆ Small 9 x 9 mm SMT (surface mount) package

Example Output Frequency Configurations (M908-02-155.5200)

Ref Clock Frequency (MHz)	PLL Multiplication Ratio	VCSO and Output Frequency (MHz)	Application
19.44	8	155.52	OC-48/STM-16

Table 1: Example Output Frequency Configurations

SIMPLIFIED BLOCK DIAGRAM

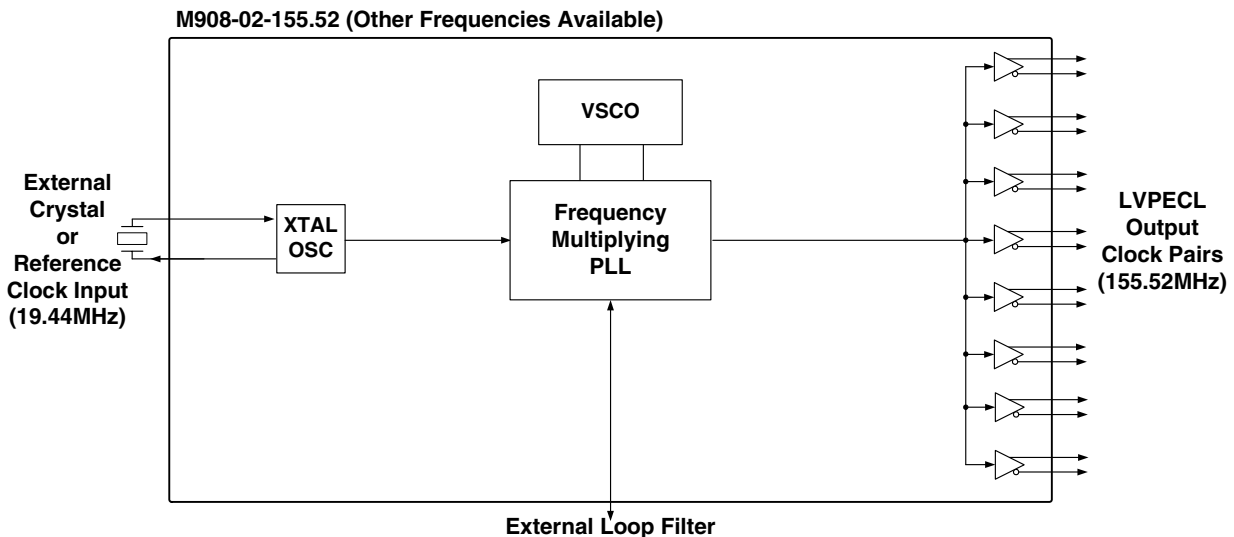


Figure 2: Simplified Block Diagram



DETAILED BLOCK DIAGRAM

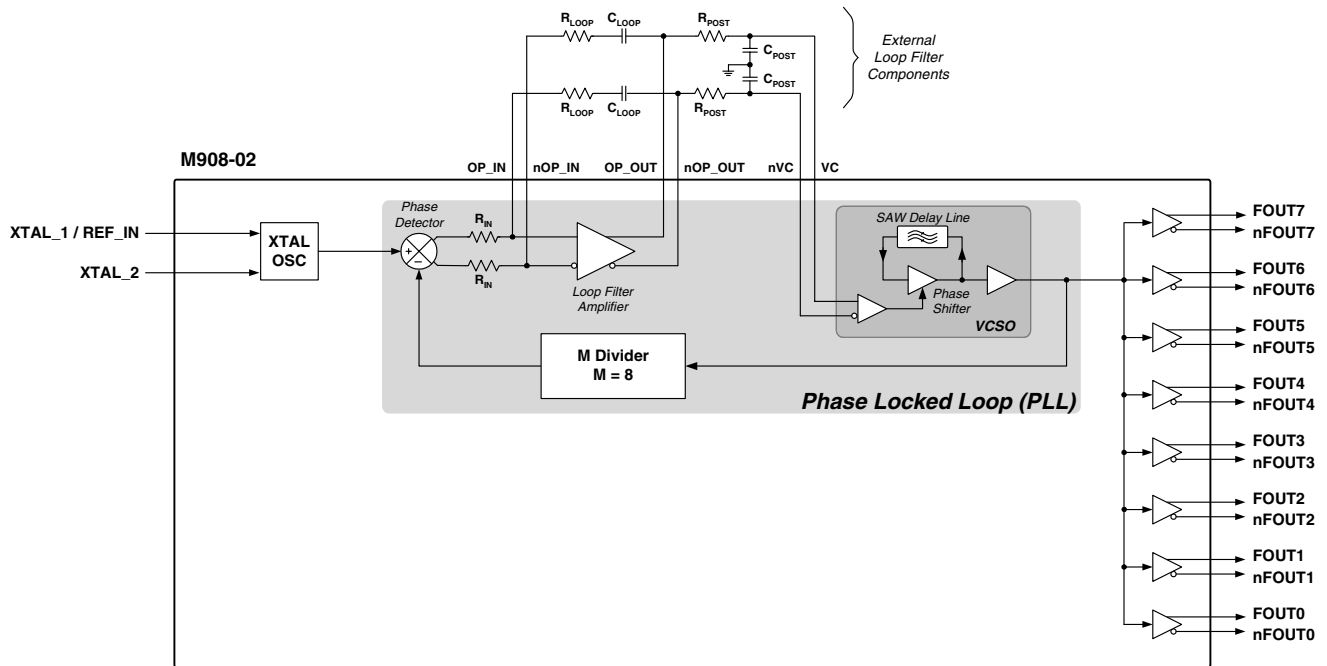


Figure 3: Detailed Block Diagram

PIN DESCRIPTIONS

Number	Name	I/O	Configuration	Description
1, 2, 3, 10, 14, 26	GND	Ground		Power supply ground connections.
4 9	OP_IN nOP_IN	Input		
5 8	nOP_OUT OP_OUT	Output		External loop filter connections. See Figure 5.
6 7	nVC VC	Input		
11, 19, 33	VCC	Power		Power supply connection, connect to +3.3V.
12, 13	FOUT0, nFOUT0			
15, 16	FOUT1, nFOUT1			
17, 18	FOUT2, nFOUT2			
20, 21	FOUT3, nFOUT3	Output	No internal terminator	Clock output pairs, differential LVPECL output (155.52 MHz for the M908-02-155.5200)
22, 23	FOUT4, nFOUT4			
24, 25	FOUT5, nFOUT5			
29, 30	FOUT6, nFOUT6			
31, 32	FOUT7, nFOUT7			
27	XTAL_1 / REF_IN	Input		External crystal connection. Also accepts LVCMOS/LVTTL compatible clock source.
28	XTAL_2	Input		External crystal connection. Leave unconnected when driving pin 27 with external clock reference.
34, 35, 36	DNC		Do Not Connect.	Internal nodes. Connection to these pins can cause erratic device operation.

Table 2: Pin Descriptions



FUNCTIONAL DESCRIPTION

The M908-02 is a PLL (Phase Locked Loop) based clock generator that generates output clocks synchronized to an input reference clock.

The M908-02 combines the flexibility of a VCSO (Voltage Controlled SAW Oscillator) with the stability of a crystal oscillator.

Input Reference

The 19.44MHz input reference can either be an external, discrete crystal device or a stable external clock source such as a packaged crystal oscillator:

- If an external crystal is used with the on-chip crystal oscillator circuit (XTAL OSC), the external crystal should be a parallel-resonant, fundamental mode crystal. Apply it to the XTAL_1 / REF_IN and XTAL_2 input pins. External crystal load capacitors are also required.
- If an external LVCMOS/LVTTL clock source is used, apply it to the XTAL_1 / REF_IN input pin.

In either case, the reference clock is supplied directly to the phase detector of the PLL.

The PLL

The PLL (Phase Locked Loop) includes the phase detector, the VCSO, and a feedback divider (labeled "M Divider").

The feedback divider is a digital circuit that divides the VCSO output frequency by a numerical value "M" in order to match the input reference frequency.

By controlling the frequency and phase of the VCSO, the phase detector precisely locks the frequency and phase of the feedback divider output to that of the input reference. This creates an output frequency that is a multiple of the reference frequency (which is output from the VCSO).

The relationship between the VCSO output frequency, the M Divider, and the input reference frequency is defined as follows:

$$F_{vcs0} = M \times F_{xtal}$$

For the M908-02-155.5200 (see "Ordering Information" on pg. 6):

- VCSO output frequency = 155.52MHz
- M = 8
- Input reference frequency = 19.44MHz

Therefore, for the M908-02-155.5200:

$$155.52\text{MHz} = 8 \times 19.44\text{MHz}$$

The VCSO center output frequency of 155.52MHz enables the product of $M \times$ input crystal frequency to fall within the lock range of the VCSO.

APPLICATION INFORMATION

This section includes information on the optional external crystal and on the external loop filter.

The subsections on the loop filter provide example component values and also briefly describe the SAW PLL simulator tool and additional application information available at www.icst.com.

External Crystal Specifications

If an external crystal is used with the on-chip crystal oscillator circuit (XTAL OSC), the external crystal should have the following general specifications:

Crystal Specifications

Parameter	Min	Typ	Max	Unit
Crystal Type	AT-cut quartz			
Mode of Oscillation	Fundamental			
f_0 Frequency Range	16		40	MHz
ESR Equivalent Series Resistance			50	Ω
Spurious Response (non-harmonic)			-40	dBc
C_L Load Capacitance, parallel load resonant	16		32	pF
P_0 Drive Level	0.1		1.0	mW

Table 3: Crystal Specifications

The external crystal will be applied to the XTAL_1 / REF_IN and XTAL_2 input pins. External crystal load capacitors are also required.

Recommended External Crystal Configuration

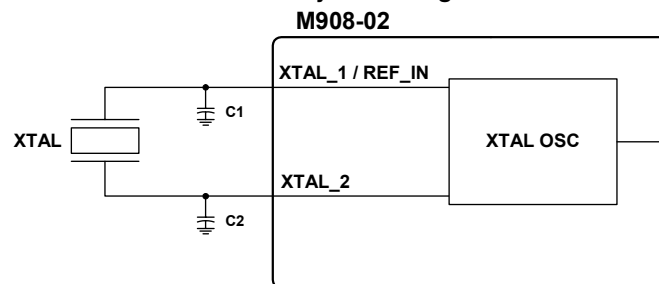


Figure 4: Recommended External Crystal Configuration

XTAL Load Capacitance Specification = 18 pF

C1 = 27 pF

C2 = 33 pF

External load capacitors C1 and C2 present a load of 15 pF to the crystal (they are seen in series by the crystal through the common ground connection). With the additional of PCB trace capacitance and M908-02 input capacitance, the total load to the crystal is about 18 pF.



External Loop Filter

To provide stable PLL operation, and thereby a low jitter output clock, the M908-02 requires the use of an external loop filter. This is provided via the provided filter pins (see Figure 5).

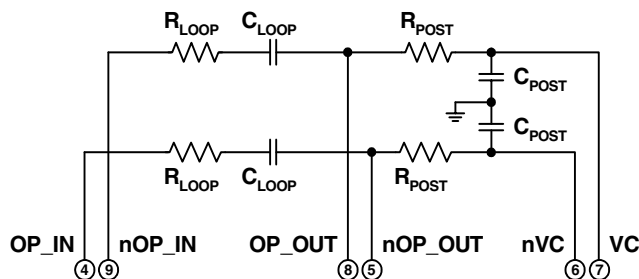


Figure 5: External Loop Filter

The loop filter is implemented as a differential circuit to minimize system noise interference. Due to the differential signal path design, the implementation requires two identical complementary RC filters as shown here.

See Table 4, Example External Loop Filter Component Values, below.

Example External Loop Filter Component Values

PLL Bandwidth (kHz)	Damping Factor	R loop (kΩ)	C loop (μF)	R post (kΩ)	C post (pF)
0.395	2.0	1.5	4.70	20	3300
1.2	2.9	4.7	1.00	20	1000
10 ¹	2.4	39.0	0.01	20	240

Table 4: Example External Loop Filter Component Values

Note 1: Recommended for minimum output jitter when using a crystal or crystal oscillator reference.

Refer to the M908-02 product web page at www.icst.com/products/summary/m908-02.htm for additional product information.

PLL Simulator Tool Available

A free PC software utility is available on the ICS website (www.icst.com). The M2000 Timing Modules PLL Simulator is a downloadable application that simulates PLL jitter and wander transfer characteristics. This enables the user to set appropriate external loop component values in a given application.

Refer to the SAW PLL Simulator Software web page at www.icst.com/products/calculators/m2000filterSWdesc.htm for additional information.

ABSOLUTE MAXIMUM RATINGS¹

Symbol	Parameter	Rating	Unit
V _I	Inputs	-0.5 to V _{CC} +0.5	V
V _O	Outputs	-0.5 to V _{CC} +0.5	V
V _{CC}	Power Supply Voltage	4.6	V
T _S	Storage Temperature	-45 to +100	°C

Table 5: Absolute Maximum Ratings

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in Recommended Conditions of Operation, DC Characteristics, or AC Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

RECOMMENDED CONDITIONS OF OPERATION

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Positive Supply Voltage	3.135	3.3	3.465	V
T _A	Ambient Operating Temperature	Commercial	0	+70	°C
		Industrial	-40	+85	°C

Table 6: Recommended Conditions of Operation



ELECTRICAL SPECIFICATIONS

DC Characteristics

Unless stated otherwise, $V_{CC} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $+70^\circ C$ (commercial), $T_A = -40^\circ C$ to $+85^\circ C$ (industrial), $F_{VCSO} = 155.52MHz$,¹
LVPECL outputs terminated with 50Ω to $V_{CC} - 2V$

	Symbol	Parameter	Min	Typ	Max	Unit
Power Supply	V_{CC}	Positive Supply Voltage	3.135	3.3	3.465	V
	I_{CC}	Power Supply Current		375		mA
Reference Clock Input	V_{IH}	Input High Voltage	$(V_{CC}/2) + 0.5$		$V_{CC} + 0.3$	V
	V_{IL}	Input Low Voltage	-0.3		$(V_{CC}/2) + 0.5$	V
	I_{IH}	Input High Current XTAL_1 / REF_IN (XTAL_2 disconnected)			150	μA
	I_{IL}	Input Low Current	-5.0			μA
Crystal or Reference Clock Input	C_{IN}	Input Capacitance XTAL_1 / REF_IN			4	pF
Differential Output	V_{OH}	Output High Voltage	$V_{CC} - 1.4$		$V_{CC} - 1.0$	V
	V_{OL}	Output Low Voltage FOUT, nFOUT (0-7)	$V_{CC} - 2.0$		$V_{CC} - 1.7$	V
	V_{P-P}	Peak to Peak Output Voltage	0.6		0.85	V

Table 7: DC Characteristics

Note 1: For other VCSO center frequencies, contact ICS

AC Characteristics

Unless implied otherwise, $V_{CC} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $+70^\circ C$ (commercial), $T_A = -40^\circ C$ to $+85^\circ C$ (industrial), $F_{VCSO} = 155.52MHz$,¹
LVPECL outputs terminated with 50Ω to $V_{CC} - 2V$

	Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
	F_{OUT}	Output Frequency Range	75		175	MHz	
	F_{IN}	Nominal Input Frequency, XTAL_1 / REF_IN		19.44		MHz	
	APR	VCSO Pull-Range	± 100	± 150		ppm	
Φ_n	Single Side Band Phase Noise @ 155.52MHz	1kHz Offset		-100		dBc/Hz	
		10kHz Offset		-110		dBc/Hz	
		100kHz Offset		-134		dBc/Hz	
J(t)	Jitter (rms)		0.7	1.0	ps	12kHz to 20MHz	
t_{DC}	Output Duty Cycle, High Time		45	50	55	%	
t_R	Output Rise Time	FOUT, nFOUT (0-7)	350	450	550	ps	20% to 80%
t_F	Output Fall Time	FOUT, nFOUT (0-7)	350	450	550	ps	20% to 80%
t_S	Output Skew	Between Any Pair			100	ps	

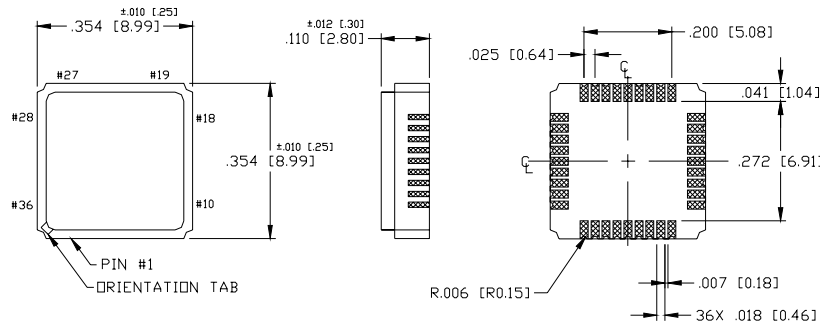
Table 8: AC Characteristics

Note 1: For other VCSO center frequencies, contact ICS



DEVICE PACKAGE - 9 x 9mm CERAMIC LEADLESS CHIP CARRIER

Mechanical Dimensions:



Refer to the SAW PLL application notes web page at www.icst.com/products/appnotes/SawPLLAppNotes.htm for application notes, including recommended PCB footprint, solder mask, and furnace profile.

NOTES:

1. DIMENSIONS ARE IN INCHES, DIMENSIONS IN [] ARE MM.
2. UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE ±.005 [-.13]

Figure 6: Device Package - 9 x 9mm Ceramic Leadless Chip Carrier

ORDERING INFORMATION

Part Numbering Scheme

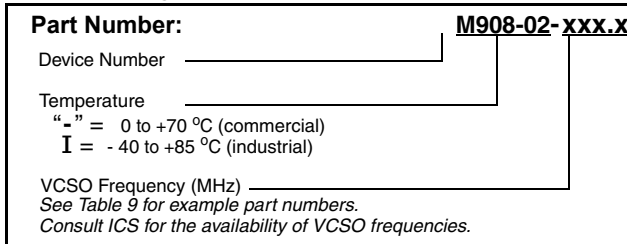


Figure 7: Part Numbering Scheme

Example Part Numbers

For Output Frequencies (MHz)	Temperature	Order Part Number
155.52	commercial	M908-02-155.5200
	industrial	M908-02I155.5200
75 to 175	commercial	M908-02-xxx.xxxx
	industrial	M908-02Ixxx.xxxx

Table 9: Example Part Numbers

Consult ICS for the availability of VCSO frequencies

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