DATA SHEET

MOS INTEGRATED CIRCUIT

μPD442012A-X

2M-BIT CMOS STATIC RAM
128K-WORD BY 16-BIT
EXTENDED TEMPERATURE OPERATION

Description

The μPD442012A-X is a high speed, low power, 2,097,152 bits (131,072 words by 16 bits) CMOS static RAM.
The μPD442012A-X has two chip enable pins (/CE1, CE2) to extend the capacity.
The μPD442012A-X is packed in 48-pin PLASTIC TSOP (I) (Normal bent).

Features

- 131,072 words by 16 bits organization
- Fast access time : 50, 55, 70, 85, 100, 120 ns (MAX.)
- Byte data control : /LB (I/O1 - I/O8), /UB (I/O9 - I/O16)
- Low voltage operation
  (BB version : V_{CC} = 2.7 to 3.6 V, BC version : V_{CC} = 2.2 to 3.6 V, DD version : V_{CC} = 1.8 to 2.2 V)
- Low V_{CC} data retention : 1.0 V (MIN.)
- Operating ambient temperature : T_A = –25 to +85 °C
- Output Enable input for easy application
- Two Chip Enable inputs : /CE1, CE2

Part number	Access time ns (MAX.)	Operating supply voltage V	Operating ambient temperature °C	Supply current		
				At operating mA (MAX.)	At standby μA (MAX.)	At data retention μA (MAX.)
μPD442012A-BBxxX	50 Note 1, 55, 70, 85	2.7 to 3.6	–25 to +85	30 Note 2 35 Note 3 40 Note 4	4	2
μPD442012A-BCxxX	70, 85, 100	2.2 to 3.6		30		
μPD442012A-DDxxX	85, 100, 120	1.8 to 2.2		15	3	

Notes 1. $V_{CC} \geq 3.0$ V

2. Cycle time ≥ 70 ns

3. Cycle time = 55 ns

4. Cycle time = 50 ns

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The mark <R> shows major revised points.

The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

Ordering Information

Part number	Package	Access time ns (MAX.)	Operating supply voltage V	Operating temperature °C	Remark
μPD442012AGY-BB55X-MJH	48-pin PLASTIC TSOP (I) (12×18) (Normal bent)	55, 50 Note	2.7 to 3.6	–25 to +85	BB version
μPD442012AGY-BB70X-MJH		70			
μPD442012AGY-BB85X-MJH		85			
μPD442012AGY-BC70X-MJH		70	2.2 to 3.6		BC version
μPD442012AGY-BC85X-MJH		85			
μPD442012AGY-BC10X-MJH		100			
μPD442012AGY-DD85X-MJH		85	1.8 to 2.2		DD version
μPD442012AGY-DD10X-MJH		100			
μPD442012AGY-DD12X-MJH		120			
μPD442012AGY-BB55X-MJH-A		55, 50 Note	2.7 to 3.6		BB version
μPD442012AGY-BB70X-MJH-A		70			
μPD442012AGY-BB85X-MJH-A		85			
μPD442012AGY-BC70X-MJH-A		70	2.2 to 3.6		BC version
μPD442012AGY-BC85X-MJH-A		85			
μPD442012AGY-BC10X-MJH-A		100			
μPD442012AGY-DD85X-MJH-A		85	1.8 to 2.2		DD version
μPD442012AGY-DD10X-MJH-A		100			
μPD442012AGY-DD12X-MJH-A		120			

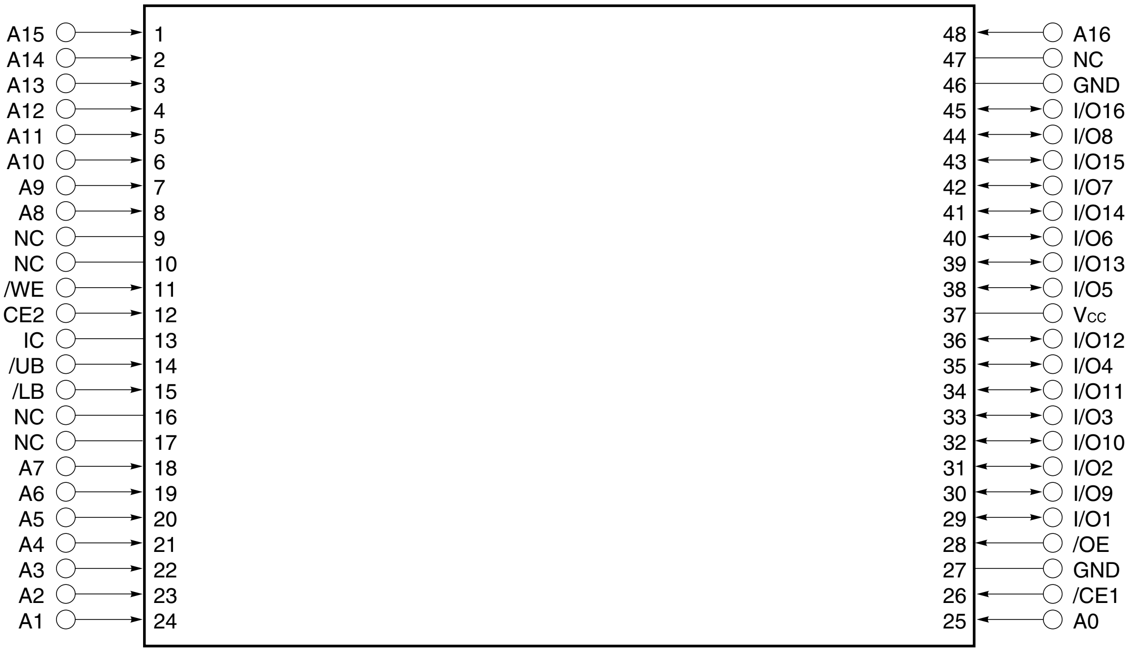
Note $V_{CC} \geq 3.0$ V

Remark Products with -A at the end of the part number are lead-free products.

Pin Configuration (Marking Side)

/xxx indicates active low signal.

48-pin PLASTIC TSOP (I) (12×18) (Normal bent)
[μPD442012AGY-BBxxX-MJH]
[μPD442012AGY-BCxxX-MJH]
[μPD442012AGY-DDxxX-MJH]
[μPD442012AGY-BBxxX-MJH-A]
[μPD442012AGY-BCxxX-MJH-A]
[μPD442012AGY-DDxxX-MJH-A]

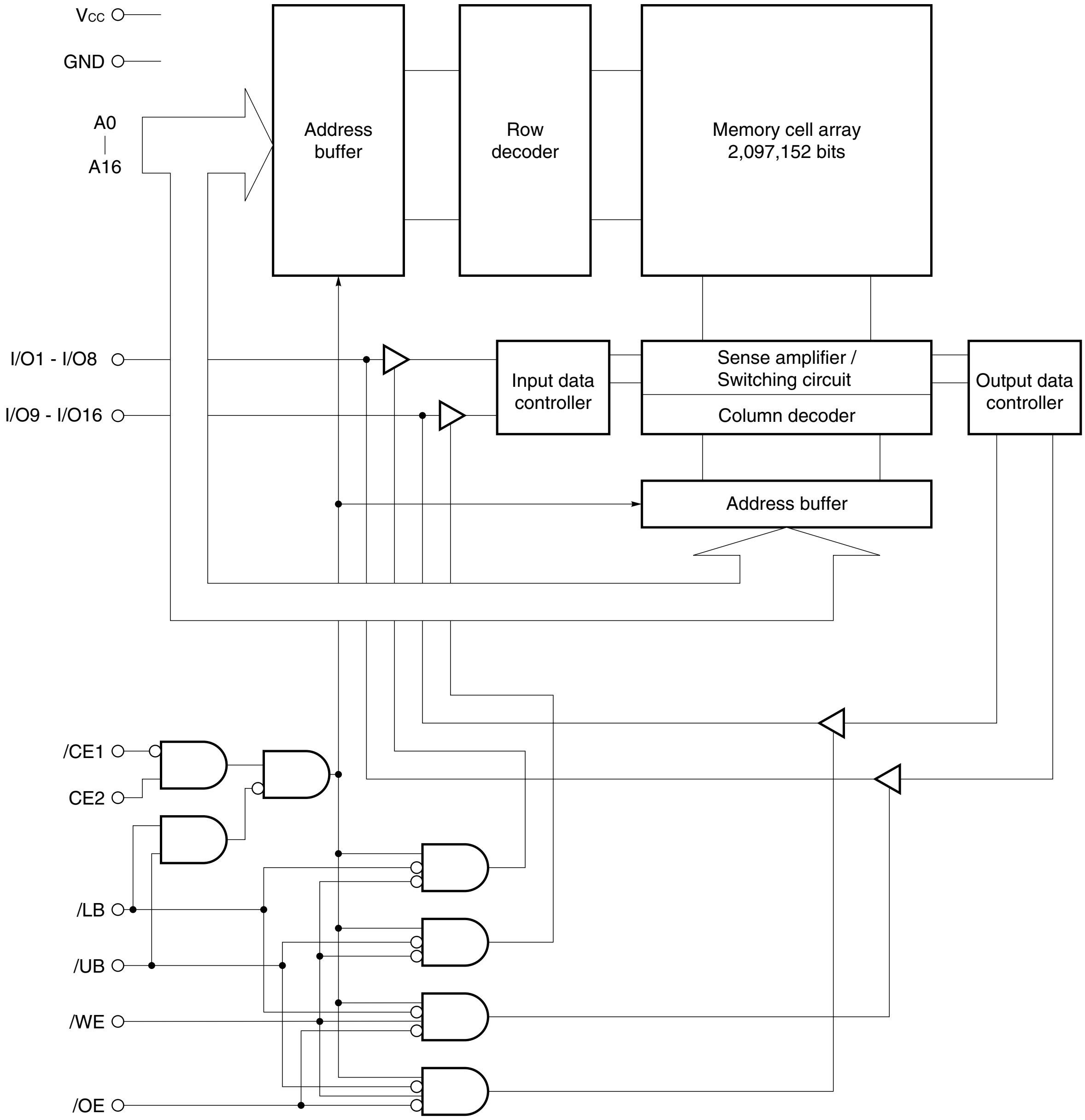


A0 - A16	:	Address inputs
I/O1 - I/O16	:	Data inputs / outputs
/CE1, CE2	:	Chip Enable 1, 2
/WE	:	Write Enable
/OE	:	Output Enable
/LB, /UB	:	Byte data select
V_{CC}	:	Power supply
GND	:	Ground
NC	:	No Connection
IC **Note**	:	Internal Connection

Note Leave this pin unconnected or connect to GND.

Remark Refer to **Package Drawing** for the 1-pin index mark.

Block Diagram



Truth Table

/CE1	CE2	/OE	/WE	/LB	/UB	Mode	I/O		Supply current
							I/O1 - I/O8	I/O9 - I/O16	
H	×	×	×	×	×	Not selected	High impedance	High impedance	I_{SB}
×	L	×	×	×	×	Not selected	High impedance	High impedance	
×	×	×	×	H	H	Not selected	High impedance	High impedance	
L	H	H	H	L	×	Output disable	High impedance	High impedance	I_{CCA}
				×	L	Output disable	High impedance	High impedance	
		L	H	L	L	Word read	D_{OUT}	D_{OUT}	
				L	H	Lower byte read	D_{OUT}	High impedance	
				H	L	Upper byte read	High impedance	D_{OUT}	
		×	L	L	L	Word write	D_{IN}	D_{IN}	
				L	H	Lower byte write	D_{IN}	High impedance	
				H	L	Upper byte write	High impedance	D_{IN}	

Remark × : V_{IH} or V_{IL}

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Product	Rating	Unit
Supply voltage	V_{CC}	μPD442012A-BBxxX, μPD442012A-BCxxX	–0.5 [Note] to +4.0	V
		μPD442012A-DDxxX	–0.5 [Note] to +2.7	
Input / Output voltage	V_T	μPD442012A-BBxxX, μPD442012A-BCxxX	–0.5 [Note] to V_{CC}+0.4 (4.0 V MAX.)	V
		μPD442012A-DDxxX	–0.5 [Note] to V_{CC}+0.4 (2.7 V MAX.)	
Operating ambient temperature	T_A		–25 to +85	°C
Storage temperature	T_{stg}		–55 to +125	°C

Note –3.0 V (MIN.) (Pulse width : 30 ns)

Caution **Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.**

Recommended Operating Conditions

Parameter	Symbol	Condition	μPD442012A-BBxxX		μPD442012A-BCxxX		μPD442012A-DDxxX		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Supply voltage	V_{CC}		2.7	3.6	2.2	3.6	1.8	2.2	V
High level input voltage	V_{IH}	2.7 V ≤ V_{CC} ≤ 3.6 V	2.4	V_{CC}+0.4	2.4	V_{CC}+0.4	–	–	V
		2.2 V ≤ V_{CC} < 2.7 V	–	–	2.0	V_{CC}+0.3	–	–	
		1.8 V ≤ V_{CC} < 2.2 V	–	–	–	–	1.6	V_{CC}+0.2	
Low level input voltage	V_{IL}		–0.3 [Note]	+0.5	–0.3 [Note]	+0.4	–0.2 [Note]	+0.2	V
Operating ambient temperature	T_A		–25	+85	–25	+85	–25	+85	°C

Note –1.0 V (MIN.) (Pulse width : 20 ns)

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V			8	pF
Input / Output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

Remarks **1.** V_{IN} : Input voltage

$V_{I/O}$: Input / Output voltage

2. These parameters are not 100% tested.

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted) (1/2)

Parameter	Symbol	Test condition		μPD442012A-BBxxX			Unit
				MIN.	TYP.	MAX.	
Input leakage current	I_{LI}	V_{IN} = 0 V to V_{CC}		–1.0		+1.0	μA
I/O leakage current	I_{LO}	$V_{I/O}$ = 0 V to V_{CC}, /CE1 = V_{IH} or CE2 = V_{IL} or /WE = V_{IL} or /OE = V_{IH}		–1.0		+1.0	μA
Operating supply current	I_{CCA1}	/CE1 = V_{IL}, CE2 = V_{IH},	Cycle time = 50 ns		–	40	mA
		$I_{I/O}$ = 0 mA,	Cycle time = 55 ns		–	35	
		Minimum cycle time	Cycle time ≥ 70 ns		–	30	
	I_{CCA2}	/CE1 = V_{IL}, CE2 = V_{IH}, $I_{I/O}$ = 0 mA, Cycle time = ∞			–	4	
	I_{CCA3}	/CE1 ≤ 0.2 V, CE2 ≥ V_{CC} – 0.2 V, Cycle time = 1 μs, $I_{I/O}$ = 0 mA, V_{IL} ≤ 0.2 V, V_{IH} ≥ V_{CC} – 0.2 V			–	4	
Standby supply current	I_{SB}	/CE1 = V_{IH} or CE2 = V_{IL} or /LB = /UB = V_{IH}			–	0.6	mA
	I_{SB1}	/CE1 ≥ V_{CC} – 0.2 V, CE2 ≥ V_{CC} – 0.2 V			0.3	4	μA
	I_{SB2}	CE2 ≤ 0.2 V			0.3	4	
	I_{SB3}	/LB = /UB ≥ V_{CC} – 0.2 V, /CE1 ≤ 0.2 V, CE2 ≥ V_{CC} – 0.2 V			0.3	4	
High level output voltage	V_{OH}	I_{OH} = –0.5 mA		2.4			V
Low level output voltage	V_{OL}	I_{OL} = 1.0 mA				0.4	V

Remarks 1. V_{IN} : Input voltage

$V_{I/O}$: Input / Output voltage

2. These DC characteristics are in common regardless of product specification.

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted) (2/2)

Parameter	Symbol	Test condition		μPD442012A-BCxxX			μPD442012A-DDxxX			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input leakage current	I_{LI}	V_{IN} = 0 V to V_{CC}		–1.0		+1.0	–1.0		+1.0	μA
I/O leakage current	I_{LO}	$V_{I/O}$ = 0 V to V_{CC}, /CE1 = V_{IH} or CE2 = V_{IL} or /WE = V_{IL} or /OE = V_{IH}		–1.0		+1.0	–1.0		+1.0	μA
Operating supply current	I_{CCA1}	/CE1 = V_{IL}, CE2 = V_{IH},			–	30		–	–	mA
		$I_{I/O}$ = 0 mA,	V_{CC} ≤ 2.7 V		–	25		–	–	
		Minimum cycle time	V_{CC} ≤ 2.2 V		–	–		–	15	
	I_{CCA2}	/CE1 = V_{IL}, CE2 = V_{IH},			–	4		–	–	
		$I_{I/O}$ = 0 mA,	V_{CC} ≤ 2.7 V		–	2		–	–	
		Cycle time = ∞	V_{CC} ≤ 2.2 V		–	–		–	1	
	I_{CCA3}	/CE1 ≤ 0.2 V, CE2 ≥ V_{CC} – 0.2 V, Cycle time = 1 μs, $I_{I/O}$ = 0 mA,			–	4		–	–	
		V_{IL} ≤ 0.2 V,	V_{CC} ≤ 2.7 V		–	3		–	–	
		V_{IH} ≥ V_{CC} – 0.2 V	V_{CC} ≤ 2.2 V		–	–		–	3	
Standby supply current	I_{SB}	/CE1 = V_{IH} or CE2 = V_{IL} or			–	0.6		–	–	mA
		/LB = /UB = V_{IH}	V_{CC} ≤ 2.7 V		–	0.6		–	–	
			V_{CC} ≤ 2.2 V		–	–		–	0.6	
	I_{SB1}	/CE1 ≥ V_{CC} – 0.2 V,			0.3	4		–	–	μA
		CE2 ≥ V_{CC} – 0.2 V	V_{CC} ≤ 2.7 V		0.25	3.5		–	–	
			V_{CC} ≤ 2.2 V		–	–		0.2	3	
	I_{SB2}	CE2 ≤ 0.2 V			0.3	4		–	–	
			V_{CC} ≤ 2.7 V		0.25	3.5		–	–	
			V_{CC} ≤ 2.2 V		–	–		0.2	3	
	I_{SB3}	/LB = /UB ≥ V_{CC} – 0.2 V,			0.3	4		–	–	
		/CE1 ≤ 0.2 V,	V_{CC} ≤ 2.7 V		0.25	3.5		–	–	
		CE2 ≥ V_{CC} – 0.2 V	V_{CC} ≤ 2.2 V		–	–		0.2	3	
High level output voltage	V_{OH}	I_{OH} = –0.5 mA		2.4			–			V
			V_{CC} ≤ 2.7 V	1.8			–			
			V_{CC} ≤ 2.2 V	–			1.5			
Low level output voltage	V_{OL}	I_{OL} = 1.0 mA				0.4			–	V
			V_{CC} ≤ 2.7 V			0.4			–	
			V_{CC} ≤ 2.2 V			–			0.4	

Remarks **1.** V_{IN} : Input voltage

$V_{I/O}$: Input / Output voltage

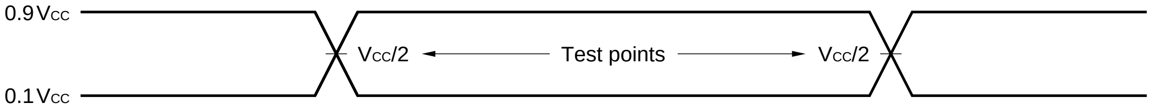
2. These DC characteristics are in common regardless of product specification.

AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

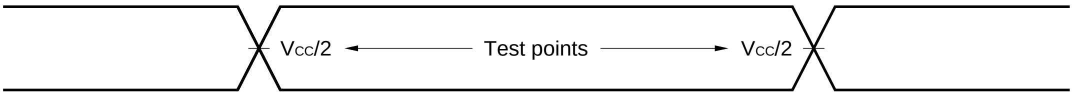
AC Test Conditions

[μPD442012A-BB55X, μPD442012A-BB70X, μPD442012A-BB85X]

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform

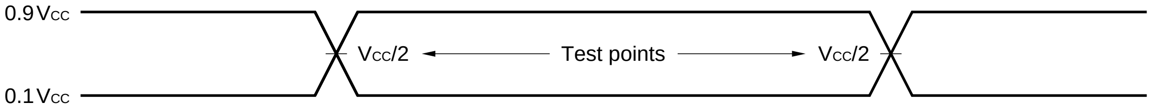


Output Load

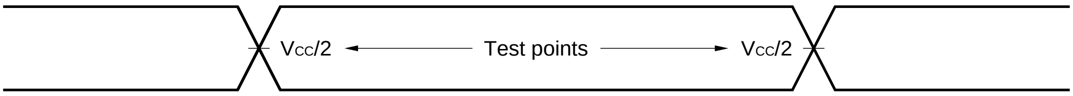
1TTL + 50 pF

[μPD442012A-BC70X, μPD442012A-BC85X, μPD442012A-BC10X]

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform

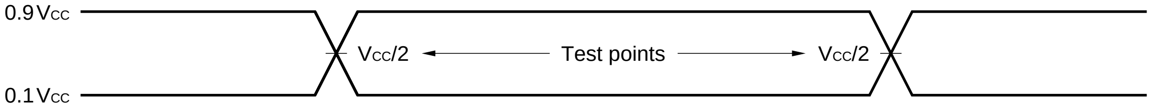


Output Load

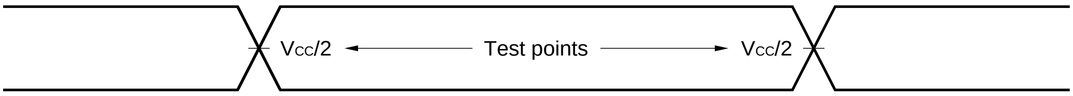
1TTL + 30 pF

[μPD442012A-DD85X, μPD442012A-DD10X, μPD442012A-DD12X]

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform



Output Load

1TTL + 30 pF

Read Cycle (1/3) (BB version)

Parameter	Symbol	μPD442012A-BB55X				μPD442012A-BB70X		μPD442012A-BB85X		Unit	Condition
		V_{CC} ≥ 3.0 V									
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	50		55		70		85		ns	
Address access time	t_{AA}		50		55		70		85	ns	**Note 1**
/CE1 access time	t_{CO1}		50		55		70		85	ns	
CE2 access time	t_{CO2}		50		55		70		85	ns	
/OE to output valid	t_{OE}		30		30		35		40	ns	
/LB, /UB to output valid	t_{BA}		50		55		70		85	ns	
Output hold from address change	t_{OH}	10		10		10		10		ns	
/CE1 to output in low impedance	t_{LZ1}	10		10		10		10		ns	**Note 2**
CE2 to output in low impedance	t_{LZ2}	10		10		10		10		ns	
/OE to output in low impedance	t_{OLZ}	5		5		5		5		ns	
/LB, /UB to output in low impedance	t_{BLZ}	10		10		10		10		ns	
/CE1 to output in high impedance	t_{HZ1}		20		20		25		30	ns	
CE2 to output in high impedance	t_{HZ2}		20		20		25		30	ns	
/OE to output in high impedance	t_{OHZ}		20		20		25		30	ns	
/LB, /UB to output in high impedance	t_{BHZ}		20		20		25		30	ns	

Notes 1. The output load is 1TTL + 50 pF.

2. The output load is 1TTL + 5 pF.

Read Cycle (2/3) (BC version)

Parameter	Symbol	μPD442012A-BC70X		μPD442012A-BC85X		μPD442012A-BC10X		Unit	Condition
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	70		85		100		ns	
Address access time	t_{AA}		70		85		100	ns	**Note 1**
/CE1 access time	t_{CO1}		70		85		100	ns	
CE2 access time	t_{CO2}		70		85		100	ns	
/OE to output valid	t_{OE}		35		40		50	ns	
/LB, /UB to output valid	t_{BA}		70		85		100	ns	
Output hold from address change	t_{OH}	10		10		10		ns	
/CE1 to output in low impedance	t_{LZ1}	10		10		10		ns	**Note 2**
CE2 to output in low impedance	t_{LZ2}	10		10		10		ns	
/OE to output in low impedance	t_{OLZ}	5		5		5		ns	
/LB, /UB to output in low impedance	t_{BLZ}	10		10		10		ns	
/CE1 to output in high impedance	t_{HZ1}		25		30		35	ns	
CE2 to output in high impedance	t_{HZ2}		25		30		35	ns	
/OE to output in high impedance	t_{OHZ}		25		30		35	ns	
/LB, /UB to output in high impedance	t_{BHZ}		25		30		35	ns	

Notes 1. The output load is 1TTL + 30 pF.

2. The output load is 1TTL + 5 pF.

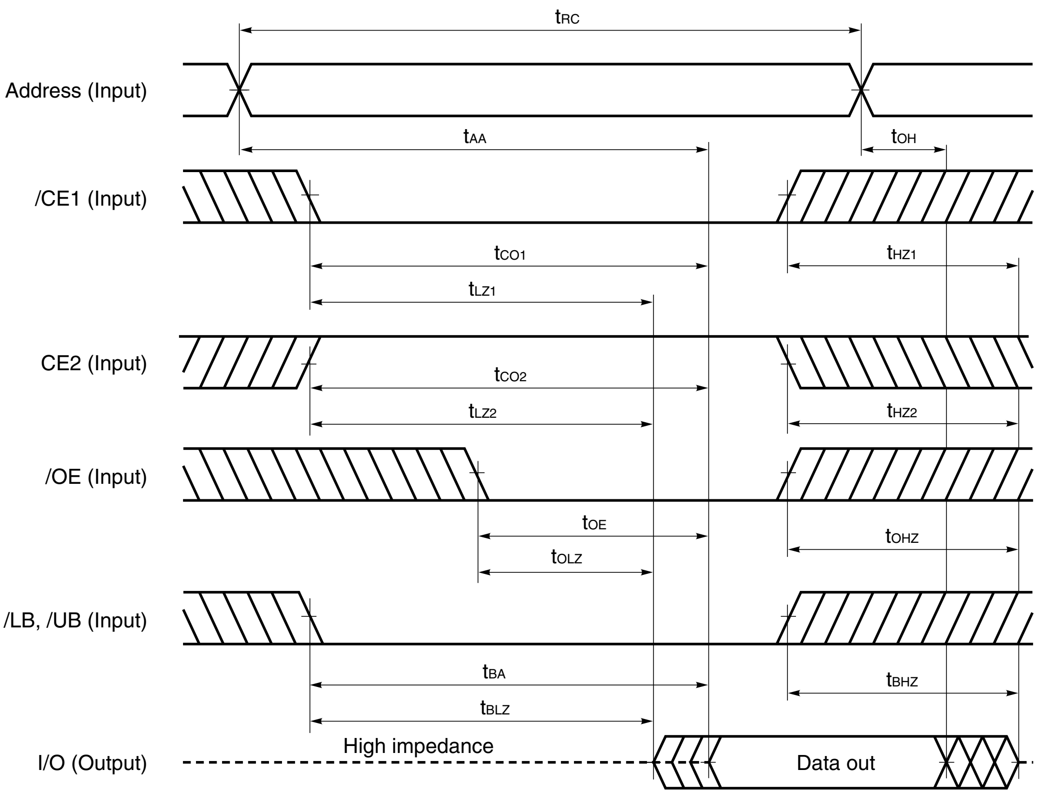
Read Cycle (3/3) (DD version)

Parameter	Symbol	μPD442012A -DD85X		μPD442012A -DD10X		μPD442012A -DD12X		Unit	Condition
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	85		100		120		ns	
Address access time	t_{AA}		85		100		120	ns	**Note 1**
/CE1 access time	t_{CO1}		85		100		120	ns	
CE2 access time	t_{CO2}		85		100		120	ns	
/OE to output valid	t_{OE}		40		50		60	ns	
/LB, /UB to output valid	t_{BA}		85		100		120	ns	
Output hold from address change	t_{OH}	10		10		10		ns	
/CE1 to output in low impedance	t_{LZ1}	10		10		10		ns	**Note 2**
CE2 to output in low impedance	t_{LZ2}	10		10		10		ns	
/OE to output in low impedance	t_{OLZ}	5		5		5		ns	
/LB, /UB to output in low impedance	t_{BLZ}	10		10		10		ns	
/CE1 to output in high impedance	t_{HZ1}		30		35		40	ns	
CE2 to output in high impedance	t_{HZ2}		30		35		40	ns	
/OE to output in high impedance	t_{OHZ}		30		35		40	ns	
/LB, /UB to output in high impedance	t_{BHZ}		30		35		40	ns	

Notes 1. The output load is 1TTL + 30 pF.

2. The output load is 1TTL + 5 pF.

Read Cycle Timing Chart



Remark In read cycle, /WE should be fixed to high level.

Write Cycle (1/3) (BB version)

Parameter	Symbol	μPD442012A-BB55X				μPD442012A-BB70X		μPD442012A-BB85X		Unit	Condition
		V_{CC} ≥ 3.0 V									
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	50		55		70		85		ns	
/CE1 to end of write	t_{CW1}	45		50		55		70		ns	
CE2 to end of write	t_{CW2}	45		50		55		70		ns	
/LB, /UB to end of write	t_{BW}	45		50		55		70		ns	
Address valid to end of write	t_{AW}	45		50		55		70		ns	
Address setup time	t_{AS}	0		0		0		0		ns	
Write pulse width	t_{WP}	40		45		50		55		ns	
Write recovery time	t_{WR}	0		0		0		0		ns	
Data valid to end of write	t_{DW}	25		25		30		35		ns	
Data hold time	t_{DH}	0		0		0		0		ns	
/WE to output in high impedance	t_{WHZ}		20		20		25		30	ns	**Note**
Output active from end of write	t_{OW}	5		5		5		5		ns	

Note The output load is 1TTL + 5 pF.

Write Cycle (2/3) (BC version)

Parameter	Symbol	μPD442012A-BC70X		μPD442012A-BC85X		μPD442012A-BC10X		Unit	Condition
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	70		85		100		ns	
/CE1 to end of write	t_{CW1}	55		70		80		ns	
CE2 to end of write	t_{CW2}	55		70		80		ns	
/LB, /UB to end of write	t_{BW}	55		70		80		ns	
Address valid to end of write	t_{AW}	55		70		80		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	50		55		60		ns	
Write recovery time	t_{WR}	0		0		0		ns	
Data valid to end of write	t_{DW}	30		35		40		ns	
Data hold time	t_{DH}	0		0		0		ns	
/WE to output in high impedance	t_{WHZ}		25		30		35	ns	**Note**
Output active from end of write	t_{OW}	5		5		5		ns	

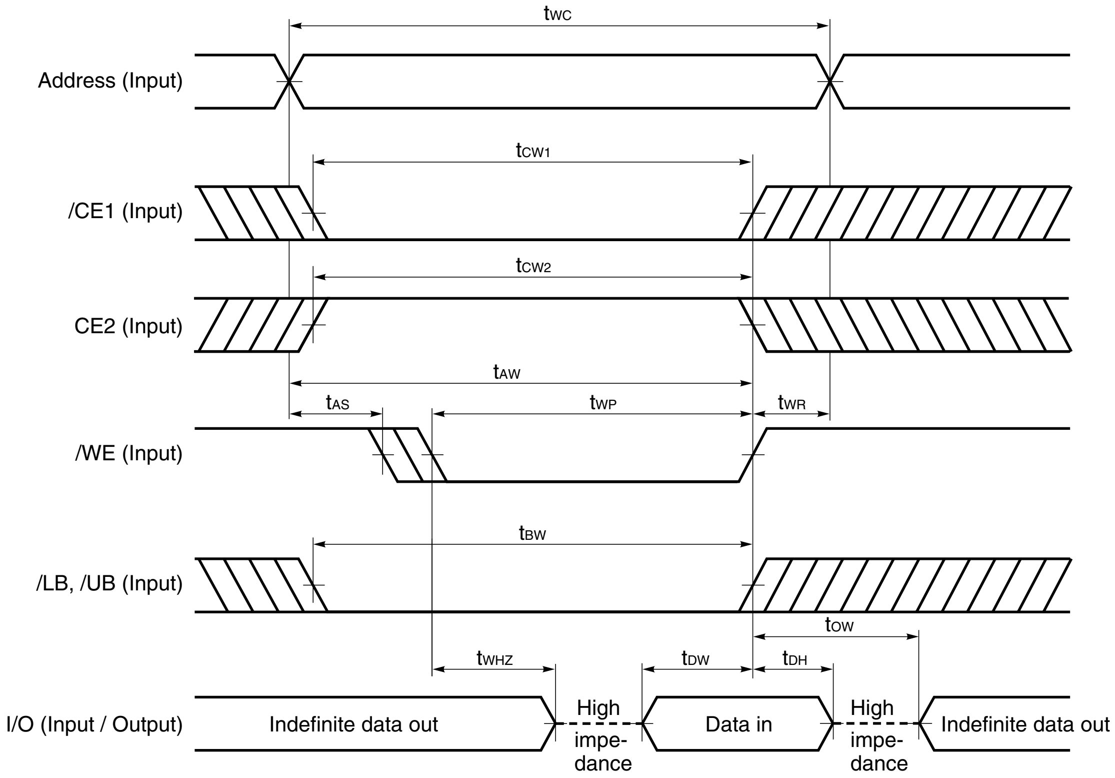
Note The output load is 1TTL + 5 pF.

Write Cycle (3/3) (DD version)

Parameter	Symbol	μPD442012A -DD85X		μPD442012A -DD10X		μPD442012A -DD12X		Unit	Condition
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	85		100		120		ns	
/CE1 to end of write	t_{CW1}	70		80		100		ns	
CE2 to end of write	t_{CW2}	70		80		100		ns	
/LB, /UB to end of write	t_{BW}	70		80		100		ns	
Address valid to end of write	t_{AW}	70		80		100		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	55		60		85		ns	
Write recovery time	t_{WR}	0		0		0		ns	
Data valid to end of write	t_{DW}	35		40		60		ns	
Data hold time	t_{DH}	0		0		0		ns	
/WE to output in high impedance	t_{WHZ}		30		35		40	ns	**Note**
Output active from end of write	t_{OW}	5		5		5		ns	

Note The output load is 1TTL + 5 pF.

Write Cycle Timing Chart 1 (/WE Controlled)



Cautions 1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.

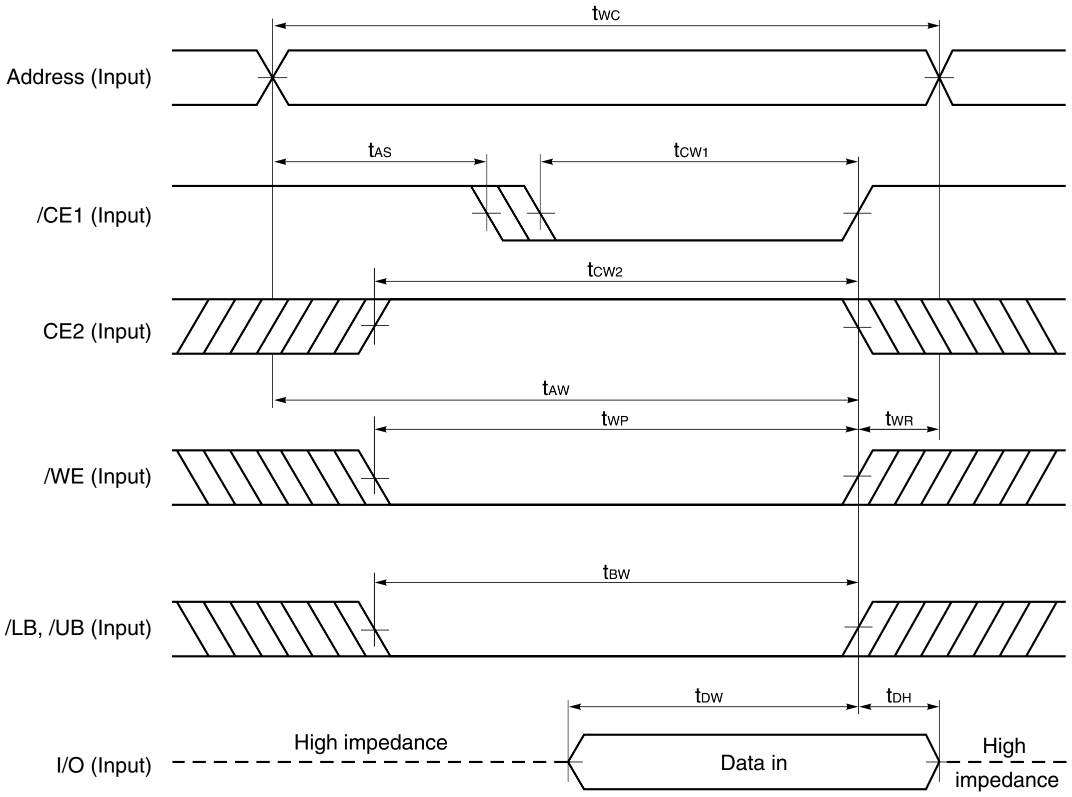
2. Do not input data to the I/O pins while they are in the output state.

Remarks 1. Write operation is done during the overlap time of a low level /CE1, a low level /WE, a low level /LB (or low level /UB) and a high level CE2.

2. If /CE1 changes to low level at the same time or after the change of /WE to low level, or if CE2 changes to high level at the same time or after the change of /WE to low level, the I/O pins will remain high impedance state.

3. When /WE is at low level, the I/O pins are always high impedance. When /WE is at high level, read operation is executed. Therefore /OE should be at high level to make the I/O pins high impedance.

Write Cycle Timing Chart 2 (/CE1 Controlled)

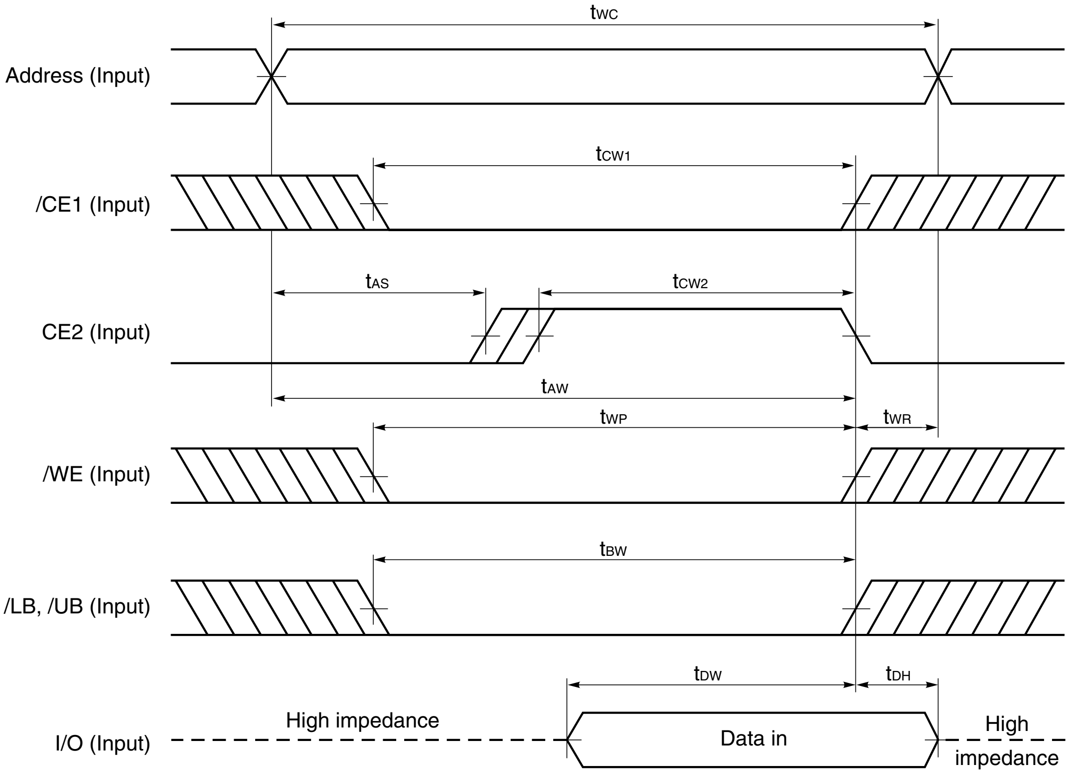


Cautions 1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.

2. Do not input data to the I/O pins while they are in the output state.

Remark Write operation is done during the overlap time of a low level /CE1, a low level /WE, a low level /LB (or low level /UB) and a high level CE2.

Write Cycle Timing Chart 3 (CE2 Controlled)

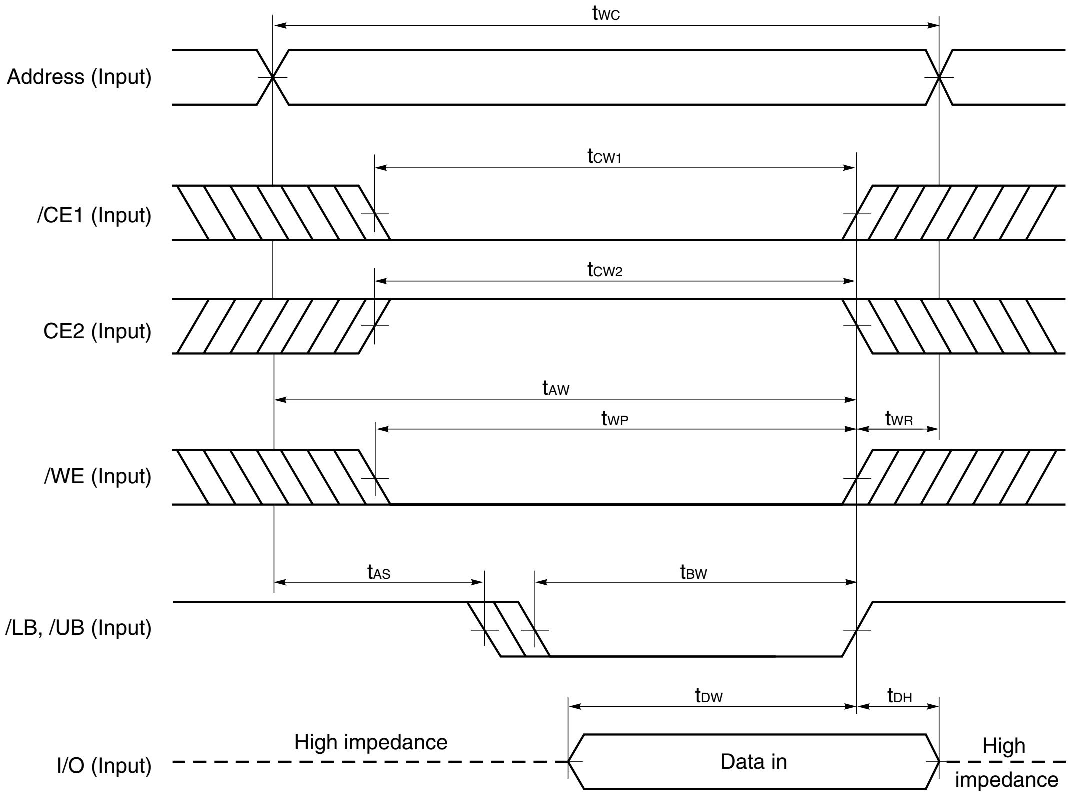


Cautions 1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.

2. Do not input data to the I/O pins while they are in the output state.

Remark Write operation is done during the overlap time of a low level /CE1, a low level /WE, a low level /LB (or low level /UB) and a high level CE2.

Write Cycle Timing Chart 4 (/LB, /UB Controlled)



Cautions 1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.

2. Do not input data to the I/O pins while they are in the output state.

Remark Write operation is done during the overlap time of a low level /CE1, a low level /WE, a low level /LB (or low level /UB) and a high level CE2.

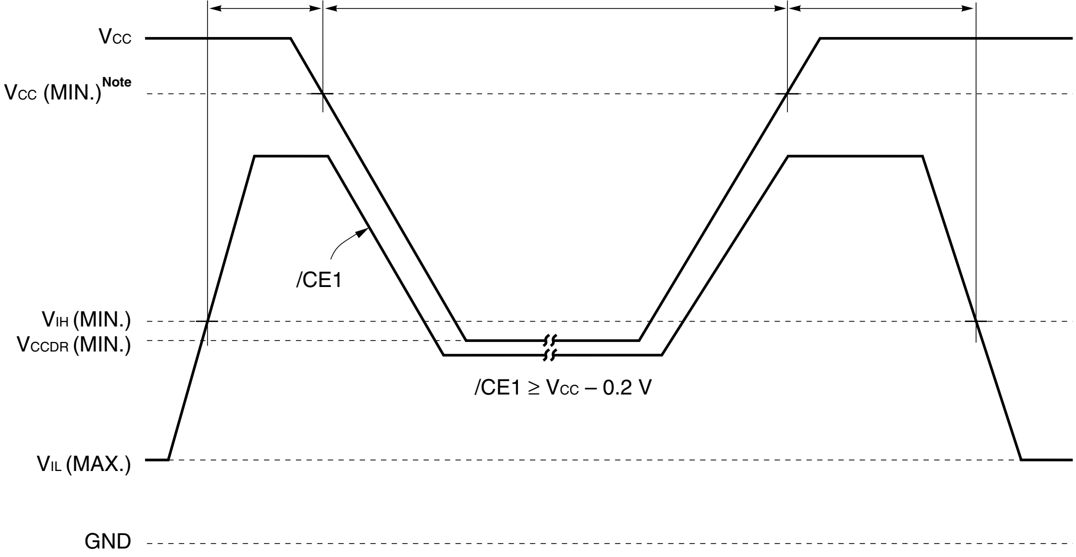
Low V_{CC} Data Retention Characteristics (T_A = –25 to +85 °C)

Parameter	Symbol	Test Condition	µPD442012A -BBxxX			µPD442012A -BCxxX			µPD442012A -DDxxX			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Data retention supply voltage	V_{CCDR1}	/CE1 ≥ V_{CC} – 0.2 V, CE2 ≥ V_{CC} – 0.2 V	1.0		3.6	1.0		3.6	1.0		2.2	V
	V_{CCDR2}	CE2 ≤ 0.2 V	1.0		3.6	1.0		3.6	1.0		2.2	
	V_{CCDR3}	/LB = /UB ≥ V_{CC} – 0.2 V, /CE1 ≤ 0.2 V, CE2 ≥ V_{CC} – 0.2 V	1.0		3.6	1.0		3.6	1.0		2.2	
Data retention supply current	I_{CCDR1}	V_{CC} = 1.2 V, /CE1 ≥ V_{CC} – 0.2 V, CE2 ≥ V_{CC} – 0.2 V		0.15	2		0.15	2		0.15	2	µA
	I_{CCDR2}	V_{CC} = 1.2 V, CE2 ≤ 0.2 V		0.15	2		0.15	2		0.15	2	
	I_{CCDR3}	V_{CC} = 1.2 V, /LB = /UB ≥ V_{CC} – 0.2 V, /CE1 ≤ 0.2 V, CE2 ≥ V_{CC} – 0.2 V		0.15	2		0.15	2		0.15	2	
Chip deselection to data retention mode	t_{CDR}		0			0			0			ns
Operation recovery time	t_R		t_{RC}^{Note}			t_{RC}^{Note}			t_{RC}^{Note}			ns

Note t_{RC} : Read cycle time

Data Retention Timing Chart

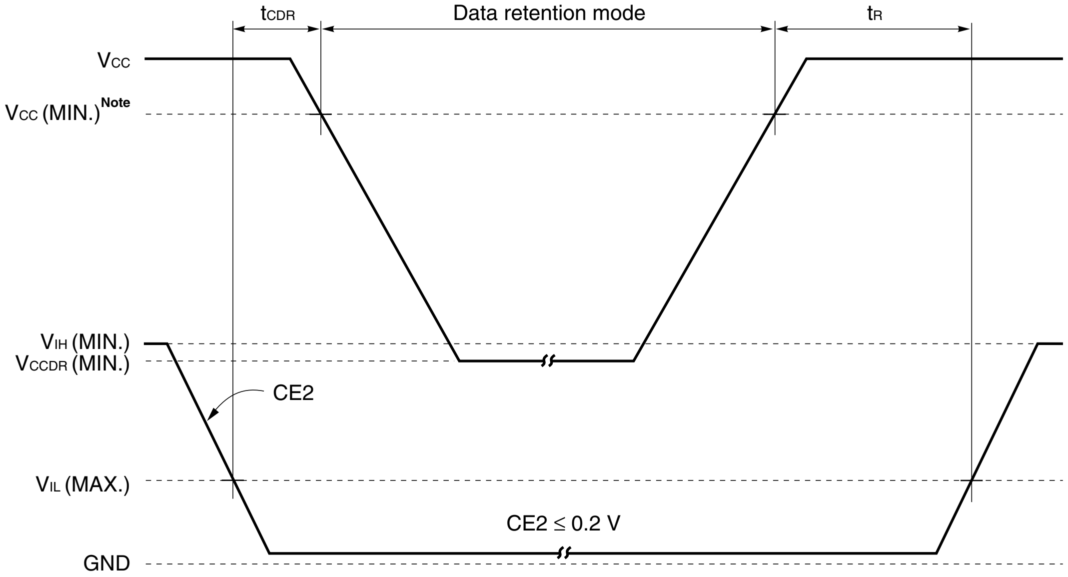
(1) /CE1 Controlled



Note BB version : 2.7 V, BC version : 2.2 V, DD version : 1.8 V

Remark On the data retention mode by controlling /CE1, the input level of CE2 must be ≥ V_{CC} – 0.2 V or ≤ 0.2 V. The other pins (Address, I/O, /WE, /OE, /LB, /UB) can be in high impedance state.

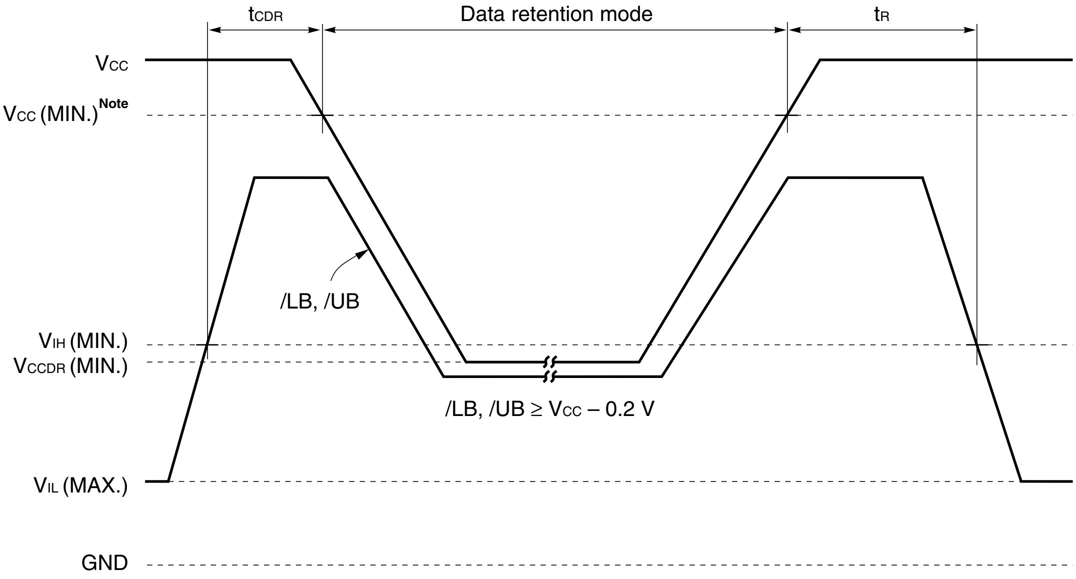
(2) CE2 Controlled



Note BB version : 2.7 V, BC version : 2.2 V, DD version : 1.8 V

Remark On the data retention mode by controlling CE2, the other pins (/CE1, Address, I/O, /WE, /OE, /LB, /UB) can be in high impedance state.

(3) /LB, /UB Controlled

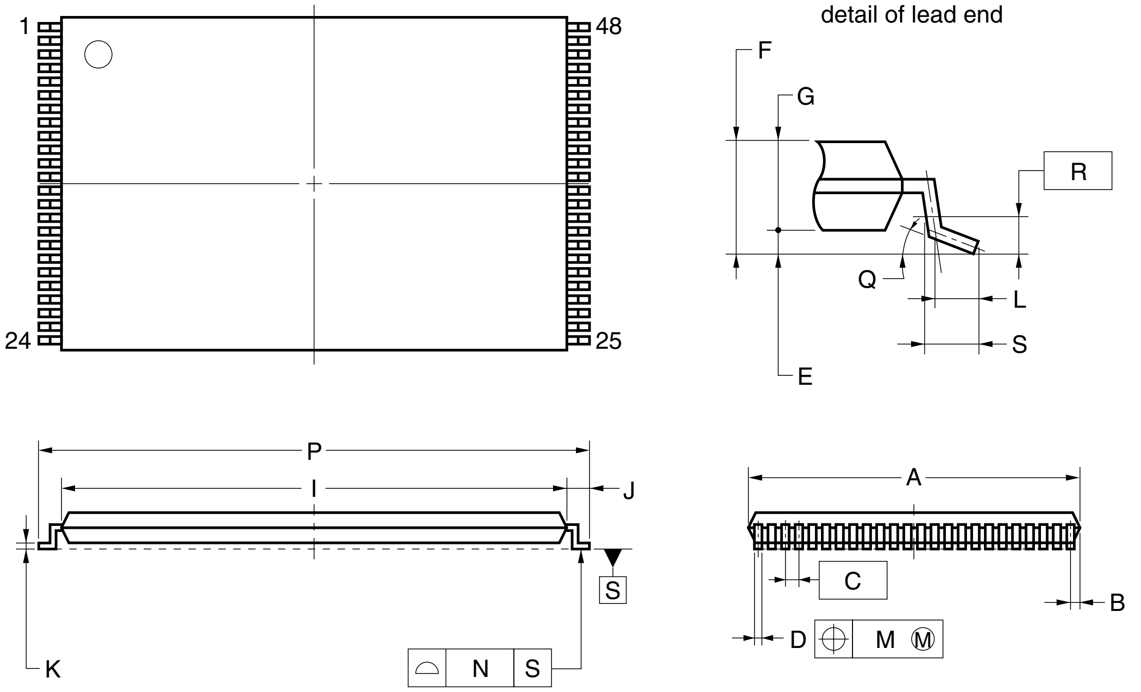


Note BB version : 2.7 V, BC version : 2.2 V, DD version : 1.8 V

Remark On the data retention mode by controlling /LB and /UB, the input level of /CE1 and CE2 must be ≥ V_{CC} – 0.2 V or ≤ 0.2 V. The other pins (Address, I/O, /WE, /OE) can be in high impedance state.

Package Drawing

48-PIN PLASTIC TSOP(I) (12x18)



NOTES

1. Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.
2. "A" excludes mold flash. (Includes mold flash : 12.4 mm MAX.)

ITEM	MILLIMETERS
A	12.0±0.1
B	0.45 MAX.
C	0.5 (T.P.)
D	0.22±0.05
E	0.1±0.05
F	1.2 MAX.
G	1.0±0.05
I	16.4±0.1
J	0.8±0.2
K	0.145±0.05
L	0.5
M	0.10
N	0.10
P	18.0±0.2
Q	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
R	0.25
S	0.60±0.15

S48GY-50-MJH1-1

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD442012A-X.

Types of Surface Mount Device

μPD442012AGY-BBxxX-MJH : 48-pin PLASTIC TSOP (I) (12×18) (Normal bent)
μPD442012AGY-BCxxX-MJH : 48-pin PLASTIC TSOP (I) (12×18) (Normal bent)
μPD442012AGY-DDxxX-MJH : 48-pin PLASTIC TSOP (I) (12×18) (Normal bent)
μPD442012AGY-BBxxX-MJH-A : 48-pin PLASTIC TSOP (I) (12×18) (Normal bent)
μPD442012AGY-BCxxX-MJH-A : 48-pin PLASTIC TSOP (I) (12×18) (Normal bent)
μPD442012AGY-DDxxX-MJH-A : 48-pin PLASTIC TSOP (I) (12×18) (Normal bent)

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Quality Grade

- A quality grade of the products is “Standard”.
- Anti-radioactive design is not implemented in the products.
- Semiconductor devices have the possibility of unexpected defects by affection of cosmic ray that reach to the ground and so forth.

Revision History

Edition/ Date	Page		Type of revision	Location	Description (Previous edition → This edition)
	This edition	Previous edition			
9th edition/ Sep. 2006	p.22	p.22	Addition	Quality Grade	Section of Quality Grade has been added.

[MEMO]

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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