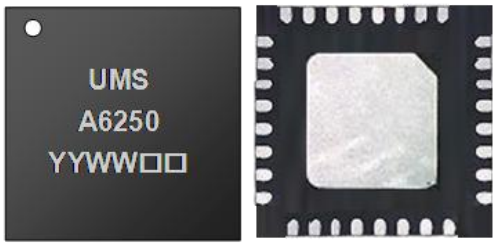
5.5-9GHz Power Amplifier

GaAs Monolithic Microwave IC in SMD leadless package

Description

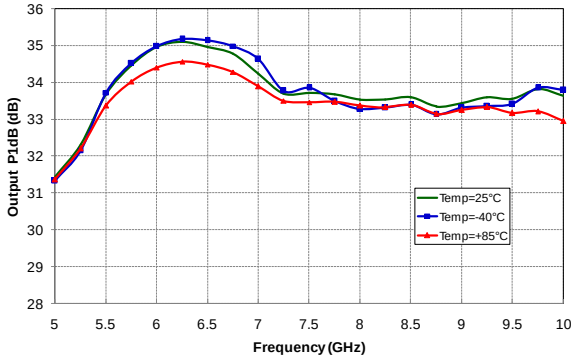
The CHA6250-QFG is a three stages monolithic GaAs high power circuit that produces more than 2 Watt output power.
It is designed for commercial communication systems.
The circuit is manufactured with a pHEMT process, 0.5µm gate length.



Main Features

- Broadband performances: 5.5- 9GHz
- 23.5dB Linear Gain
- 33.5dBm output power @1dB comp.
- 43dBm output TOI
- 29% PAE@ 1dB compression
- DC bias: Vd=7Volt@Id=0.9A
- 32L-QFN5x5

Output power at 1dB comp.



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	5.5		9.0	GHz
Gain	Linear Gain		23.5		dB
OTOI	Output TOI		43.0		dBm
Pout	Output Power @1dB comp.		33.5		dBm

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Electrical Characteristics

Tamb.= +25°C, Vd = +7.0V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	5.5		9	GHz
Gain	Linear Gain	21	23.5	27	dB
G_T	Linear Gain variation versus Temperature		-0.03		dB/°C
RL_in	Input Return Loss		-18		dB
RL_out	Output Return Loss		-14		dB
OP1dB	Output power @1dB comp. [5.5 - 6.8GHz] Output power @1dB comp. [6.8 - 9GHz]	32.5 31.5	33.5 32.5		dBm dBm
Psat	Saturated output power		34.5		dBm
OTOI	Output TOI		43		dBm
PAE	Power Added Efficiency @ 1dB compression		29		%
Idq	Quiescent Drain current		900	1000	mA
Vg	Gate voltage		-0.5		V

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".

Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	7.5V	V
Idq	Drain bias current	1.06	A
Vg	Gate bias voltage	-2 to +0	V
Pin	Input continuous power	15	dBm
Tj	Junction temperature (2)	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Typical Bias Conditions

Tamb.= +25°C

Symbol	Pad N°	Parameter	Values	Unit
VD1	30	DC Drain voltage 1st stage	7	V
VD2	28	DC Drain voltage 2nd stage	7	V
VD3	25	DC Drain voltage 3rd stage	7	V
VG	13	DC Gate voltage tuned for Idq= 0.9A	-0.5	V

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Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered). The temperature is monitored at the package back-side interface (Tcase) as shown below.
The system maximum temperature must be adjusted in order to guarantee that Tcase remains below than the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

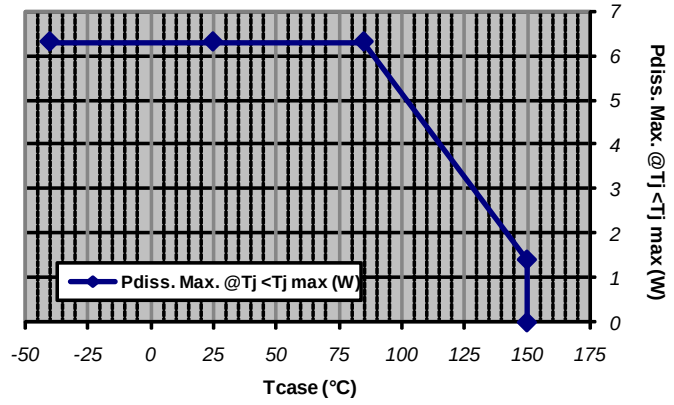
A derating must be applied on the dissipated power if the Tcase temperature can not be maintained below than the maximum temperature specified (see the curve Pdiss. Max) in order to guarantee the nominal device life time (MTTF).

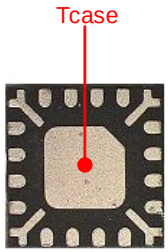
DEVICE THERMAL SPECIFICATION : CHA6250-QFG			
Recommended max. junction temperature (Tj max)		:	169 °C
Junction temperature absolute maximum rating		:	175 °C
Max. continuous dissipated power (Pdiss. Max.)		:	6.3 W
=> Pdiss. Max. derating above Tcase(1)=	85 °C	:	75 mW/°C
Junction-Case thermal resistance (Rth J-C)(2)		:	<13 °C/W
Minimum Tcase operating temperature(3)		:	-40 °C
Maximum Tcase operating temperature(3)		:	85 °C
Minimum storage temperature		:	-55 °C
Maximum storage temperature		:	150 °C

(1) Derating at junction temperature constant = Tj max.

(2) Rth J-C is calculated for a worst case considering the ***hottest junction*** *of the MMIC and all the devices biased.*

(3) Tcase=Package back side temperature measured under the die-attach-pad (see the drawing below).





Example: QFN 16L 3x3
Location of temperature reference point (Tcase) on package's bottom side

6.4

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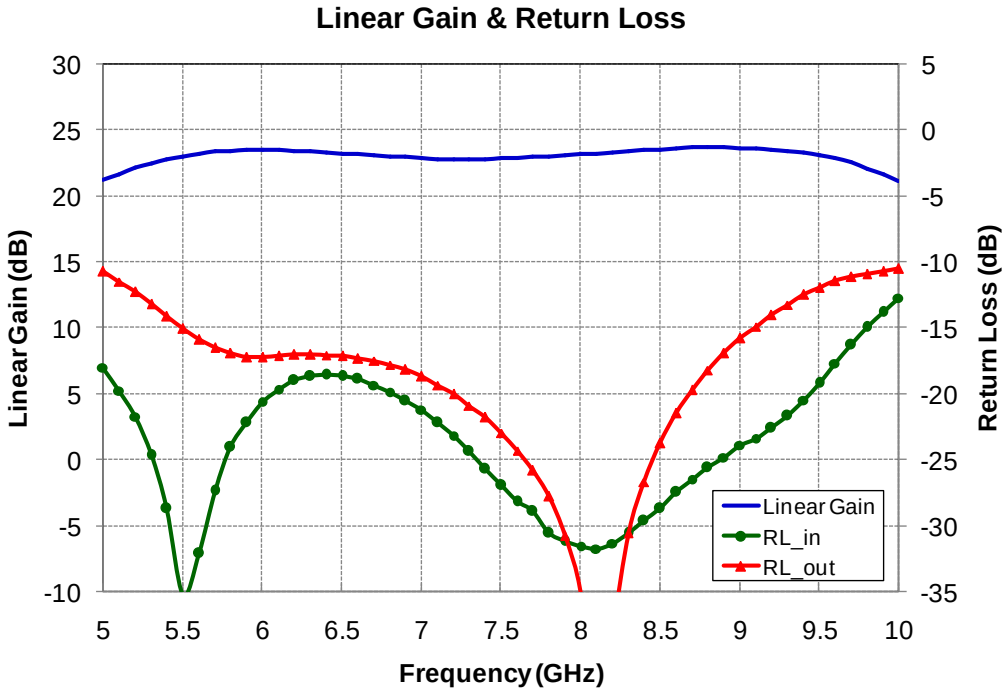
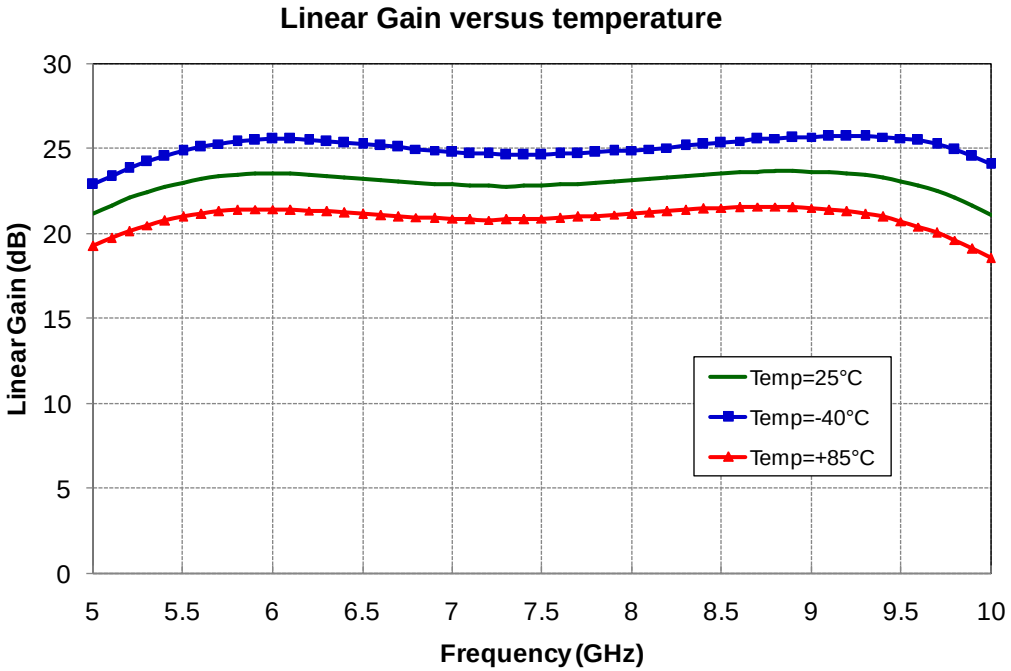
Typical Board Measurements

Tamb.= +25°C, Vd = +7.0V, Idq = 900mA
Measurement in the plan of the connectors, using the proposed land pattern & board, as defined in paragraph “Evaluation mother board”





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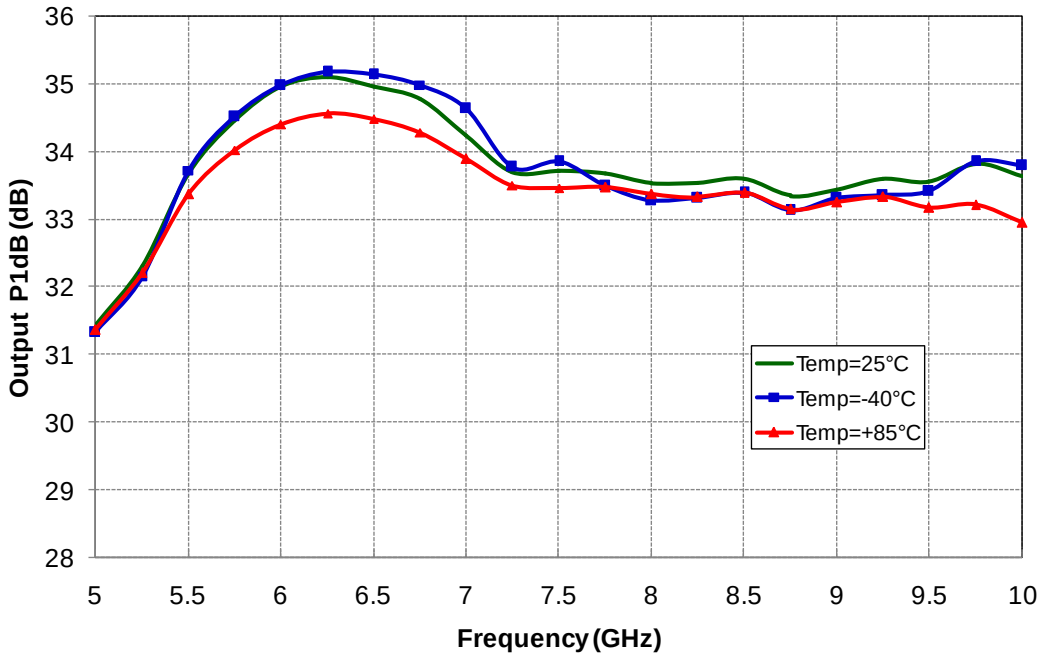
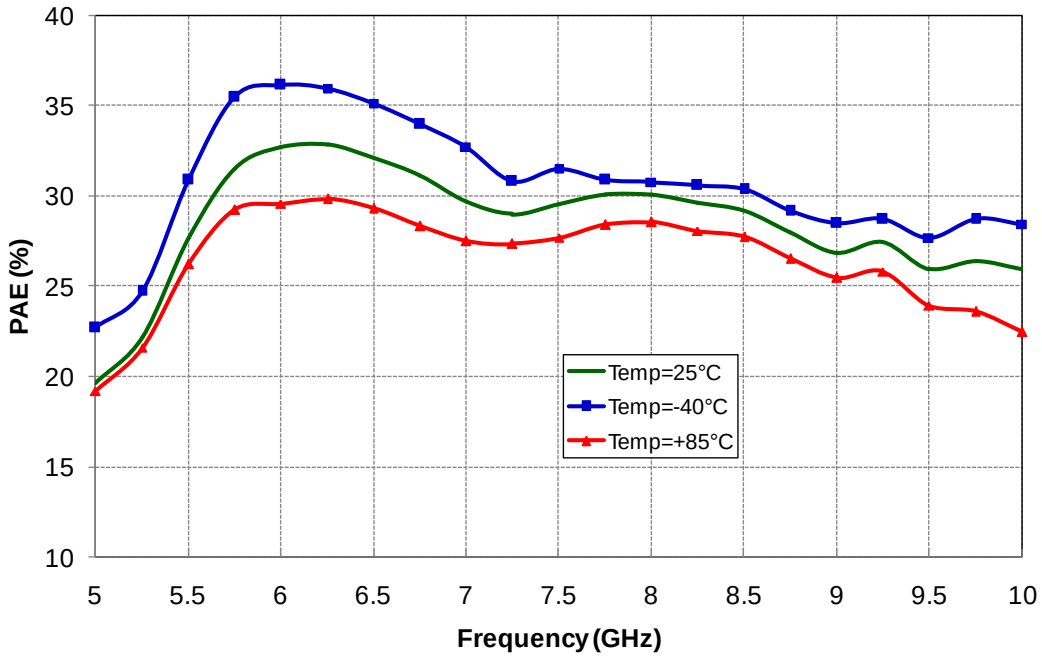
Typical Board Measurements

Tamb.= +25°C, Vd = +7.0V, Idq = 900mA
Measurement in the QFN access plans, using the proposed land pattern & board, as defined in paragraph “Evaluation mother board”

Output power at 1 dB Compression



Power Added Efficiency at 1 dB Compression



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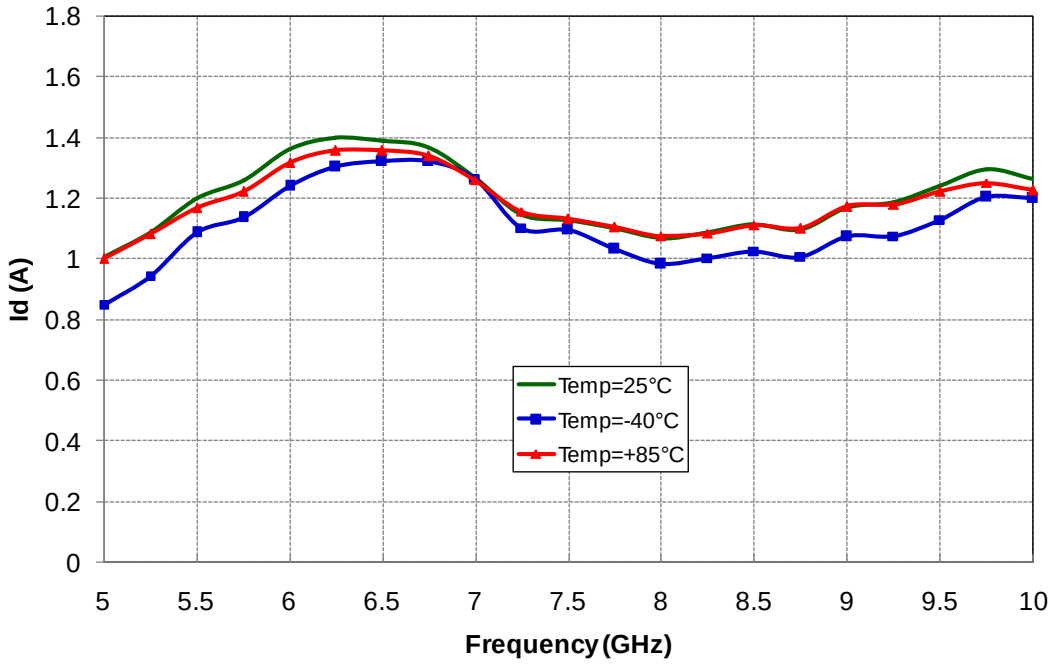
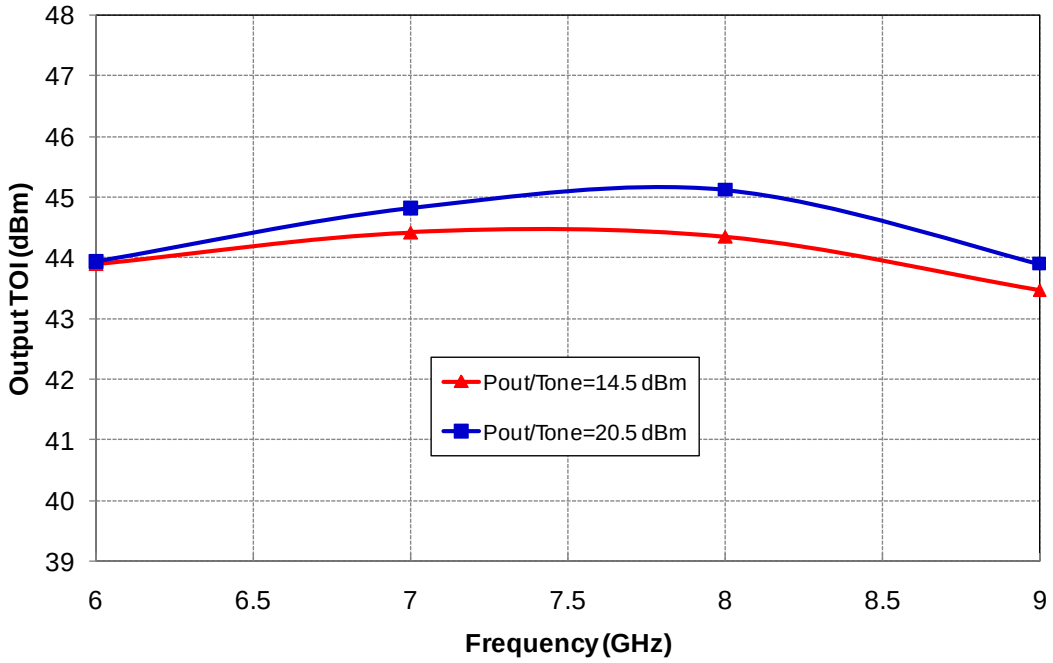
Typical Board Measurements

Tamb.= +25°C, Vd = +7.0V, Idq = 900mA

Drain current at 1 dB Compression



Output TOI (dBm) at two Pout/Tone



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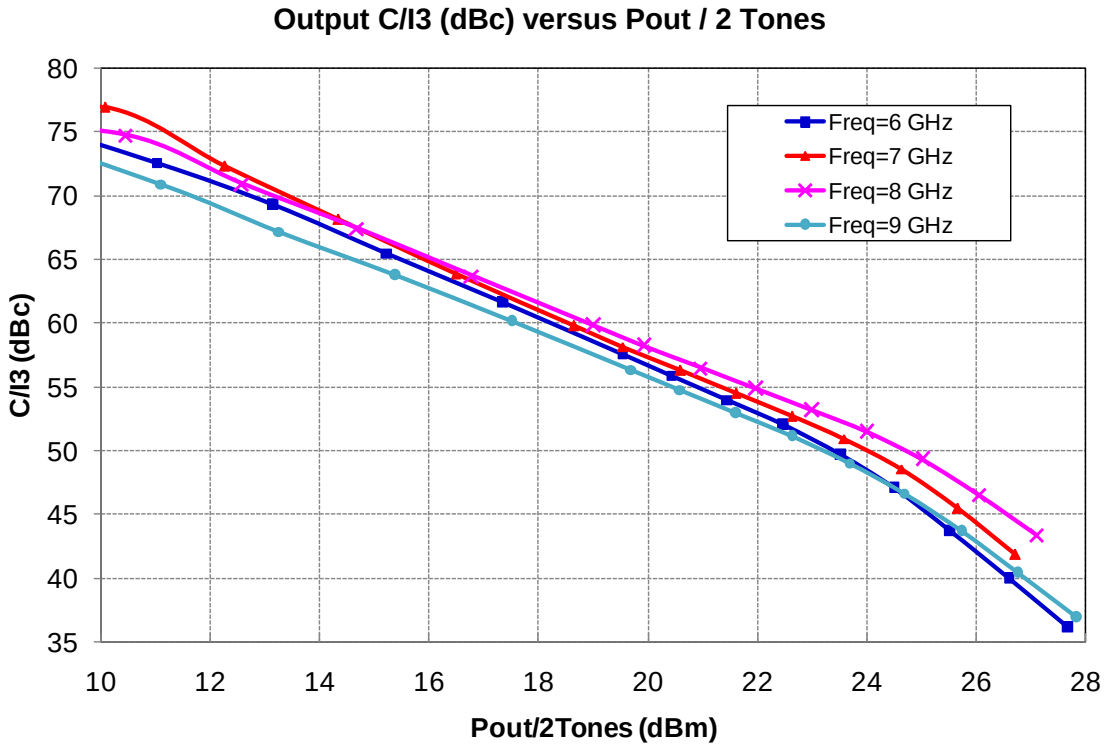
Typical Board Measurements

Tamb.= +25°C, Vd = +7.0V, Idq = 900mA



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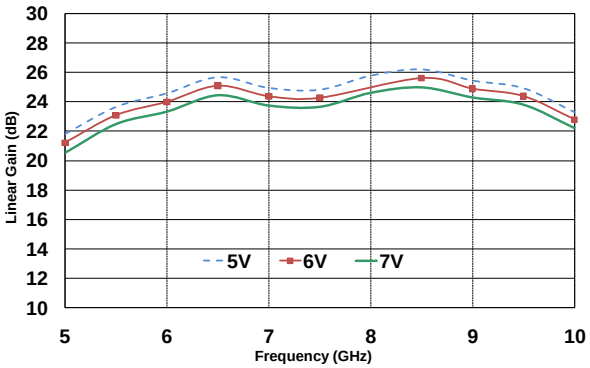
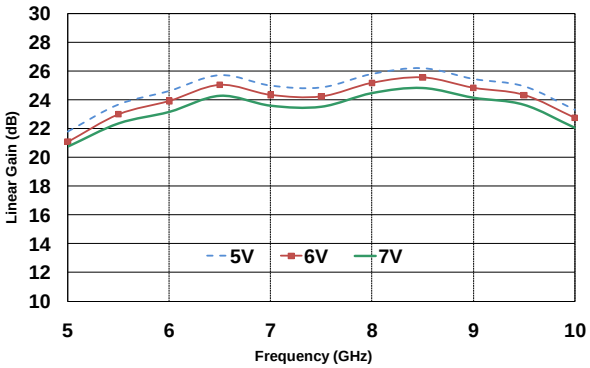
Typical Board Measurements

Tamb.= +25°C

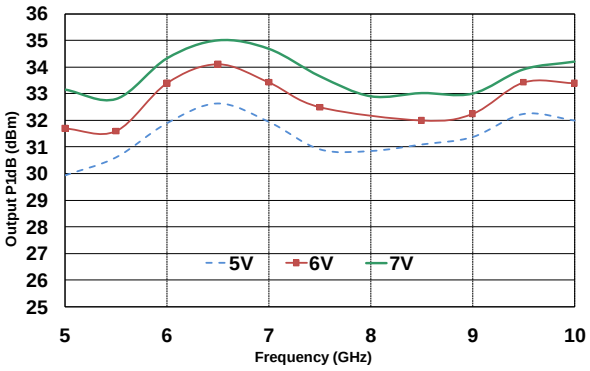
Linear gain vs Vd at 0.9A



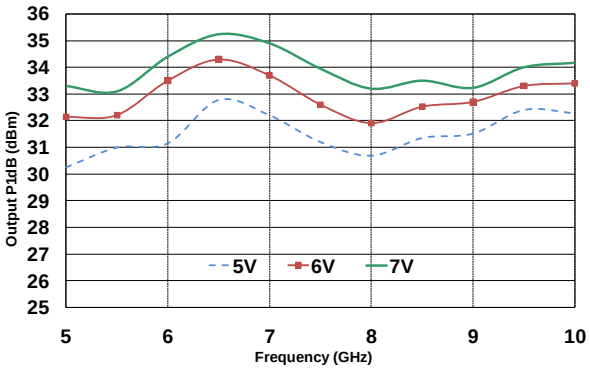
Linear gain vs Vd at 1A



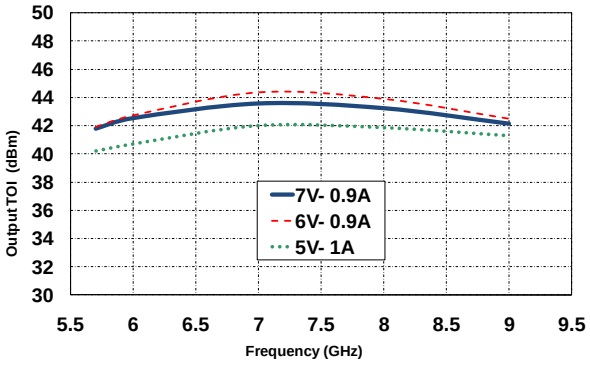
Power at 1dB vs Vd at 0.9A



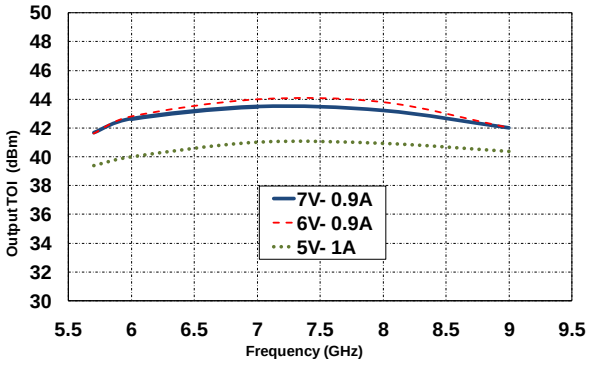
Power at 1dB vs Vd at 1A



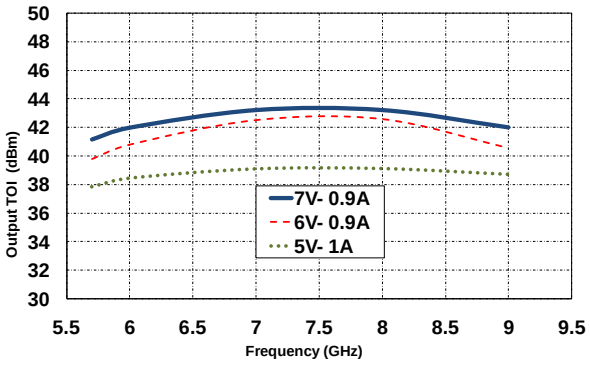
Output TOI at Pout/ Tone= 7dBm



Output TOI at Pout/ Tone= 13dBm



Output TOI at Pout/ Tone= 19dBm



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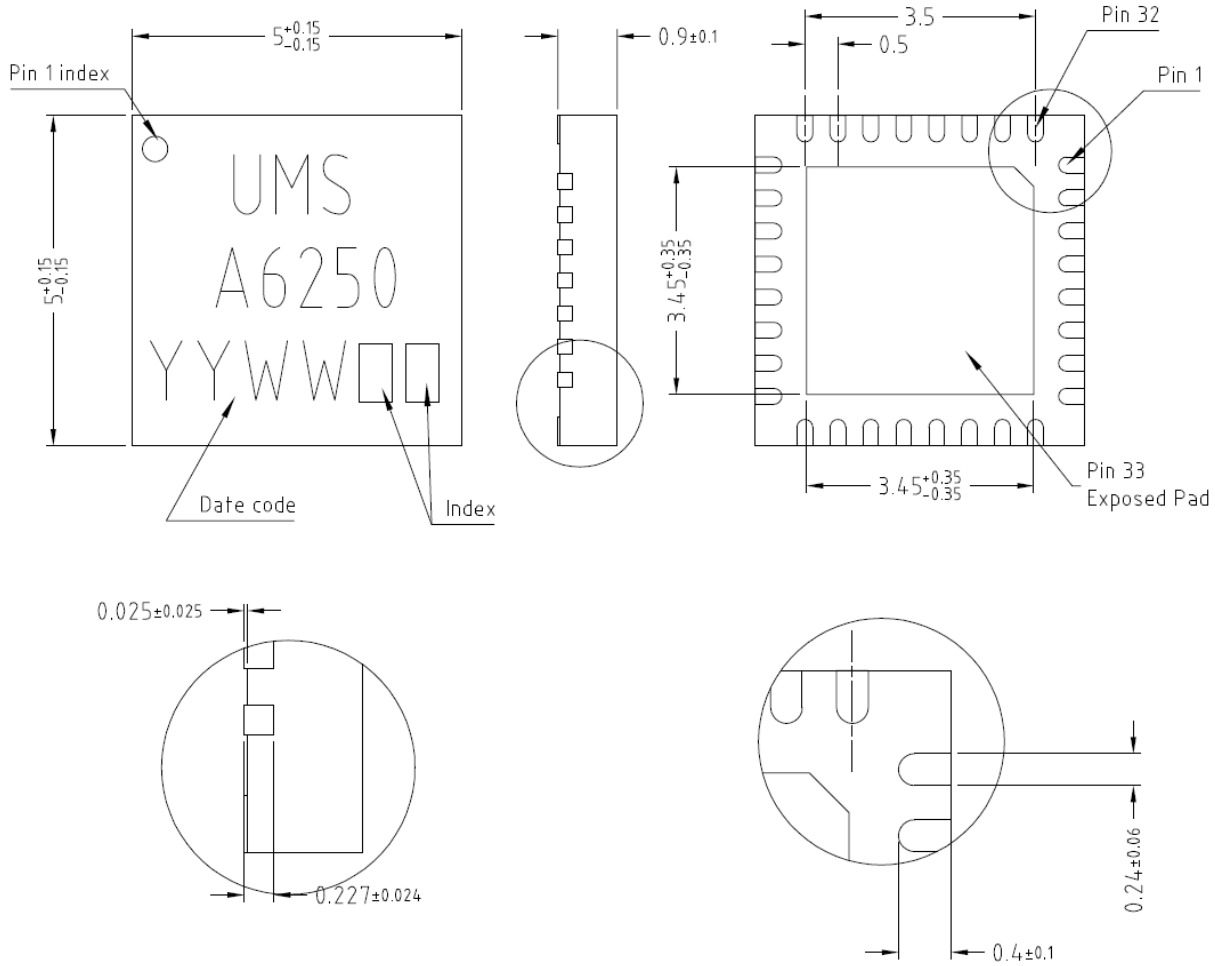
Package outline (1)



Matt tin, Lead Free	(Green)	1- Nc	12- Gnd(2)	23- Nc
Units :	mm	2- Nc	13- VG	24- Nc
From the standard :	JEDEC MO-220	3- Gnd(2)	14- Nc	25- VD3
	(VGGD)	4- RF IN	15- Nc	26- Gnd(2)
33- GND		5- Gnd(2)	16- Nc	27- Nc
		6- Nc	17- Nc	28- VD2
		7- Nc	18- Nc	29- Gnd(2)
		8- Nc	19- Nc	30- VD1
		9- Nc	20- Gnd(2)	31- Nc
		10- Nc	21- RF OUT	32- Nc
		11- Nc	22- Gnd(2)	

(1) The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (http://www.ums-gaas.com) for exact package dimensions.

(2) It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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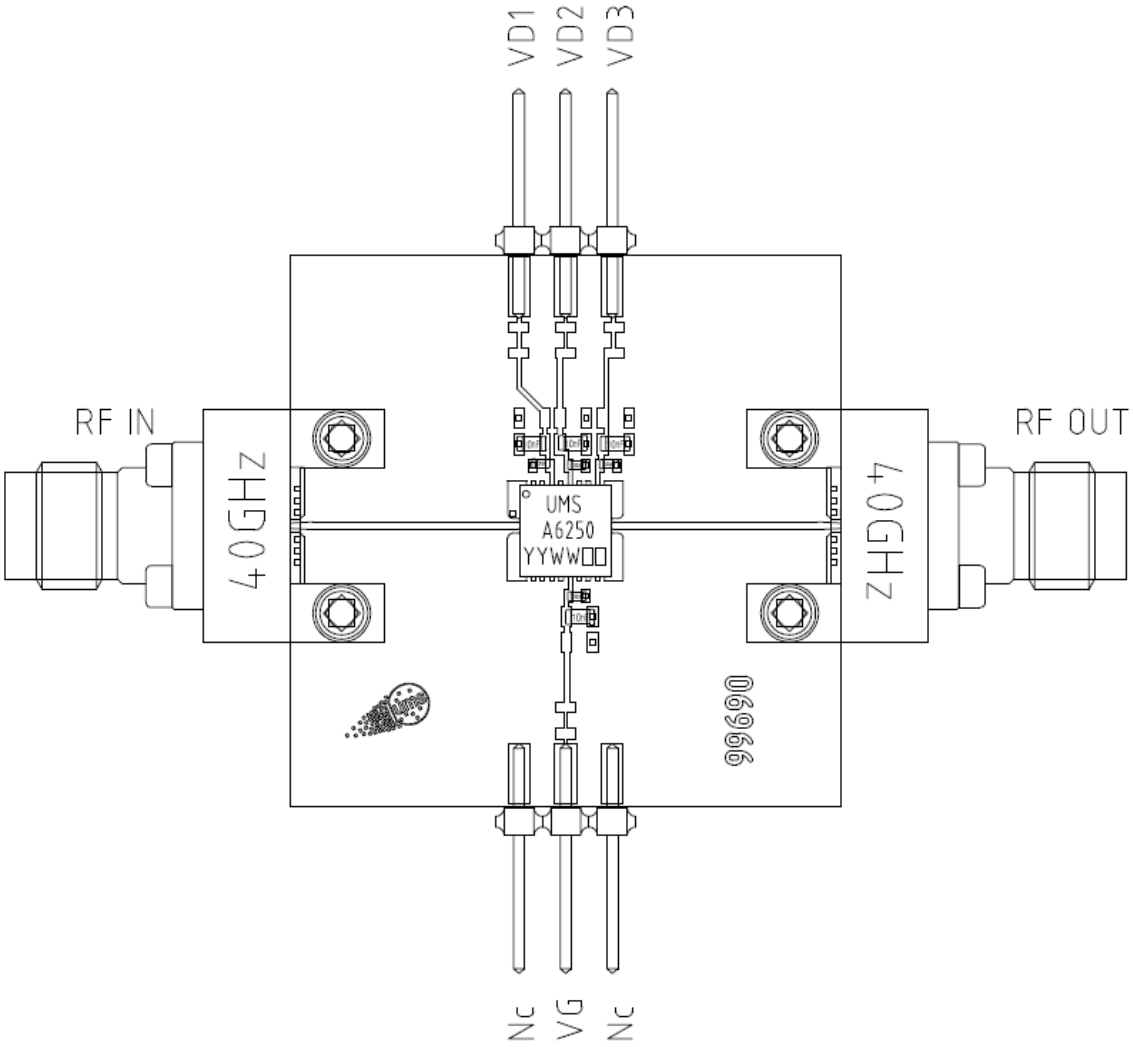
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board. Module should be designed to dissipate around 6.3W
- First decoupling network is done with 100pF capacitors, second decoupling network is done with 10nF capacitors.
- See application note AN0017 for details.



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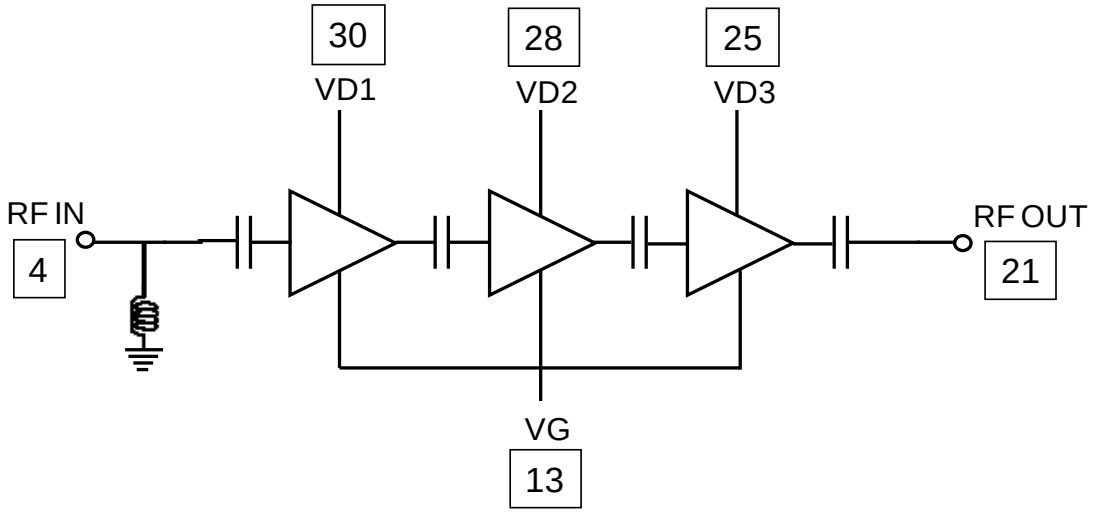
Notes

Due to ESD protection circuits on RF input, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF access.



The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling (100pF & 10nF) on the PC board, as close as possible to the package.

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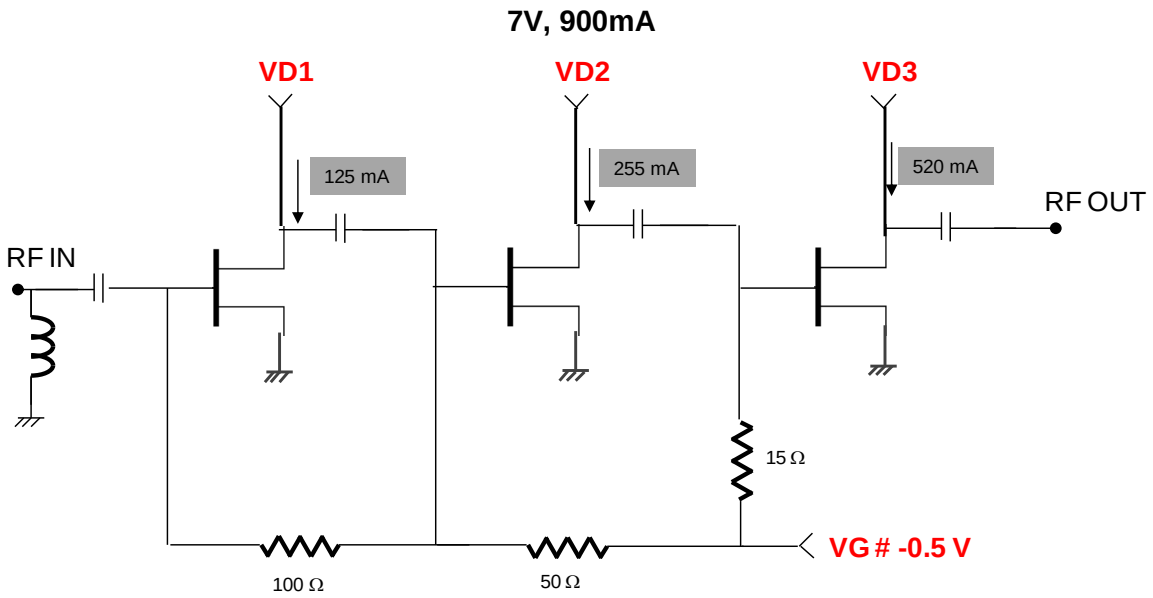
DC Schematic



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Note

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Recommended package footprint

Refer to the application note AN0017 available at http://www.ums-gaas.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 5x5 RoHS compliant package:	CHA6250-QFG/XY	
	Stick: XY = 20	Tape & reel: XY = 21

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