**Philips Components**

| Data sheet | |
|---|---|
| **status** | Product specification |
| **date of issue** | June 1990 |

# FCB61C65(L/LL)

## 8 K x 8 Fast CMOS low-power static RAM

### FEATURES

- Operating supply voltage 5 V ± 10%
- Inputs and outputs ESD protected
- Automatic power-down after a completed read access
- Access time: 55 ns and 70 ns
- Low current consumption:
  - active 70 mA max.
  - standby (TTL) 3 mA max.
  - standby (CMOS) 100 µA max. (L-version)
  - standby (CMOS) 1 µA max. (LL-version)
- Suitable for battery back-up operation: (FCB61C65L/LL only)
  - data retention voltage 2 V min.
  - data retention current 50 µA max. (L-version)
  - data retention current 1 µA max. (LL-version)
- Latched data outputs giving stable data between consecutive accesses
- Easy memory expansion
- Common data I/O interface
- All inputs and outputs TTL and CMOS compatible
- All inputs have a Schmitt trigger switching action
- Three-state outputs
- Operating temperature 0 C to +70 C

### GENERAL DESCRIPTION

The FCB61C65(L/LL) is a 65536-bit fast, low-power, static random access memory organized as 8192 words of 8 bits each.

The chip enable inputs $\overline{CE}1$ and CE2 are available for memory expansion and to control the low-power/ standby mode.

The device operates from a 5 V power supply and has an access time of 55 ns and 70 ns.

The FCB61C65(L/LL) is ideally suited for memory applications where fast access time, low power and ease of use are required.

The FCB61C65(L/LL) is a CMOS device which uses a 6 transistor memory cell.

The IC is fabricated in a CMOS double-metal single-poly process using ion-implanted silicon gate technology.

### ORDERING AND PACKAGE INFORMATION

| EXTENDED TYPE NUMBER | PACKAGE | | | |
|---|---|---|---|---|
| | PINS | PIN POSITION | MATERIAL | CODE |
| FCB61C65 (L/LL)-XXP | 28 | DIL (600 mil) | plastic | SOT117 |
| FCB61C65 (L/LL)-XXT | 28 | SOXL (330 mil) | plastic | SOT213 |

# 8 K x 8 Fast CMOS low-power static RAM FCB61C65(L/LL)

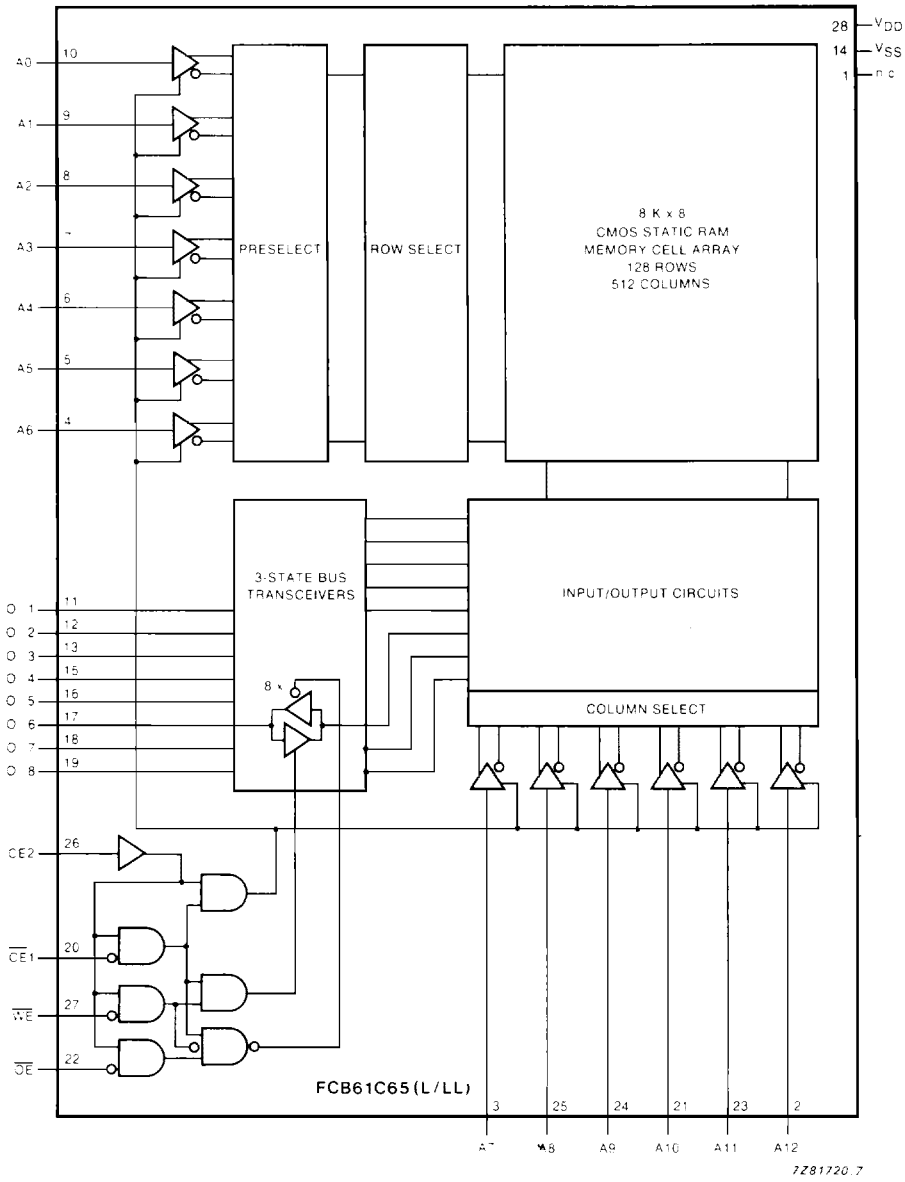



Fig.1 Block diagram.

# 8 K x 8 Fast CMOS low-power static RAM

# FCB61C65(L/LL)

## TRUTH TABLE

| $\overline{CE1}$ | CE2 | $\overline{OE}$ | $\overline{WE}$ | MODE | $I_{DD}$ | I/O PIN | REF. CYCLE |
|---|---|---|---|---|---|---|---|
| H | X | X | X | not selected | $I_{SB}$* | HIGH Z | |
| X | L | X | X | not selected | $I_{SB}$* | HIGH Z | |
| L | H | L | H | read | $I_{DD}/I_{DD1}$* | D OUT | read |
| L | H | H | L | write | $I_{DD}$ | D IN | write |
| L | H | L | L | write | $I_{DD}$ | D IN | write |
| L | H | H | H | ready-read | $I_{DD}/I_{DD1}$* | HIGH Z | |

* Including L/LL versions if input levels are CMOS.

## PINNING

| SYMBOL | PIN | DESCRIPTION |
|---|---|---|
| n.c. | 1 | not connected |
| A12 | 2 | address input |
| A7 to A0 | 3 to 10 | address inputs |
| I/O 1 to I/O 3 | 11 to 13 | data inputs/outputs |
| $V_{SS}$ | 14 | ground |
| I/O 4 to I/O 8 | 15 to 19 | data inputs/outputs |
| $\overline{CE1}$ | 20 | chip enable 1 |
| A10 | 21 | address input |
| $\overline{OE}$ | 22 | output enable |
| A11, A9, A8 | 23 to 25 | address inputs |
| CE2 | 26 | chip enable 2 |
| $\overline{WE}$ | 27 | write enable |
| $V_{DD}$ | 28 | +5 V supply |

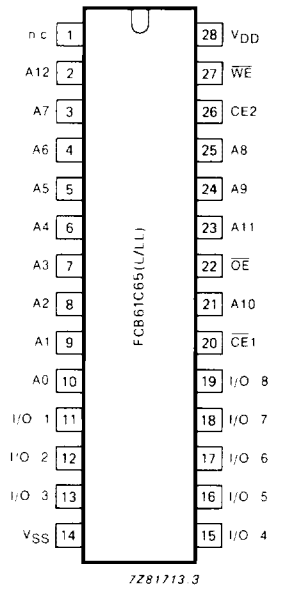



Fig.2 Pinning diagram.

## DECOUPLING ARRANGEMENTS

The FCB61C65(L/LL) is an address activated circuit. When an address change occurs, the operation is executed by an internal pulse generated from the Address Transition Detector (ATD). The current variation following an address or chip enable change may induce noise on the supply lines. This noise can be eliminated using a 100 nF capacitor with good high frequency characteristics as close as possible to the memory between $V_{DD}$ and $V_{SS}$.

## LIMITING VALUES

Limiting values are in accordance with the Absolute Maximum System (IEC 134)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_I$ | voltage range on any pin with respect to $V_{SS}$ | DC inputs | −0.5 | +7.0 | V |
| $V_I$ | | max. pulse width = 50 ns | −1.5 | +7.0 | V |
| $T_{amb}$ | operating ambient temperature | | 0 | +70 | °C |
| $T_{bias}$ | temperature range with bias | | −10 | +85 | °C |
| $T_{stg}$ | storage temperature range | | −55 | +125 | °C |
| $P_{tot}$ | total power dissipation | | - | 1 | W |

### Note

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to operation under the conditions specified in the DC and timing characteristics. Exposure to higher than the rated voltages for extended periods of time could effect device reliability.

## HANDLING

Input and outputs are protected against electro static discharge in normal handling, however, to be totally safe it is desirable to take normal precautions appropriate to handling MOS devices.

## RECOMMENDED OPERATION CONDITIONS

$T_{amb}$ = 0 to +70 °C

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| $V_{DD}$ | supply voltage | 4.5 | 5.5 | V |
| $V_{IH}$ | input voltage HIGH | 2.2 | $V_{DD}$+0.5 | V |
| $V_{IL}$ | input voltage LOW | −0.5* | 0.8 | V |

* $V_{IL}$ = −1.5 V for a maximum pulse width of 50 ns.

## DC CHARACTERISTICS

$V_{DD}$ = 5 V ± 10%; $T_{amb}$ = 0 to 70 °C. Typical readings taken at $V_{DD}$ = 5 V; $T_{amb}$ = 25 °C. All voltages are referenced to $V_{SS}$ (0 V) unless otherwise specified. DC characteristics are valid after thermal equilibrium has been established.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_{LI}$ | input leakage current | $V_I = V_{SS}$ to $V_{DD}$ | −1 | - | 1 | µA |
| $I_{LO}$ | output leakage current | $\overline{CE1}$ or $\overline{OE}$ = $V_{IH}$ or CE2 = $V_{IL}$; $V_{I/O} = V_{SS}$ to $V_{DD}$ | −1 | - | 1 | µA |
| $I_{DD}$ | average operating current | cycle time 55 ns; 100% duty factor; note 1 $I_{I/O}$ = 0 mA | - | 40 | 70 | mA |
| $I_{DD}$ | average operating current | cycle time 70 ns; 100% duty factor; note 1 $I_{I/O}$ = 0 mA | - | 35 | 60 | mA |
| $I_{DD1}$ | DC operating current | $\overline{WE}$ = $V_{IH}$; $I_{I/O}$ = 0 mA; f = 0 Hz | - | 3 | 6 | mA |
| | | $\overline{WE}$ = CMOSH; $V_I$ = CMOS; note 2 | | | | |
| $I_{DDL}$ | FCB61C65L only | | - | 2 | 100 | µA |
| $I_{DDLL}$ | FCB61C65LL only | | - | 0.05 | 1.0 | µA |
| $I_{SB}$ | standby current | $\overline{CE1}$ = $V_{IH}$ or CE2 = $V_{IL}$ | - | 1.5 | 3.0 | mA |
| | | $\overline{CE1}$ = CMOSH and CE2 = CMOS or CE2 = CMOSL | | | | |
| $I_{SBL}$ | FCB61C65L only | | - | 2 | 100 | µA |
| $I_{SBLL}$ | FCB61C65LL only | | - | 0.05 | 1.0 | µA |
| $V_{OL}$ | output voltage LOW | $I_{OL}$ = 4 mA | - | - | 0.4 | V |
| $V_{OL}$ | output voltage LOW | $I_{OL}$ = 20 µA | - | - | 0.2 | V |
| $V_{OH}$ | output voltage HIGH | $I_{OH}$ = −1 mA | 2.4 | - | - | V |
| $V_{OH}$ | output voltage HIGH | $I_{OH}$ = −20 µA | $V_{DD}$−0.2 | - | - | V |

### Notes to the DC characteristics

1. $I_{DD} \leq 50$ mA at a cycle time of 100 ns and $\leq 45$ mA at a cycle time of 120 ns.

2. CMOS = CMOSH: $V_{DD} - 0.2\ V \leq$ level $\leq V_{DD} + 0.2\ V$ or
   CMOSL: $-0.2\ V \leq$ level $\leq +0.2\ V$.

## CAPACITANCES

f = 1 MHz; $T_{amb}$ = 25 °C (parameters in this table are sampled and not 100% tested).

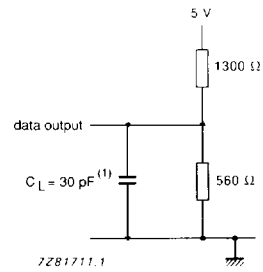
| SYMBOL | PARAMETER | CONDITIONS | MAX. | UNIT |
|---|---|---|---|---|
| | input capacitance | | | |
| $C_I$ | $\overline{CE1}$, CE2, $\overline{WE}$, $\overline{OE}$ | $V_I$ = 0 V | 8 | pF |
| $C_I$ | all other inputs | $V_I$ = 0 V | 7 | pF |
| $C_{I/O}$ | input/output capacitance | $V_{I/O}$ = 0 V | 8 | pF |

## TIMING CHARACTERISTICS

$V_{DD}$ = 5 V ± 10%; $T_{amb}$ = 0 to 70 °C; inputs pulse levels = 0.4 to 2.4 V; input rise and fall times = 5 ns; input and output timing reference levels = 1.5 V and output loading as in Figure 3; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | 55 TYPE | | 70 TYPE | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | |
| **Read cycle** | | | | | | | |
| $t_{RC}$ | read cycle time | | 55 | - | 70 | - | ns |
| $t_{AA}$ | address access time | | - | 55 | - | 70 | ns |
| $t_{ACE}$ | chip enable access time | | - | 55 | - | 70 | ns |
| $t_{OE}$ | output enable access time | | - | 30 | - | 35 | ns |
| $t_{CLZ}$ | chip enable to output LOW Z | note 6 | 5 | - | 5 | - | ns |
| $t_{OLZ}$ | output enable to output LOW Z | note 6 | 5 | - | 5 | - | ns |
| $t_{CHZ}$ | chip disable to output HIGH Z | note 6 | - | 30 | - | 30 | ns |
| $t_{OHZ}$ | output disable to output HIGH Z | note 6 | - | 30 | - | 30 | ns |
| $t_{OH}$ | output hold time | | 10 | - | 10 | - | ns |
| **Write cycle** | | | | | | | |
| $t_{WC}$ | write cycle time | | 55 | - | 70 | - | ns |
| $t_{CW}$ | chip enable to end of write | note 11 | 50 | - | 65 | - | ns |
| $t_{AW}$ | address valid to end of write | | 50 | - | 65 | - | ns |
| $t_{AS}$ | address set up time | | 0 | - | 0 | - | ns |
| $t_{WP}$ | write pulse width | note 9 | 30 | - | 35 | - | ns |
| $t_{WR}$ | write recovery time | note 10 | 0 | - | 0 | - | ns |
| $t_{WHZ}$ | write enable to output HIGH Z | note 16 | - | 20 | - | 25 | ns |
| $t_{DW}$ | data to write time overlap | | 25 | - | 30 | - | ns |
| $t_{DH}$ | data hold from write time | | 5 | - | 5 | - | ns |
| $t_{OW}$ | end of write to output LOW Z | note 16 | 5 | - | 5 | - | ns |

### Output load




(1) $C_L$ = 5 pF for $t_{CLZ}$, $t_{CHZ}$, $t_{WHZ}$, $t_{OLZ}$, $t_{OHZ}$ and $t_{OW}$.

Fig.3 Output load.

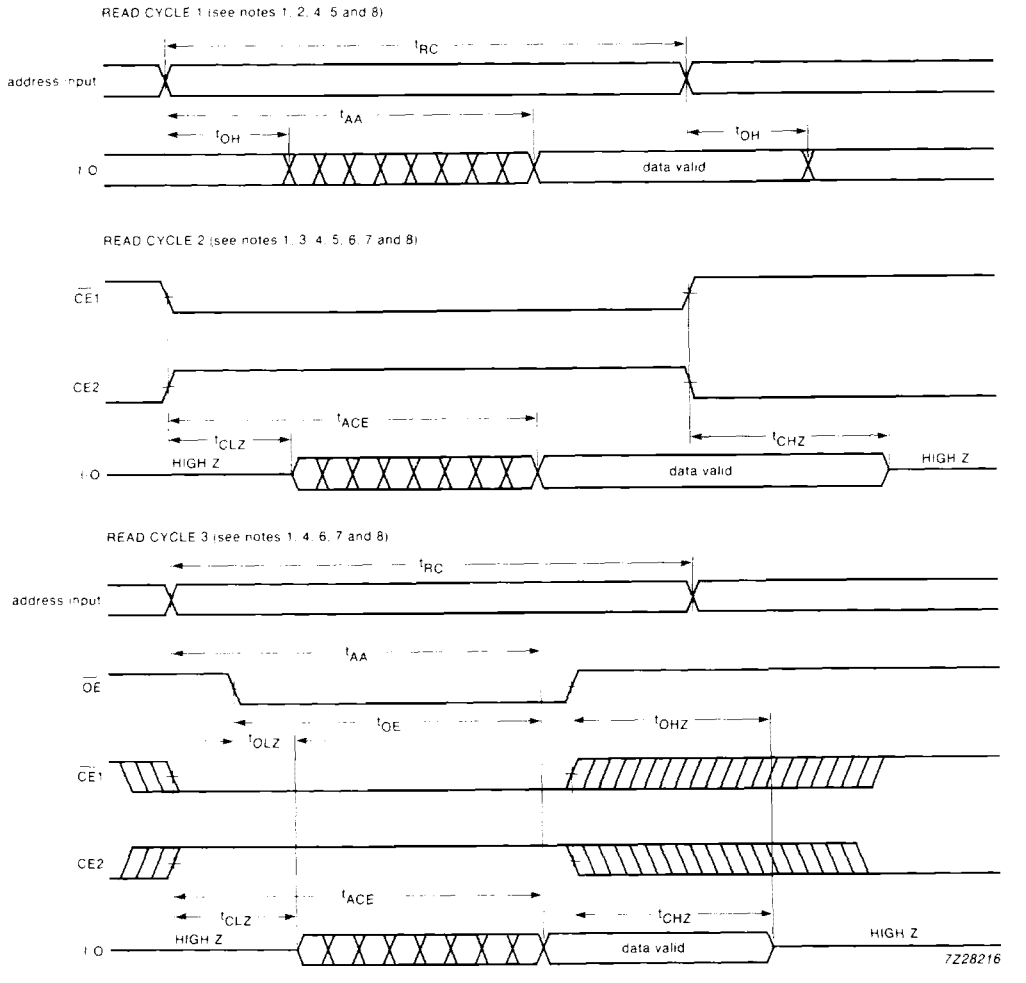



Fig.4 Read cycle timing.

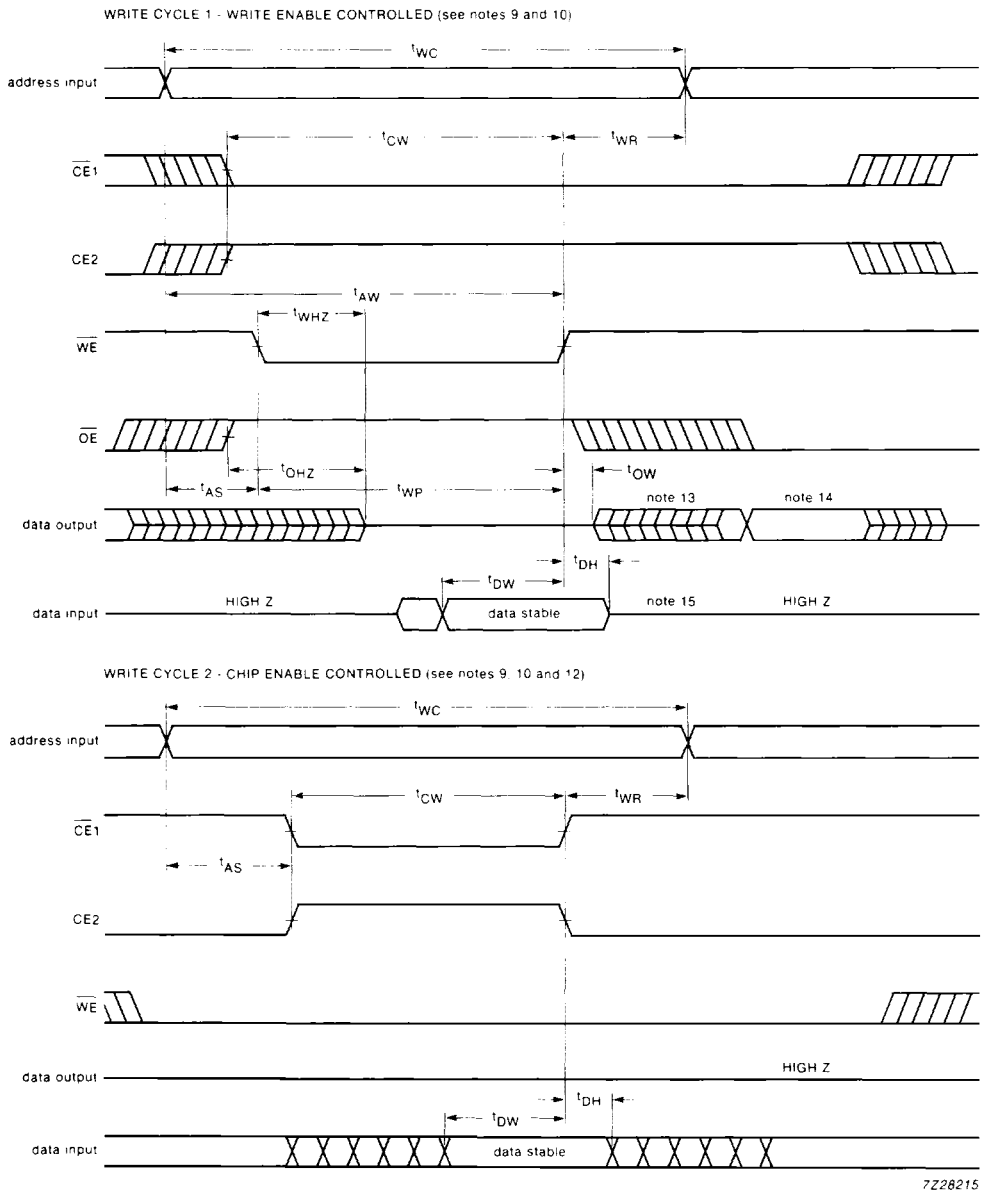



Fig.5 Write cycle timing.

### Notes to the timing characteristics

**Read cycle** (see Fig.4)

1. $\overline{WE}$ is HIGH for read cycle.
2. Device is continuously selected, $\overline{CE}1$ is LOW and CE2 is HIGH.
3. Address is valid prior to or coincident with $\overline{CE}1$ LOW or CE2 HIGH transition.
4. When $\overline{CE}1$ is LOW and CE2 HIGH, the address inputs may not be floating.
5. $\overline{OE}$ is LOW.
6. $C_L$ = 5 pF for $t_{CLZ}$, $t_{CHZ}$, $t_{OLZ}$, output transition measured at ± 200 mV from preceding steady state. These parameters are sampled and not 100% tested.
7. $t_{CLZ}$ and $t_{ACE}$ are measured from the last $\overline{CE}1$ going LOW or CE2 going HIGH. $t_{CHZ}$ is measured from the first of $\overline{CE}1$ going HIGH or CE2 going LOW.
8. If D OUT in two consecutive read cycles is the same, D OUT remains stable.

**Write cycle** (see Fig.5)

9. A write occurs during an overlap of LOW $\overline{CE}1$, a HIGH CE2 and a LOW $\overline{WE}$.
10. $t_{WR}$ is measured from the earlier of CE2 going to LOW or $\overline{CE1}$ or $\overline{WE}$ going HIGH at the end of a write cycle.
11. If the $\overline{CE}1$/CE2 transition occurs simultaneously to or after the $\overline{WE}$ LOW transition the outputs remain in a high impedance state.
12. $\overline{OE}$ is continuously LOW.
13. D OUT is in the same phase as the write data of this write cycle.
14. D OUT is the read data of the next address.
15. If $\overline{CE}1$ is LOW (CE2 is HIGH) and I/O pins are in the output state during this period then input data signals of opposite phase to the outputs must not be applied.
16. $C_L$ = 5 pF for $t_{WHZ}$ and $t_{OW}$, measured at ± 200 mV from steady state. These parameters are sampled and not 100% tested.

## DATA RETENTION CHARACTERISTICS FOR LOW POWER/STANDBY MODE

(FCB61C65L/LL only)

$T_{amb}$ = 0 to +70 °C; $I_{DRL/LL}$ measurements are valid after thermal equilibrium has been established.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Supply** | | | | | | |
| $V_{DR}$ | supply voltage for data retention | $\overline{CE}1$ = CMOSH or CE2 = CMOSL with other $V_I$ = CMOS; note 1 | 2.0 | - | 5.5 | V |
| | supply current during data retention | $V_{DR}$ = 3 V; CE2 = CMOSL; other $V_I$ = CMOS or $\overline{CE}1$ = CMOSH; other $V_I$ = CMOS | | | | |
| $I_{DRL}$ | FCB61C65L only | | - | 2 | 50 | µA |
| $I_{DRLL}$ | FCB61C65LL only | | - | 0.05 | 1 | µA |
| **Timing** | | | | | | |
| $t_{CDR}$ | chip disable to data retention time | | 0 | - | - | ns |
| $t_R$ | recovery time to fully active | note 2 | $t_{RC}$ | - | - | ns |

**Notes to the data retention characteristics**

1. CMOS = CMOSH: $V_{DR} - 0.2\ V \leq$ level $\leq V_{DR} + 0.2\ V$ or
   CMOSL: $-0.2\ V \leq$ level $\leq +0.2\ V$.

2. $t_{RC}$ = read cycle time.

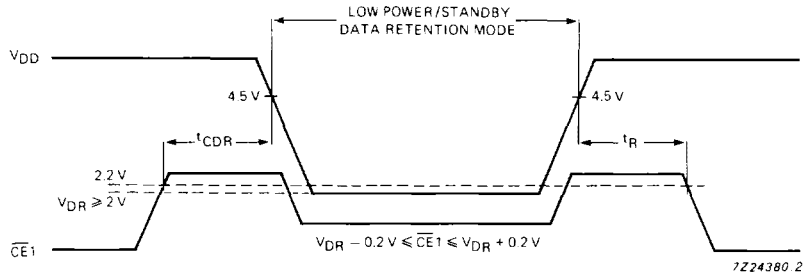



Fig.6 Data retention waveform ($\overline{CE}1$ controlled).

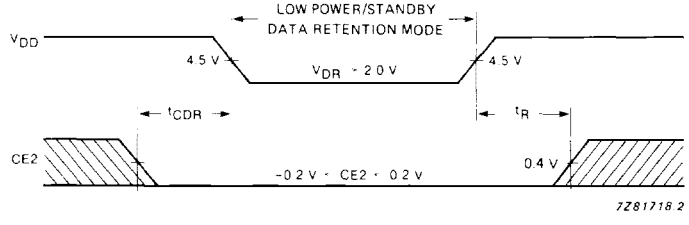



Fig.7 Data retention waveform (CE2 controlled).