



**GoldStar**  
GOLDSTAR ELECTRON CO., LTD.

## GM76C256/L/LL

32,768 WORDS  $\times$  8 BIT  
CMOS STATIC RAM

### Description

The GM76C256/L/LL is a 262,144 bit static random access memory organized as 32,768 words by 8 bits using CMOS technology, and operated from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 70mA (max) at minimum cycle time of 85ns.

When  $\overline{CS}$  is a logical high, the device is placed in low power standby mode in which standby current is 2mA (max).

The GM76C256/L/LL has two control inputs. Chip select ( $\overline{CS}$ ) allows for device selection and data retention control, and output enable ( $\overline{OE}$ ) provides fast memory access.

Thus the GM76C256/L/LL is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required. The GM76C256/L/LL is offered in 28 pin DIP (600 mil) and SOP (330mil).

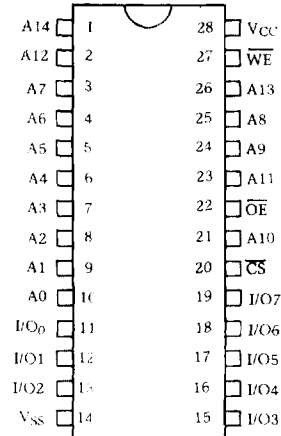
### Features

- High Speed: Fast Access and Cycle Time 85/100 Max.
- Low Power Standby and Low Power Operation; Standby: 0.55mW Max. (Low Power Version) Standby: 0.17mW Max. (Low Low Power Version)
- Operation: 335mW Max.
- Completely Static RAM: No Clock or Timing Strobe Required
- Equal Access and Cycle Time
- Capability of Battery Back up Operation
- Standard 28 DIP and SOP

### Pin Description

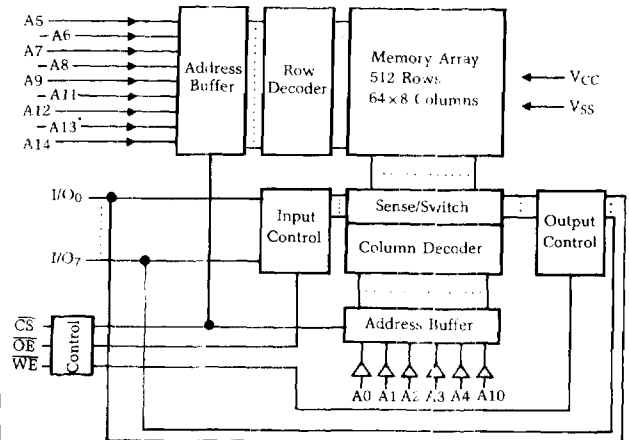
| Pin             | Function            |
|-----------------|---------------------|
| A0 ~ A14        | Address Input       |
| $\overline{WE}$ | Write Enable Input  |
| $\overline{OE}$ | Output Enable Input |
| $\overline{CS}$ | Chip Select Input   |
| I/O0 ~ I/O7     | Data Input/Output   |
| V <sub>CC</sub> | Power Supply +5V    |
| V <sub>SS</sub> | Ground              |

### Pin Configuration



(Top View)

### Block Diagram



## Absolute Maximum Ratings\*

| Symbol           | Parameter                      | Rating                       | Unit  |
|------------------|--------------------------------|------------------------------|-------|
| T <sub>A</sub>   | Ambient Temperature under Bias | 0 ~ 70                       | °C    |
| T <sub>STG</sub> | Storage Temperature            | -65 ~ 150                    | °C    |
| T <sub>SOL</sub> | Soldering Temperature and Time | 260, 10 (at lead)            | °C, S |
| V <sub>CC</sub>  | Supply Voltage                 | -0.3 ~ 7.0                   | V     |
| V <sub>IN</sub>  | Input Voltage                  | -0.3* ~ 7.0                  | V     |
| V <sub>I/O</sub> | Input and Output Voltage       | -0.5 ~ V <sub>CC</sub> + 0.5 | V     |
| P <sub>D</sub>   | Power Dissipation              | 1.0                          | W     |

\*: -3.0V at pulse width 50ns Max.

Recommended Operating Conditions (T<sub>A</sub> = 0 ~ 70°C)

| Symbol          | Parameter                     | Min  | Typ | Max | Unit |
|-----------------|-------------------------------|------|-----|-----|------|
| V <sub>CC</sub> | Supply Voltage                | 4.5  | 5.0 | 5.5 | V    |
| V <sub>IH</sub> | Input High Voltage            | 2.2  | —   | 6.0 | V    |
| V <sub>IL</sub> | Input Low Voltage             | -0.3 | —   | 0.8 | V    |
| V <sub>DR</sub> | Data Retention Supply Voltage | 2.0  | —   | 5.5 | V    |

## Truth Table

| $\overline{\text{CS}}$ | $\overline{\text{WE}}$ | $\overline{\text{OE}}$ | Input/Outputs | Mode                |
|------------------------|------------------------|------------------------|---------------|---------------------|
| H                      | X                      | X                      | High-Z        | Deselect Power Down |
| L                      | H                      | L                      | Data Out      | Read                |
| L                      | L                      | X                      | Data In       | Write               |
| L                      | H                      | H                      | High-Z        | Deselect            |

Note: X means don't care.

DC Electrical Characteristics: (V<sub>CC</sub> = 5V ± 10%, T<sub>A</sub> = 0 ~ 70°C)

| Symbol            | Parameter                              | Test Conditions                                                                                                                                                                                        | Min | Typ | Max            | Unit           |
|-------------------|----------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|----------------|----------------|
| V <sub>OH</sub>   | Output High Voltage                    | I <sub>OH</sub> = -1.0mA                                                                                                                                                                               | 2.4 | —   | —              | V              |
| V <sub>OL</sub>   | Output Low Voltage                     | I <sub>OL</sub> = 2.1mA                                                                                                                                                                                | —   | —   | 0.4            | V              |
| I <sub>IL</sub>   | Input Leakage Current                  | V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>                                                                                                                                                    | -2  | —   | +2             | μA             |
| I <sub>OL</sub>   | Output Leakage Current                 | $\overline{\text{CS}} = \text{V}_{\text{IH}}$ or $\overline{\text{WE}} = \text{V}_{\text{IL}}$ or $\overline{\text{OE}} = \text{V}_{\text{IH}}$ , V <sub>SS</sub> ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> | -2  | —   | +2             | μA             |
| I <sub>CCS1</sub> | Stand-by Power Supply Current          | $\overline{\text{CS}} = \text{V}_{\text{IH}}$                                                                                                                                                          | —   | —   | 2              | mA             |
| I <sub>CCS2</sub> |                                        | $\overline{\text{CS}} \geq \text{V}_{\text{CC}} - 0.2\text{V}$<br>GM76C256<br>GM76C256L<br>GM76C256LL                                                                                                  | —   | 2*  | 1<br>100<br>30 | mA<br>μA<br>μA |
| I <sub>CC</sub>   | Operating Supply Current               | $\overline{\text{CS}} = \text{V}_{\text{IL}}$ , V <sub>I/O</sub> = 0mA                                                                                                                                 | —   | —   | 45             | mA             |
| I <sub>CC1</sub>  | Average Operating Power Supply Current | Min. Cycle, duty = 100%<br>I <sub>I/O</sub> = 0mA                                                                                                                                                      | —   | —   | 70             | mA             |

\*TYP Values are measured at 25°C, V<sub>CC</sub> = 5V

AC Operating Characteristics ( $V_{CC} = 5V \pm 10\%$ ,  $T_A = 0 \sim 70^\circ C$ )

### Read Cycle

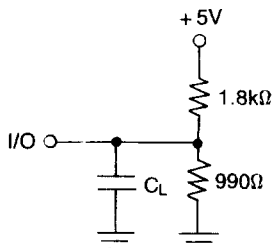
| Symbol    | Parameter                            | Conditions | GM76C256L-85 |     | GM76C256L-10 |     | Unit |
|-----------|--------------------------------------|------------|--------------|-----|--------------|-----|------|
|           |                                      |            | Min          | Max | Min          | Max |      |
| $t_{RC}$  | Read Cycle Time                      | *1         | 85           | —   | 100          | —   | ns   |
| $t_{AA}$  | Address Access Time                  |            | —            | 85  | —            | 100 | ns   |
| $t_{ACS}$ | Chip Select Access Time              |            | —            | 85  | —            | 100 | ns   |
| $t_{OE}$  | Output Enable to Output Valid        |            | —            | 45  | —            | 50  | ns   |
| $t_{OH}$  | Output Hold from Address Change      |            | 5            | —   | 10           | —   | ns   |
| $t_{CLZ}$ | Chip Selection to Output in Low-Z    | *2         | 10           | —   | 10           | —   | ns   |
| $t_{OLZ}$ | Output Enable to Output in Low-Z     |            | 5            | —   | 5            | —   | ns   |
| $t_{CHZ}$ | Chip Deselection to Output in High-Z |            | 0            | 30  | 0            | 35  | ns   |
| $t_{OHZ}$ | Output Disable to Output in High-Z   |            | 0            | 30  | 0            | 35  | ns   |

### Write Cycle

| Symbol    | Parameter                       | Conditions | GM76C256L-85 |     | GM76C256L-10 |     | Unit |
|-----------|---------------------------------|------------|--------------|-----|--------------|-----|------|
|           |                                 |            | Min          | Max | Min          | Max |      |
| $t_{WC}$  | Write Cycle Time                | *1         | 85           | —   | 100          | —   | ns   |
| $t_{CW}$  | Chip Selection to End of Write  |            | 75           | —   | 80           | —   | ns   |
| $t_{AW}$  | Address Valid to End of Write   |            | 75           | —   | 80           | —   | ns   |
| $t_{AS}$  | Address Setup Time              |            | 0            | —   | 0            | —   | ns   |
| $t_{WP}$  | Write Pulse Width               |            | 60           | —   | 60           | —   | ns   |
| $t_{WR}$  | Write Recovery Time             |            | 5            | —   | 5            | —   | ns   |
| $t_{DW}$  | Data to Write Time Overlap      |            | 40           | —   | 40           | —   | ns   |
| $t_{DH}$  | Data Hold from Write Time       |            | 0            | —   | 0            | —   | ns   |
| $t_{WHZ}$ | Write to Output in High-Z       | *2         | 0            | 30  | 0            | 35  | ns   |
| $t_{OW}$  | Output Active from End of Write |            | 5            | —   | 5            | —   | ns   |

**\*1 Test Conditions**

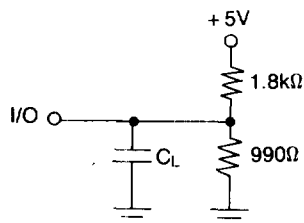
1. Input pulse level: 0.6V to 2.4V
2.  $t_r = t_f = 5\text{ns}$
3. Input and output timing reference levels: 1.5V
4. Output load  $C_L = 100\text{pF}$



$C_L = 100\text{pF}$  (Includes Jig Capacitance)

**\*2 Test Conditions**

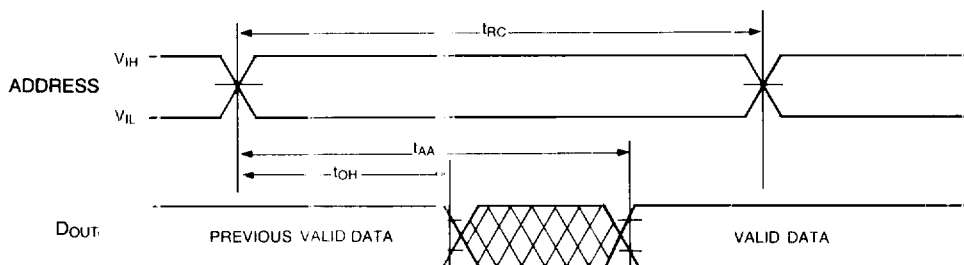
1. Input pulse level: 0.6V to 2.4V
2.  $t_r = t_f = 5\text{ns}$
3. Input timing reference levels: 1.5V
4. Output timing reference levels:  
±200mV (the level displaced from stable output voltage level)
5. Output load  $C_L = 5\text{pF}$



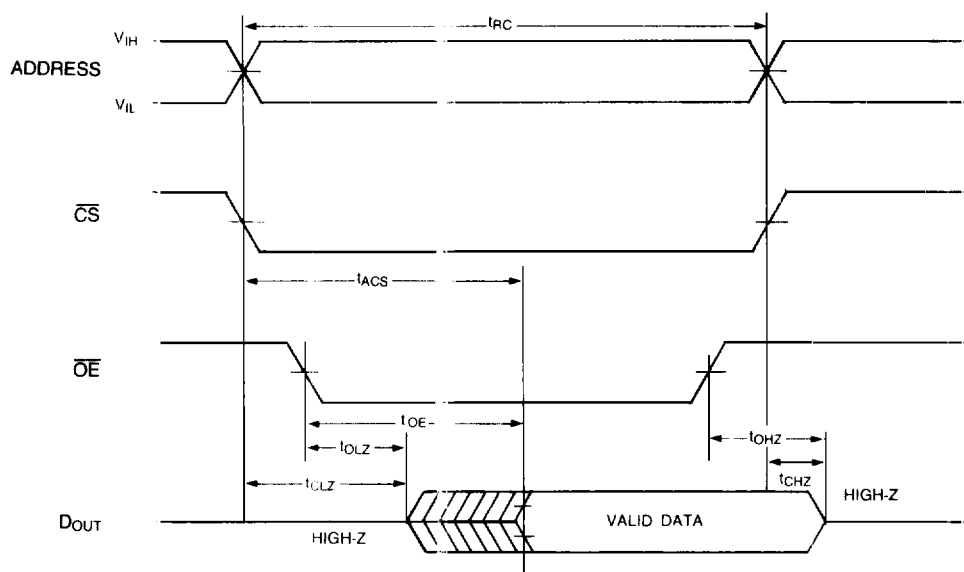
$C_L = 5\text{pF}$  (Includes Jig Capacitance)

## TIMING WAVEFORMS

## Read Cycle 1 (Notes 1, 3)

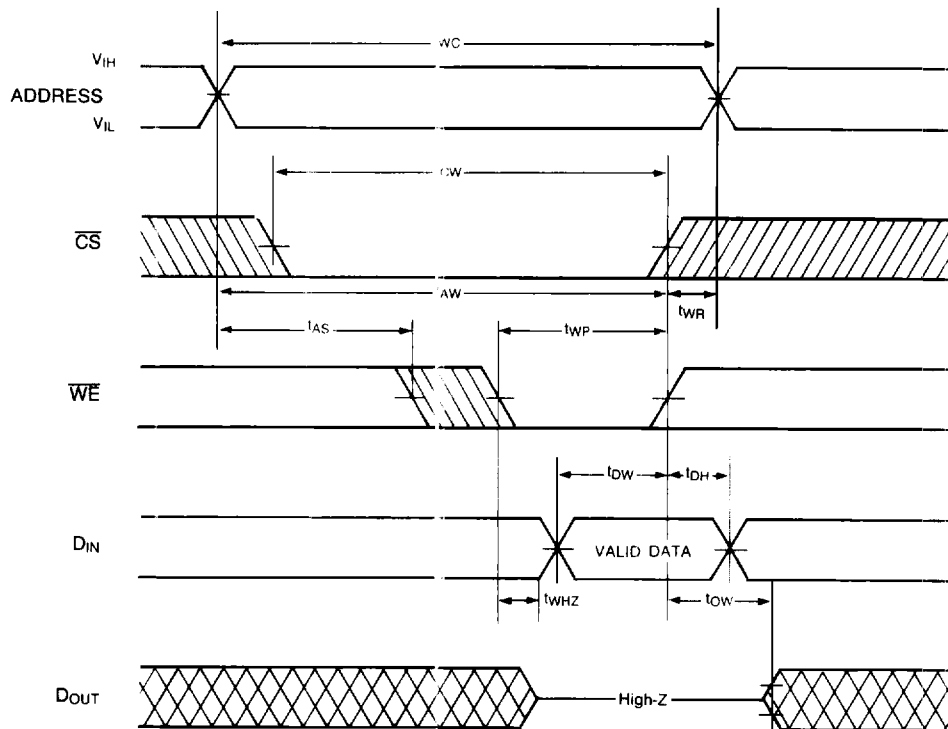


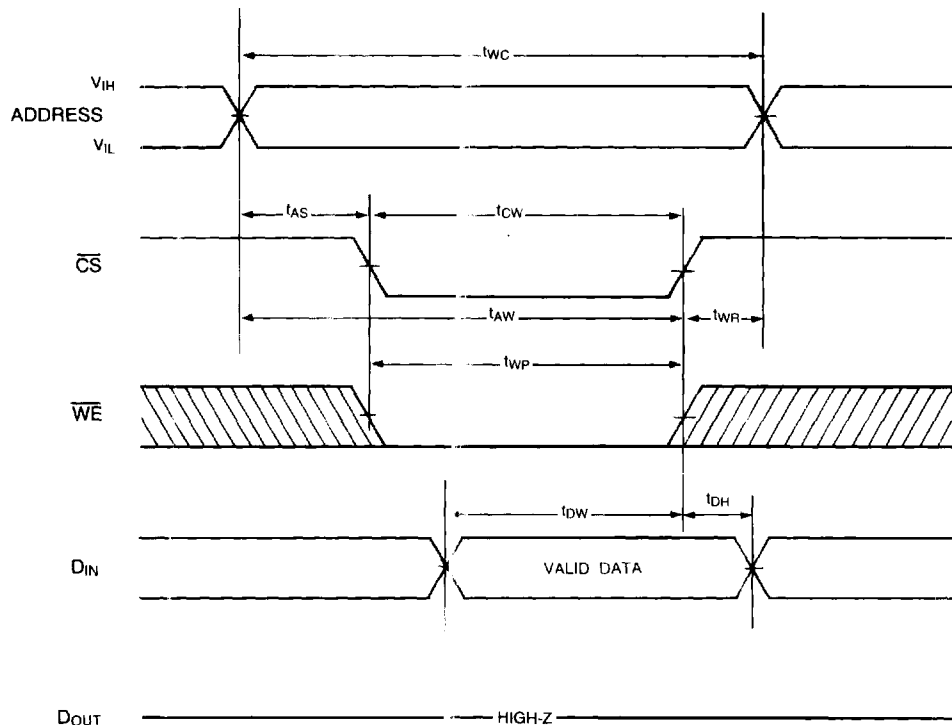
## Read Cycle 2 (Notes 2, 3)



## Notes:

1. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CS} = V_{IL}$ .
2. Address valid prior to or coincident with  $\overline{CS}$  transition low.
3.  $\overline{WE}$  is high for read cycle.

Write Cycle 1 ( $\overline{WE}$  Controlled) (Note 1, 2)

Write Cycle 2 ( $\overline{\text{CS}}$  Controlled) (Note 1, 2, 3)

## Notes:

1. The internal write time of the memory is defined by the overlap of  $\overline{\text{CS}}$  low and  $\overline{\text{WE}}$  low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
2. Data I/O is high impedance if  $\overline{\text{OE}} = V_{\text{IH}}$ .
3. If  $\overline{\text{CS}}$  goes high simultaneously with  $\overline{\text{WE}}$  high, the output remains in a high impedance state.

**Capacitance**

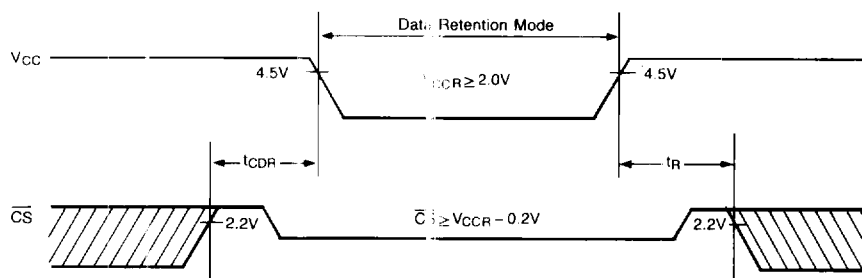
| Symbol    | Parameter          | Test Condition                                                         | Min | Max | Unit |
|-----------|--------------------|------------------------------------------------------------------------|-----|-----|------|
| $C_{IN}$  | Input Capacitance  | $T_A = 25^\circ\text{C}$ , $f = 1\text{MHz}$<br>$V_{CC} = 5.0\text{V}$ | —   | 6   | pF   |
| $C_{OUT}$ | Output Capacitance |                                                                        | —   | 8   |      |

Note: Tested on a sample basis

**Data Retention Characteristics: ( $T_A = 0 \sim 70^\circ\text{C}$ )**

| Symbol    | Parameter                     | Test Conditions                                              | Min        | Typ | Max | Unit          |
|-----------|-------------------------------|--------------------------------------------------------------|------------|-----|-----|---------------|
| $V_{CCR}$ | Data Retention Supply Voltage | $\overline{CS} \geq V_{CCR} - 0.2\text{V}$                   | 2.0        | —   | 5.5 | V             |
| $I_{CCR}$ | Data Retention Current        | $V_{CC} = 3.0\text{V}$ ,<br>$\overline{CS} \geq 2.8\text{V}$ | —          | —   | 50  | $\mu\text{A}$ |
| $t_{CDR}$ | Chip Select Data Hold Time    | Refer to the figure below                                    | 0          | —   | —   | ns            |
| $t_R$     | Operation Recovery Time       |                                                              | $t_{RC}^*$ | —   | —   | ns            |

Note\*: Read Cycle Time

**Data Retention Timing**

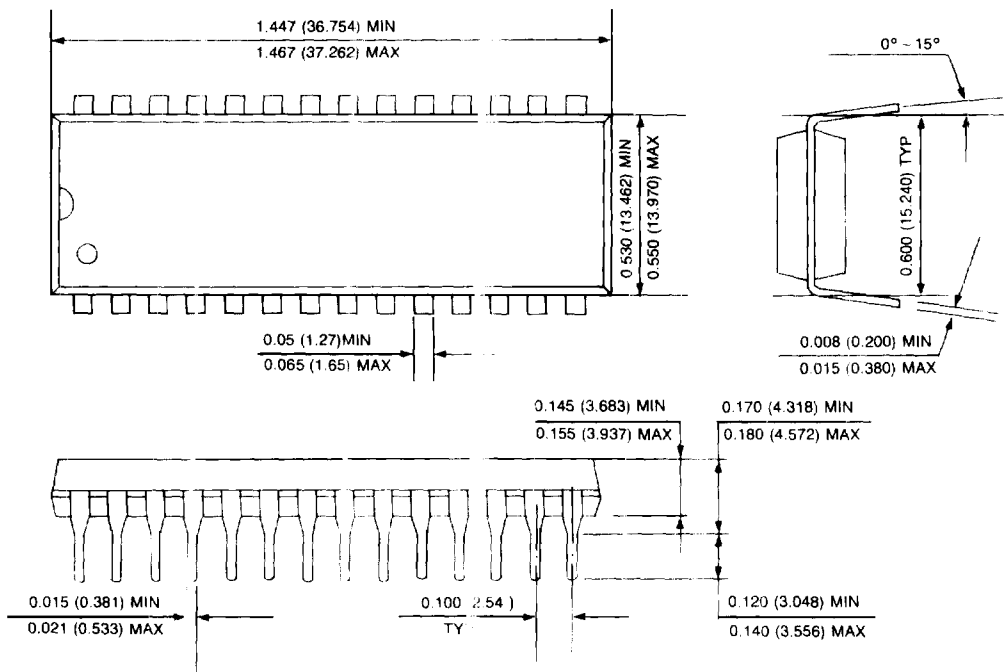
Note: When retaining data in standby mode, supply voltage can be lowered within a certain range. Read or write cycle cannot be performed while the supply voltage is low.



**Package Dimensions**

**28 DIP**

Unit: inches (mm)



**28 SOP**

