

mitsubishi 8-BIT SINGLE-CHIP MICROCOMPUTER
740 FAMILY / 38000 SERIES

38K0
Group

User's Manual

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Preface

This user's manual describes Mitsubishi's CMOS 8-bit microcomputers 38K0 Group.

After reading this manual, the user should have a thorough knowledge of the functions and features of the 38K0 Group, and should be able to fully utilize the product. The manual starts with specifications and ends with application examples.

For details of software, refer to the "740 Family Software Manual".

BEFORE USING THIS MANUAL

This user's manual consists of the following three chapters. Refer to the chapter appropriate to your conditions, such as hardware design or software development. Chapter 3 also includes necessary information for systems development. You must refer to that chapter.

1. Organization

● CHAPTER 1 HARDWARE

This chapter describes features of the microcomputer and operation of each peripheral function.

● CHAPTER 2 APPLICATION

This chapter describes usage and application examples of peripheral functions, based mainly on setting examples of relevant registers.

● CHAPTER 3 APPENDIX

This chapter includes necessary information for systems development using the microcomputer, such as the electrical characteristics, the notes, and the list of registers.

*For the mask ROM confirmation form and the mark specifications, refer to the "Mitsubishi MCU Technical Information" Homepage (<http://www.infocom.maec.co.jp/>).

2. Structure of register

The figure of each register structure describes its functions, contents at reset, and attributes as follows :

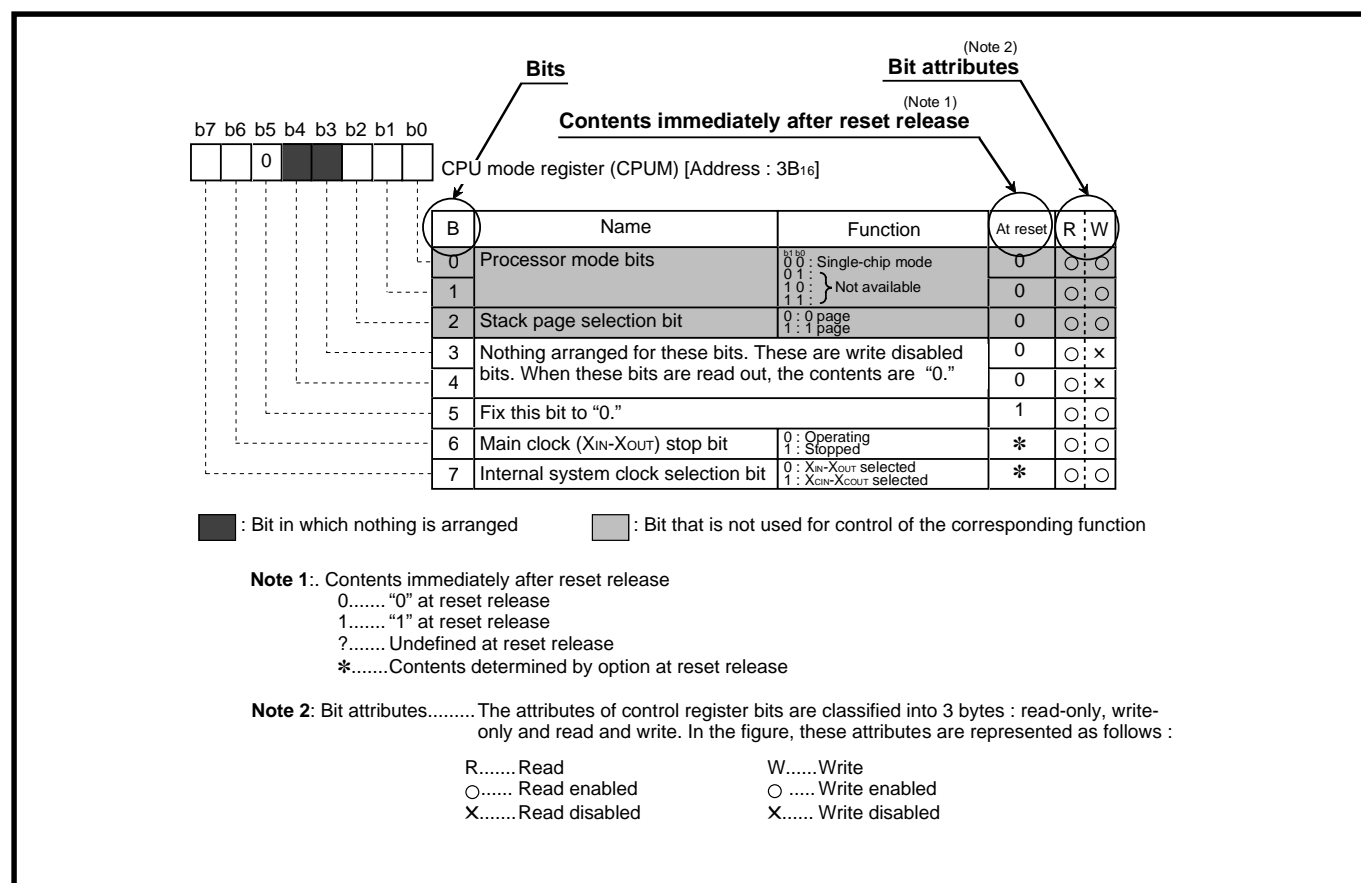


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CHAPTER 1

HARDWARE

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FEATURES
PIN CONFIGURATION
FUNCTIONAL BLOCK
PIN DESCRIPTION
PART NUMBERING
GROUP EXPANSION
FUNCTIONAL DESCRIPTION
NOTES ON PROGRAMMING
NOTES ON USAGE
DATA REQUIRED FOR MASK ORDERS
FUNCTIONAL DESCRIPTION
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HARDWARE

DESCRIPTION/FEATURES/PIN CONFIGURATION

DESCRIPTION

The 38K0 group is the 8-bit microcomputer based on the 740 family core technology.

The 38K0 group has the USB function, an 8-bit bus interface, a Serial I/O, three 8-bit timers, and an 8-channel 10-bit A-D converter, which are available for the PC peripheral I/O device.

The various microcomputers in the 38K0 group include variations of internal memory size and packaging. For details, refer to the section on part numbering.

FEATURES

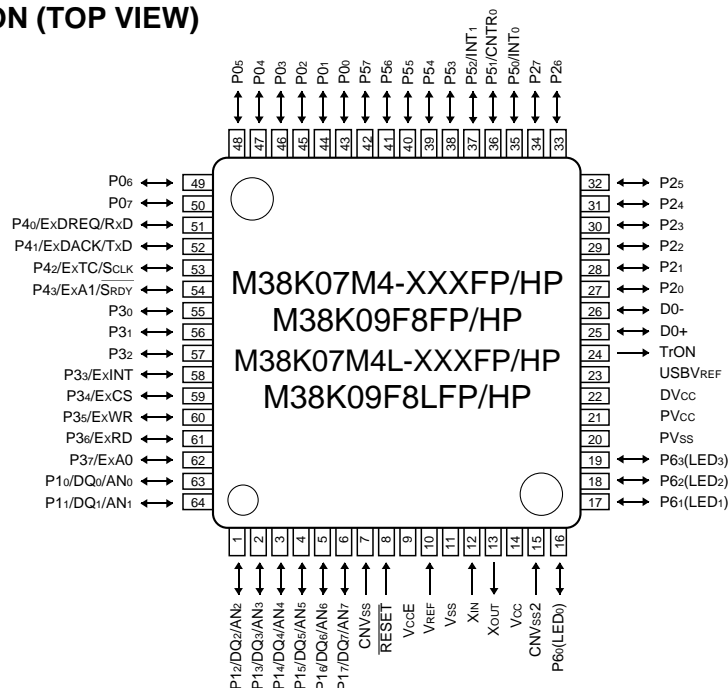
- Basic machine-language instructions 71
- The minimum instruction execution time 0.25 μ s
(at 8 MHz system clock*)
- System clock*: Reference frequency to internal circuit except USB function
- Memory size
 - ROM 16 K to 32 K bytes
 - RAM 1024 to 2048 bytes
- Programmable input/output ports 48
- Software pull-up resistors
- Interrupts 15 sources, 15 vectors
- USB function (Full-Speed USB2.0 specification) 4 endpoints
- External bus interface 8-bit X 1 channel
- Timers 8-bit X 3
- Watchdog timer 16-bit X 1
- Serial I/O 8-bit X 1 (UART or Clock-synchronized)
- A-D converter 10-bit X 8 channels
(8-bit reading available)

- LED direct drive port 4
- Clock generating circuit
(connect to external ceramic resonator or quartz-crystal oscillator)
- Power source voltage (Standard)
 - System clock/Internal clock division mode
 - At 8 MHz/Through mode ($\phi = 8$ MHz) 4.00 to 5.25 V
 - At 6 MHz/Through mode ($\phi = 6$ MHz) 4.00 to 5.25 V
- Power source voltage (L version)
 - System clock/Internal clock division mode
 - At 12 MHz/Through mode ($\phi = 12$ MHz) (under planning)
..... 4.50 to 5.25 V
 - At 12 MHz/2-divide mode($\phi = 6$ MHz) 4.00 to 5.25 V
 - At 8 MHz/Through mode ($\phi = 8$ MHz) 4.00 to 5.25 V
 - At 6 MHz/Through mode ($\phi = 6$ MHz) 3.00 to 5.25 V
- Power dissipation
 - At 5 V power source voltage 125 mW (typ.)
(at 8 MHz system clock, in through mode)
 - At 3.3 V power source voltage 30 mW (typ.)
(at 6 MHz system clock, in through mode)
- Operating temperature range -20 to 85°C
- Packages
 - FP 64P6U-A (64-pin 14 X 14 mm LQFP)
 - HP 64P6Q-A (64-pin 10 X 10 mm LQFP)

Notes

The specifications of this product are subject to change because it is under development. Inquire the use of Mitsubishi Electric Corporation.

PIN CONFIGURATION (TOP VIEW)



Package type : 64P6U-A/64P6Q-A

Fig. 1 Pin configuration of 38K0 group

FUNCTIONAL BLOCK

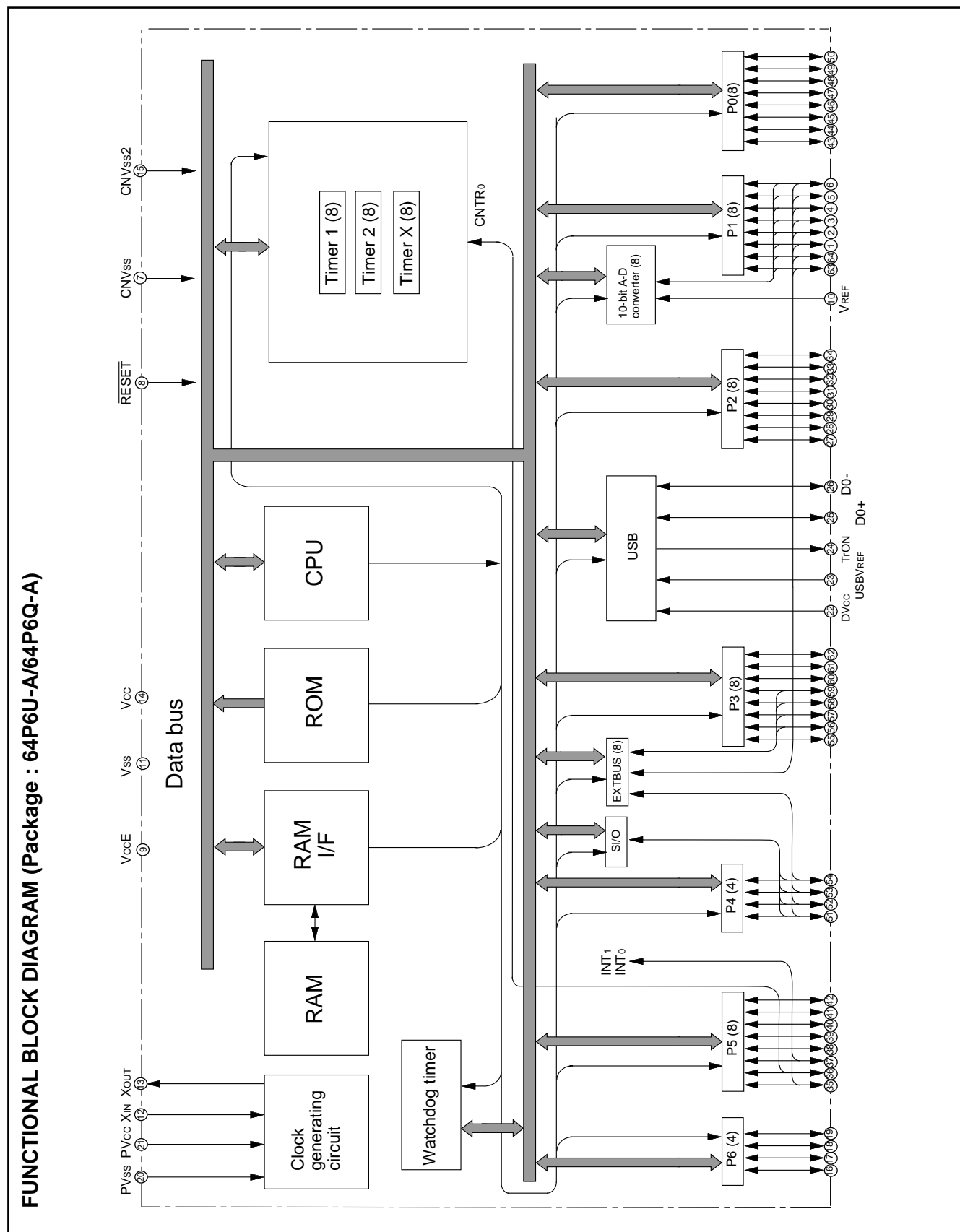


Fig. 2 Functional block diagram

HARDWARE

PIN DESCRIPTION

PIN DESCRIPTION

Table 1. Pin description

Pin	Name	Function	Function except a port function
VCC, VSS	Power source	• Apply voltage of 4.0 V – 5.25V (Standard) or 3.0 V – 5.25 V (L version) to VCC, and 0 V to VSS.	
VCC_E	Analog power source	• Power source pin for ports P1, P3, P4 and analog circuit. Connect this pin to VCC.	
CNVSS	CNVSS	• This pin controls the operation mode of the chip. Connect this pin to VSS. In the flash memory mode, this pin becomes VPP power source input pin.	
CNVSS2	CNVSS2	• This pin controls the operation mode of the chip. Connect this pin to VSS.	
VREF	Analog reference voltage input	• Reference voltage input pin for A-D converter.	
DVCC, PVCC, PVSS	Analog power source	• Power source pin for analog circuit. • Connect the DVCC and PVCC pins to VCC, and the PVSS pin to VSS.	
RESET	Reset input	• Reset input pin for active “L”	
XIN	Clock input	• Input and output pins for the main clock generating circuit. • Connect a ceramic resonator or a quartz-crystal oscillator between the XIN and XOUT pins to set the oscillation frequency.	
XOUT	Clock output	• If an external clock is used, connect the clock source to the XIN pin and leave the XOUT pin open.	
USBVREF	USB reference power source	• Power source pin for USB port circuit. In Vcc = 4.00 to 5.25 V use the built-in USB reference voltage circuit. In Vcc = 3.60 to 4.00 V apply 3.3 V power supply from the external because use of the built-in USB reference voltage circuit is prohibited in this voltage range. In Vcc = 3.00 to 3.60 V connect this pin to VCC because use of the built-in USB reference voltage circuit is prohibited in this voltage range.	
TrON	USB reference voltage output	• Output pin to pull-up D0+ by 1.5 kΩ external resistor.	
D0+, D0-	USB upstream I/O	• USB upstream I/O port • USB input level • USB output level output structure	
P00–P07	I/O port P0	• 8-bit I/O port • I/O direction register allows each pin to be individually programmed as either input or output. • CMOS compatible input level • CMOS 3-state output structure • Pull-up control is enabled.	• Key input pins (key-on wake up interrupt)
P10/DQ0/AN0–P17/DQ7/AN7	I/O port P1	• 8-bit I/O port • I/O direction register allows each pin to be individually programmed as either input or output. • CMOS compatible input level • CMOS 3-state output structure	• A-D converter input pins • External bus interface function pins
P20–P27	I/O port P2	• 8-bit I/O port • I/O direction register allows each pin to be individually programmed as either input or output. • CMOS compatible input level • CMOS 3-state output structure	
P30–P32	I/O port P3	• 8-bit I/O port • I/O direction register allows each pin to be individually programmed as either input or output. • CMOS compatible input level • CMOS 3-state output structure	
P33/ExINT P34/ExCS P35/ExWR P36/ExRD P37/ExA0			• External bus interface function pins
P40/ExDREQ/RxD P41/ExDACK/TxD P42/ExTC/SCLK P43/ExA1/SDY	I/O port P4	• 4-bit I/O port • I/O direction register allows each pin to be individually programmed as either input or output. • CMOS compatible input level • CMOS 3-state output structure	• Serial I/O function pins • External bus interface function pins
P50/INT0	I/O port P5	• 8-bit I/O port • I/O direction register allows each pin to be individually programmed as either input or output. • CMOS compatible input level • CMOS 3-state output structure	• Interrupt input pin
P51/CNTR0			• Timer X function pin
P52/INT1			• Interrupt input pin
P53–P57			
P60–P63	I/O port P6	• 4-bit I/O port • I/O direction register allows each pin to be individually programmed as either input or output. • CMOS compatible input level • CMOS 3-state output structure • Output large current for LED drive is enabled.	

PART NUMBERING

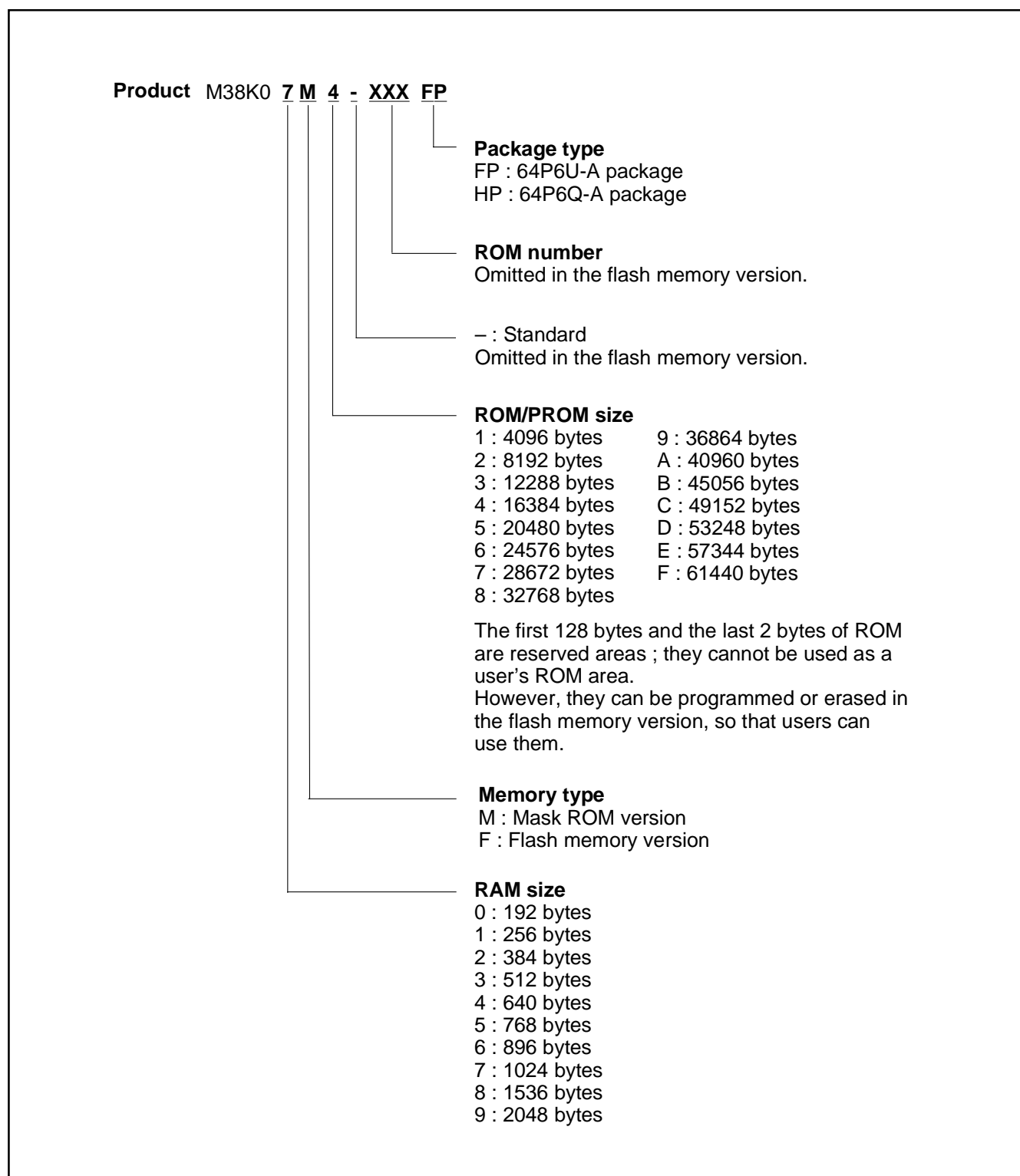


Fig. 3 Part numbering

HARDWARE

GROUP EXPANSION

GROUP EXPANSION

Mitsubishi plans to expand the 38K0 group as follows.

Memory Type

Support for mask ROM and flash memory versions.

Memory Size

Flash memory size 32 Kbytes
Mask ROM size 16 Kbytes
RAM size 1024 to 2048 bytes

Packages

64P6U-A 0.8 mm-pitch plastic molded LQFP
64P6Q-A 0.5 mm-pitch plastic molded LQFP
100D0M 0.65 mm-pitch metal seal PIGGY BACK

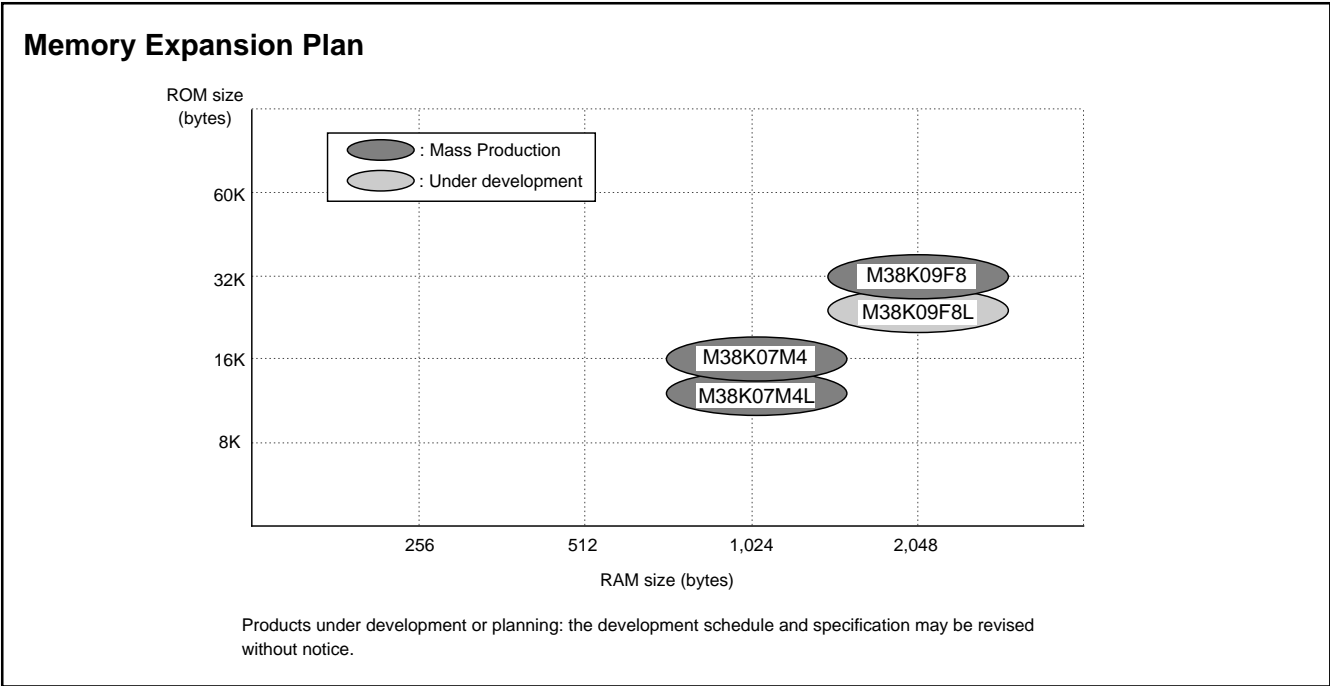


Fig. 4 Memory expansion plan

Currently products are listed below.

Table 2. List of 38K0 group products (Standard) As of December 2002

Product	ROM size (bytes) ROM size for User in ()	RAM size (bytes)	Package	Remarks
M38K07M4-XXXFP	16384 (16254)	1024	64P6U-A	Mask ROM version
M38K07M4-XXXHP			64P6Q-A	
M38K09F8FP	32768 (32638)	2048	64P6U-A	Flash memory version
M38K09F8HP			64P6Q-A	
M38K09RFS	—	2048	100D0M	Emulator MCU (for program evaluation)

Table 3. List of 38K0 group products (L version) As of December 2002

Product	ROM size (bytes) ROM size for User in ()	RAM size (bytes)	Package	Remarks
M38K07M4L-XXXFP	16384 (16254)	1024	64P6U-A	Mask ROM version
M38K07M4L-XXXHP			64P6Q-A	
M38K09F8LFP	32768 (32638)	2048	64P6U-A	Flash memory version
M38K09F8LHP			64P6Q-A	
M38K09RFS	—	2048	100D0M	Use of Standard product only

FUNCTIONAL DESCRIPTION
CENTRAL PROCESSING UNIT (CPU)

The 38K0 group uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine instructions or the 740 Family Software Manual for details on the instruction set.

Machine-resident 740 family instructions are as follows:

The FST and SLW instruction cannot be used.

The STP, WIT, MUL, and DIV instruction can be used.

The CPU has the 6 registers. The register structure is shown in Figure 5.

[Accumulator (A)]

The accumulator is an 8-bit register. Data operations such as data transfer, etc., are executed mainly through the accumulator.

[Index Register X (X)]

The index register X is an 8-bit register. In the index addressing modes, the value of the OPERAND is added to the contents of register X and specifies the real address.

[Index Register Y (Y)]

The index register Y is an 8-bit register. In partial instruction, the value of the OPERAND is added to the contents of register Y and specifies the real address.

[Stack Pointer (S)]

The stack pointer is an 8-bit register used during subroutine calls and interrupts. This register indicates start address of stored area (stack) for storing registers during subroutine calls and interrupts. The low-order 8 bits of the stack address are determined by the contents of the stack pointer. The high-order 8 bits of the stack address are determined by the stack page selection bit. If the stack page selection bit is "0", the high-order 8 bits becomes "0016". If the stack page selection bit is "1", the high-order 8 bits becomes "0116".

Figure 6 shows the store and the return movement into the stack. If there are registers other than those described in Figure 5, the users need to store them with the program.

[Program Counter (PC)]

The program counter is a 16-bit counter consisting of two 8-bit registers PCH and PCL. It is used to indicate the address of the next instruction to be executed.

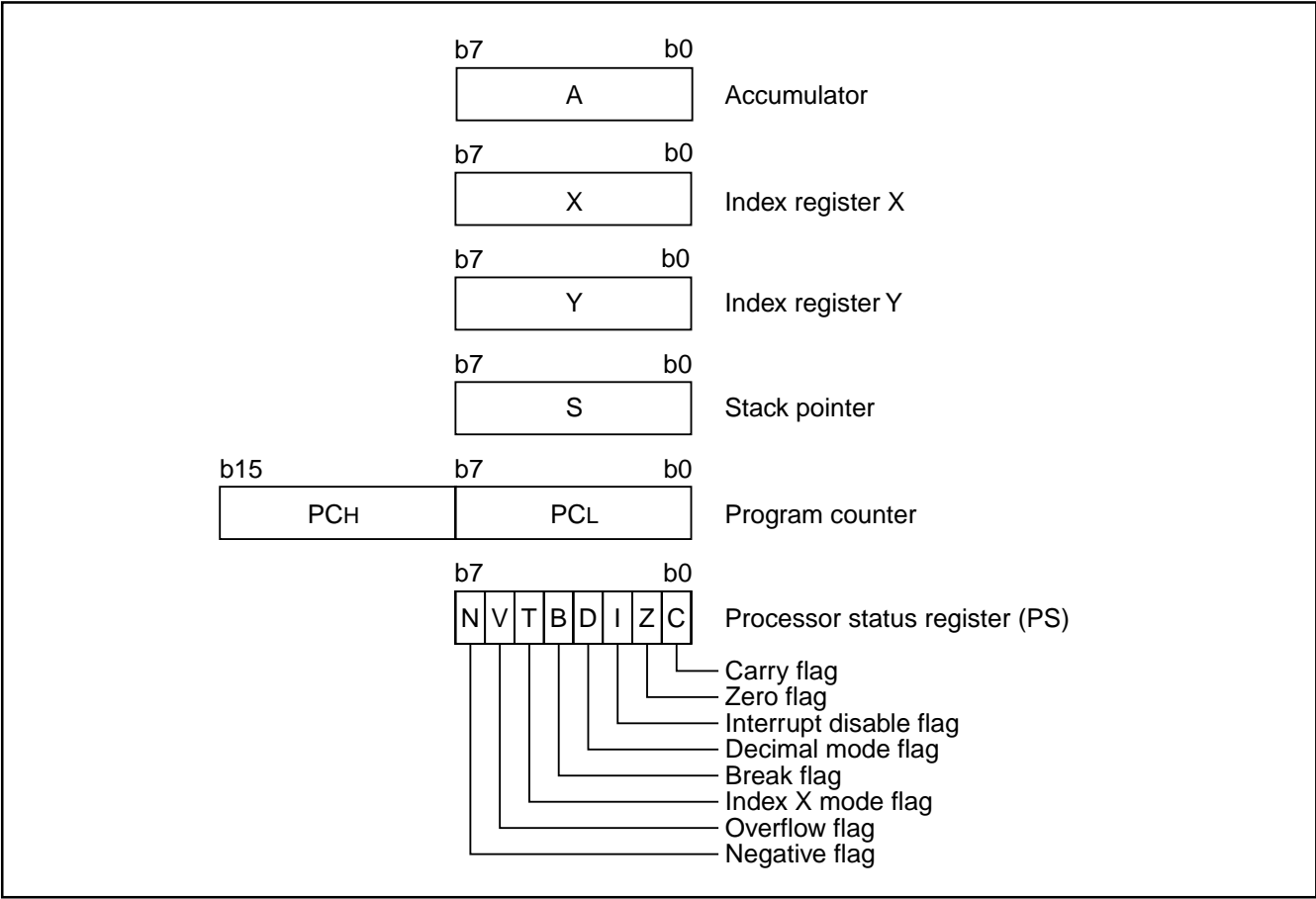


Fig. 5 740 Family CPU register structure

HARDWARE

FUNCTIONAL DESCRIPTION

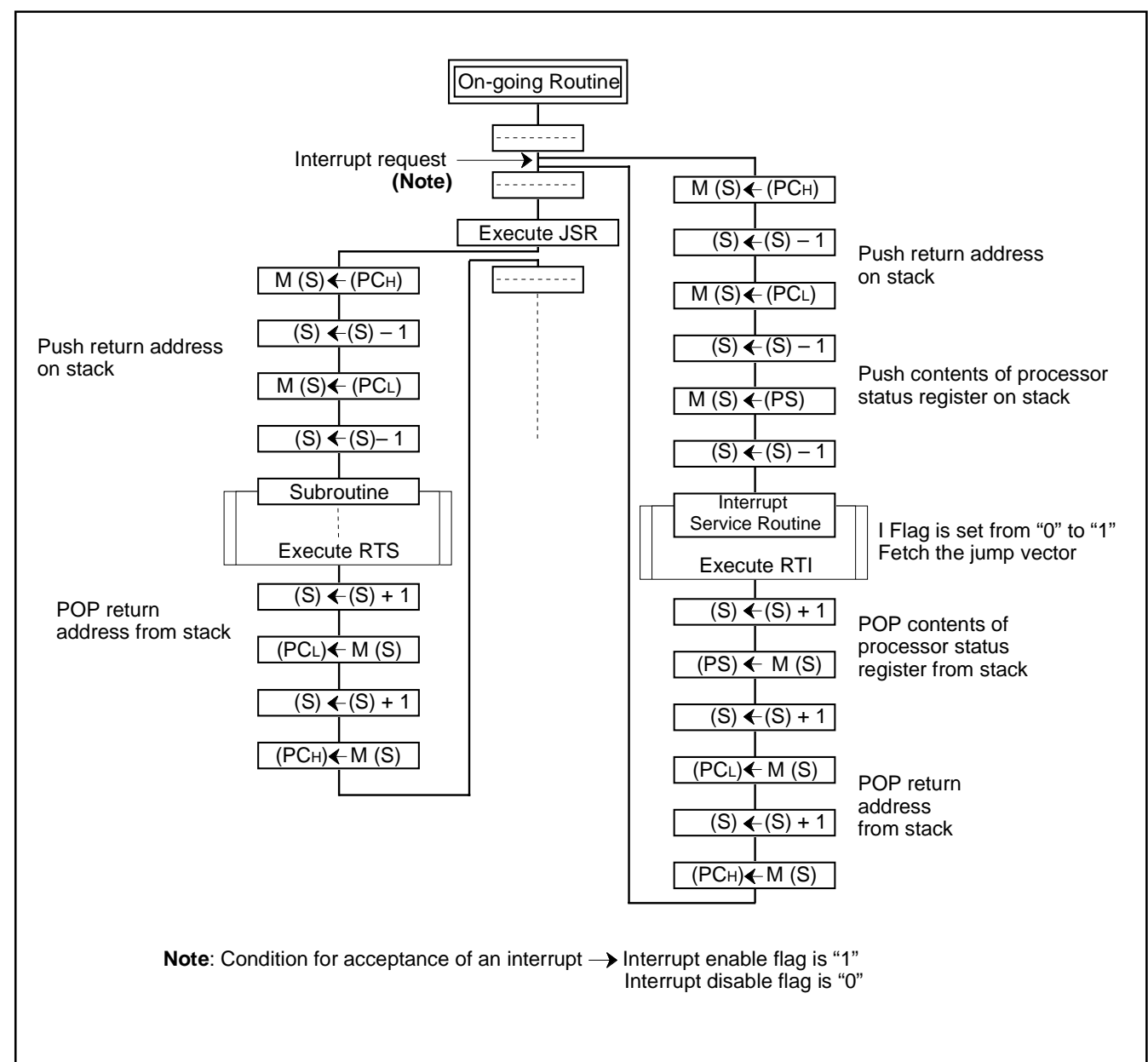


Fig. 6 Register push and pop at interrupt generation and subroutine call

Table 4 Push and pop instructions of accumulator or processor status register

	Push instruction to stack	Pop instruction from stack
Accumulator	PHA	PLA
Processor status register	PHP	PLP

[Processor status register (PS)]

The processor status register is an 8-bit register consisting of 5 flags which indicate the status of the processor after an arithmetic operation and 3 flags which decide MCU operation. Branch operations can be performed by testing the Carry (C) flag, Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag. In decimal mode, the Z, V, N flags are not valid.

- Bit 0: Carry flag (C)

The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It can also be changed by a shift or rotate instruction.

- Bit 1: Zero flag (Z)

The Z flag is set if the result of an immediate arithmetic operation or a data transfer is "0", and cleared if the result is anything other than "0".

- Bit 2: Interrupt disable flag (I)

The I flag disables all interrupts except for the interrupt generated by the BRK instruction.

Interrupts are disabled when the I flag is "1".

- Bit 3: Decimal mode flag (D)

The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is "0"; decimal arithmetic is executed when it is "1".

Decimal correction is automatic in decimal mode. Only the ADC

- Bit 4: Break flag (B)

The B flag is used to indicate that the current interrupt was generated by the BRK instruction. The BRK flag in the processor status register is always "0". When the BRK instruction is used to generate an interrupt, the processor status register is pushed onto the stack with the break flag set to "1".

- Bit 5: Index X mode flag (T)

When the T flag is "0", arithmetic operations are performed between accumulator and memory. When the T flag is "1", direct arithmetic operations and direct data transfers are enabled between memory locations.

- Bit 6: Overflow flag (V)

The V flag is used during the addition or subtraction of one byte of signed data. It is set if the result exceeds +127 to -128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the overflow flag.

- Bit 7: Negative flag (N)

The N flag is set if the result of an arithmetic operation or data transfer is negative. When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag.

Table 5 Set and clear instructions of each bit of processor status register

	C flag	Z flag	I flag	D flag	B flag	T flag	V flag	N flag
Set instruction	SEC	—	SEI	SED	—	SET	—	—
Clear instruction	CLC	—	CLI	CLD	—	CLT	CLV	—

HARDWARE

FUNCTIONAL DESCRIPTION

[CPU Mode Register (CPUM)] 003B16

The CPU mode register contains the stack page selection bit and the internal system clock selection bit.

The CPU mode register is allocated at address 003B16.

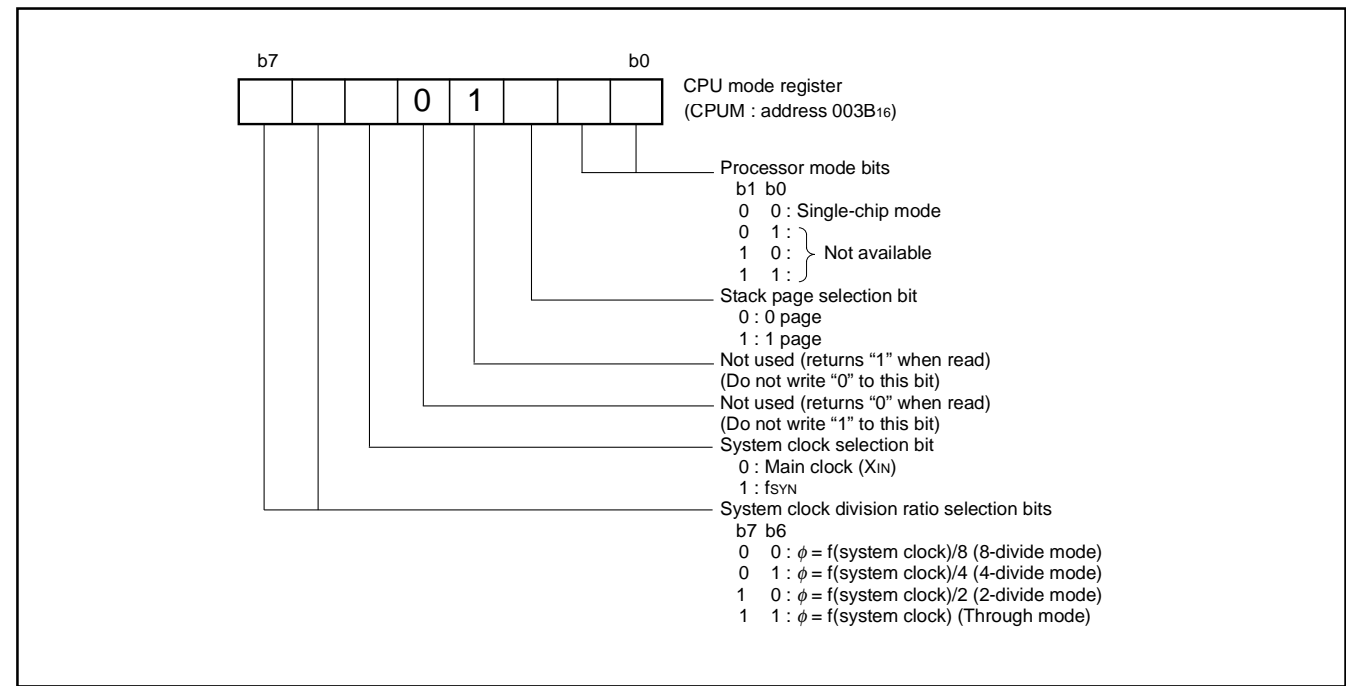


Fig. 7 Structure of CPU mode register

MEMORY

Special Function Register (SFR) Area

The Special Function Register area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is user area for storing programs. In the flash memory version, program and erase can be performed in the reserved area.

Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

Zero Page

The 256 bytes from addresses 0000_{16} to $00FF_{16}$ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special Page

The 256 bytes from addresses $FF00_{16}$ to $FFFF_{16}$ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

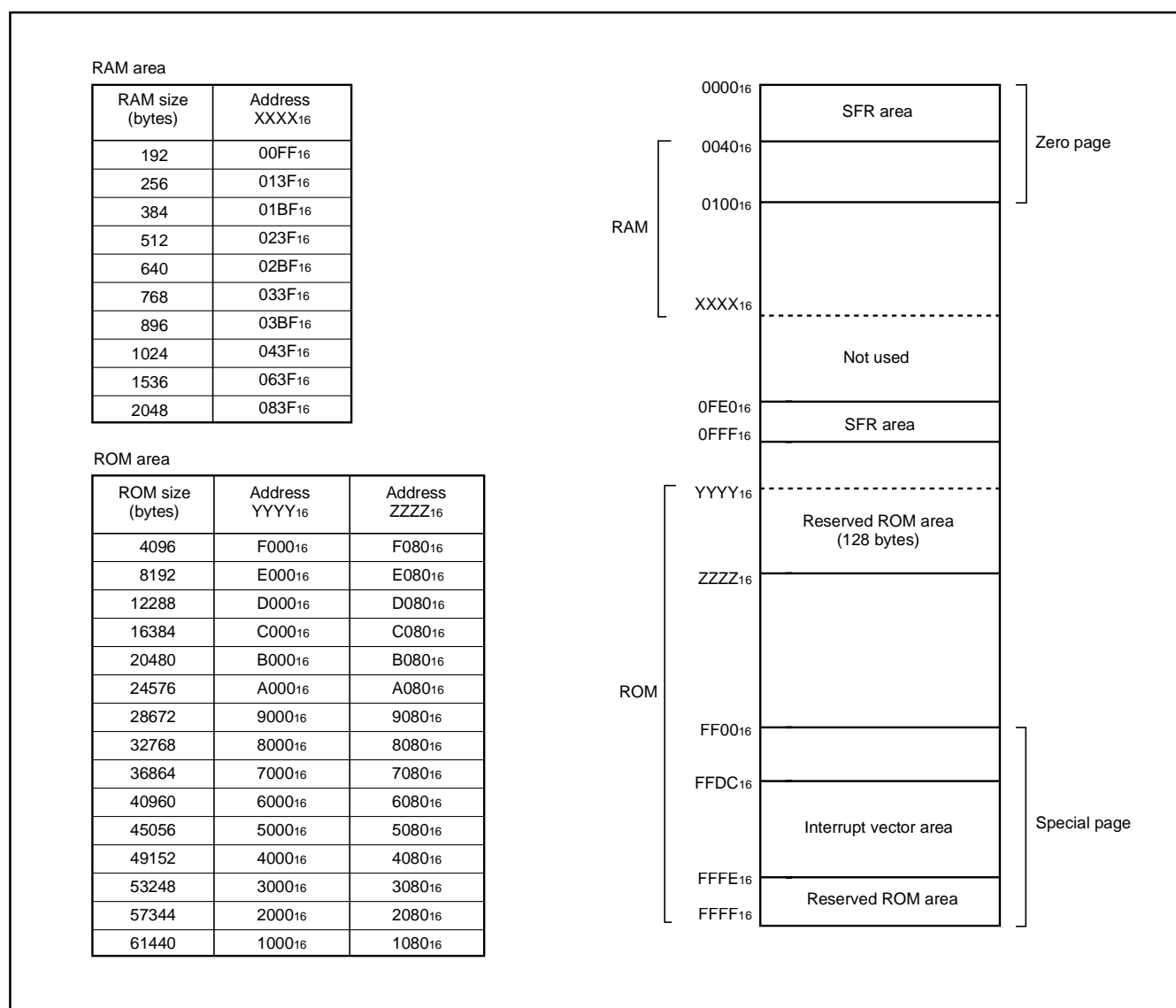


Fig. 8 Memory map diagram

HARDWARE

FUNCTIONAL DESCRIPTION

0000 ₁₆	Port P0 (P0)	0020 ₁₆	Prescaler 12 (PRE12)
0001 ₁₆	Port P0 direction register (P0D)	0021 ₁₆	Timer 1 (T1)
0002 ₁₆	Port P1 (P1)	0022 ₁₆	Timer 2 (T2)
0003 ₁₆	Port P1 direction register (P1D)	0023 ₁₆	Timer X mode register (TM)
0004 ₁₆	Port P2 (P2)	0024 ₁₆	Prescaler X (PREX)
0005 ₁₆	Port P2 direction register (P2D)	0025 ₁₆	Timer X (TX)
0006 ₁₆	Port P3 (P3)	0026 ₁₆	Transmit/Receive buffer register (TB/RB)
0007 ₁₆	Port P3 direction register (P3D)	0027 ₁₆	Serial I/O status register (SIOSTS)
0008 ₁₆	Port P4 (P4)	0028 ₁₆	Reserved (Note)
0009 ₁₆	Port P4 direction register (P4D)	0029 ₁₆	Reserved (Note)
000A ₁₆	Port P5 (P5)	002A ₁₆	Reserved (Note)
000B ₁₆	Port P5 direction register (P5D)	002B ₁₆	Reserved (Note)
000C ₁₆	Port P6 (P6)	002C ₁₆	Reserved (Note)
000D ₁₆	Port P6 direction register (P6D)	002D ₁₆	Reserved (Note)
000E ₁₆	Reserved (Note)	002E ₁₆	Reserved (Note)
000F ₁₆	Reserved (Note)	002F ₁₆	Reserved (Note)
0010 ₁₆	USB control register (USBCON)	0030 ₁₆	EXB interrupt source enable register (EXBICON)
0011 ₁₆	USB function enable register (USBAE)	0031 ₁₆	EXB interrupt source register (EXBIREQ)
0012 ₁₆	USB function address register (USBA0)	0032 ₁₆	Reserved (Note)
0013 ₁₆	Reserved (Note)	0033 ₁₆	EXB index register (EXBINDEX)
0014 ₁₆	Frame number register Low (FNUML)	0034 ₁₆	EXB field register 1 (EXBREG1)
0015 ₁₆	Frame number register High (FNUMH)	0035 ₁₆	EXB field register 2 (EXBREG2)
0016 ₁₆	USB interrupt source enable register (USBICON)	0036 ₁₆	A-D control register (ADCON)
0017 ₁₆	USB interrupt source register (USBIREQ)	0037 ₁₆	A-D conversion register 1 (AD1)
0018 ₁₆	Endpoint index register (USBINDEX)	0038 ₁₆	A-D conversion register 2 (AD2)
0019 ₁₆	Endpoint field register 1 (EPXXREG1)	0039 ₁₆	Watchdog timer control register (WDTCON)
001A ₁₆	Endpoint field register 2 (EPXXREG2)	003A ₁₆	Reserved (Note)
001B ₁₆	Endpoint field register 3 (EPXXREG3)	003B ₁₆	CPU mode register (CPUM)
001C ₁₆	Endpoint field register 4 (EPXXREG4)	003C ₁₆	Interrupt request register 1 (IREQ1)
001D ₁₆	Endpoint field register 5 (EPXXREG5)	003D ₁₆	Interrupt request register 2 (IREQ2)
001E ₁₆	Endpoint field register 6 (EPXXREG6)	003E ₁₆	Interrupt control register 1 (ICON1)
001F ₁₆	Endpoint field register 7 (EPXXREG7)	003F ₁₆	Interrupt control register 2 (ICON2)
0FE0 ₁₆	Serial I/O control register (SIOCON)	0FF0 ₁₆	Port P0 pull-up control register (PULL0)
0FE1 ₁₆	UART control register (UARTCON)	0FF1 ₁₆	Reserved (Note)
0FE2 ₁₆	Baud rate generator (BRG)	0FF2 ₁₆	Port P5 pull-up control register (PULL5)
0FE3 ₁₆	Reserved (Note)	0FF3 ₁₆	Interrupt edge selection register (INTEDGE)
0FE4 ₁₆	Reserved (Note)	0FF4 ₁₆	Reserved (Note)
0FE5 ₁₆	Reserved (Note)	0FF5 ₁₆	Reserved (Note)
0FE6 ₁₆	Reserved (Note)	0FF6 ₁₆	Reserved (Note)
0FE7 ₁₆	Reserved (Note)	0FF7 ₁₆	Reserved (Note)
0FE8 ₁₆	Reserved (Note)	0FF8 ₁₆	PLL control register (PLLCON)
0FE9 ₁₆	Reserved (Note)	0FF9 ₁₆	Reserved (Note)
0FEA ₁₆	Reserved (Note)	0FFA ₁₆	Reserved (Note)
0FEB ₁₆	Reserved (Note)	0FFB ₁₆	MISRG
0FEC ₁₆	Endpoint field register 8 (EPXXREG8)	0FFC ₁₆	Reserved (Note)
0FED ₁₆	Endpoint field register 9 (EPXXREG9)	0FFD ₁₆	Reserved (Note)
0FEE ₁₆	Reserved (Note)	0FFE ₁₆	Flash memory control register (FMCR)
0FEF ₁₆	Reserved (Note)	0FFF ₁₆	Reserved (Note)

Note: Do not write any data to these addresses, because these areas are reserved.

Fig. 9 Memory map of special function register (SFR)

I/O PORTS

The I/O ports have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, and each pin can be set to be input port or output port.

When “0” is written to the bit corresponding to a pin, that pin becomes an input pin. When “1” is written to that bit, that pin becomes an output pin.

If data is read from a pin set to output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

Table 6 I/O ports functions

Table 6 I/O ports functions						
Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Diagram No.
P00–P07	Port P0	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	Key-on wake up	Port P0 pull-up control register	(1)
P10–P17	Port P1		CMOS compatible input level CMOS 3-state output (Power source is VccE)	A-D conversion input External bus interface function I/O	A-D control register EXB control register	(2)
P20–P27	Port P2		CMOS compatible input level CMOS 3-state output	_____	_____	(3)
P30–P32	Port P3		CMOS compatible input level CMOS 3-state output (Power source is VccE)	_____	_____	(4)
P33/ExINT				External bus interface function output	EXB control register	(5)
P34/ExCS P35/ExWR P36/ExRD P37/ExA0				External bus interface function input	EXB control register	(6)
P40/RxD/ ExDREQ				Port P4	Serial I/O input External bus interface function output	Serial I/O control register EXB control register
P41/TxD/ ExDACK	Serial I/O output External bus interface function input		Serial I/O control register EXB control register		(8)	
P42/SCLK/ ExTC	Serial I/O I/O External bus interface function input		Serial I/O control register EXB control register		(9)	
P43/ $\overline{\text{SRDY}}$ / ExA1	Serial I/O output External bus interface function input		Serial I/O control register EXB control register		(10)	
P50/INT0 P52/INT1	Port P5		CMOS compatible input level CMOS 3-state output	External interrupt input	Port P5 pull-up control register Interrupt edge selection register	(11)
P51/CNTR0				Timer X function I/O	Timer X mode register	(12)
P53–P57				_____	_____	(13)
P60–P63	Port P6			_____	_____	(14)

Note: Make sure that the input level at each pin is either 0 V or Vcc during execution of the STP instruction. When an input level is at an intermediate potential, a current will flow from Vcc to Vss through the input-stage gate.

HARDWARE

FUNCTIONAL DESCRIPTION

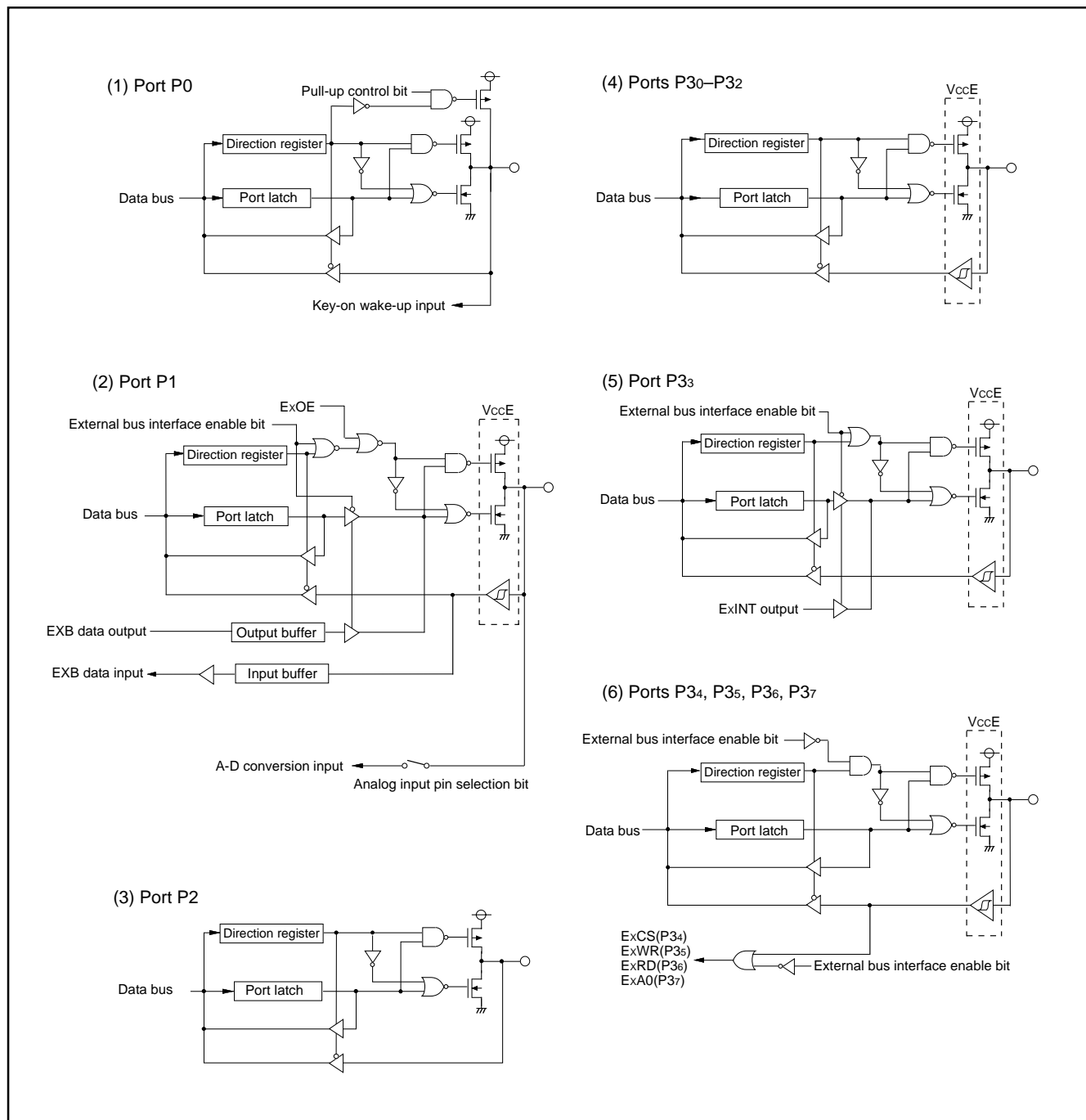


Fig. 10 Port block diagram (1)



HARDWARE

FUNCTIONAL DESCRIPTION

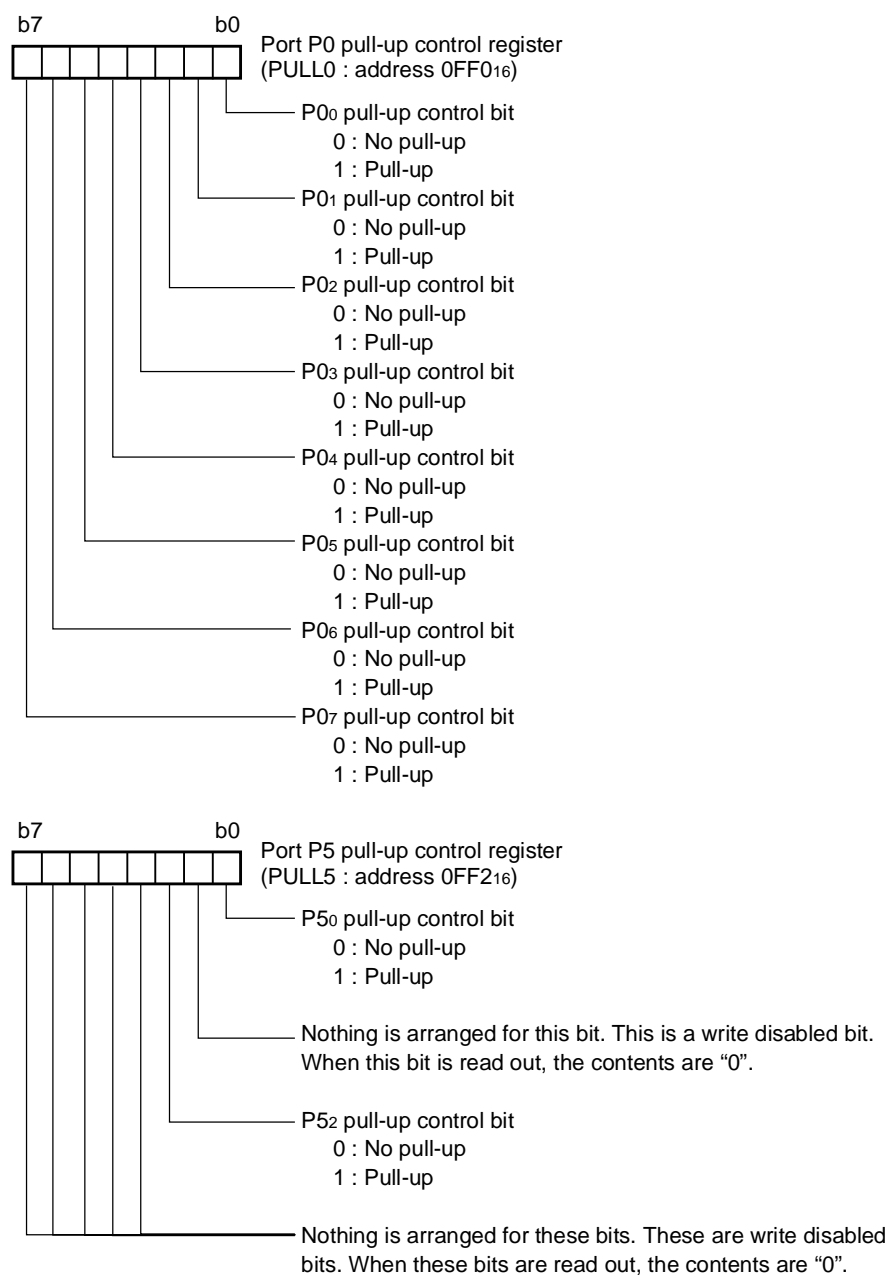


Fig. 12 Structure of port I/O-related registers

INTERRUPTS

Interrupts occur by fifteen sources: four external, ten internal, and one software.

Interrupt Control

Each interrupt is controlled by an interrupt request bit, an interrupt enable bit, and the interrupt disable flag except for the software interrupt set by the BRK instruction. An interrupt occurs if the corresponding interrupt request and enable bits are "1" and the interrupt disable flag is "0".

Interrupt enable bits can be set or cleared by software.

Interrupt request bits can be cleared by software, but cannot be set by software.

The BRK instruction cannot be disabled with any flag or bit. The I flag disables all interrupts except the BRK instruction interrupt.

When several interrupts occur at the same time, the interrupts are received according to priority.

Interrupt Operation

By acceptance of an interrupt, the following operations are automatically performed:

1. The contents of the program counter and the processor status register are automatically pushed onto the stack.
2. The interrupt disable flag is set and the corresponding interrupt request bit is cleared.
3. The interrupt jump destination address is read from the vector table into the program counter.

■Notes on interrupts

When setting the followings, the interrupt request bit may be set to "1".

- When switching external interrupt active edge

Related register: Interrupt edge selection register (address 0FF316), Timer X mode register (address 002316)

When not requiring for the interrupt occurrence synchronized with these setting, take the following sequence.

- ①Set the corresponding interrupt enable bit to "0" (disabled).
- ②Set the interrupt edge select bit (active edge switch bit).
- ③Set the corresponding interrupt request bit to "0" after 1 or more instructions have been executed.
- ④Set the corresponding interrupt enable bit to "1" (enabled).

Table 7 Interrupt vector addresses and priority

Interrupt Source	Priority	Vector Addresses (Note 1)		Interrupt Request Generating Conditions
		High	Low	
Reset (Note 2)	1	FFFD16	FFFC16	At reset
USB bus reset	2	FFFB16	FFFA16	At detection of USB bus reset signal (2.5 μ s interval SE0)
USB SOF	3	FFF916	FFF816	At detection of USB SOF signal
USB device	4	FFF716	FFF616	At detection of resume signal (K state or SE0) or suspend signal (3 ms interval bus idle), or at completion of transaction
External bus	5	FFF516	FFF416	At completion of reception or transmission or at completion of DMA transmission
INT0	6	FFF316	FFF216	At detection of either rising or falling edge of INT0 input
Timer X	7	FFF116	FFF016	At timer X underflow
Timer 1	8	FFEF16	FFEE16	At timer 1 underflow
Timer 2	9	FFED16	FFEC16	At timer 2 underflow
INT1	10	FFEB16	FFEA16	At detection of either rising or falling edge of INT1 input
(Note 3)	—	FFE916	FFE816	(Note 4)
Serial I/O reception	11	FFE716	FFE616	At completion of serial I/O data reception
Serial I/O transmission	12	FFE516	FFE416	At completion of serial I/O data transmission
CNTR0	13	FFE316	FFE216	At detection of either rising or falling edge of CNTR0 input
Key-on wake up	14	FFE116	FFE016	At falling of conjunction of input level for port P0 (at input mode)
A-D conversion	15	FFDF16	FFDE16	At completion of A-D conversion
BRK instruction	16	FFDD16	FFDC16	At BRK instruction execution

Notes 1: Vector addresses contain interrupt jump destination addresses.

2: Reset function in the same way as an interrupt with the highest priority.

3: Nothing is arranged in these vector addresses.

4: Fix bit 1 of interrupt control register 2 (address 003F16) to "0".

HARDWARE

FUNCTIONAL DESCRIPTION

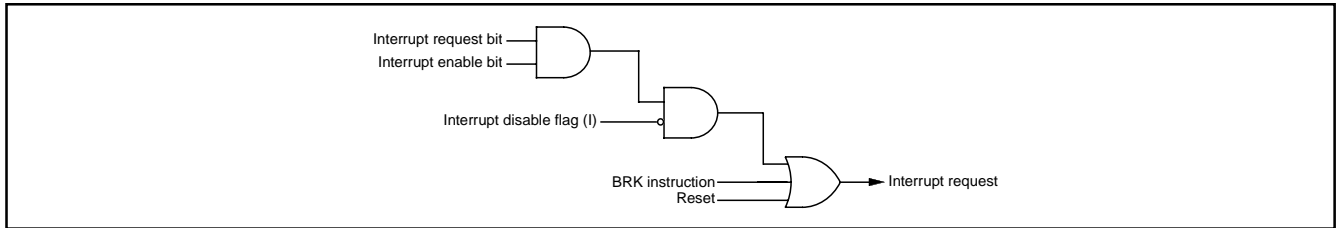


Fig. 13 Interrupt control

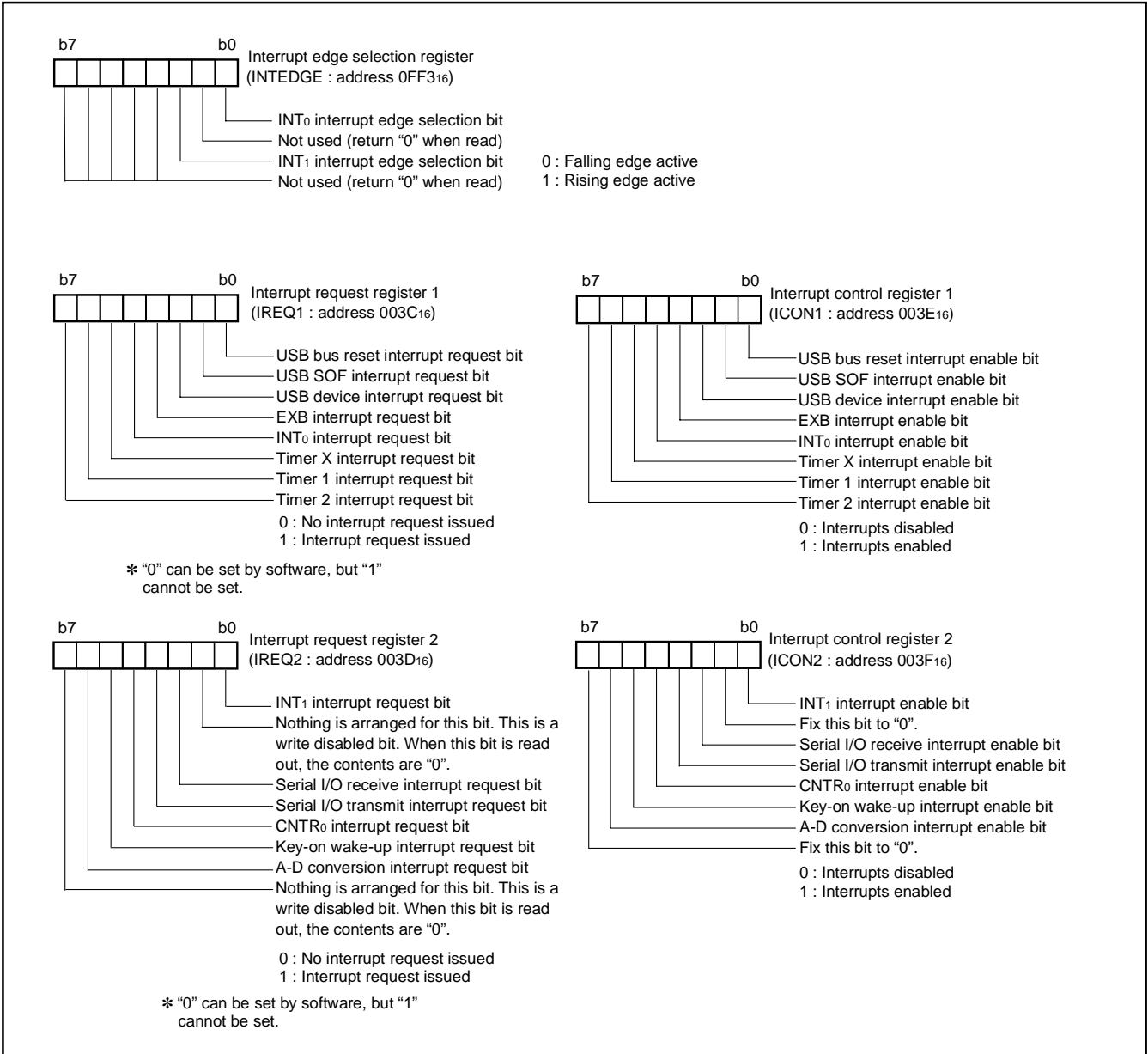


Fig. 14 Structure of interrupt-related registers

"1" to "0". An example of using a key input interrupt is shown in Figure 15, where an interrupt request is generated by pressing one of the keys consisted as an active-low key matrix which inputs to ports P00–P03.



HARDWARE

FUNCTIONAL DESCRIPTION

TIMERS

The 38K0 group has three timers: timer X, timer 1, and timer 2. The division ratio of each timer or prescaler is given by $1/(n + 1)$, where n is the value in the corresponding timer or prescaler latch. All timers are down count timers. When the timer reaches "0016", an underflow occurs at the next count pulse and the corresponding timer latch is reloaded into the timer and the count is continued. When a timer underflows, the interrupt request bit corresponding to that timer is set to "1".

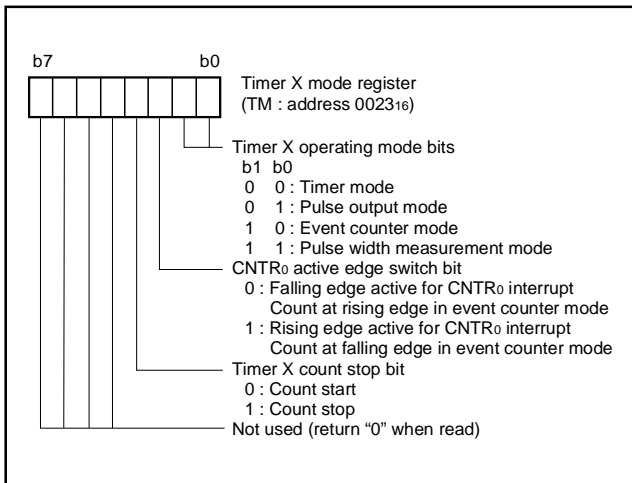


Fig. 16 Structure of timer X mode register

Timer 1 and Timer 2

The count source of prescaler 12 is the system clock divided by 16. The output of prescaler 12 is counted by timer 1 and timer 2, and a timer underflow periodically sets the interrupt request bit.

Timer X

Timer X can each select in one of four operating modes by setting the timer X mode register.

(1) Timer Mode

The timer counts the count source selected by timer count source selection bit.

(2) Pulse Output Mode

The timer counts the system clock divided by 16. Whenever the contents of the timer reach "0016", the signal output from the CNTR0 pin is inverted. If the CNTR0 active edge selection bit is "0", output begins at "H".

If it is "1", output starts at "L". When using a timer in this mode, set the corresponding port P51 direction register to output mode.

(3) Event Counter Mode

Operation in event counter mode is the same as in timer mode, except that the timer counts signals input through the CNTR0 pin. When the CNTR0 active edge selection bit is "0", the rising edge of the CNTR0 pin is counted.

When the CNTR0 active edge selection bit is "1", the falling edge of the CNTR0 pin is counted.

(4) Pulse Width Measurement Mode

If the CNTR0 active edge selection bit is "0", the timer counts the system clock divided by 16 while the CNTR0 pin is at "H". If the CNTR0 active edge selection bit is "1", the timer counts it while the CNTR0 pin is at "L".

The count can be stopped by setting "1" to the timer X count stop bit in any mode. The corresponding interrupt request bit is set each time a timer underflows.

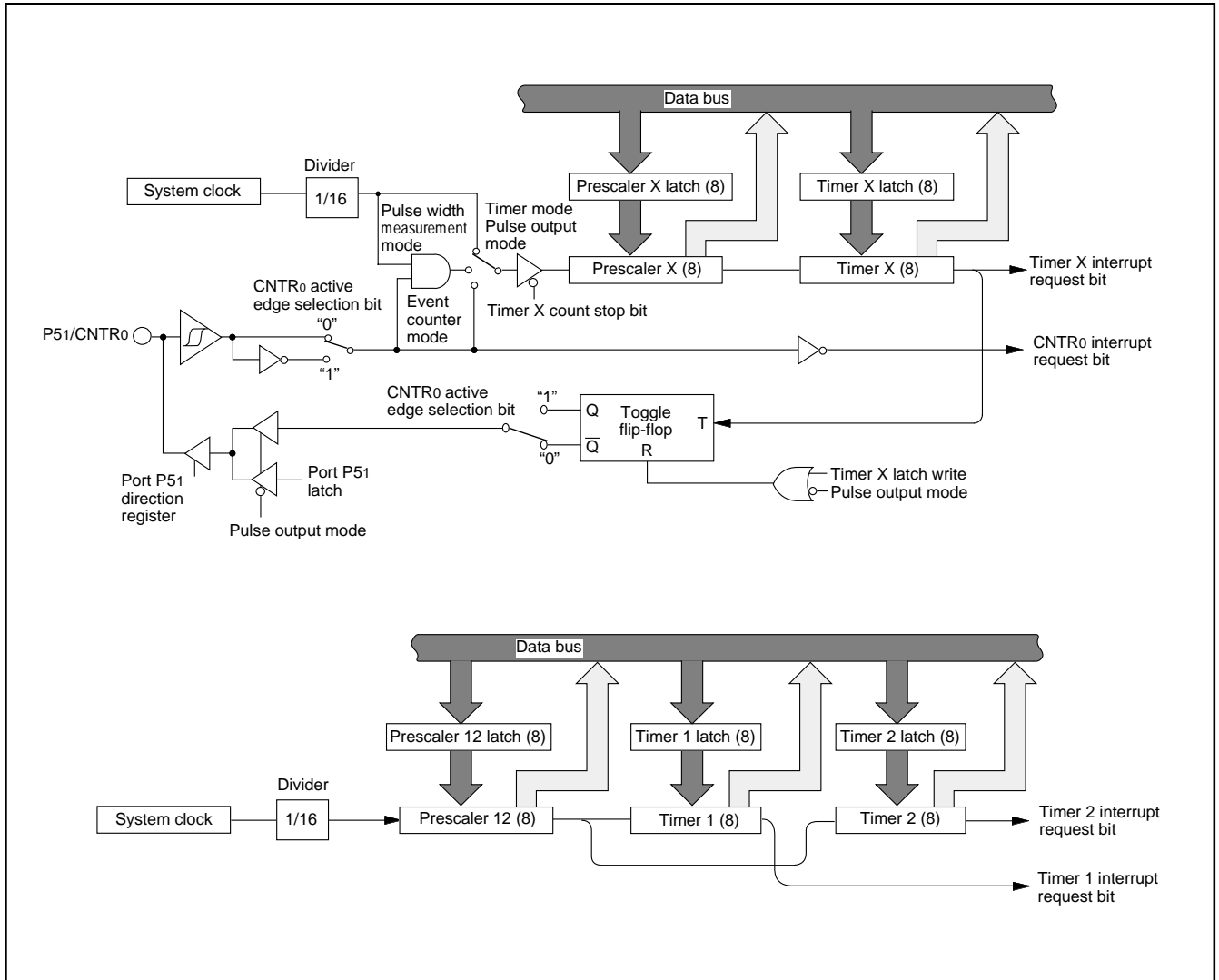


Fig. 17 Timer block diagram

HARDWARE

FUNCTIONAL DESCRIPTION

SERIAL I/O

Serial I/O can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer (baud rate generator) is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O Mode

Clock synchronous serial I/O mode can be selected by setting the mode selection bit of the serial I/O control register (bit 6 of address 0FE0₁₆) to "1".

For clock synchronous serial I/O, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the Transcemit/Receive buffer register.

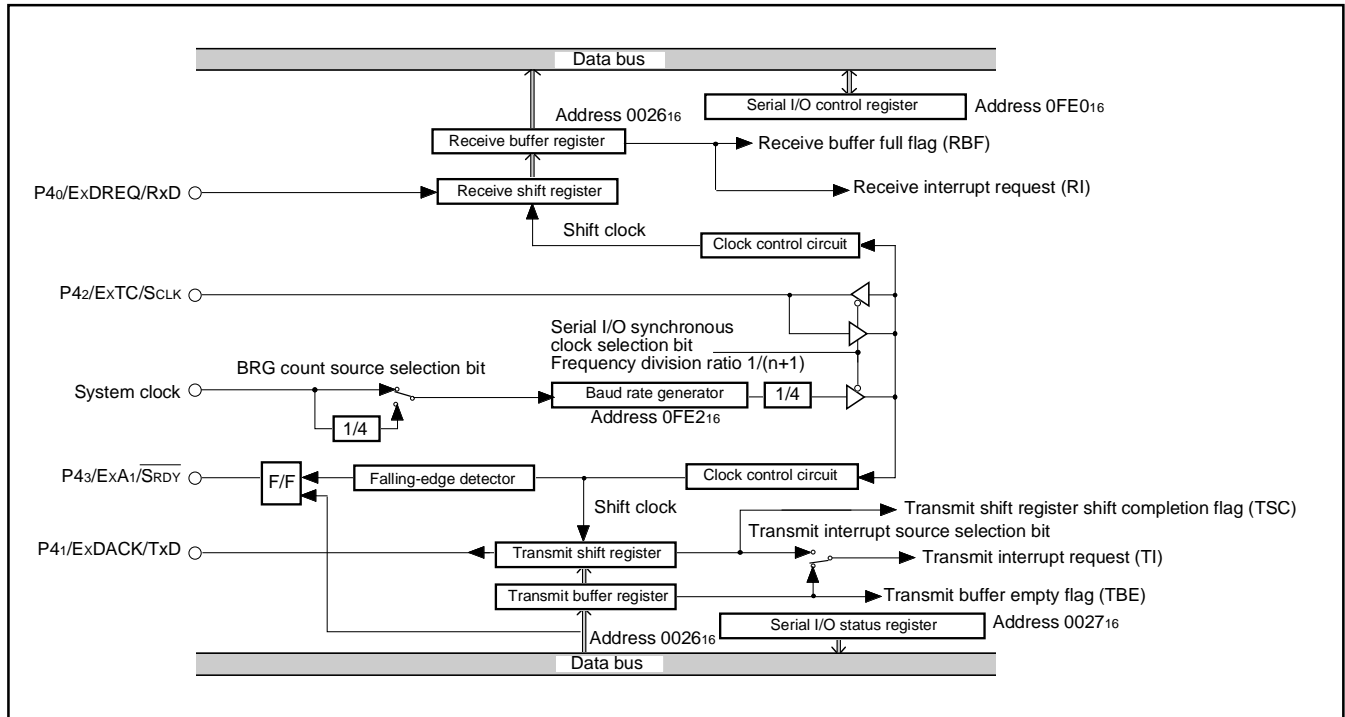


Fig. 18 Block diagram of clock synchronous serial I/O

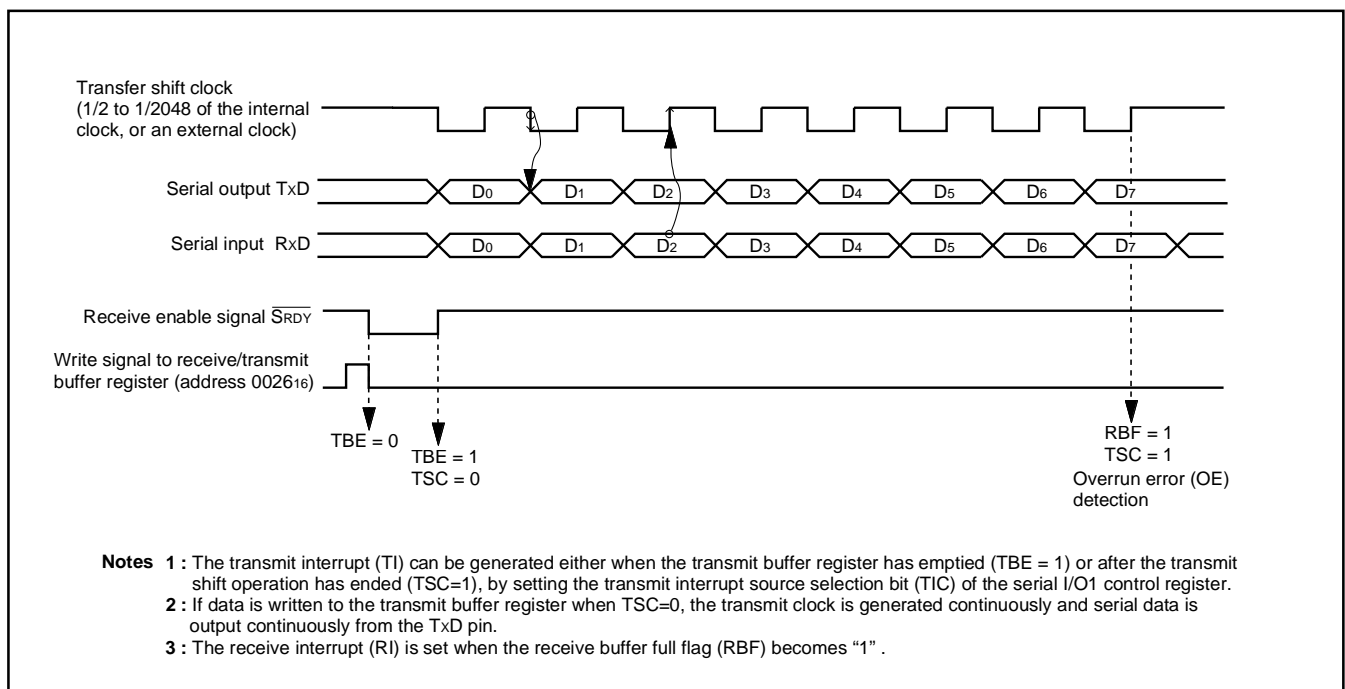


Fig. 19 Operation of clock synchronous serial I/O function

(2) Asynchronous Serial I/O (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by setting the serial I/O mode selection bit of the serial I/O control register to "0".

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer regis-

ter, but the two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer, and receive data is read from the receive buffer.

The transmit buffer can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.

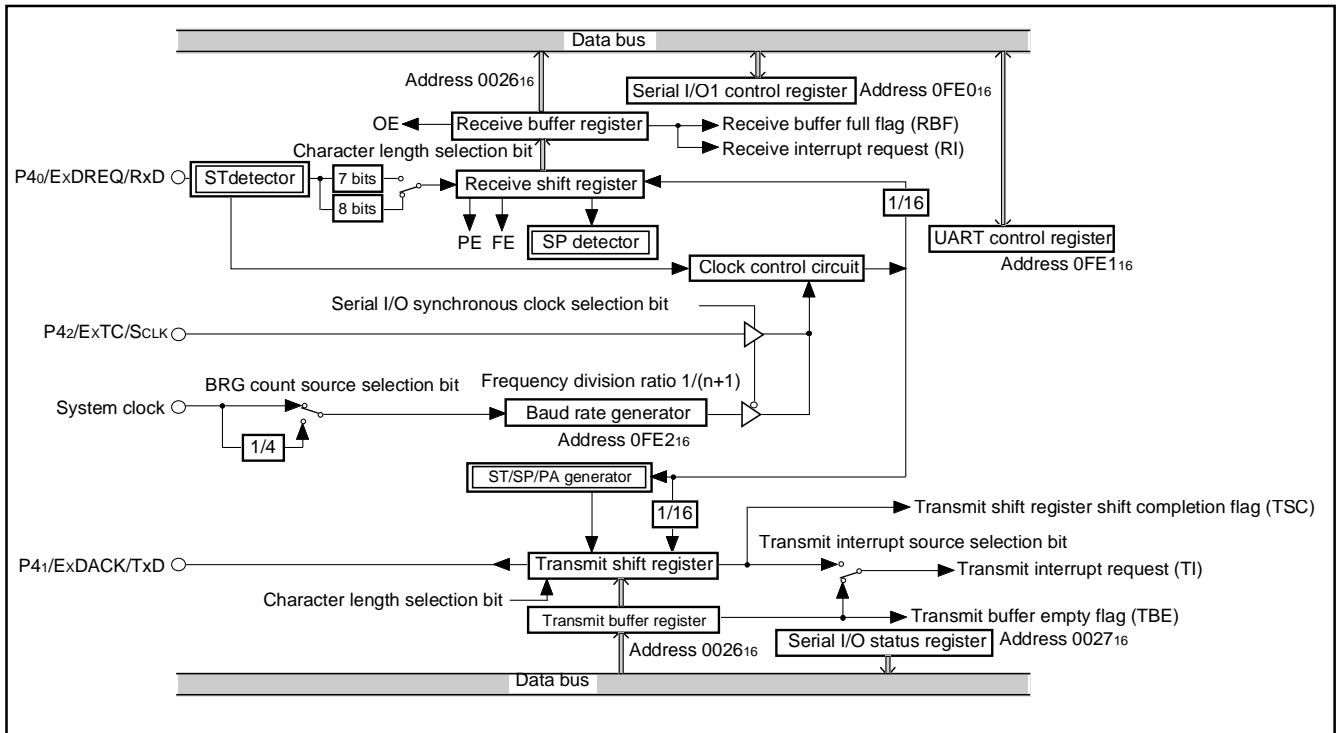


Fig. 20 Block diagram of UART serial I/O

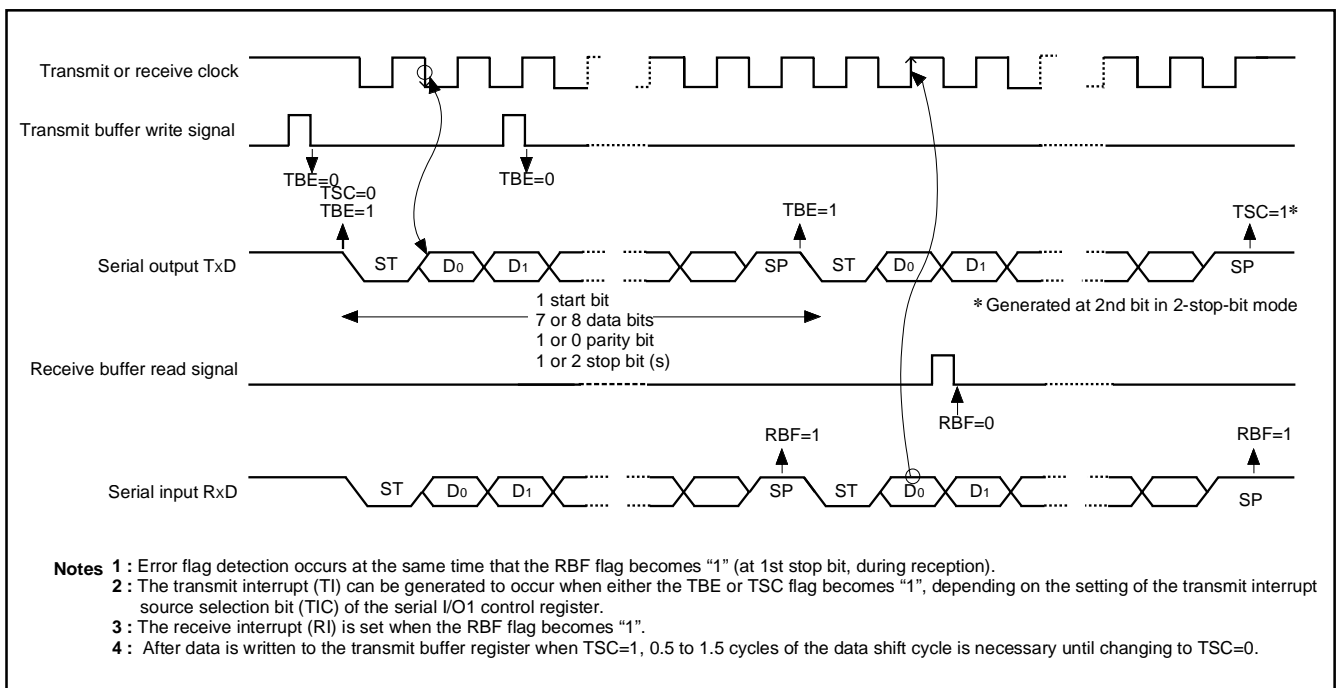


Fig. 21 Operation of UART serial I/O function

HARDWARE

FUNCTIONAL DESCRIPTION

[Serial I/O Control Register (SIOCON)] 0FE0₁₆

The serial I/O control register contains eight control bits for the serial I/O function.

[UART Control Register (UARTCON)] 0FE1₁₆

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer.

[Serial I/O Status Register (SIOSTS)] 0027₁₆

The read-only serial I/O status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to "0" when the receive buffer is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing "0" to the serial I/O enable bit SIOE (bit 7 of the serial I/O control register) also clears all the status flags, including the error flags.

All bits of the serial I/O status register are initialized to "0" at reset, but if the transmit enable bit (bit 4) of the serial I/O control register has been set to "1", the transmit shift register shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become "1".

[Transmit Buffer/Receive Buffer Register (TB/RB)] 0026₁₆

The transmit buffer register and the receive buffer register are located at the same address. The transmit buffer register is write-only and the receive buffer register is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer register is "0".

[Baud Rate Generator (BRG)] 0FE2₁₆

The baud rate generator determines the baud rate for serial transfer.

The baud rate generator divides the frequency of the count source by $1/(n + 1)$, where n is the value written to the baud rate generator.

■Notes on serial I/O

When setting the transmit enable bit to "1", the serial I/O transmit interrupt request bit is automatically set to "1". When not requiring the interrupt occurrence synchronized with the transmission enabled, take the following sequence.

- ① Set the serial I/O transmit interrupt enable bit to "0" (disabled).
- ② Set the transmit enable bit to "1".
- ③ Set the serial I/O transmit interrupt request bit to "0" after 1 or more instructions have been executed.
- ④ Set the serial I/O transmit interrupt enable bit to "1" (enabled).

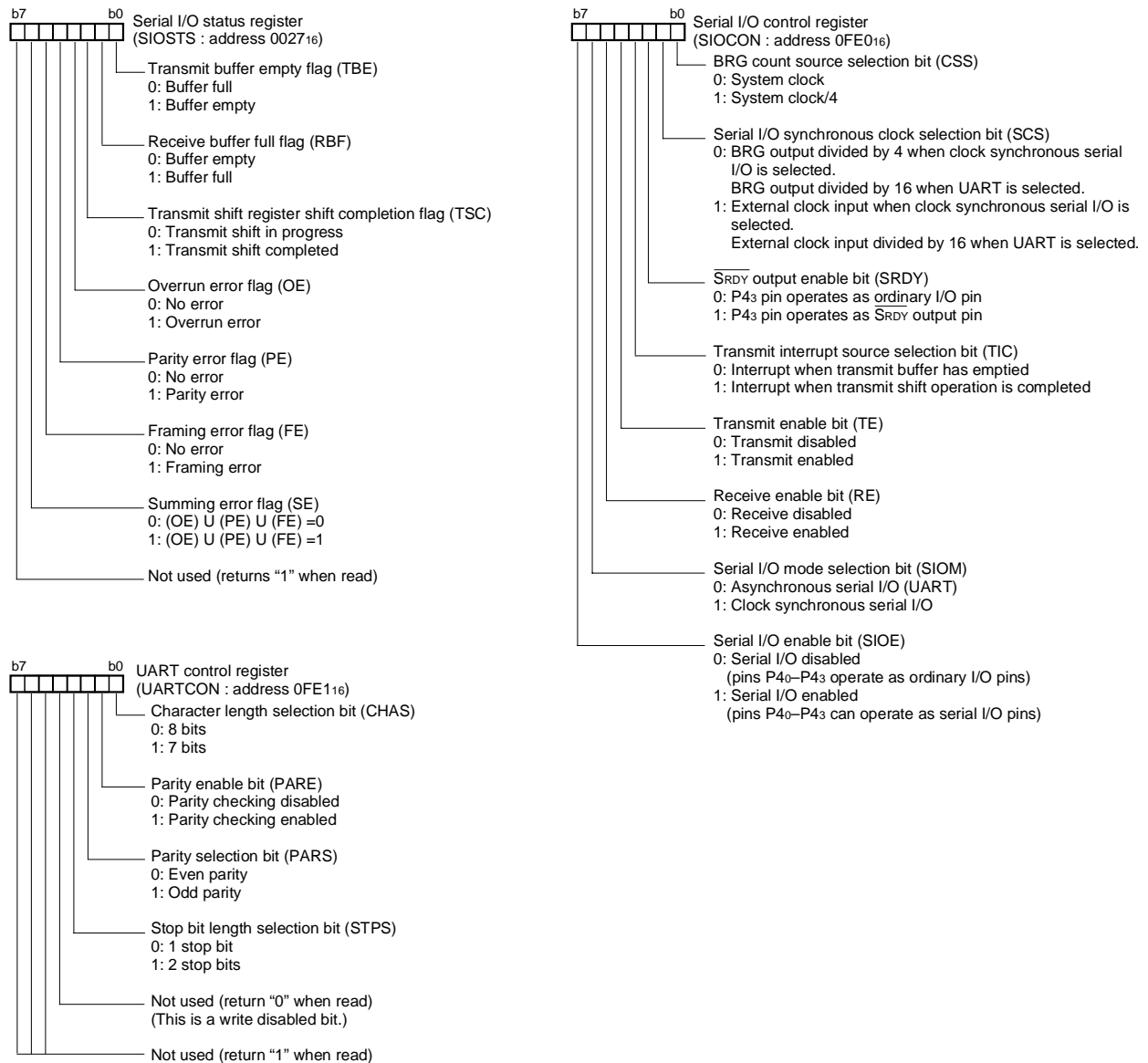


Fig. 22 Structure of serial I/O control registers

HARDWARE

FUNCTIONAL DESCRIPTION

USB FUNCTION

38K0 Group is equipped with a USB function control circuit (USBFCC) that enables effective interfacing with the host-PC. This circuit is in compliance with USB2.0's Full-Speed Transfer Mode (12 Mbps, equivalent to USB1.1). This circuit also supports all four transfer-types specified in the standard USB specification. The USBFCC has four endpoints that can select its transfer type. Although Endpoint 0 is fixed to Control Transfer, the Endpoints 1 to 3 can be set to Interrupt Transfer, Bulk Transfer, or Isochronous Transfer.

A dedicated circuit automatically performs stage management for Control Transfer and packet management for transactions, which are necessary for matching of data transmit/receive timing, error detection, and retry after error. This dedicated control circuit enables the user to develop a program or timing design very easily. Each endpoint can be programmed for data transfer conditions so that the endpoints are adaptive for all USB device class transfer systems.

The data buffer of each endpoint can be assigned to any area in the multi-channel RAM. This feature offers highly efficient memory usage by avoiding re-buffering and enabling simple data modification.

The transmit/receive data is directly transferred to the data buffer via the control circuit (direct RAM access type) without disturbing the CPU operation. This mechanism enables the CPU to transfer data smoothly with no drop in performance. In addition to this buffer function, a double-buffer setting will keep a re-buffering stall at a minimum and increase the overall data throughput (max. 64 bytes X 2 channels).

As other special signals control, the endpoints have detection functions for the USB bus reset signal, resume signal, suspend signal, and SOF signal, and also have a remote wake-up signal transmit function.

When completing data transfer or receiving a special signal, the endpoint generates the corresponding interrupt to the CPU (3 vectors/18 factors).

With all this essential yet comprehensive built-in hardware, your system using the 38K0 group will be ready for any USB application that comes its way.

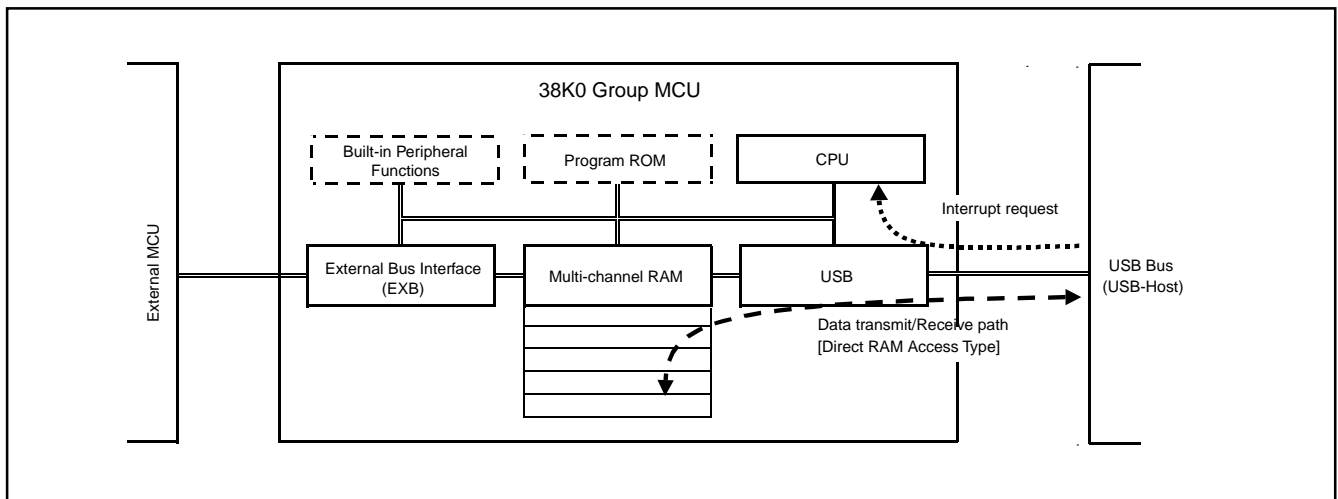


Fig. 23 USB function overview

USB Data Transfer

The USB specification promises 12 Mbps data transfer in the full-speed mode, that is equivalent to 1.5 M bytes per second of data transactions.

However, in USB data transfer, bit-stuffing may be executed depending on the bit patterns of the transfer data, possibly resulting in 1-byte data (normally 8 bits) handled as up to 10 bits.

Because USB uses asynchronous transfers, the clock cycle of the USB internal reference clock may change to adjust to the clock phase. Therefore, the access timing of the USBFCC for the multi-channel RAM will change owing to the frequency of internal clock ϕ .

When the USBFCC is operating at $\phi = 8$ MHz, access for a normal

transfer is performed every 5 to 6 cycles and access for a bit-stuffing transfer is performed in up to 7 cycles.

If the EXB function is enabled in the above conditions, this function generates a maximum wait of 1 clock cycle, so that the access is performed every 4 to 8 cycles.

When operating at $\phi = 6$ MHz, a normal access is performed every 4 cycles. If the clock-phase correction of the reference clock occurs, access is performed every 3 to 5 cycles.

If bit stuffing occurs at this clock rate, the access cycle will be extended to up to 6 cycles. When the EXB function that generates a maximum 1-wait cycle is used in this condition, the access cycle will be 2 (min.) to 7 (max.) cycles.

USB Function Control Circuit (USBFCC) Block Diagram

The following diagram shows the USBFCC block diagram. The circuit comprises:

- (1) Serial Interface Engine (SIE)
- (2) Device Control Unit (DCU)
- (3) Internal Memory Interface (MIF)
- (4) CPU Interface (CIF)

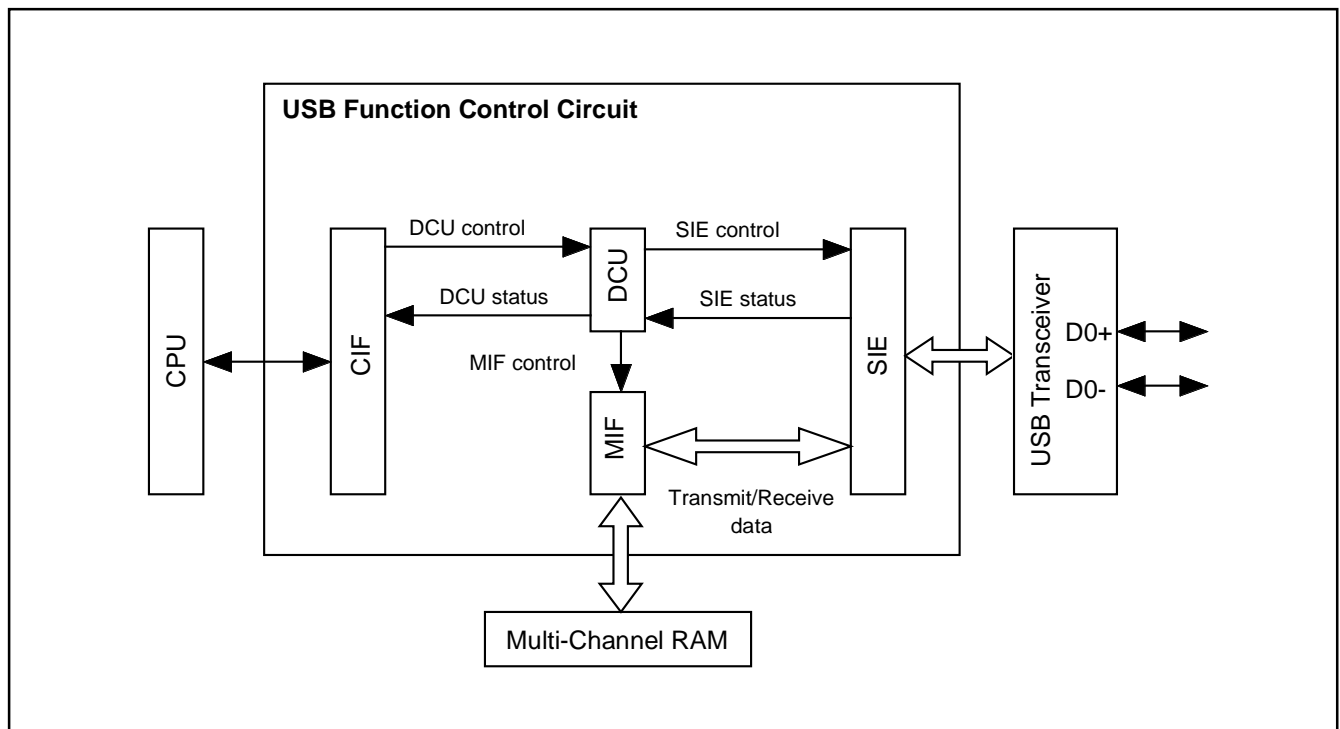


Fig. 24 USB Function Control Circuit (USBFCC) block diagram

(1) Serial Interface Engine (SIE)

The SIE performs the following USB lower-layer protocols (packets, transactions):

- Sampling of receive data and clock, generation of transmit clock
- Serial-to-parallel conversion of transmit/receive data
- NRZI (Non Return Zero Invert) encode/decode
- Bit stuffing/unstuffing
- SYNC (Synchronization Pattern) detection, EOP (End of Packet) detection
- USB address detection, endpoint detection
- CRC (Cyclic Redundancy Check) generation and checking

(2) Device Control Unit (DCU)

The DCU manages the following USB upper-layer protocols (address/endpoint and control-transfer sequence):

- Status control for each endpoint
- Control-transfer sequence control
- Memory interface status control

(3) Memory Interface (MIF)

The MIF controls the flow of data transfer between the SIE and the multi-channel RAM under the management of the DCU.

(4) CPU Interface (CIF)

The CIF performs the following functions:

- Mode setting via registers, DCU control signal generation, DCU status signal reading
- Interrupt signal generation
- Internal bus interface control.

HARDWARE

FUNCTIONAL DESCRIPTION

USB Port External Circuit Configuration

The operation mode of the USB port driver circuit can be configured by USB control register (address 0010₁₆).

Figure 25 and Figure 26 show the USB port external circuit block diagram.

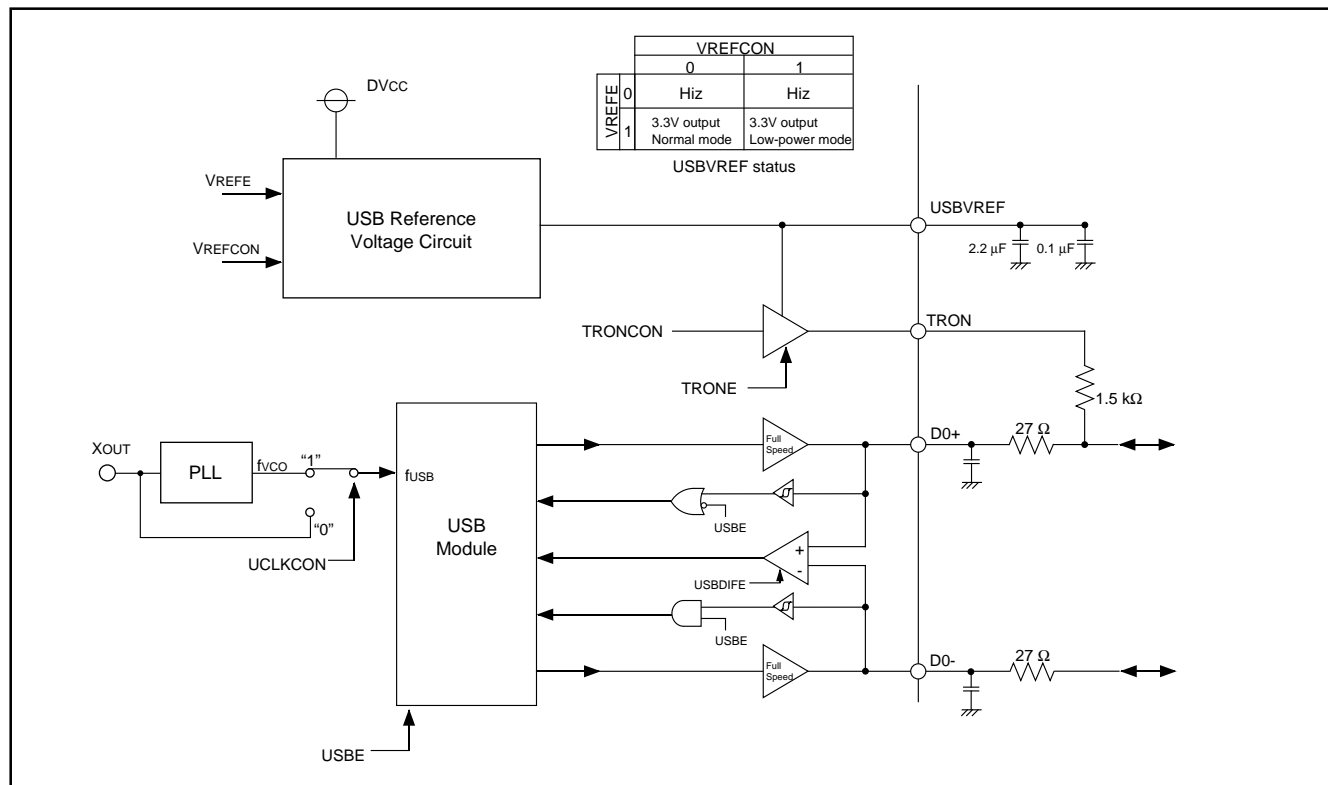


Fig. 25 USB port external circuit (D0+, D0-, USBVREF, TrON) block diagram ($4.0V \leq V_{CC} \leq 5.25V$)

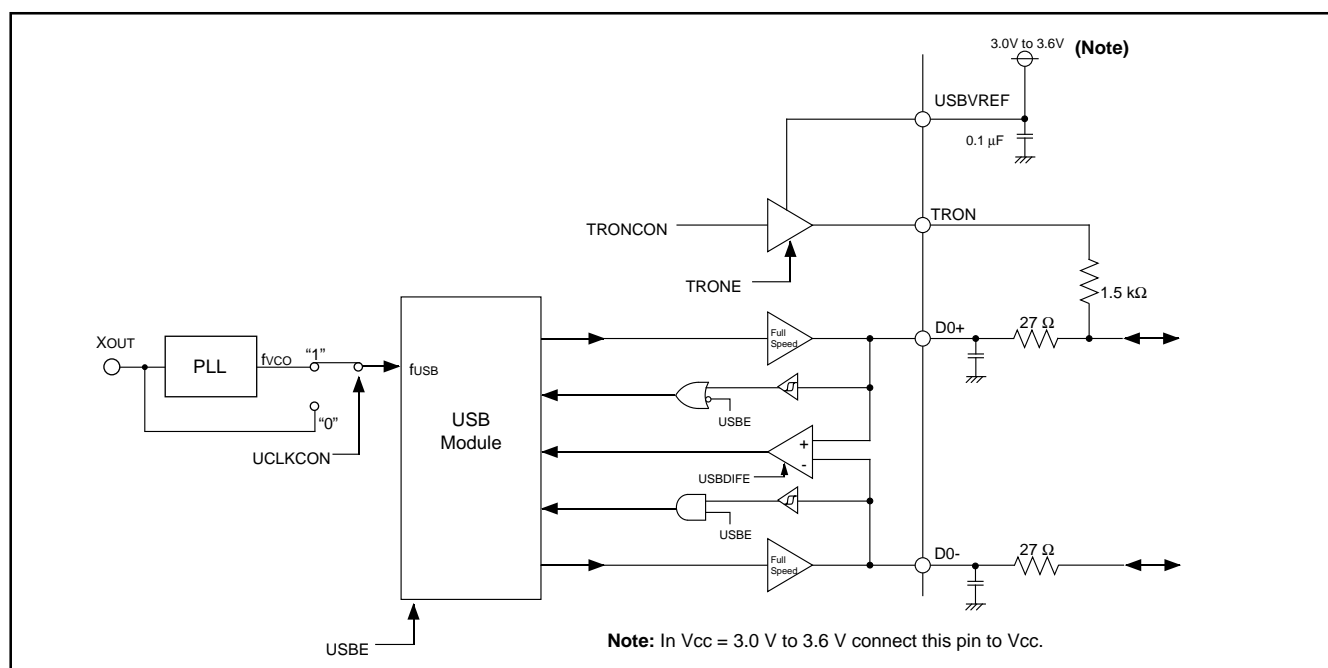


Fig. 26 USB port external circuit (D0+, D0-, USBVREF, TrON) block diagram ($3.0V \leq V_{CC} \leq 4.0V$)

Endpoint Buffer Area Setting

The buffer area used in data transfer can be assigned to any area of the multi-channel RAM for each endpoint.

●Buffer area beginning address

The buffer area configuration register (address 0FED₁₆) defines the beginning address of the buffer area (every 32 bytes) for each Endpoint. However, the only RAM area is configurable.

- 00h [Address 0000₁₆], 01h [Address 0020₁₆]: Not configurable
- 02h [Address 0040₁₆] to 1Fh [Address 03E0₁₆]: Configurable

●Interrupt-source dependant buffer area offset address

An offset value is added to the beginning address of each source, which is specified by the interrupt source register (address 001D₁₆), for each endpoint.

This section describes in detail the beginning address specified by the buffer area set register as offset address 00h, according to each endpoint.

(1) Endpoint 00

Endpoint 00 has two kinds of interrupt sources for accessing the buffer. The respective address offsets are:

- BSRDY00 (SETUP Buffer Ready Interrupt): Offset address = 00h
- BRDY00 (OUT or IN Buffer Ready Interrupt): Offset address = 08h

(2) Endpoint 01

The buffer area offset address for each interrupt source for of Endpoint 01 varies according to the contents of the EP01 set register (address 0019₁₆).

- In single buffer mode (DBLB01 = "0"):

Endpoint 01 has only one interrupt source for accessing the buffer.

B0RDY01 (Buffer 0 Ready Interrupt): Offset address = 00h

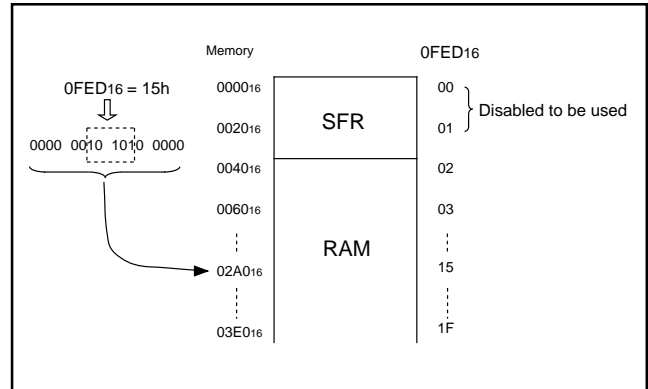


Fig. 27 Example setting of buffer area beginning address

- In double buffer mode (DBLB01 = "1"):

Endpoint 01 has two kinds of interrupt sources for accessing the buffer.

B0RDY01 (Buffer 0 Ready Interrupt): Offset address = 00h

B1RDY01 (Buffer 1 Ready Interrupt):

The offset address varies according to the double buffer beginning address set bit (BSIZ01).

- Offset address = 08h when BSIZ01 = 00
- Offset address = 10h when BSIZ01 = 01
- Offset address = 40h when BSIZ01 = 10
- Offset address = 80h when BSIZ01 = 11

(3) Endpoints 02 and 03

Same as Endpoint 01.

Notes

The selected RAM area must be within addresses 0040₁₆ to 03FF₁₆.

Make sure the buffer area beginning address is set in agreement with the offset address and the number of transmit/receive data bytes.

This is particularly important when in the double buffer mode or when handling 64-byte data.

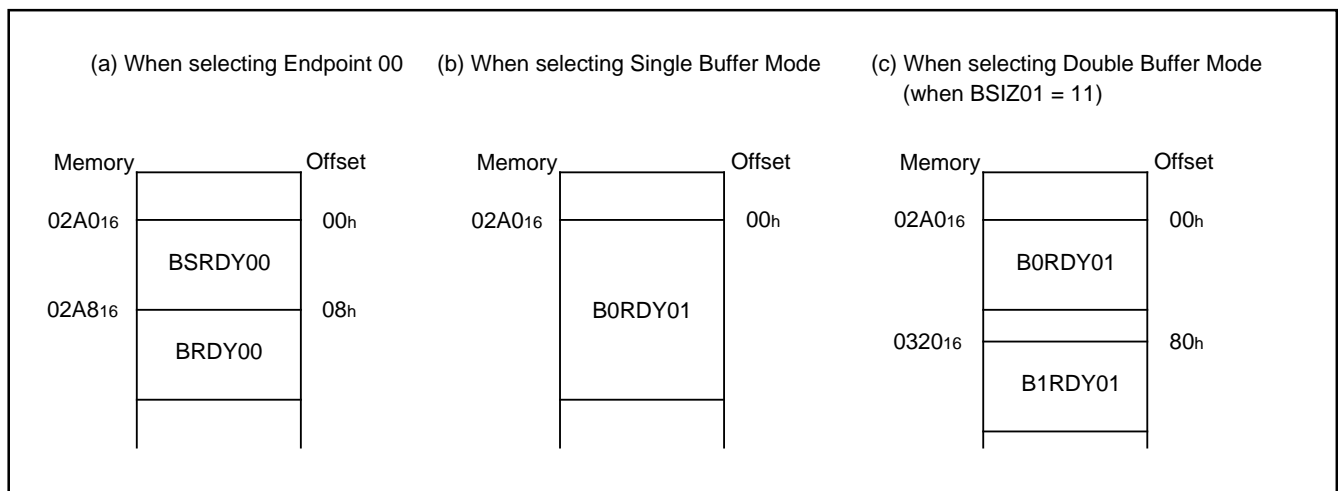


Fig. 28 Examples of interrupt source dependant buffer area offset address

HARDWARE

FUNCTIONAL DESCRIPTION

USB Interrupt Function

USB Interrupt Control Circuit (USBINTCON) has 3 requests and 16 USB-device interrupt request sources. Each interrupt source register enables the user to easily determine which interrupt has occurred.

Table 8 shows the list of USB interrupt sources.

Table 8 USB interrupt sources

Interrupt request bit (IREQ1: Address 003C ₁₆)	USB interrupt bit (USBIREQ: Address 0017 ₁₆)	Interrupt source
USB bus reset	—	At USB bus reset signal detection: After enabling the USB module (USBE = "1"), an interrupt request occurs when 2.5 μ s SE0 state is detected in D0+/D0- port. (Equivalent to 120-clock length when fusb = 48 MHz)
USB SOF	—	At SOF packet receive: After enabling the USB module (USBE = "1"), an interrupt request occurs when SOF packet is detected in D0+/D0- port. Its occurrence does not depend on frame-time or CRC value after SOF packet is transferred. (Normally, SOF packet detection occurs only when fusb = 48 MHz)
USB device	EP00	At Endpoint 00 data transfer complete: <ul style="list-style-type: none">•Buffer ready (read/write enabled state)•Control transfer completed•Status stage transition•SETUP buffer ready (read enabled state)•Control transfer error
	EP01	At Endpoint 01 data transfer complete: <ul style="list-style-type: none">•Buffer 0 ready (read/write enabled state)•Buffer 1 ready (read/write enabled state)•Transfer error
	EP02	At Endpoint 02 data transfer complete: <ul style="list-style-type: none">•Buffer 0 ready (read/write enabled state)•Buffer 1 ready (read/write enabled state)•Transfer error
	EP03	At Endpoint 03 data transfer complete: <ul style="list-style-type: none">•Buffer 0 ready (read/write enabled state)•Buffer 1 ready (read/write enabled state)•Transfer error
	SUS	At suspend signal detection: After enabling the USB module (USBE = "1"), an interrupt request occurs when 3 ms J state is detected in D0+/D0- port. (Equivalent to 144,000 clock-length when fusb = 48MHz)
	RSM	At resume signal detection: After enabling the USB module (USBE = "1") and resume interrupt (RSME = "1"), an interrupt request occurs when a bus state change (J state to SE0 or K state) is detected in D0- port.

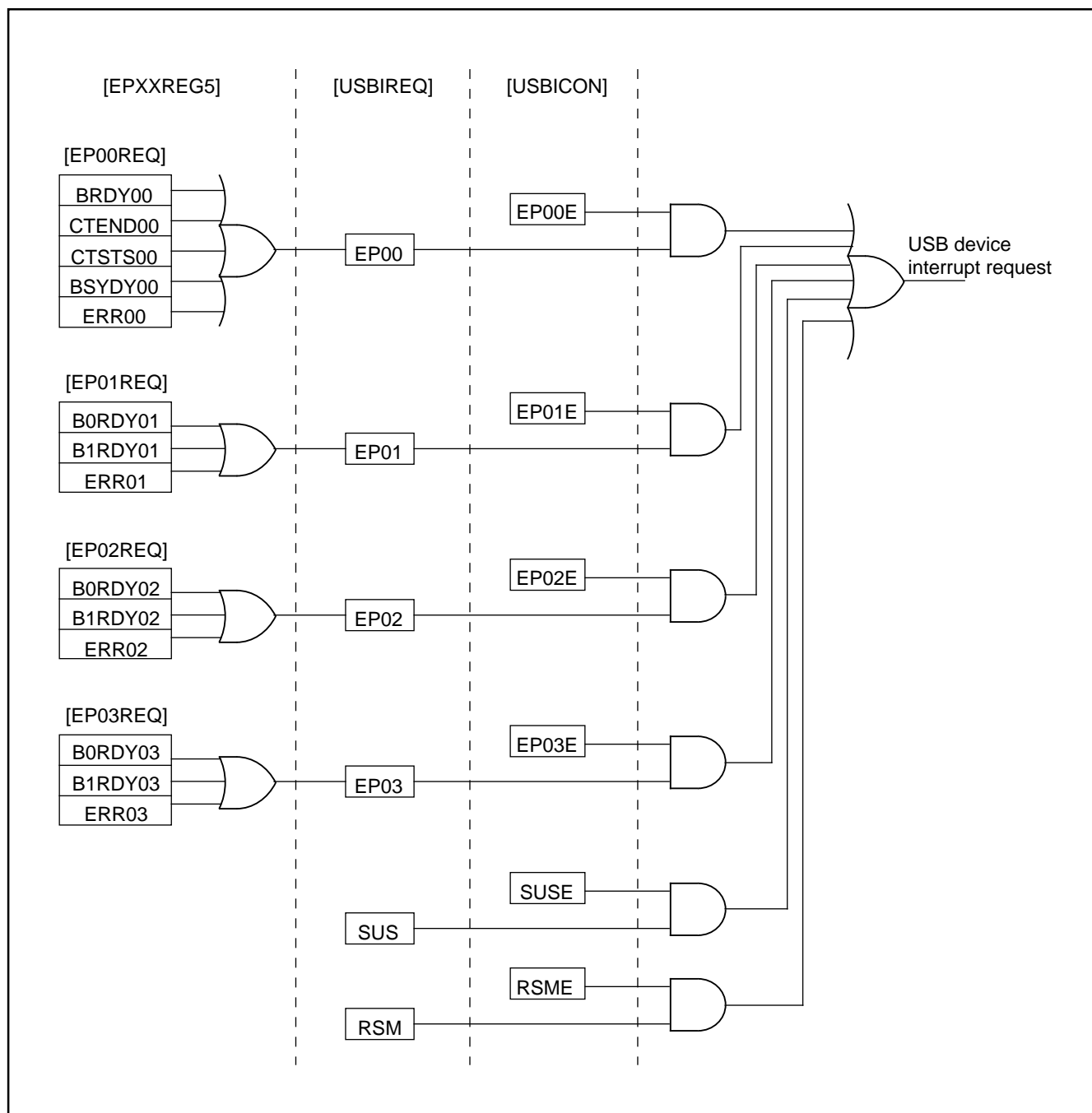


Fig. 29 USB device interrupt control

HARDWARE

FUNCTIONAL DESCRIPTION

USB Register List

The USB register list is shown below.

Address	Register Name	SYMBOL	USB SFR							
			bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0010 ₁₆	USB control register	USBCON	USBE	UCLKCON	USBDFE	VREFE	VREFCON	TRONE	TRONCON	WKUP
0011 ₁₆	USB function enable register	USBAE								AD0E
0012 ₁₆	USB function address register	USBA0								
0013 ₁₆										
0014 ₁₆	Frame number register Low	FNUML								
0015 ₁₆	Frame number register High	FNUMH								
0016 ₁₆	USB interrupt source enable register	USBICON	RSME	SUSE			EP03E	EP02E	EP01E	EP00E
0017 ₁₆	USB interrupt source register	USBIREQ	RSM	SUS			EP03	EP02	EP01	EP00
0018 ₁₆	Endpoint index register	USBINDEX								EPIDX[1:0]
0019 ₁₆	Endpoint field register 1	EPXXREG1								
001A ₁₆	Endpoint field register 2	EPXXREG2								
001B ₁₆	Endpoint field register 3	EPXXREG3								
001C ₁₆	Endpoint field register 4	EPXXREG4								
001D ₁₆	Endpoint field register 5	EPXXREG5								
001E ₁₆	Endpoint field register 6	EPXXREG6								
001F ₁₆	Endpoint field register 7	EPXXREG7								
0FEC ₁₆	Endpoint field register 8	EPXXREG8								
0FED ₁₆	Endpoint field register 9	EPXXREG9								

(1) Endpoint 00

0019 ₁₆	EP00 stage register	EP00STG								SETUP00
001A ₁₆	EP00 control register 1	EP00CON1								PID00[1:0]
001B ₁₆	EP00 control register 2	EP00CON2								BVAL00
001C ₁₆	EP00 control register 3	EP00CON3								CTENDE00
001D ₁₆	EP00 interrupt source register	EP00REQ			ERR00	BSRDY00	CTSTS00	CTEND00		BRDY00
001E ₁₆	EP00 byte number register	EP00BYT						BBYT00[3:0]		
001F ₁₆										
0FEC ₁₆										
0FED ₁₆	EP00 buffer area set register	EP00BUF						BADD00[4:0]		

(2) Endpoint 01

0019 ₁₆	EP01 set register	EP01CFG	TYP01[1:0]	DIR01	ITMD01	SQCL01	DBLB01		BSIZ01[1:0]	
001A ₁₆	EP01 control register 1	EP01CON1							PID01[1:0]	
001B ₁₆	EP01 control register 2	EP01CON2								B0VAL01
001C ₁₆	EP01 control register 3	EP01CON3								B1VAL01
001D ₁₆	EP01 interrupt source register	EP01REQ					ERR01	B1RDY01		B0RDY01
001E ₁₆	EP01 byte number register 0	EP01BYT0				B0BYT01[6:0]				
001F ₁₆	EP01 byte number register 1	EP01BYT1				B1BYT01[6:0]				
0FEC ₁₆	EP01 MAX. packet size register	EP01MAX				MXPS01[6:0]				
0FED ₁₆	EP01 buffer area set register	EP01BUF						BADD01[4:0]		

(3) Endpoint 02

0019 ₁₆	EP02 set register	EP02CFG	TYP02[1:0]	DIR02	ITMD02	SQCL02	DBLB02		BSIZ02[1:0]	
001A ₁₆	EP02 control register 1	EP02CON1							PID02[1:0]	
001B ₁₆	EP02 control register 2	EP02CON2								B0VAL02
001C ₁₆	EP02 control register 3	EP02CON3								B1VAL02
001D ₁₆	EP02 interrupt source register	EP02REQ					ERR02	B1RDY02		B0RDY02
001E ₁₆	EP02 byte number register 0	EP02BYT0				B0BYT02[6:0]				
001F ₁₆	EP02 byte number register 1	EP02BYT1				B1BYT02[6:0]				
0FEC ₁₆	EP02 MAX. packet size register	EP02MAX				MXPS02[6:0]				
0FED ₁₆	EP02 buffer area set register	EP02BUF						BADD02[4:0]		

(4) Endpoint 03

0019 ₁₆	EP03 set register	EP03CFG	TYP03[1:0]	DIR03	ITMD03	SQCL03	DBLB03		BSIZ03[1:0]	
001A ₁₆	EP03 control register 1	EP03CON1							PID03[1:0]	
001B ₁₆	EP03 control register 2	EP03CON2								B0VAL03
001C ₁₆	EP03 control register 3	EP03CON3								B1VAL03
001D ₁₆	EP03 interrupt source register	EP03REQ					ERR03	B1RDY03		B0RDY03
001E ₁₆	EP03 byte number register 0	EP03BYT0				B0BYT03[6:0]				
001F ₁₆	EP03 byte number register 1	EP03BYT1				B1BYT03[6:0]				
0FEC ₁₆	EP03 MAX. packet size register	EP03MAX				MXPS03[6:0]				
0FED ₁₆	EP03 buffer area set register	EP03BUF						BADD03[4:0]		

 : Not used

Fig. 30 USB related registers

USB Related Registers

The USB related registers are shown below.

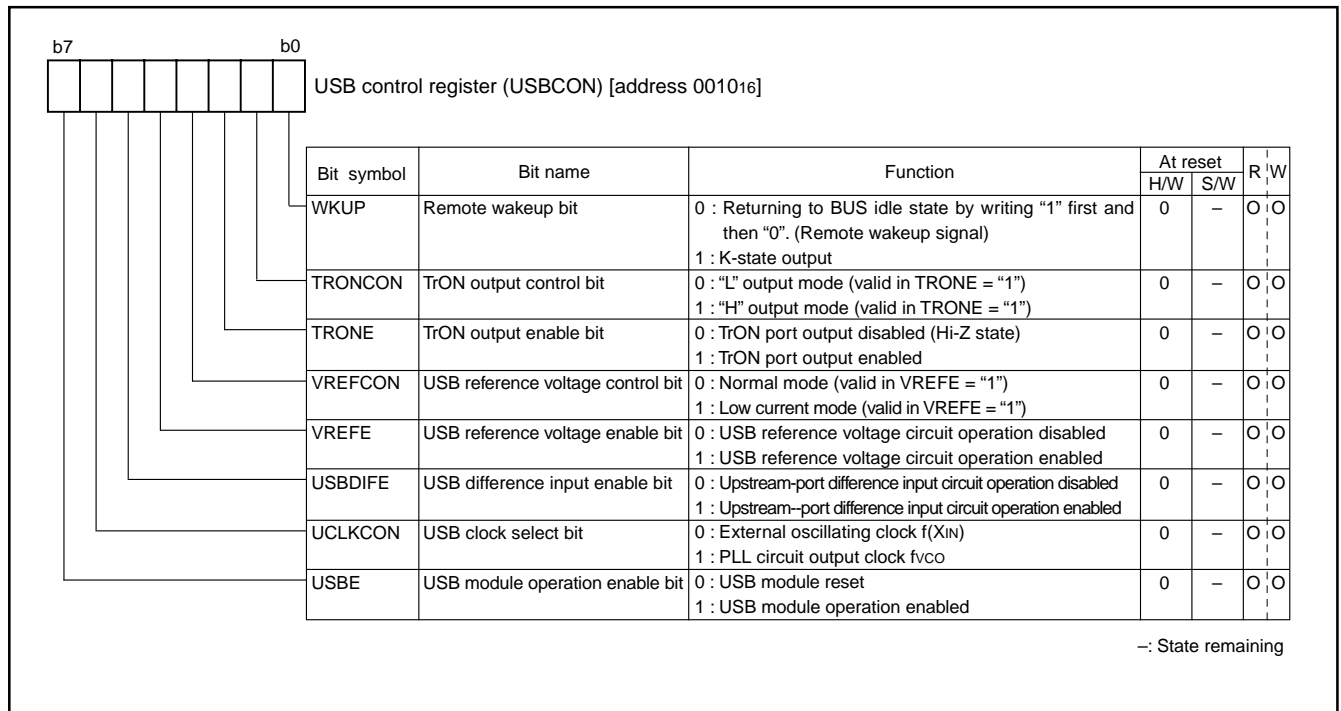


Fig. 31 Structure of USB control register

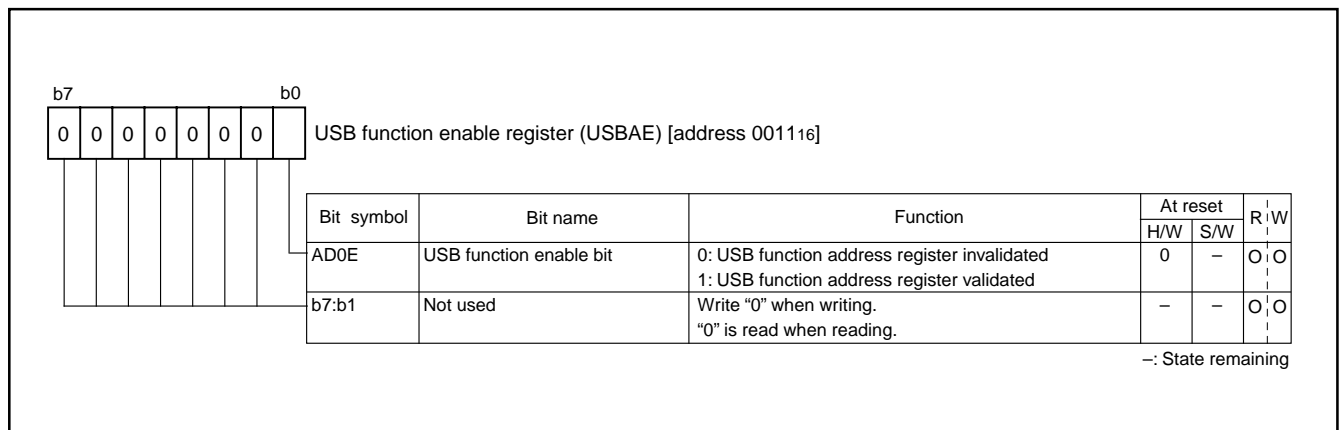


Fig. 32 Structure of USB function enable register

HARDWARE

FUNCTIONAL DESCRIPTION

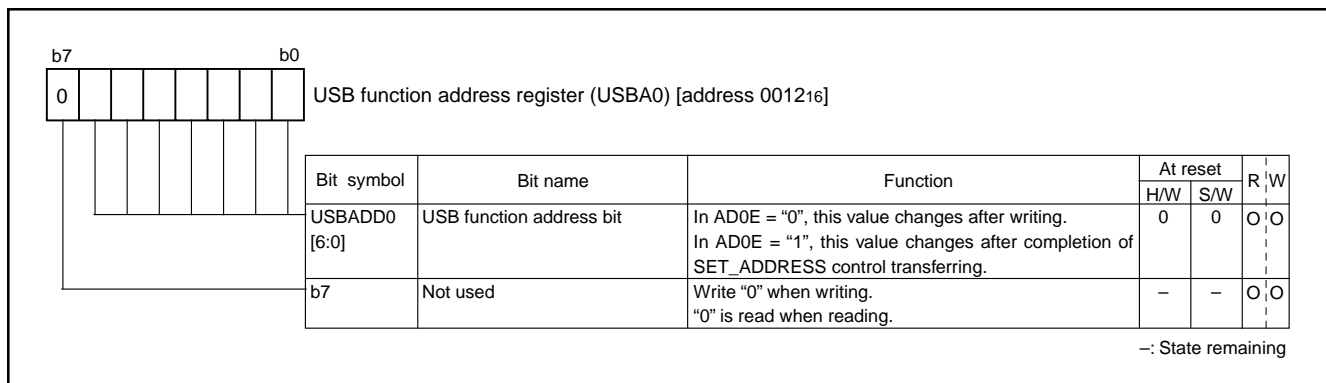


Fig. 33 Structure of USB function address register

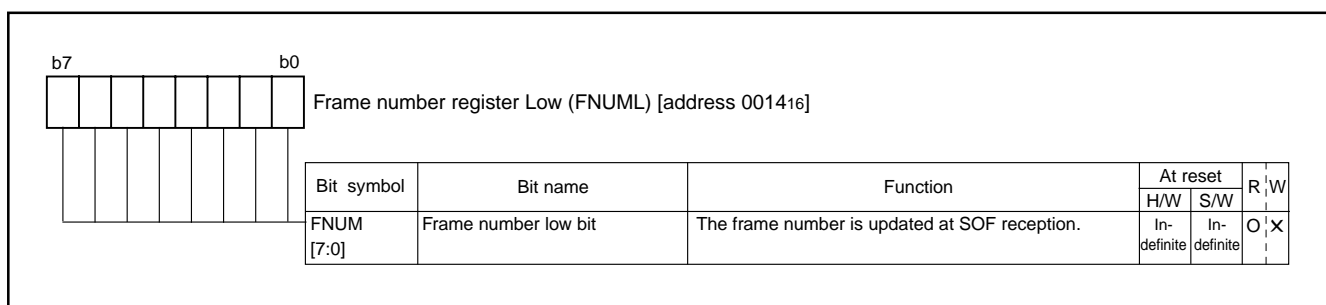


Fig. 34 Structure of Frame number register Low

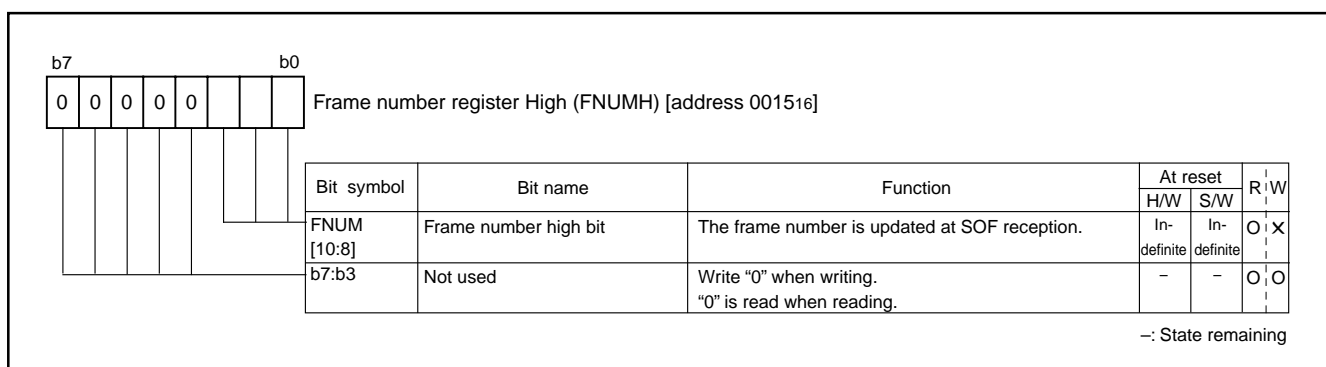


Fig. 35 Structure of Frame number register High

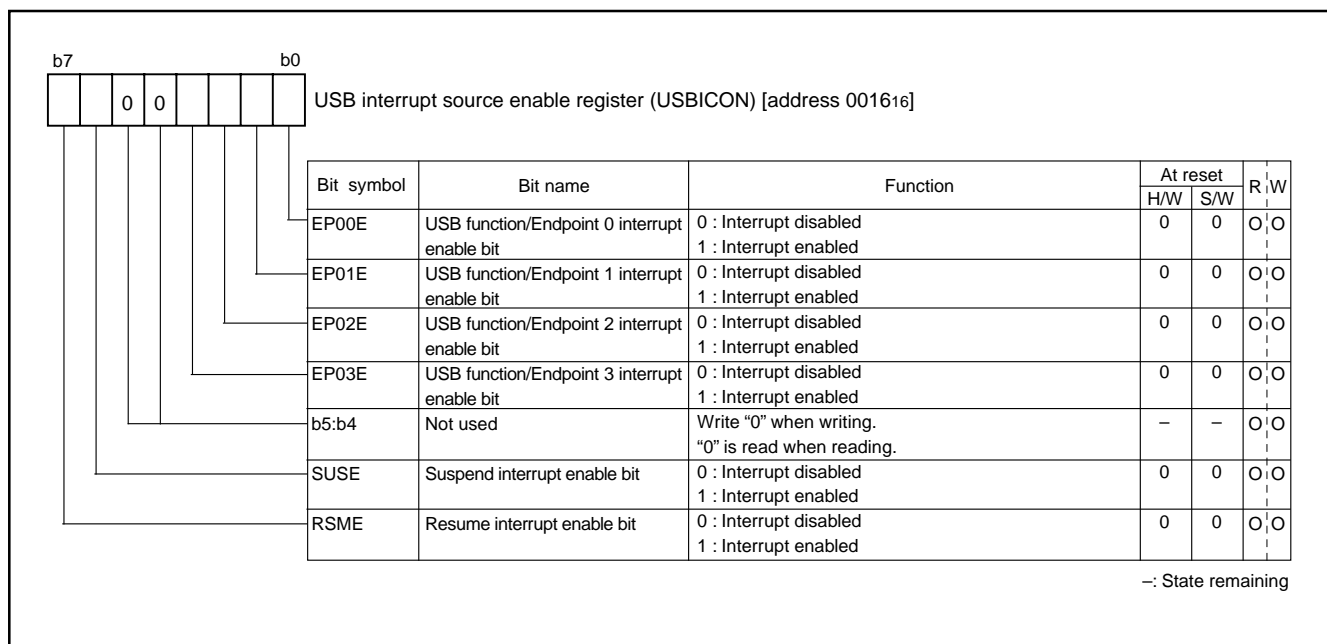


Fig. 36 Structure of USB interrupt source enable register

HARDWARE

FUNCTIONAL DESCRIPTION

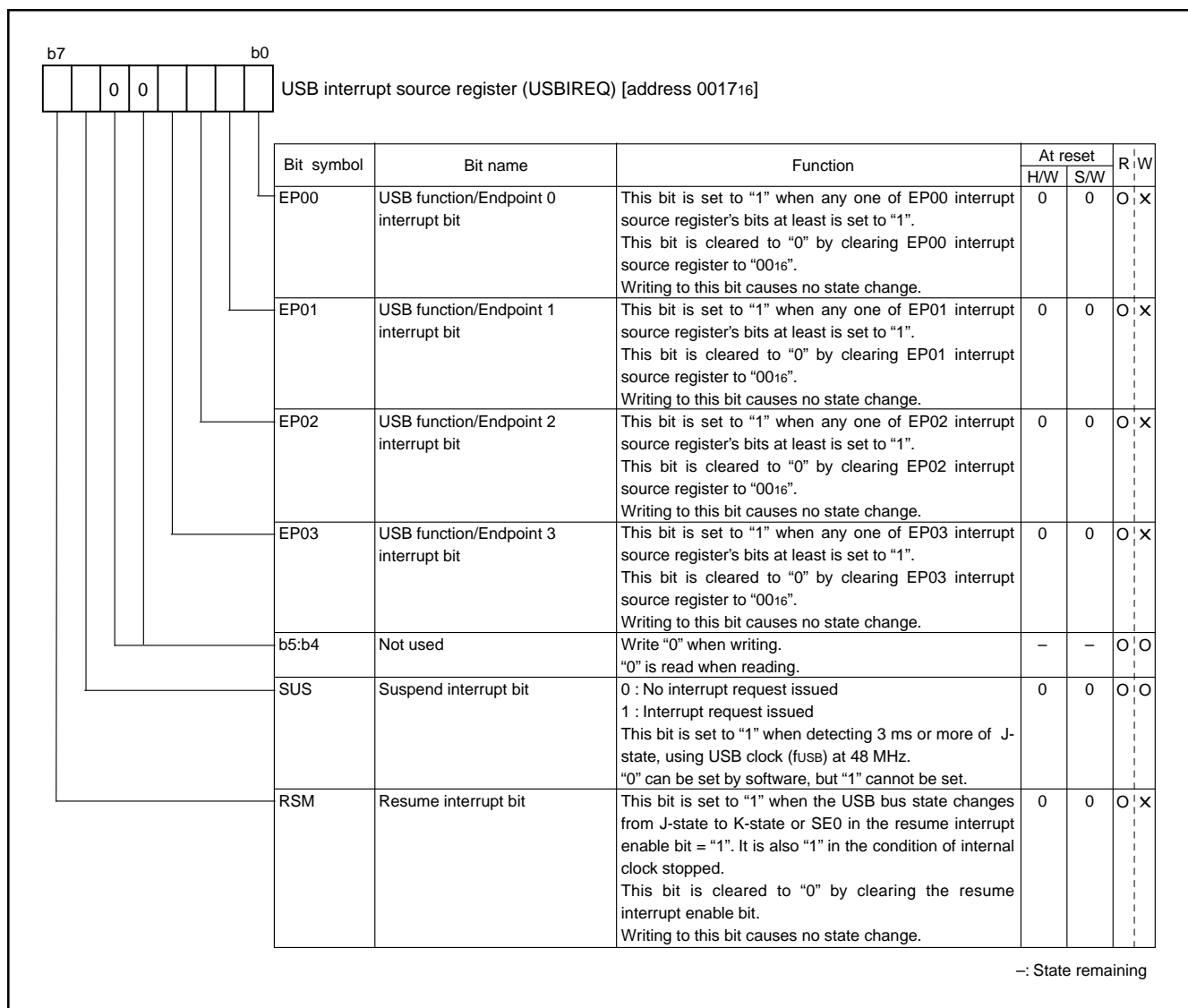


Fig.37 Structure of USB interrupt source register

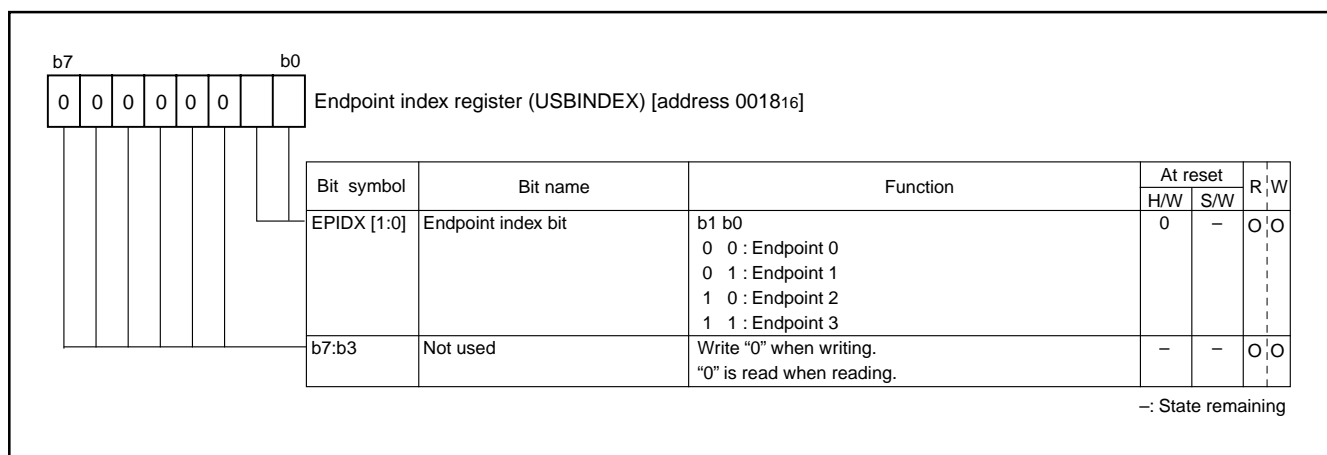


Fig. 38 Structure of Endpoint index register

(1) Endpoint 00

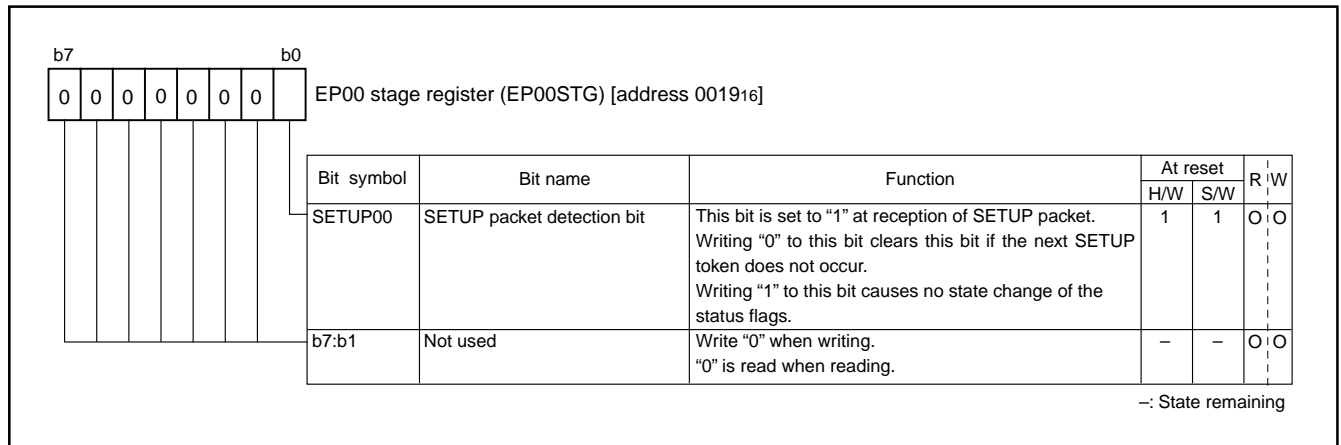


Fig. 39 Structure of EP00 stage register

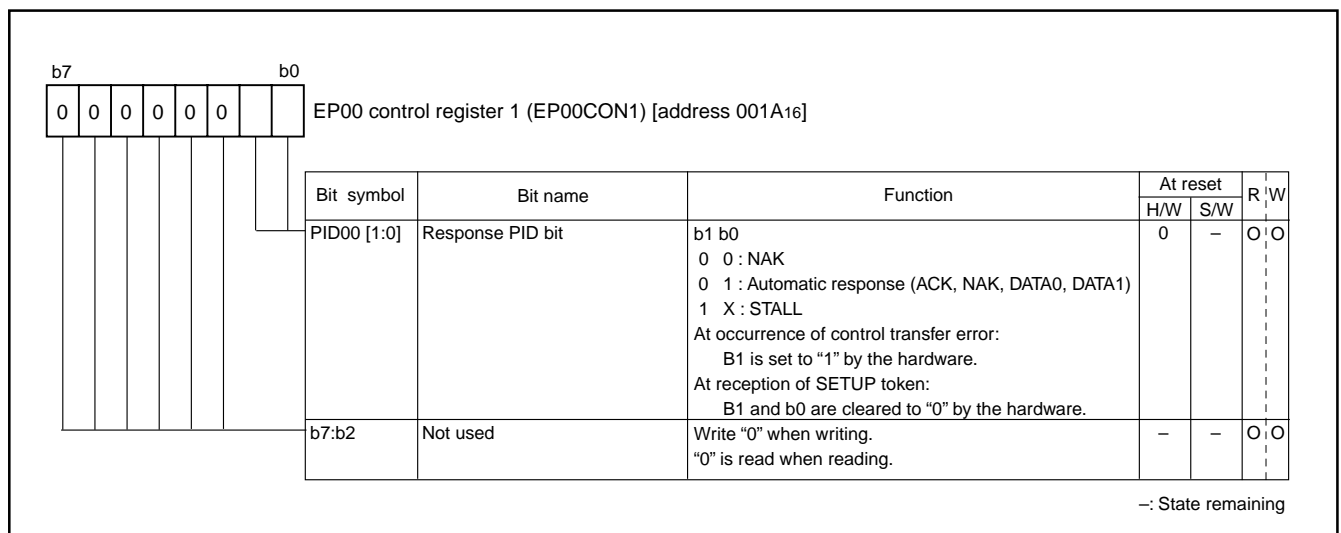


Fig. 40 Structure of EP00 control register 1

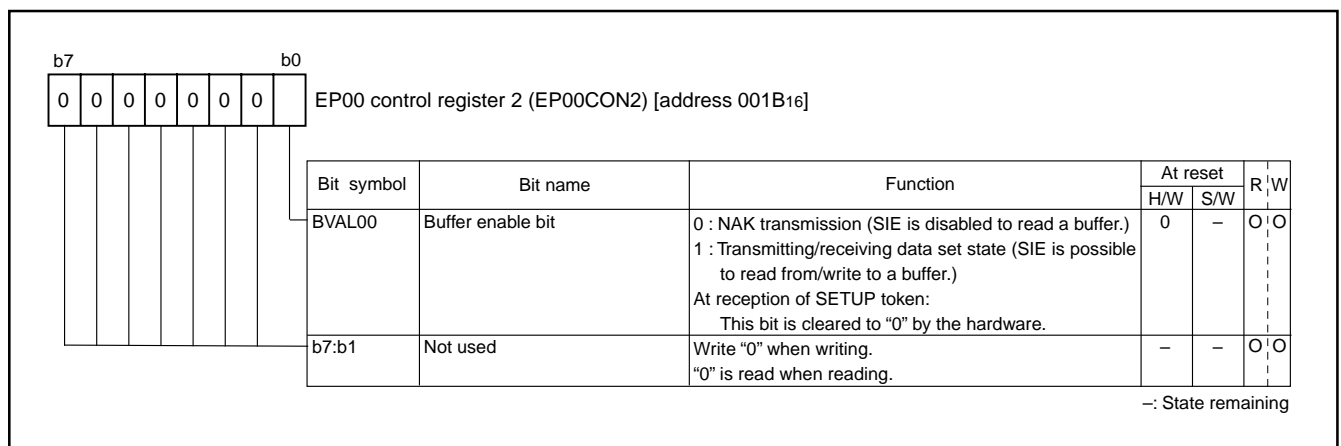


Fig. 41 Structure of EP00 control register 2

HARDWARE

FUNCTIONAL DESCRIPTION

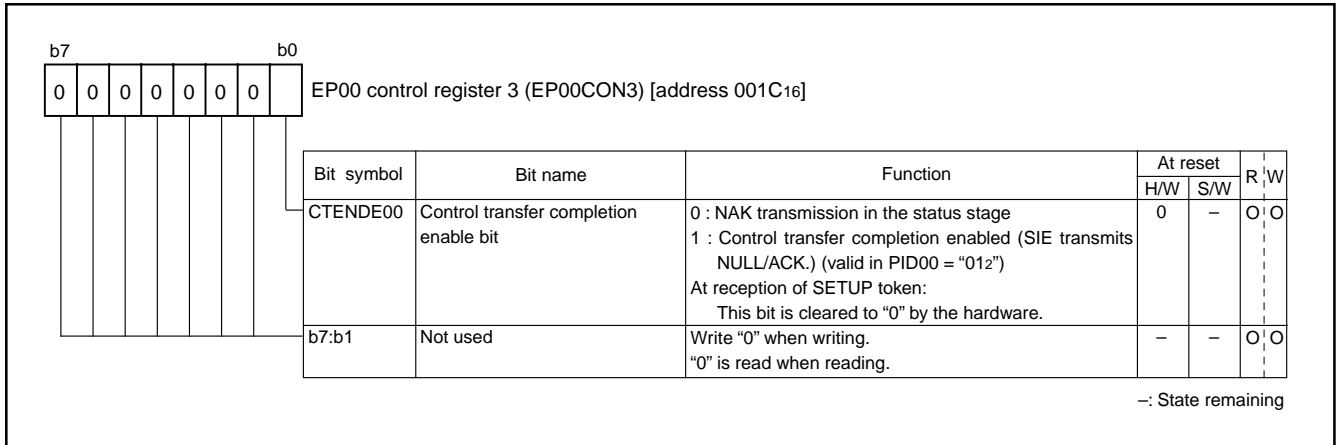


Fig. 42 Structure of EP0 control register 3

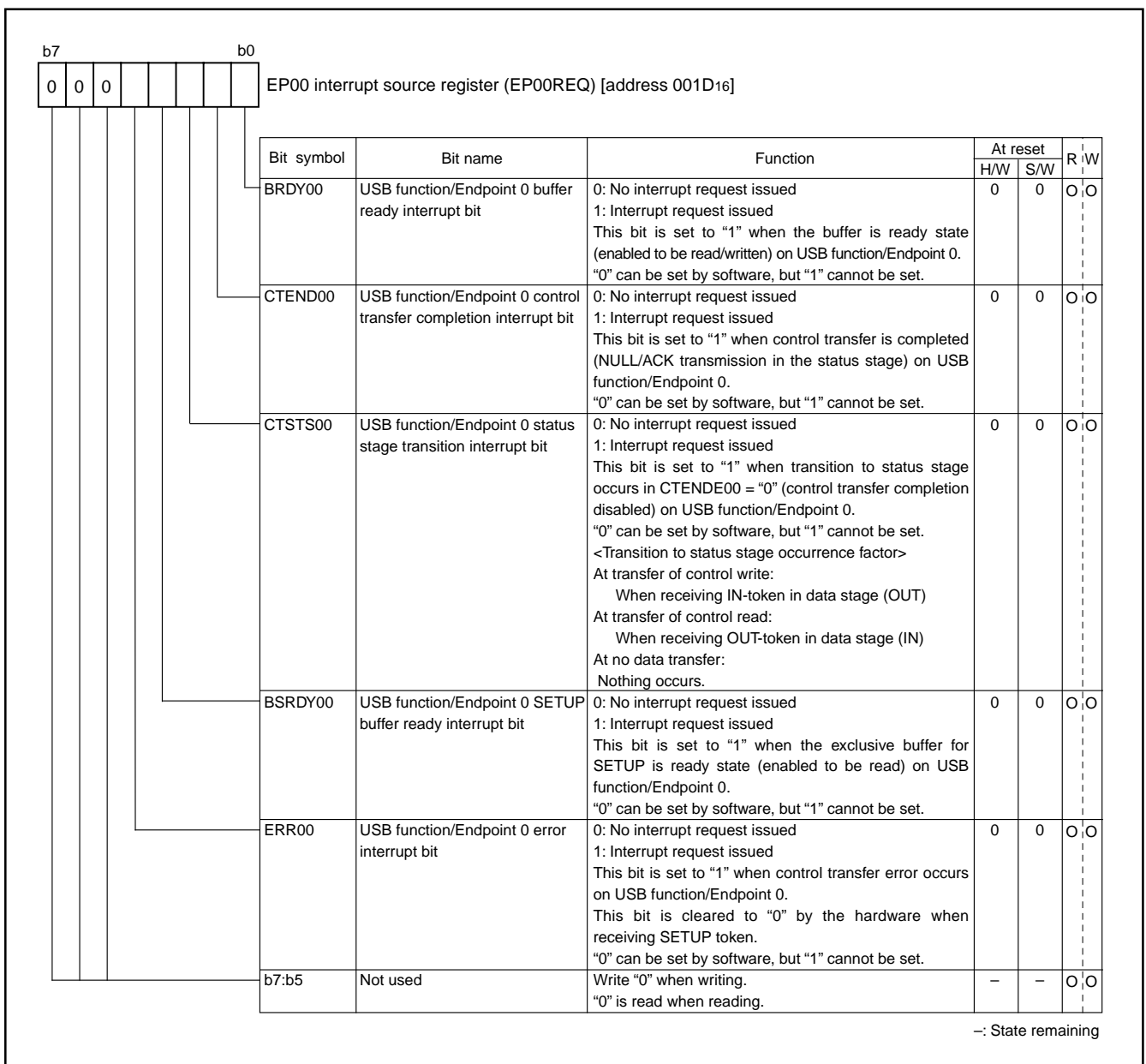


Fig. 43 Structure of EP0 interrupt source register

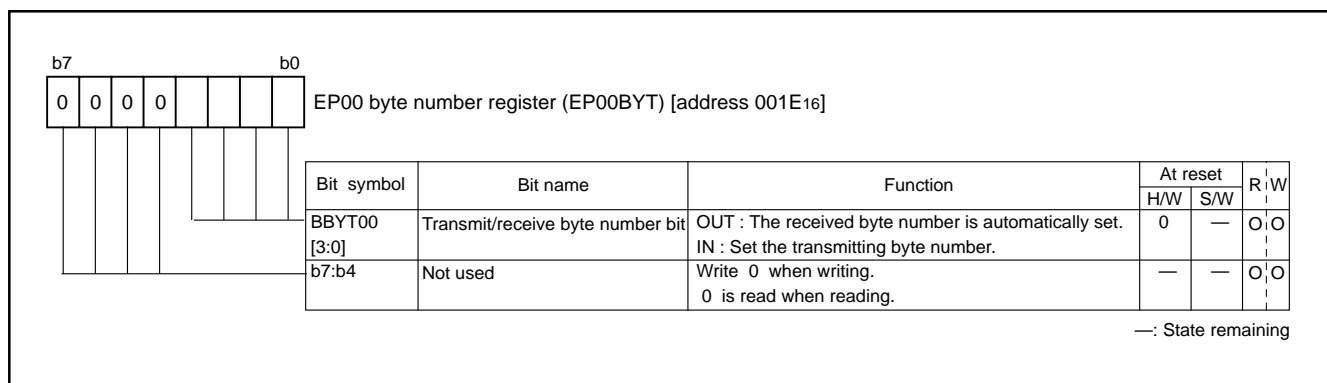


Fig. 44 Structure of EP00 byte number register

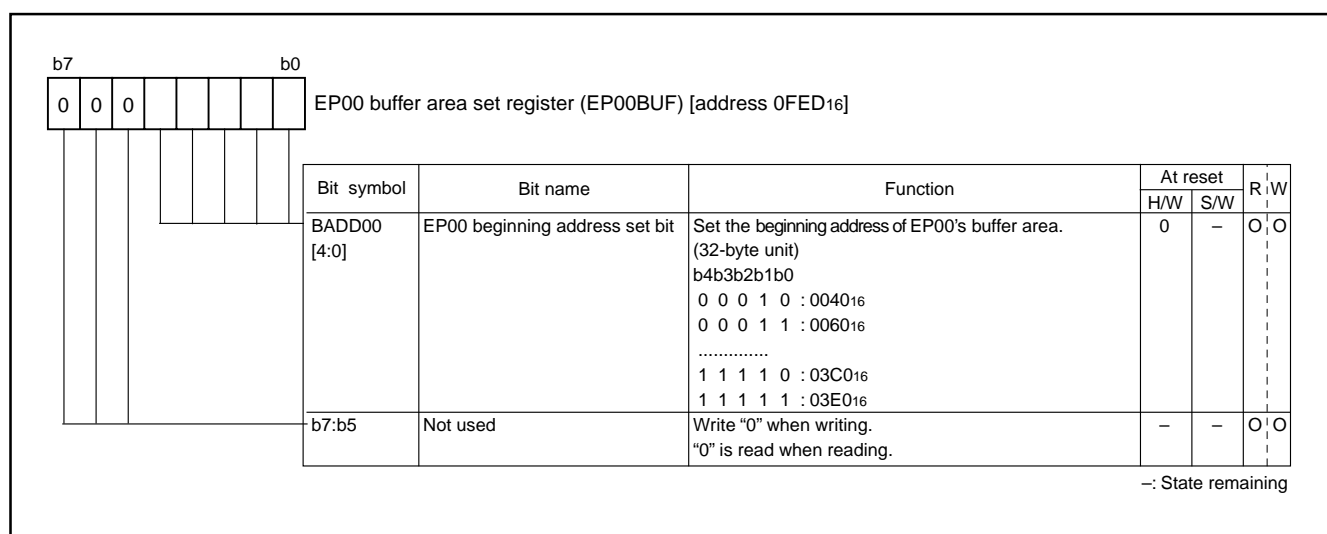


Fig. 45 Structure of EP00 buffer area set register

HARDWARE

FUNCTIONAL DESCRIPTION

(2) Endpoint 01

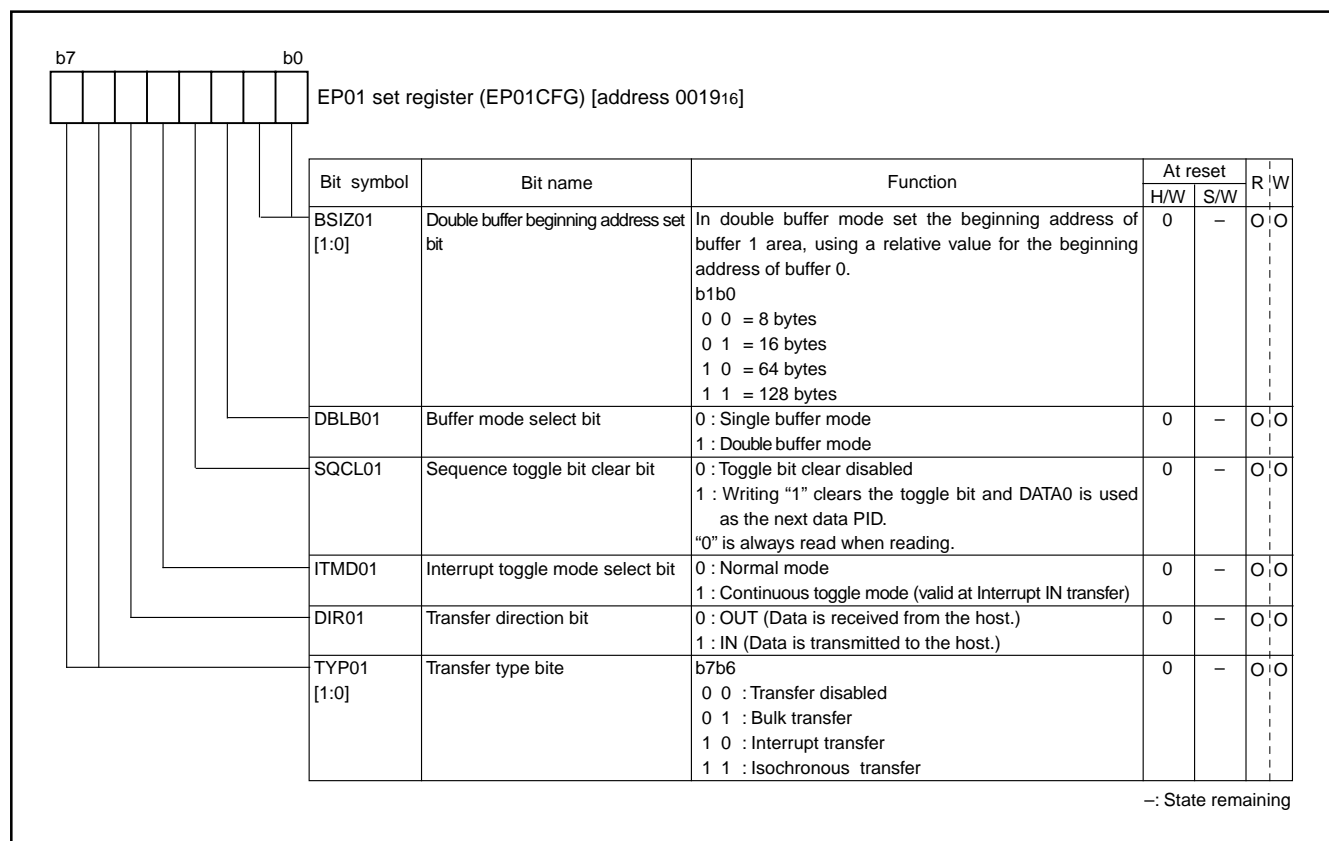


Fig. 46 Structure of EP01 set register

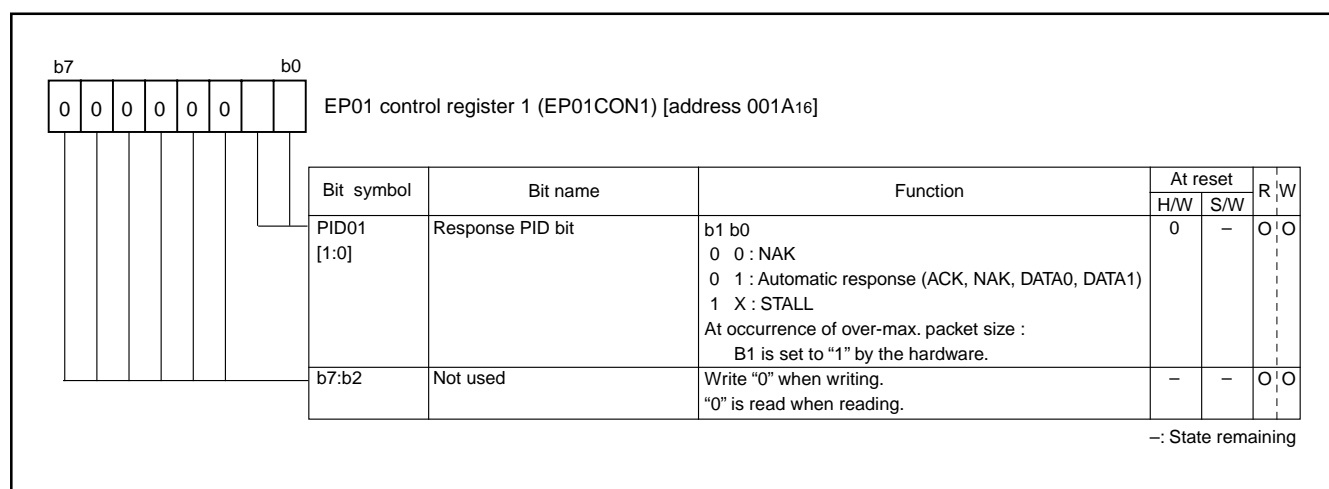


Fig. 47 Structure of EP01 control register 1

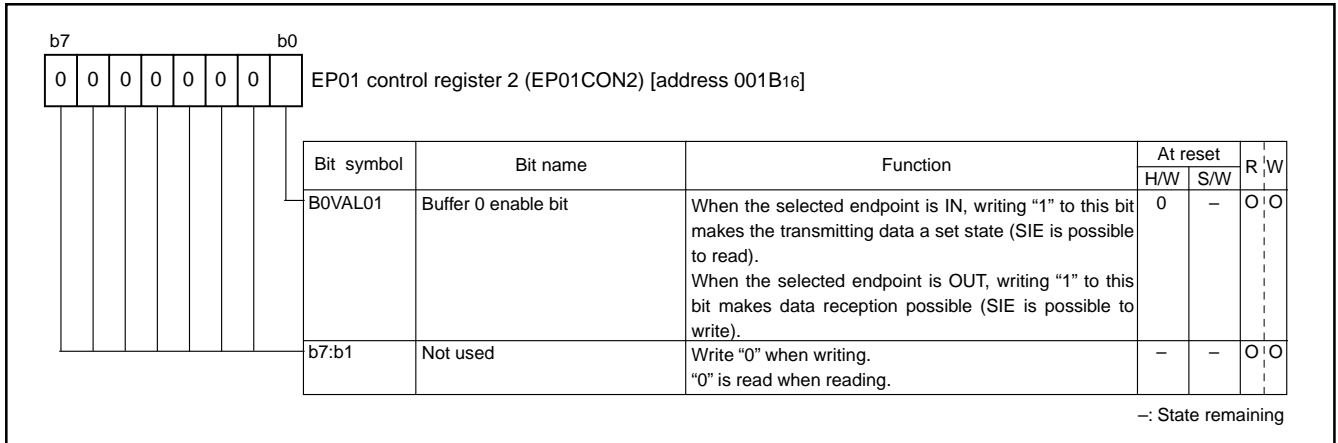


Fig. 48 Structure of EP01 control register 2

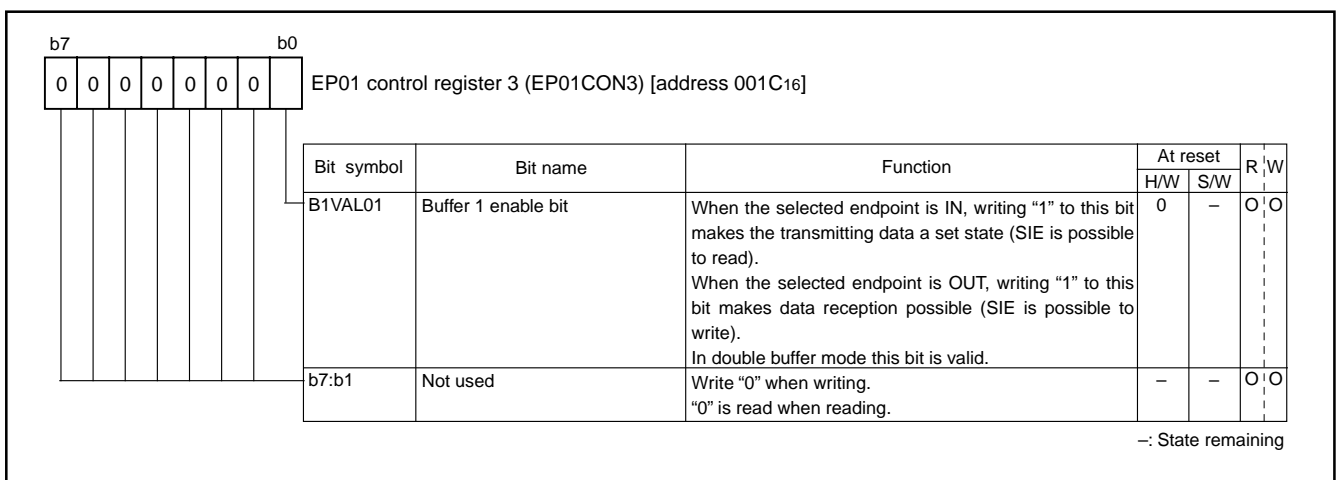


Fig. 49 Structure of EP01 control register 3

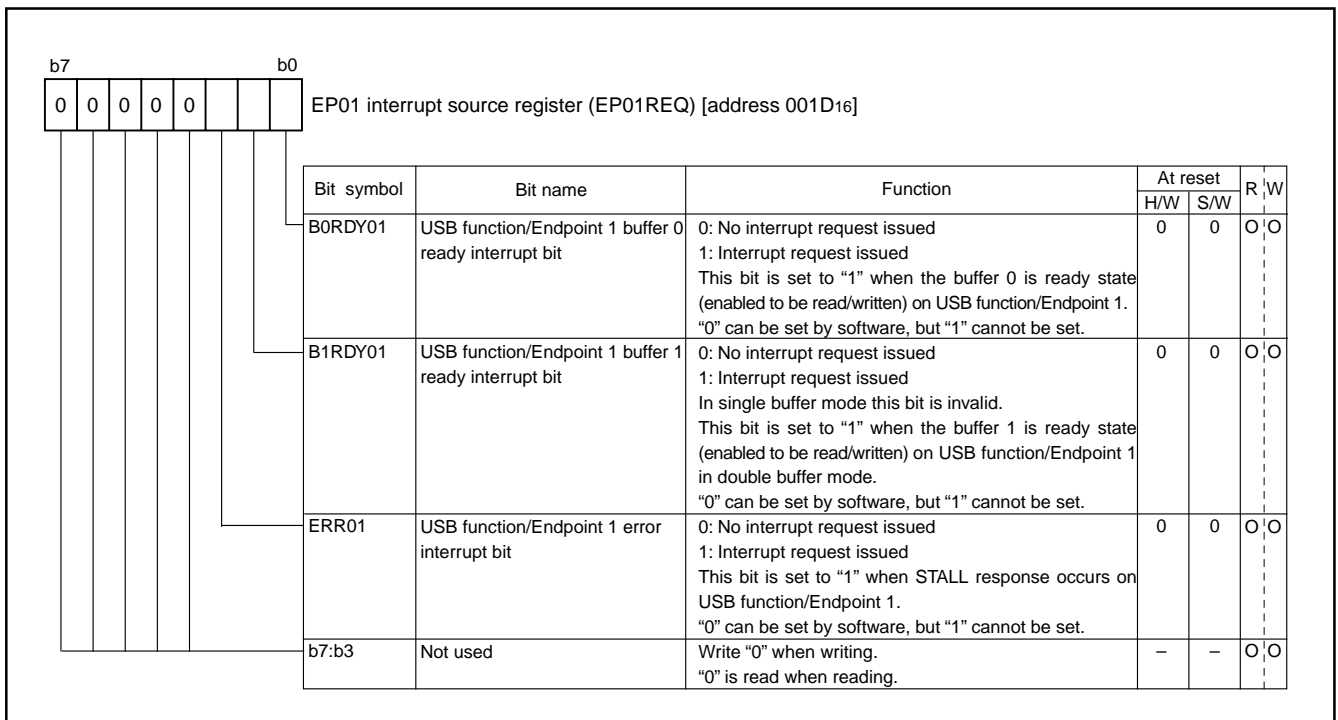


Fig. 50 Structure of EP01 interrupt source register

HARDWARE

FUNCTIONAL DESCRIPTION

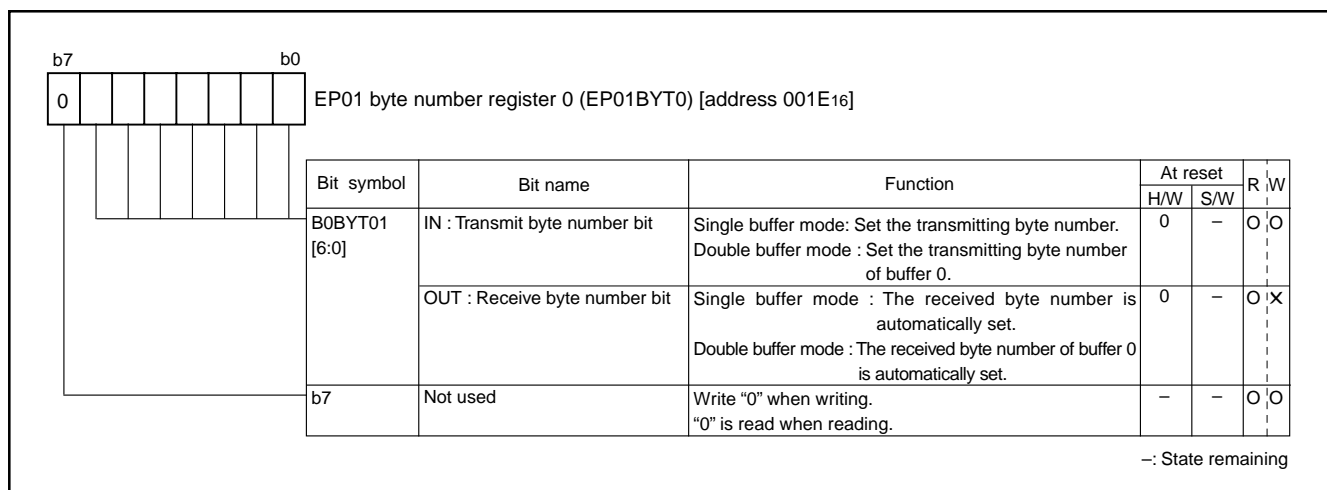


Fig. 51 Structure of EP01 byte number register 0

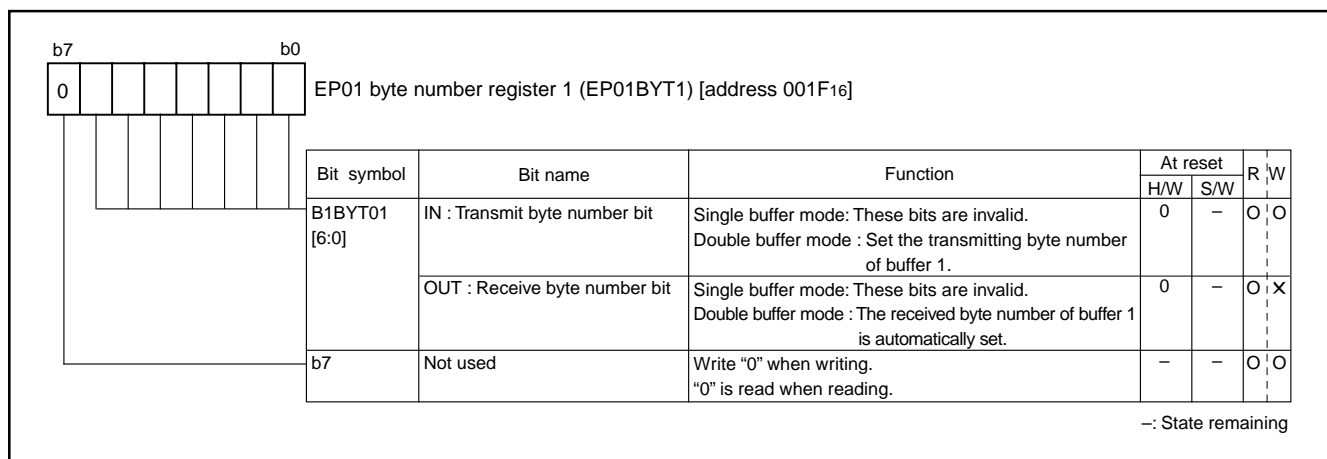


Fig. 52 Structure of EP01 byte number register 1

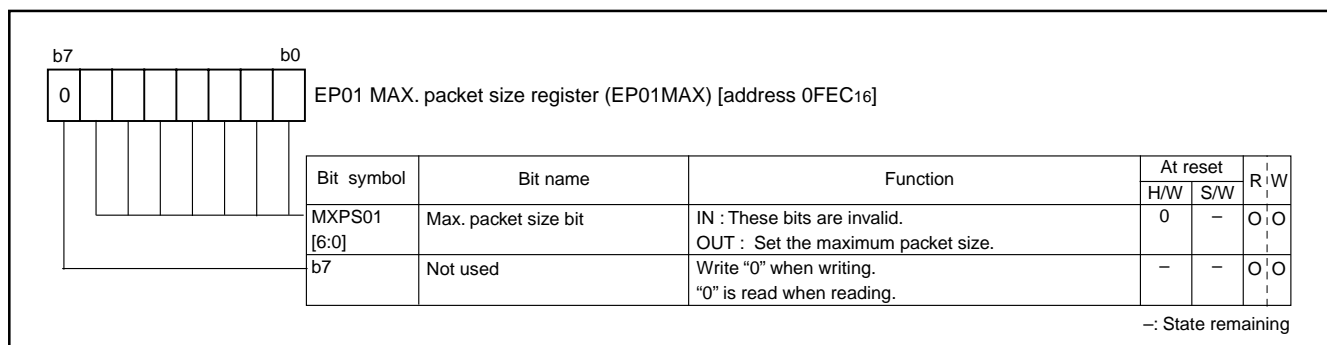


Fig. 53 Structure of EP01 MAX. packet size register



HARDWARE

FUNCTIONAL DESCRIPTION

(3) Endpoint 02

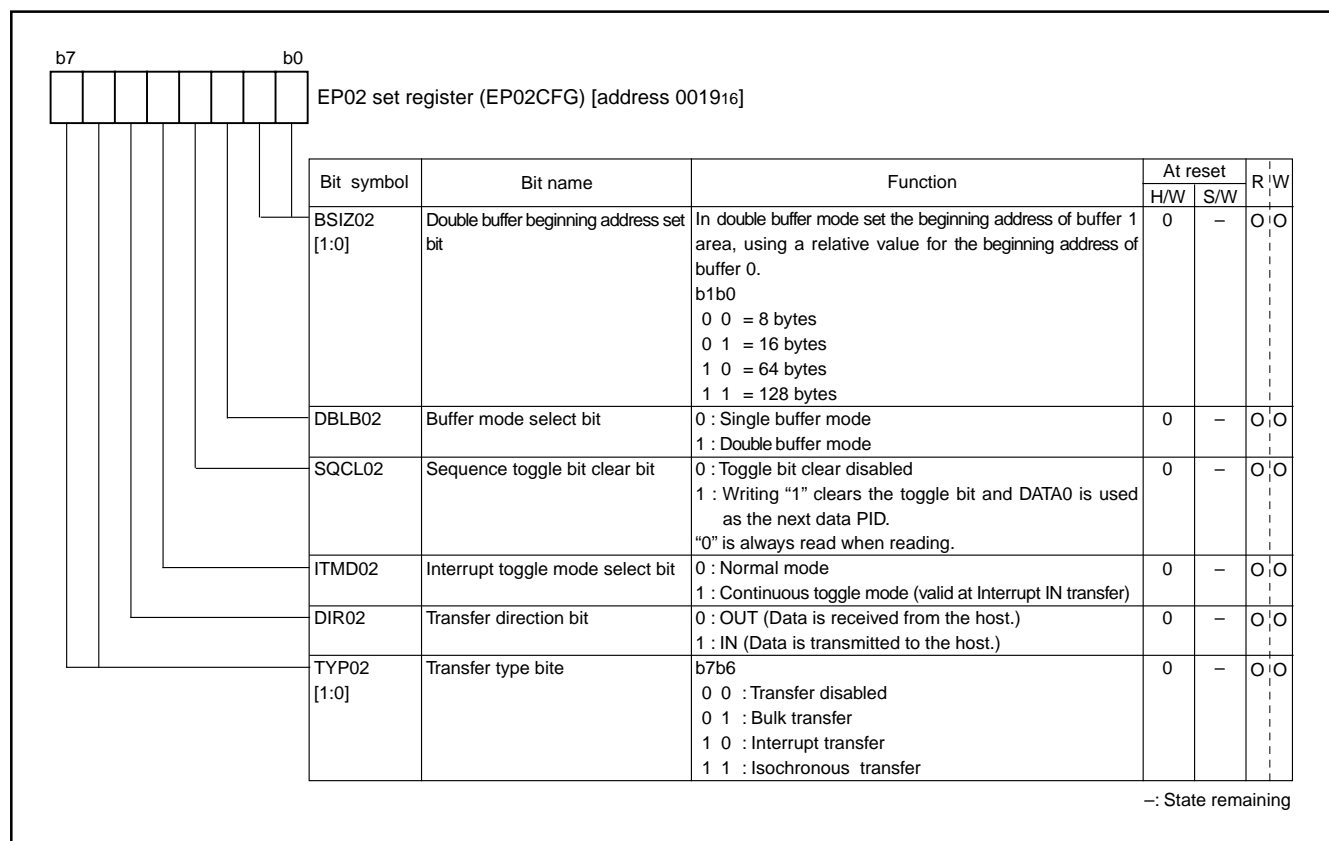


Fig. 55 Structure of EP02 set register

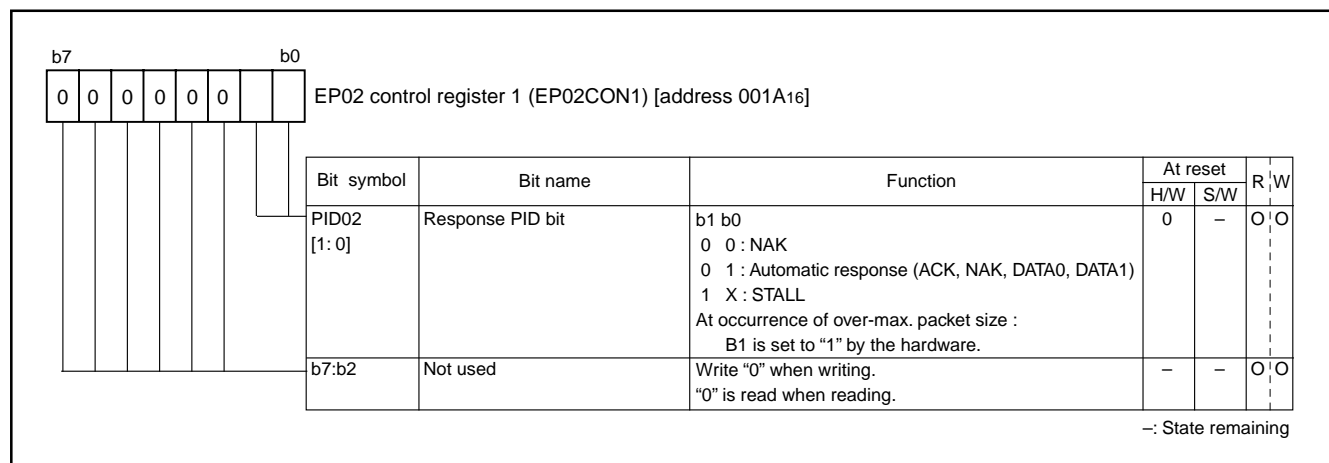


Fig. 56 Structure of EP02 control register 1

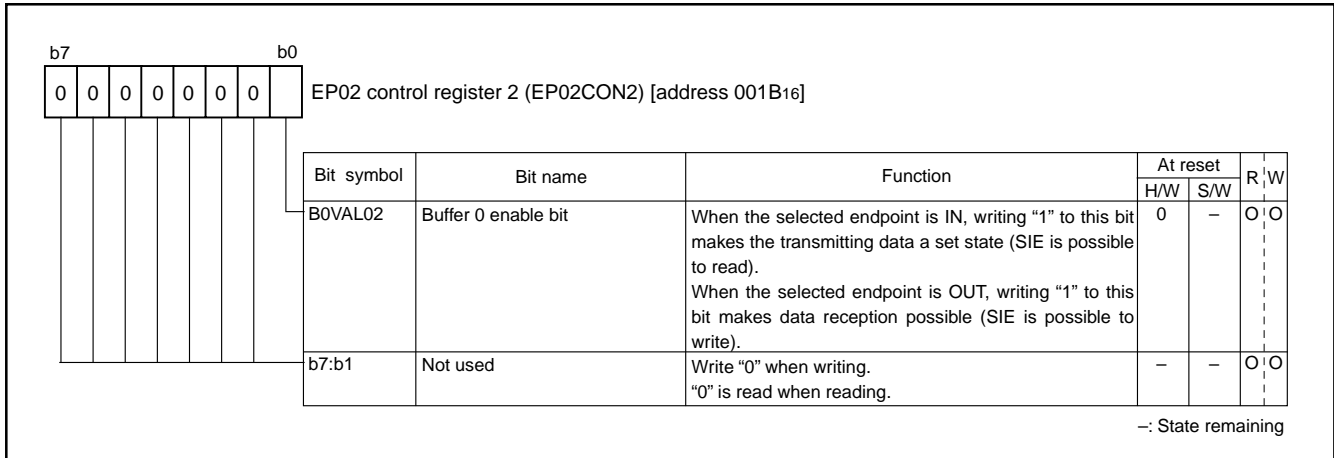


Fig. 57 Structure of EP02 control register 2

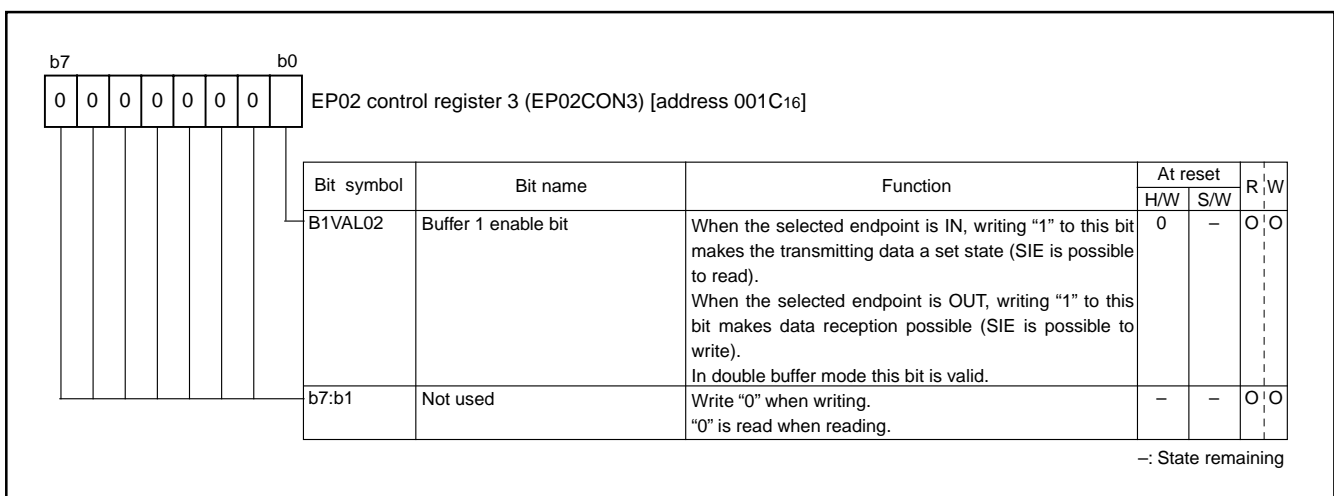


Fig. 58 Structure of EP02 control register 3

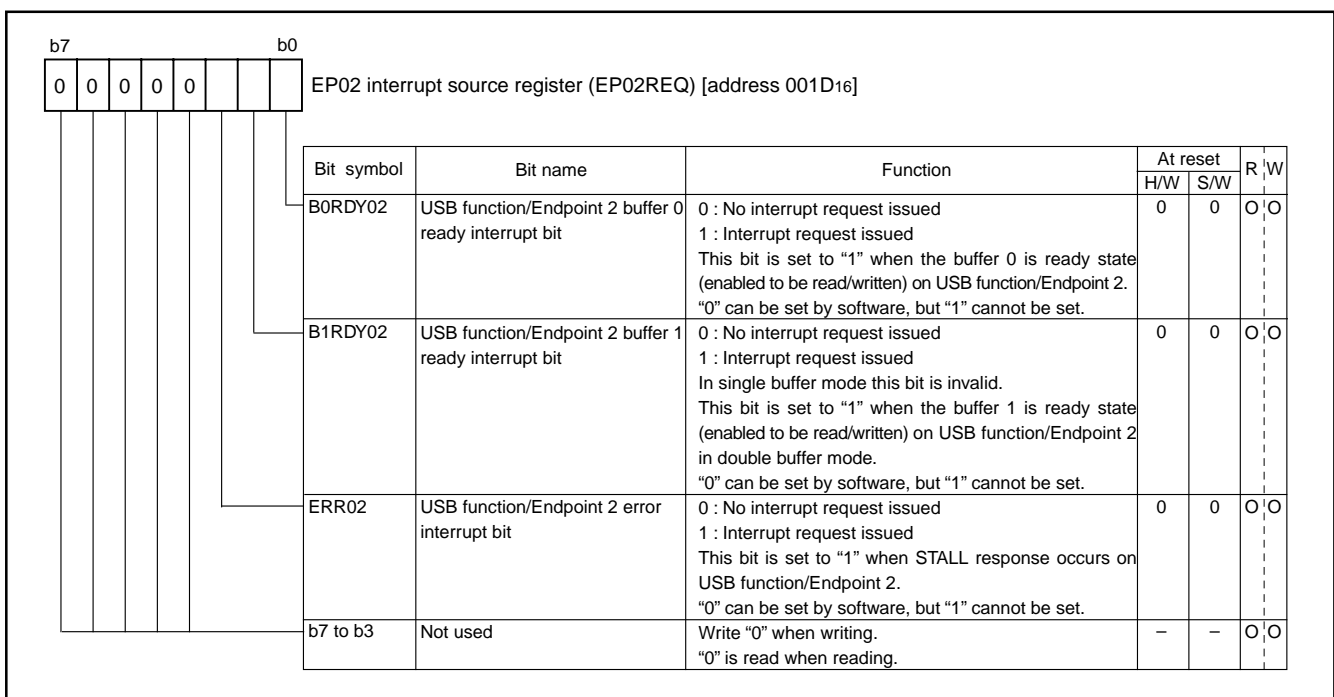


Fig. 59 Structure of EP02 interrupt source register

HARDWARE

FUNCTIONAL DESCRIPTION

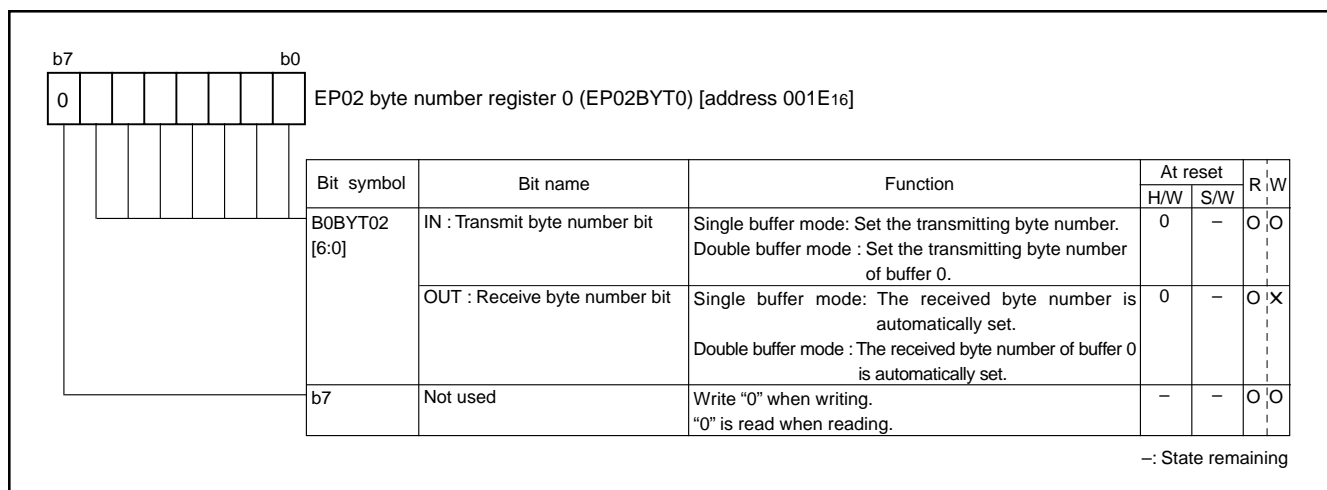


Fig. 60 Structure of EP02 byte number register 0

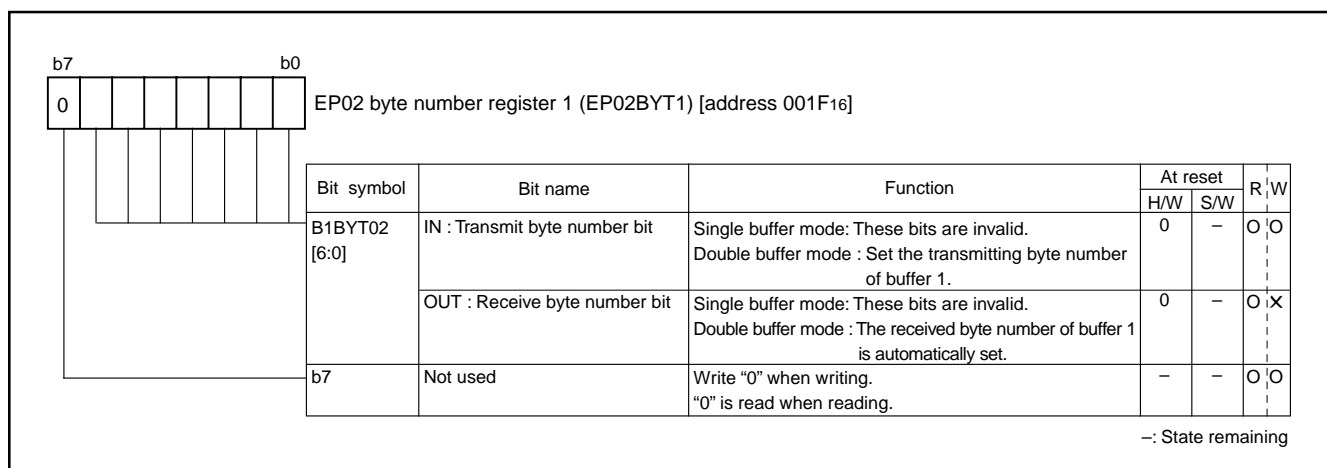


Fig. 61 Structure of EP02 byte number register 1

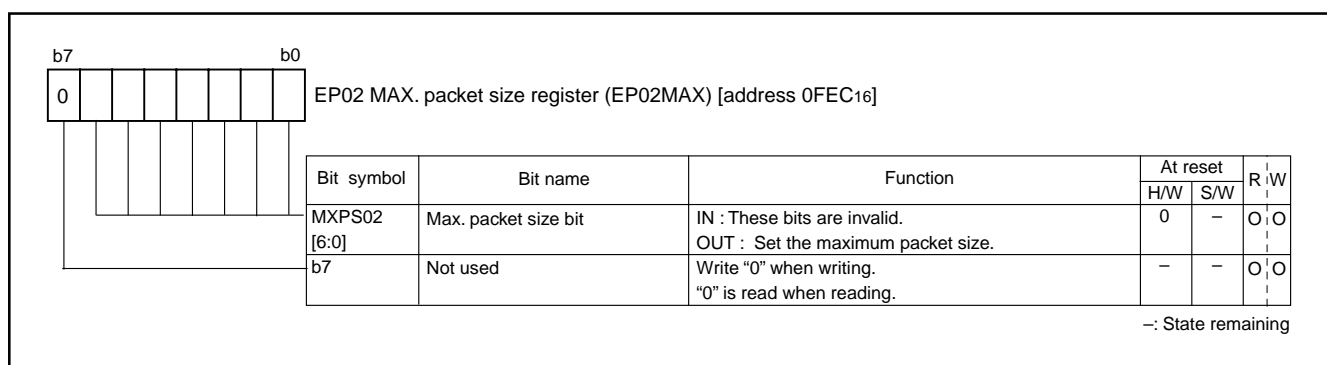
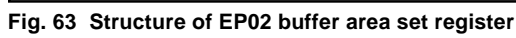


Fig. 62 Structure of EP02 MAX. packet size register



HARDWARE

FUNCTIONAL DESCRIPTION

(4) Endpoint 03

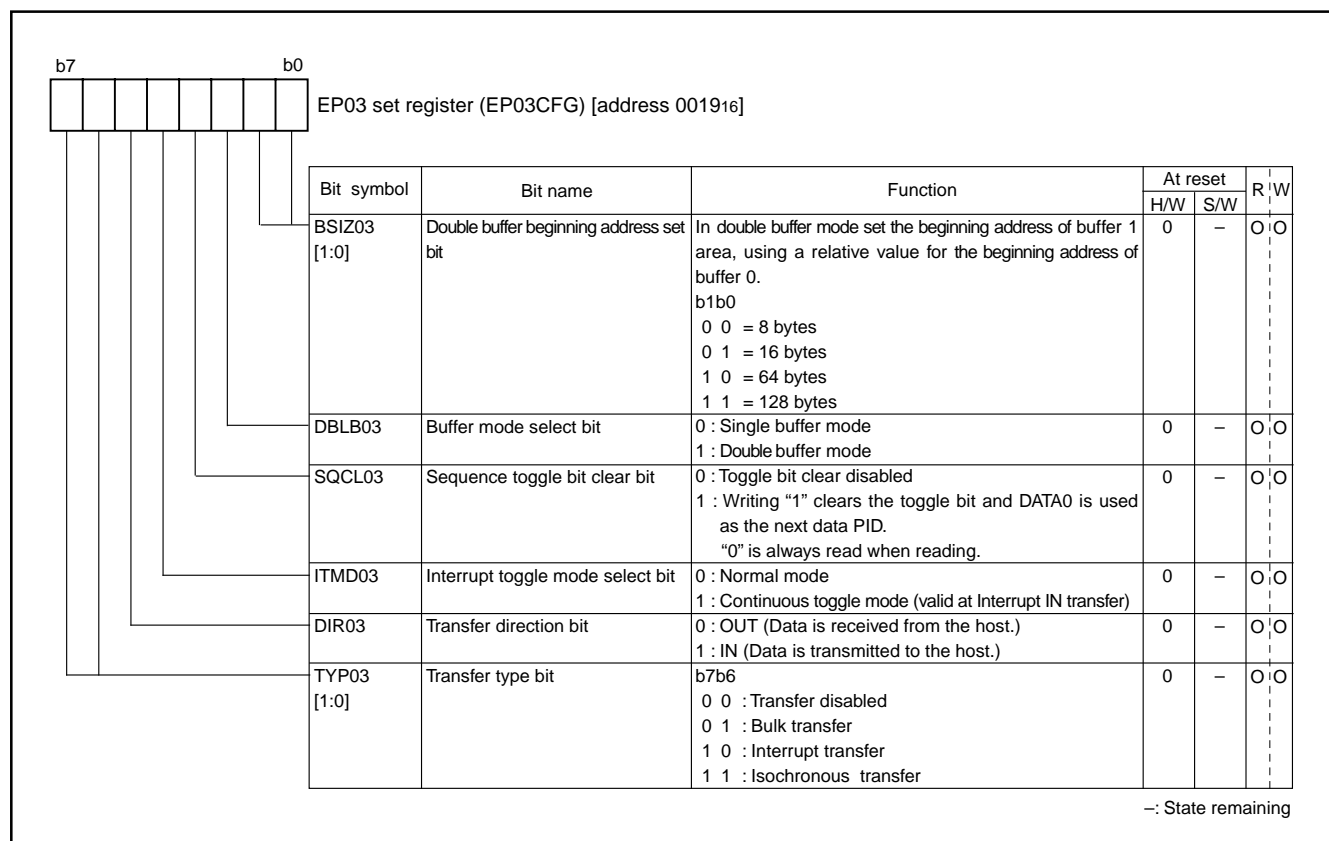


Fig. 64 Structure of EP03 set register

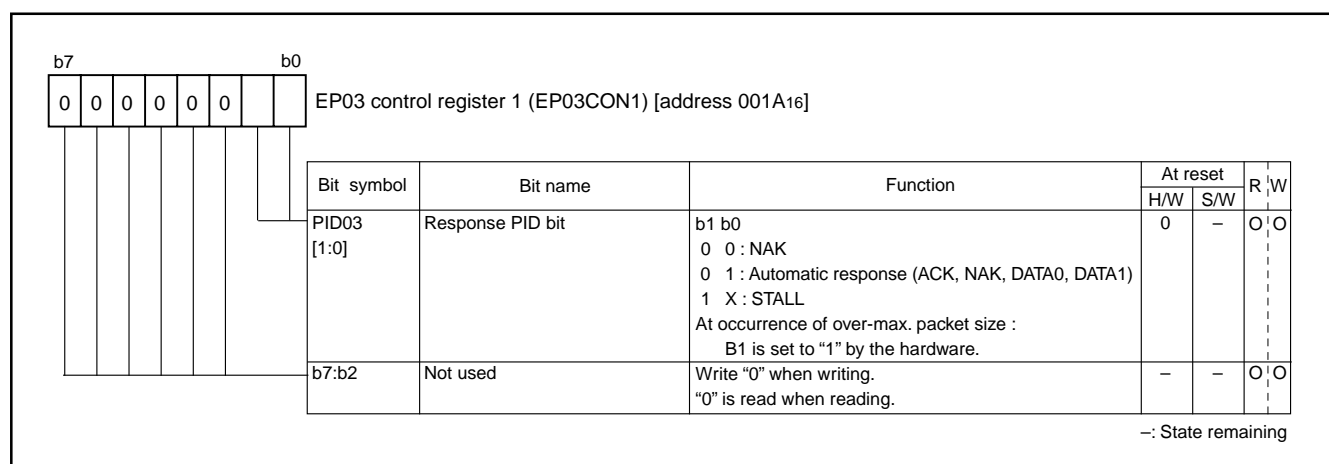


Fig. 65 Structure of EP03 control register 1

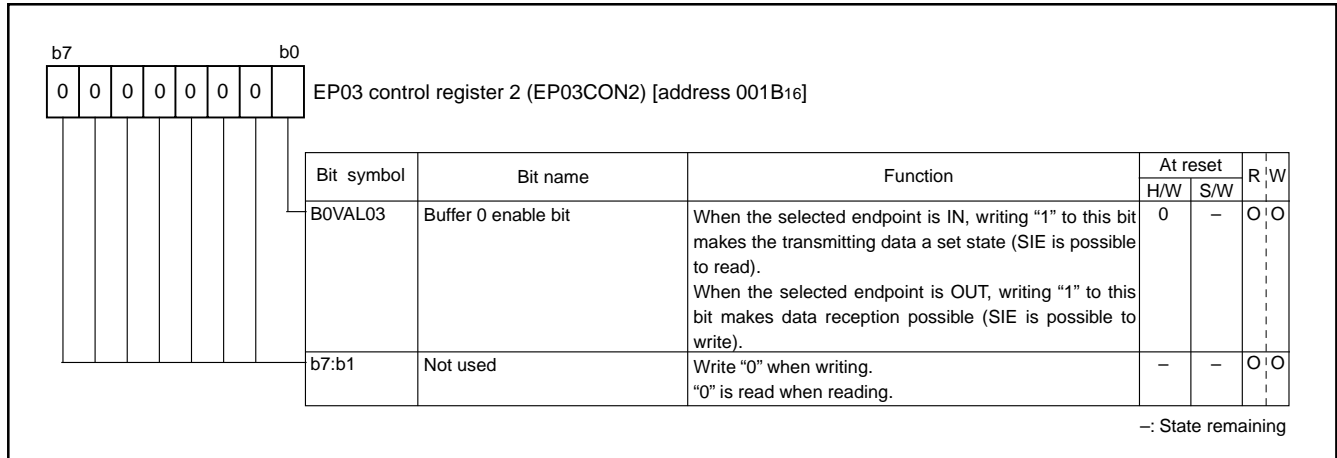


Fig. 66 Structure of EP03 control register 2

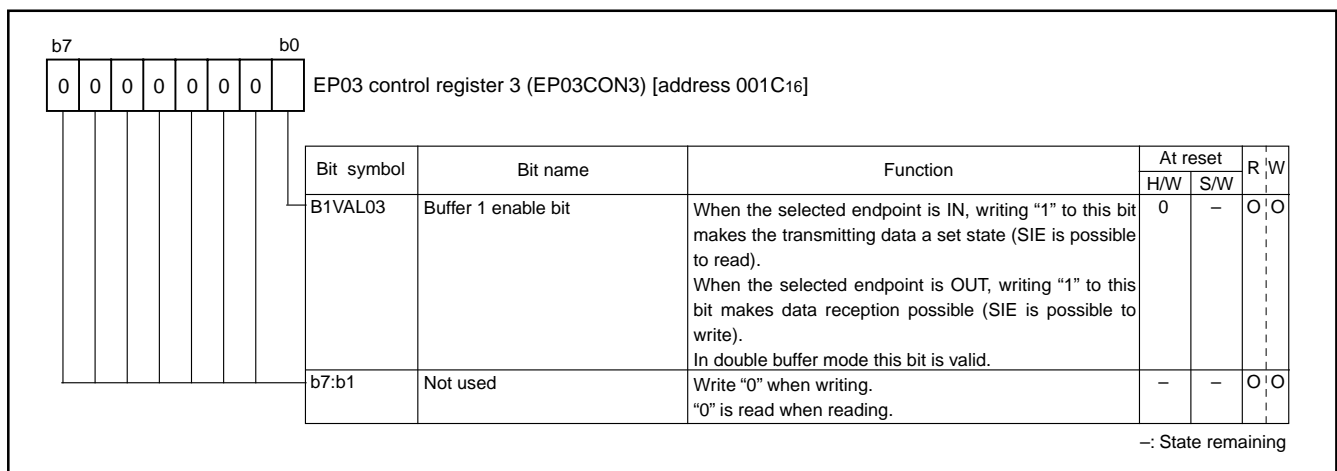


Fig. 67 Structure of EP03 control register 3

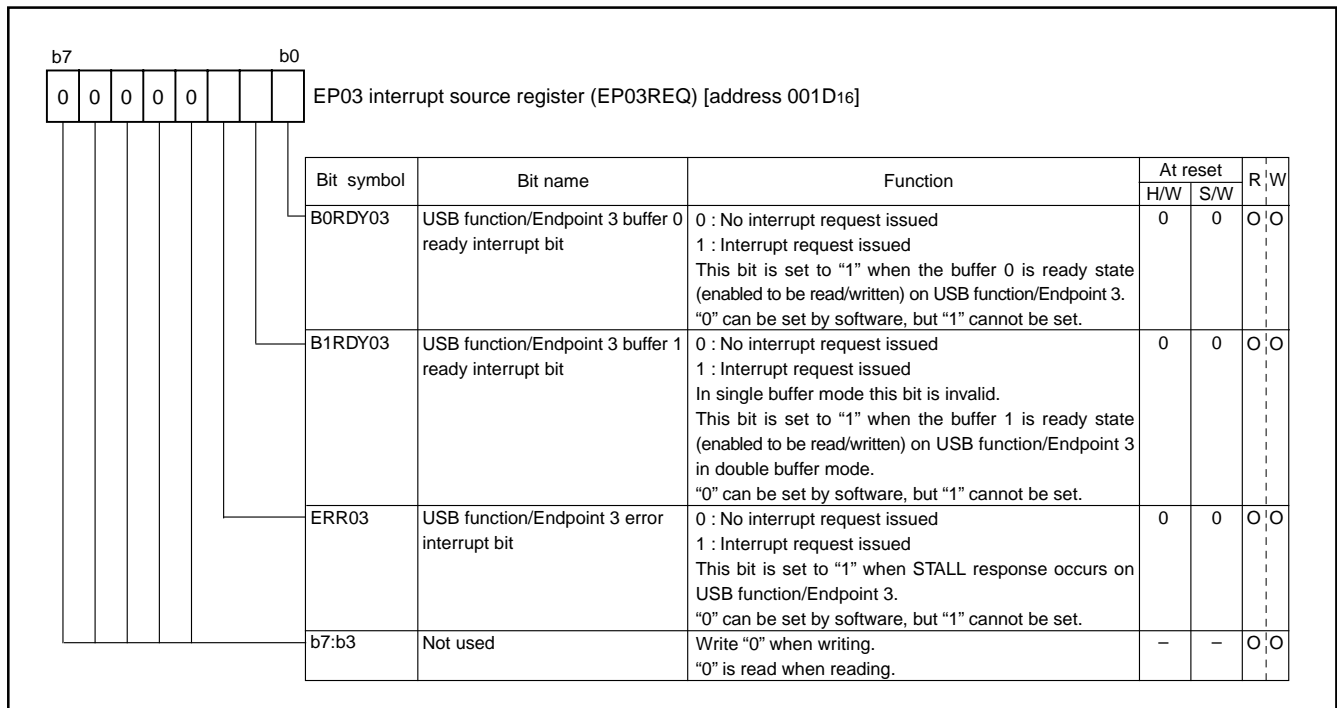


Fig. 68 Structure of EP03 interrupt source register

HARDWARE

FUNCTIONAL DESCRIPTION

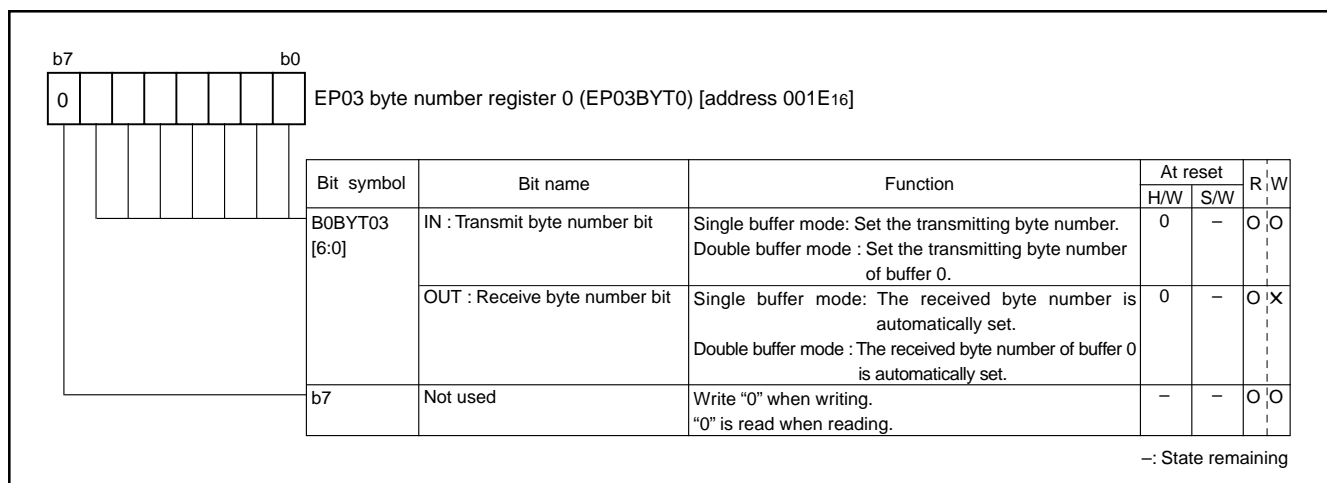


Fig. 69 Structure of EP03 byte number register 0

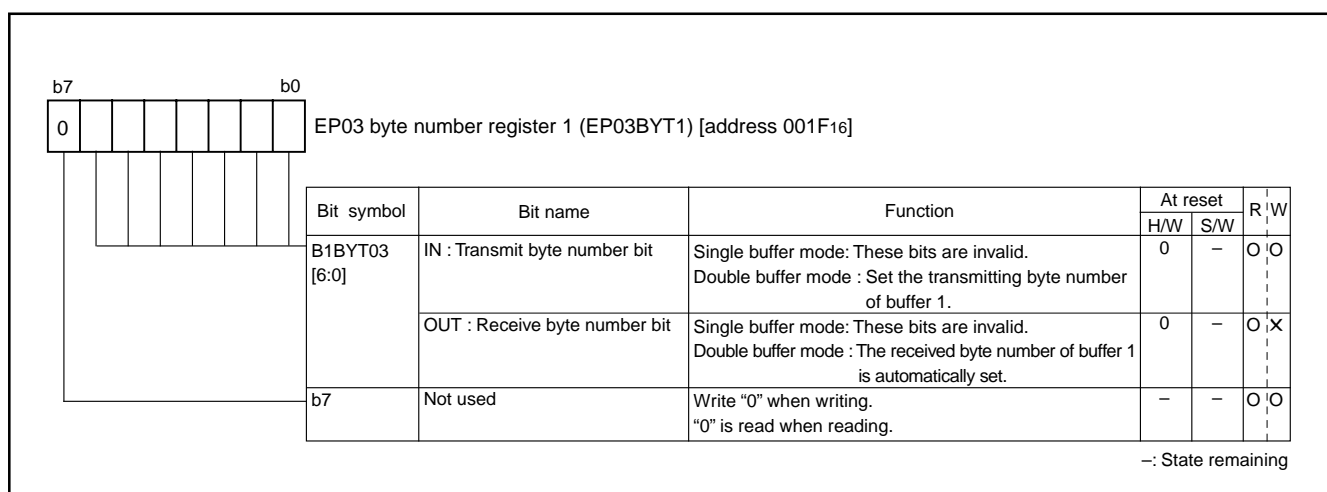


Fig. 70 Structure of EP03 byte number register 1

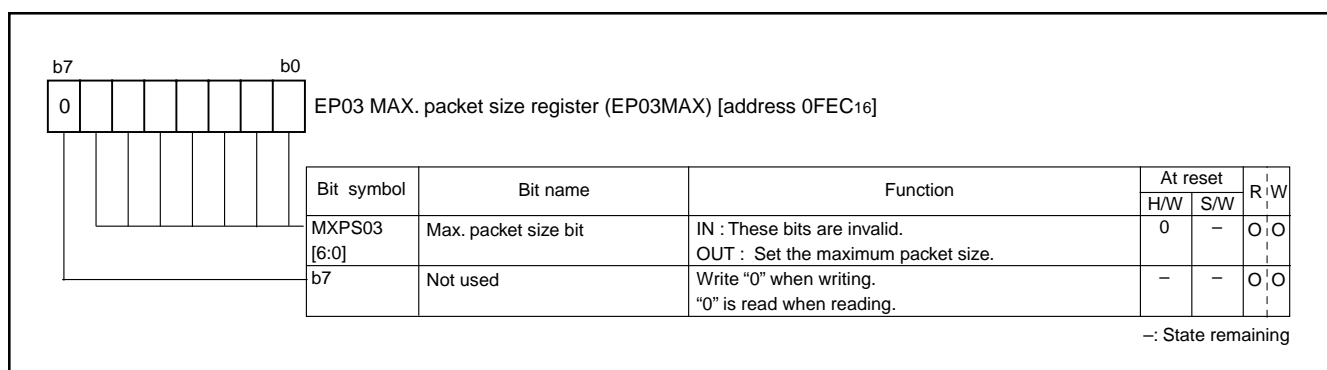
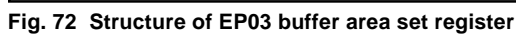


Fig. 71 Structure of EP03 MAX. packet size register



HARDWARE

FUNCTIONAL DESCRIPTION

EXTERNAL BUS INTERFACE (EXB)

The external bus interface (EXB) controls the data transfer between the external MCU and the 38K0 group's CPU or its

memory (multichannel RAM). The external bus interface is shown below.

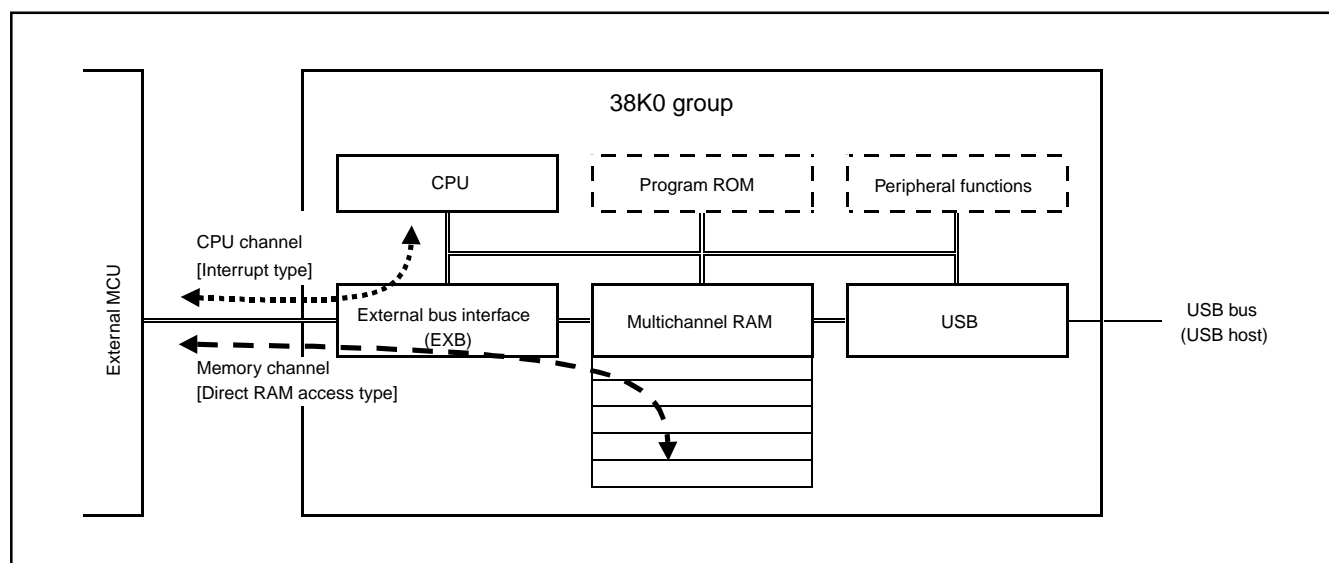


Fig. 73 External bus interface

●CPU channel

It is a data transfer course by the interrupt processing between the external MCU and the 38K0 group's CPU.

●Memory channel

It is a data transfer course by direct RAM access of the memory channel controller between the external MCU and the 38K0 group's memory (multichannel RAM)

●Data transfer of memory channel

When the burst mode is selected with the burst bit of the memory channel operation mode register, data transfer can be carried out at the highest speed. After the external bus interface detects a rise of external read signal/write signal and synchronizes it with the internal clock ϕ , it completes the data transfer between the transmit/receive buffer and the multichannel RAM in two clocks.

However, the waiting time of two clocks at a maximum is generated to access the multichannel RAM in USB being operating because the USB has priority to access.

Therefore, it is necessary to set up the access interval which fills the following timing with the external MCU bus side.

In $\phi = 8$ MHz, data transfer at about 2 Mbytes/second is possible at a maximum. When there is access simultaneously from the USB, it is about 1.3 Mbytes/second.

In $\phi = 6$ MHz, data transfer at about 1.5 Mbytes/second is possible at a maximum. When there is access simultaneously from the USB, it is about 1 Mbytes/second.

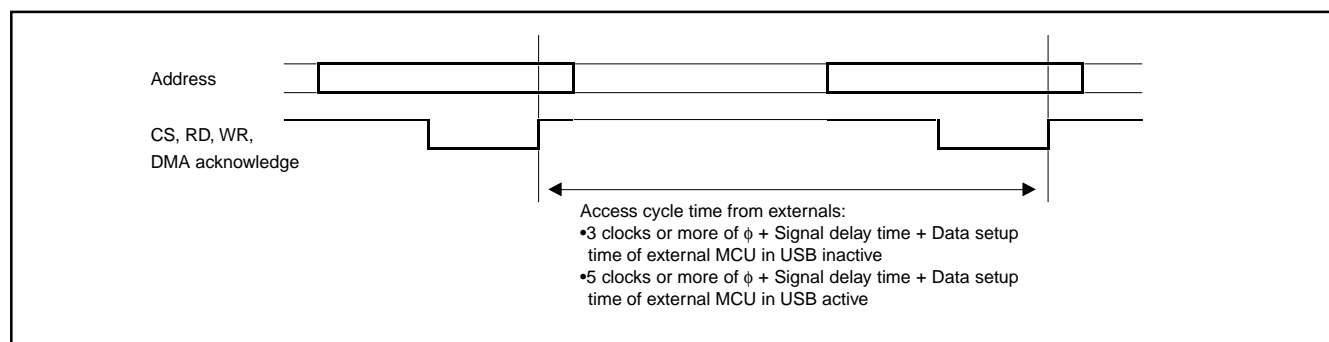


Fig. 74 Data transfer timing of memory channel

EXB Pin Assignment

The external bus interface (EXB) pins are shown bellow.

The 38K0 group can transmit/receive a data to/from an external MCU, using the following signals:

- Control input signal 4 (ExCS, ExA0, ExRD, ExWR)
- Data input/output pin 8 (DQ0 to DQ7)
- Interrupt output signal 1 (ExINT)

Additionally, the DMA interface signal and the buffer status read select signal of 38K0 group can be set up per one by the program.

- Control input signal 3 (ExTC, ExDACK, ExRD, ExA1)
- Interrupt output signal 1 (ExDREQ)

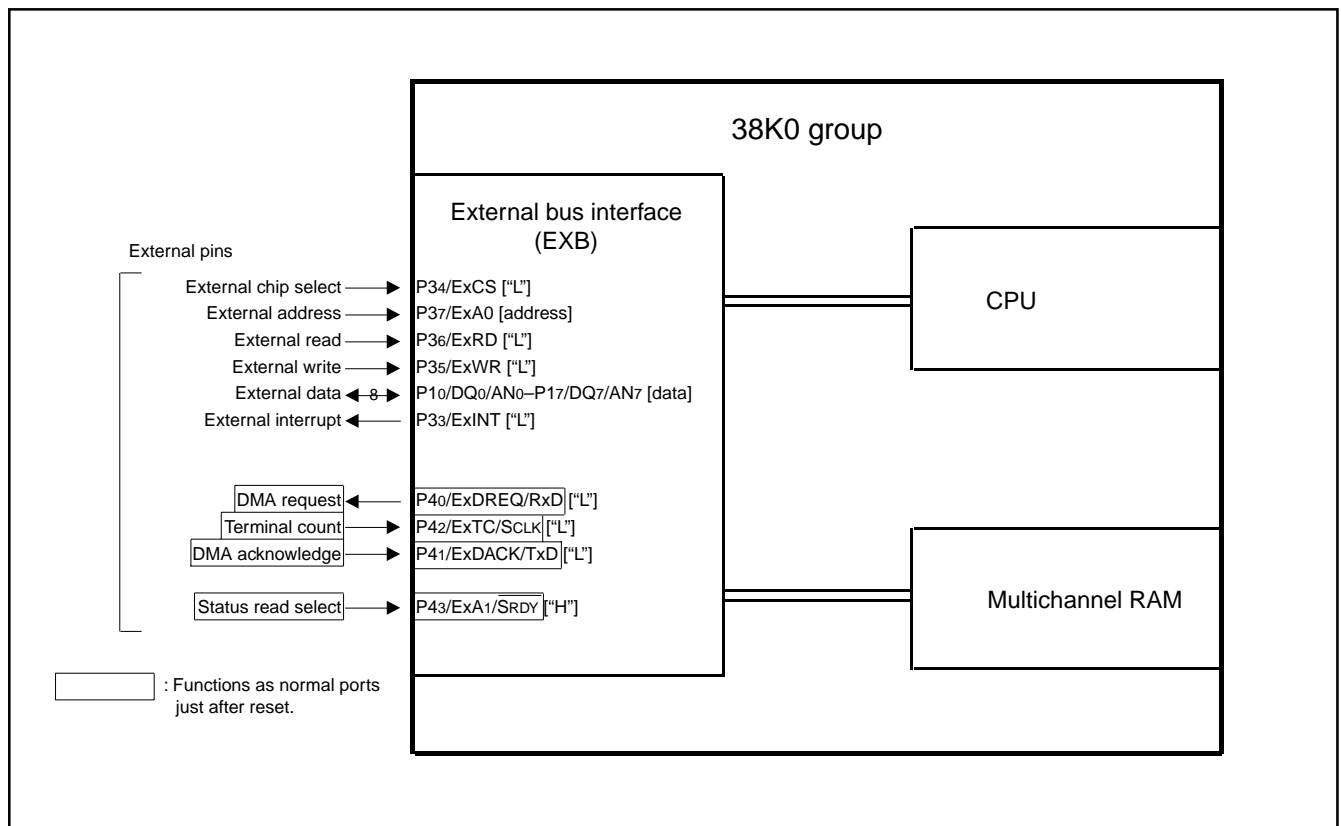


Fig. 75 External bus interface (EXB) pin assignment

HARDWARE

FUNCTIONAL DESCRIPTION

EXB Block Diagram

The block diagram of external bus interface (EXB) is shown below.

The external bus interface (EXB) consists of:

- (1) External I/O interface part
- (2) CPU interface part
- (3) Internal memory interface part
- (4) Transmit/Receive data buffer part

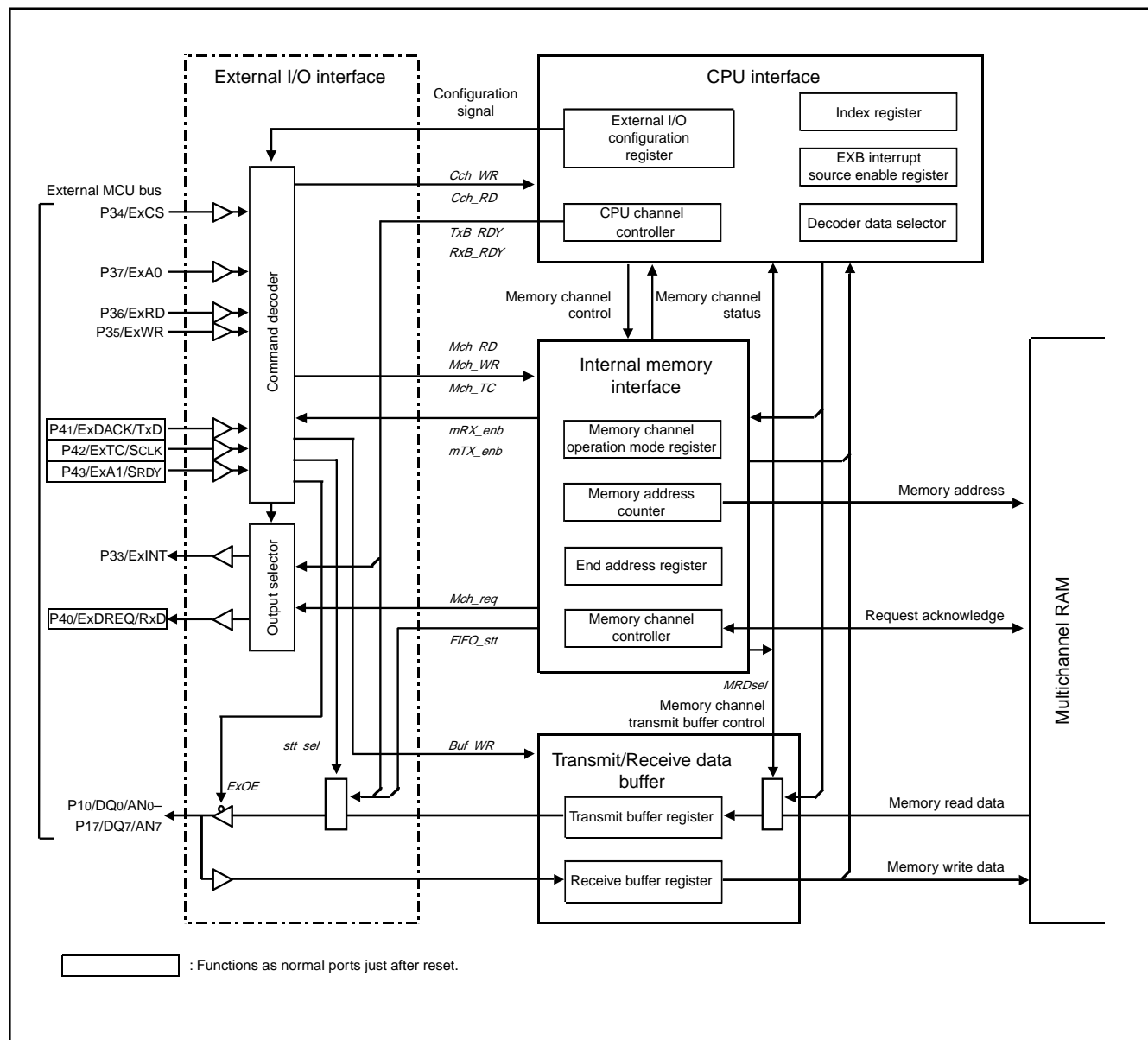


Fig. 76 Block diagram of external bus interface (EXB)

(1) External I/O Interface Part

The external I/O interface part consists of a command decoder and an output selector. A command decoder generates the following signals to each unit.

●CPU interface part

- CPU channel read (Cch_RD)
- CPU channel write (Cch_WR)

●Internal memory interface part

- Memory channel read (Mch_RD)
- Memory channel write (Mch_WR)
- Memory channel terminal count (Mch_TC)

●Transmit/receive data buffer part

- Buffer write (Buf_WR)

●External I/O interface part

- Status selection (stt_sel)
- Output enable (ExOE)

Access to the CPU channel can be controlled only by setup of external signals.

Access to the memory channel can be controlled by the value of the external I/O configuration register and the state (mRX_enb, mTX_enb signals) of the internal memory interface part.

The output selector has the function which selects from the state of CPU channel (TxB_RDY and RxD_RDY) and the state of memory channel (Mch_req) as the signal assigned to P33/ExINT pin and P40/ExDREQ/RxD pin.

(2) CPU Interface Part

The CPU interface part consists of the decoder/data selector of the CPU channel, the CPU write register and CPU channel controller

●Decoder/data selector of CPU channel

A write operation to the CPU register is performed by generating a write signal for each register with an address decode signal and a write signal.

A read operation from the CPU register is performed by generating an output enable signal of the internal data bus with an module select signal and a read signal and generating a select signal for each register with an address decode signal.

●CPU write register

There are three CPU write registers as follows:

- EXB interrupt source enable register
- Index register
- External I/O configuration register

The EXB interrupt source register is a read-only register.

A status signal of the CPU channel controller and a status signal of the memory channel controller in the internal memory interface part are generated.

●CPU channel controller

The CPU channel controller generates the following signals, using bits 0 and 1 (RXB_ENB, TXB_ENB) of EXB interrupt source enable register.

- Memory channel transmitting buffer control signal (MRD_sel), generated in the internal memory interface part
- CPU channel command signal (Cch_RD, Cch_WR), generated in the external I/O interface part
- Signals RxB_RDY/RxB_full and TxB_RDY/TxB_empty, generated with read/write signals from the CPU channel

HARDWARE

FUNCTIONAL DESCRIPTION

(3) Internal Memory Interface Part

The internal memory interface part consists of the CPU register and the memory channel controller.

●CPU register

The CPU register consists of the follows:

- Memory channel operation mode register
- Memory address counter
- End address register

The CPU can set the beginning address into the memory address counter when the memory channel operation enable bit (MC_ENB) of EXB interrupt source enable register is "0". When this bit is "1", the write operation from the CPU is invalid and each access from the external bus causes count-up operation.

●Memory channel controller

The CPU register consists of the follows:

- Main sequencer
- Internal memory request signal generating circuit
- External memory channel request signal generating circuit
- Address end detection circuit
- Terminal end input processing circuit

(4) Transmit/Receive Data Buffer Part

The transmit/receive data buffer part consists of the 8-bit transmit buffer register (TXBUF) and the 8-bit receive buffer register (RXBUF).

Both CPU channel and memory channel use the same transmit buffer register/receive buffer register to transfer a data to an external MCU bus.

(5) External Pin

The external bus interface has the following pins to connect with an external MCU bus.

- Chip select P34/ExCS
- Address P37/ExA0
- Data P10/DQ0/AN0 to P17/DQ7/AN7
- Read P36/ExRD
- Write P35/ExWR
- Interrupt request P33/ExINT

It also has the following pins to connect with an external DMAC. Each pin can be programmed for an ordinary port function or a DMA interface pin function.

- DMA request P40/ExDREQ/RxD
- DMA acknowledgment P41/ExDACK/TxD
- Terminal count P42/ExTC/SCLK

It also has the status read select pin (P43/ExA1/ $\overline{\text{SRDY}}$ pin) to confirm a ready status of the data buffer from an external MCU bus. This pin functions as a port just after reset. The status read select function can be set by a program.

- Status read select P43/ExA1/ $\overline{\text{SRDY}}$

●CPU channel: Communication with 38K0 group CPU

When a read/write operation is performed from an external MCU bus in address signal ExA0 = "H", the interrupt is generated and the 38K0 group CPU can confirm its access. The 38K0 group CPU judges the interrupt source and it starts a data transmission/reception with an external MCU bus.

●Memory channel: Communication with 38K0 group memory multichannel RAM

When a read/write operation is performed from an external MCU bus in address signal ExA0 = "L", access to the multichannel RAM is performed. Then an address of the multichannel RAM is made by the external bus interface and it is increased at each access completion. Consequently, FIFO access is performed.

Even if a read/write operation is performed in DACK = "L" instead of ExCS = "L" and ExA0 = "L", FIFO access to the multichannel RAM is performed.

The beginning address and the end address must be set by the CPU in advance.

●P33/ExINT pin

Any one of the following signals for this pin can be selected:

- TxB_RDY (transmit buffer ready) output
- RxB_RDY (receive buffer ready) output
- Mch_req (memory channel request) output

Either TxB_RDY or RxB_RDY is normally selected. The memory channel request is for an access request signal to the memory channel.

In a small system, a data transfer processing to the internal memory is performed in the interrupt routine. According to that situation, the 38K0 group has the function automatically to switch an interrupt factor attached on the interrupt pin by program.

●P40/ExDREQ/RxD pin

This pin is a port at the initial state. Which signal can be set by program.

- RxB_RDY (receive buffer ready) output
- Mch_req (memory channel request) output

Mch_req of DMAC is normally selected. The output method of the memory channel request signal depends on the burst bit (BURST) of memory channel operation mode register. When the burst bit is "0", this signal is periodically output at each 1-byte transfer. (See Figures 94 and 97.)

When the burst bit is "1", this signal is continuously output while the memory address counter is counting from the beginning address to the end address (See Figures 95 and 98.)

●P41/ExDACK/TxD pin

This pin is a port at the initial state. The DMA acknowledge signal can be set by program.

The DMA acknowledge signal DACK = "L" is the same state as that of CS = "L" and A0 = "L". Access to multichannel RAM is started by a rise of read signal or write signal which is set during this term.

Note: If the DMA acknowledge signal and the chip select signal are simultaneously active (DACK = "L" and CS = "L"), also set the address signal A0 to "L". If A0 is "H", the memory channel and the CPU channel are activated simultaneously and it might cause some error.

●P42/ExTC/SCLK pin

This pin is a port at the initial state. The terminal count signal can be set by program.

If the terminal count signal is set at one bus cycle while a memory channel operation write is being performed, the 38K0 group confirms that its bus cycle is the write cycle of the last data and sets the memory channel status bits to "112", and the interrupt is generated and the memory channel operation ends even if the memory address counter has not reached the end address.

The CPU can obtain the last address where the data is written by reading out the value of memory address counter. (See Figure 96.)

HARDWARE

FUNCTIONAL DESCRIPTION

EXB Register List

The EXB register list is shown below.

Address	Register Name	SYMBOL	EXB SFR							
			bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0030 ₁₆	EXB interrupt source enable register	EXBICON						MC_ENB	TXB_ENB	RXB_ENB
0031 ₁₆	EXB interrupt source register	EXBIREQ						MC_STS[1:0]	TXB_EMPTY	RXB_FULL
0033 ₁₆	EXB index register	EXBINDEX	0	0	0	0	0	INDEX[2:0]		
0034 ₁₆	Register window 1 (low)	EXBREG1	LOW_WIN[7:0]							
0035 ₁₆	Register window 2 (high)	EXBREG2	HIGH_WIN[7:0]							

: Not used

0 : "0" fixed

Fig. 77 EXB related registers (1)

•EXB interrupt source enable register

This register enables/disables access from an external bus and an internal interrupt.

•EXB interrupt source register

This register indicates the state of CPU channel's transmit/receive buffer register and the memory channel. The same value can be read out from the external MCU bus by using the buffer status read select signal (A1 pin = "H").

•EXB index register/Register windows 1, 2

The accessible register is switched by treating addresses 0034₁₆ and 0035₁₆ as a register window depending on the value of EXB index register at address 0033₁₆.

Index	low high	Register Name	SYMBOL	EXB SFR							
				bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0016	low	External I/O configuration register	EXBCFGL				A1_CTR	INT_CTR[2:0]			EXB_CTR
	high		EXBCFGH				TC_CTR	DAK_CTR[1:0]		DRQ_CTR[1:0]	
0116	low	Transmit/Receive buffer register	RXBUF/TXBUF	At CPU read : RXBUF[7:0] At CPU write : TXBUF[7:0]							
	high		—								
0216	low	Memory channel operation mode register	MCHMOD						BURST	MC_DIR[1:0]	
	high		—								
0316	low	Memory address counter	MEMADL	IM_A[7:0]							
	high		MEMADH	0	0	0	0	0	IM_A[10:8]		
0416	low	End address register	ENDADL	END_A[7:0]							
	high		ENDADH	0	0	0	0	0	END_A[10:8]		

: Not used
0 : "0" fixed

Fig. 78 EXB related registers (2)

•External I/O configuration register

This register selects the function of each pin.

•Transmit/Receive buffer register

This register consists of the receive buffer register (RXBUF) and the transmit buffer register (TXBUF)

•Memory channel operation mode register

This register sets the operation mode of the memory channel.

•Memory address counter

This is a counter to set the beginning address which FIFO accesses. This register is increased by access from the external MCU bus.

•End address register

This register is to set the end address which FIFO accesses.

EXB Related Registers

The EXB related registers are shown below.

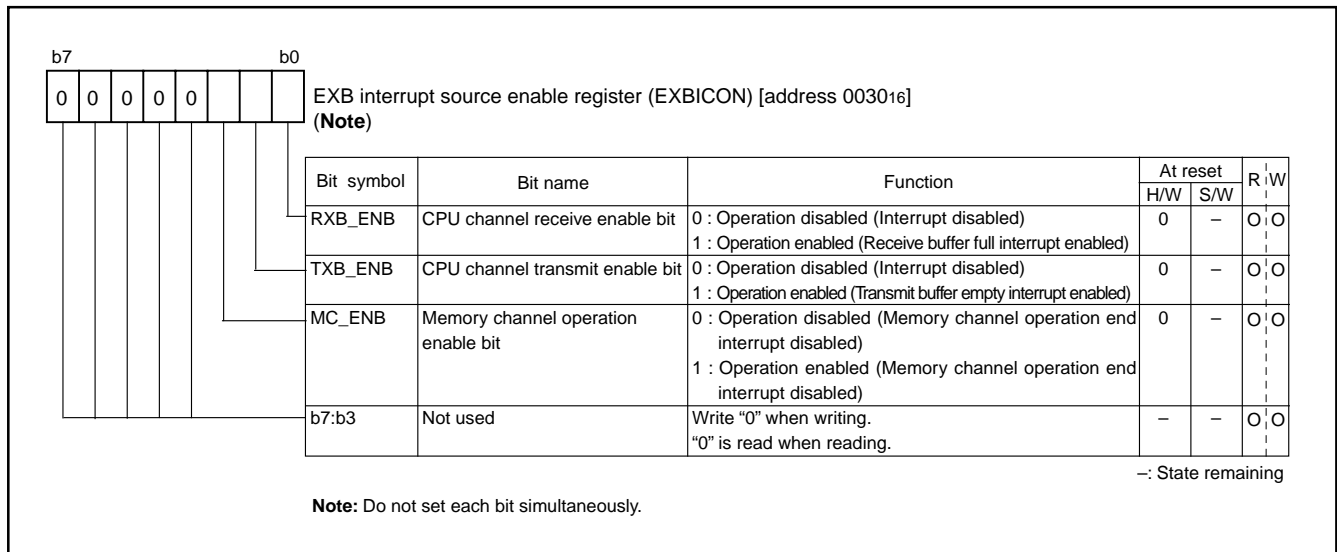


Fig. 79 Structure of EXB interrupt source enable register

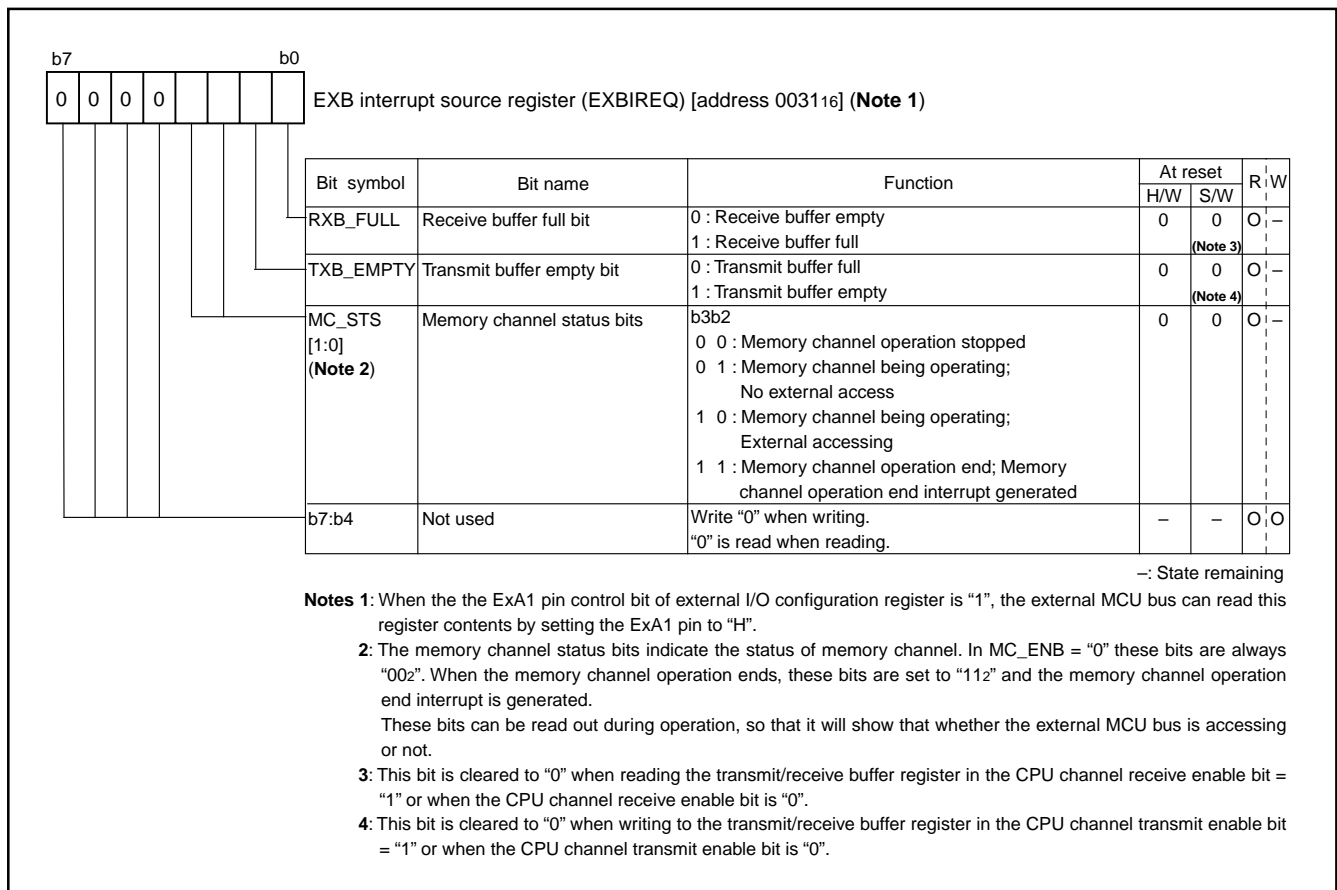


Fig. 80 Structure of EXB interrupt source register

HARDWARE

FUNCTIONAL DESCRIPTION

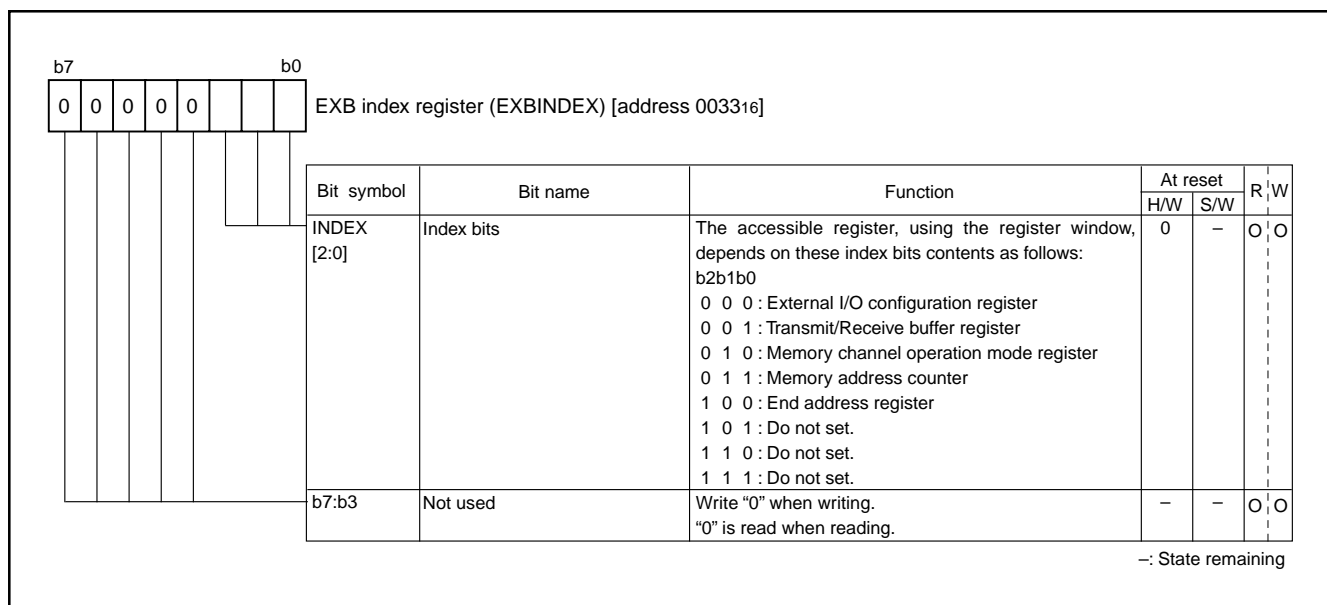


Fig. 81 Structure of EXB index register

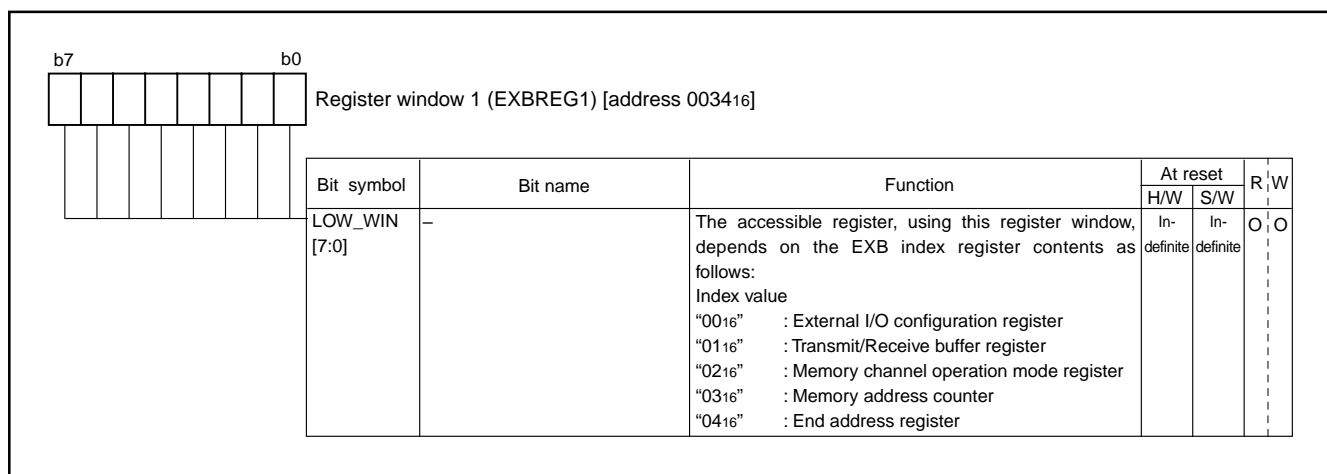


Fig. 82 Structure of Register window 1

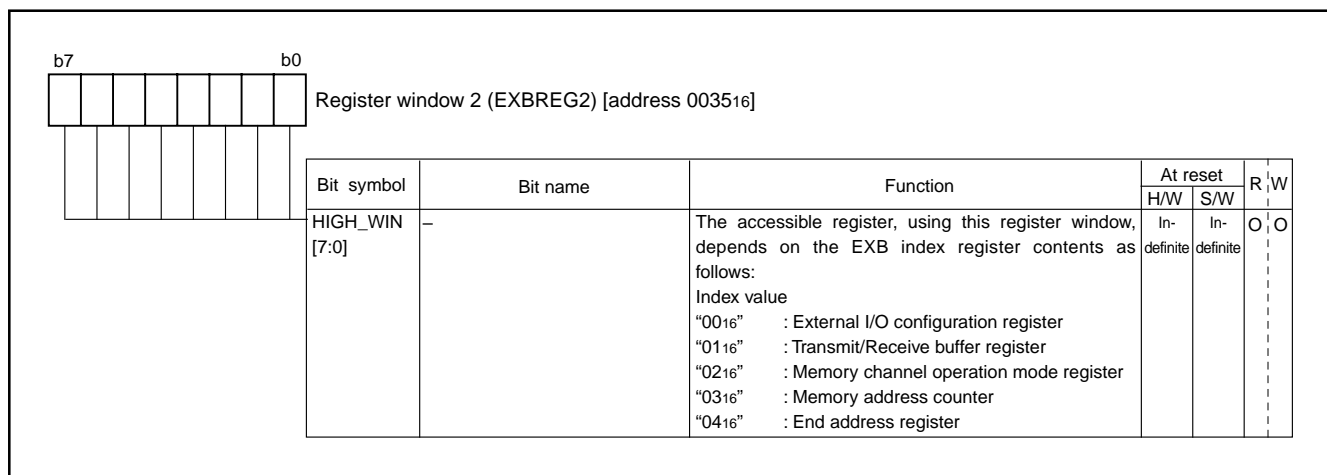


Fig. 83 Structure of Register window 2

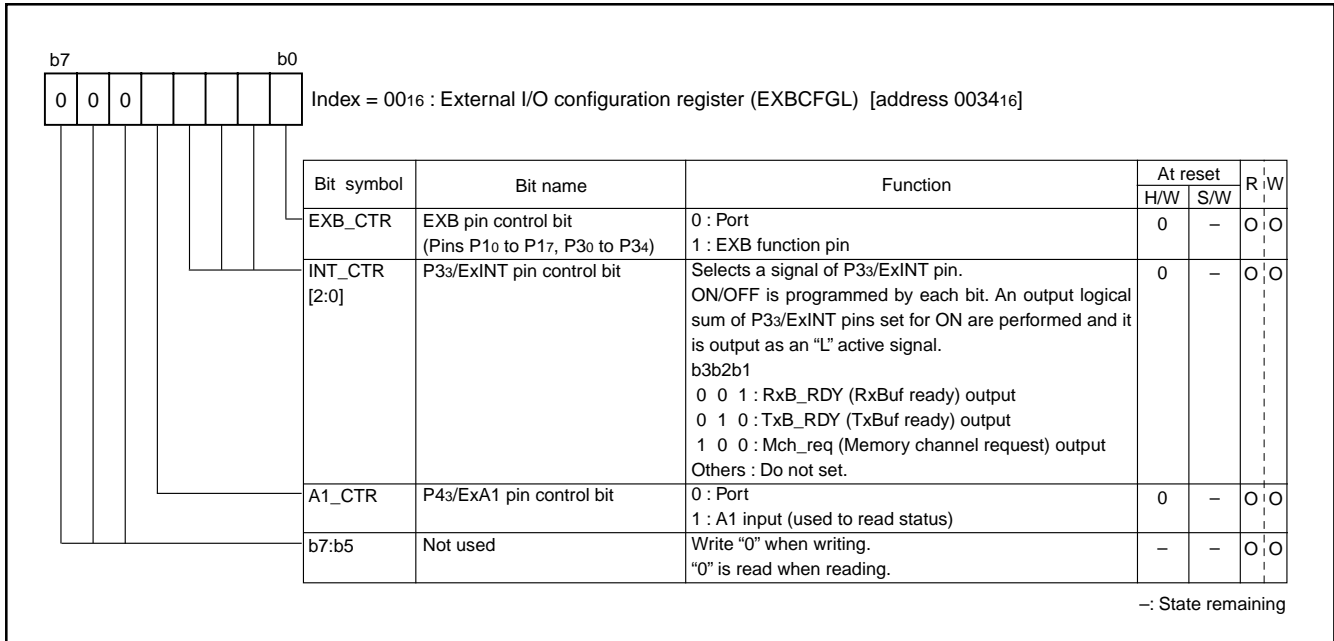


Fig. 84 Index00[low]; Structure of External I/O configuration register

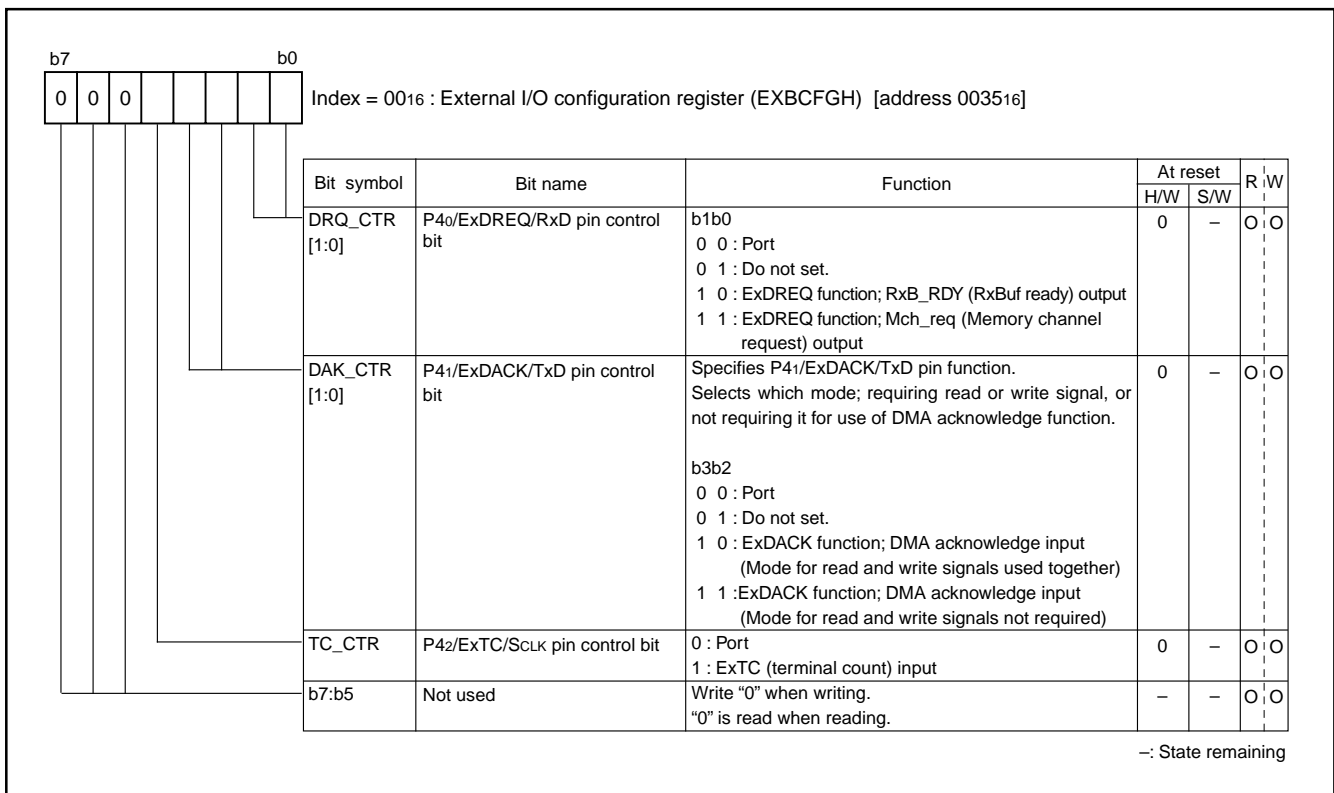


Fig. 85 Index00[high]; Structure of External I/O configuration register

HARDWARE

FUNCTIONAL DESCRIPTION

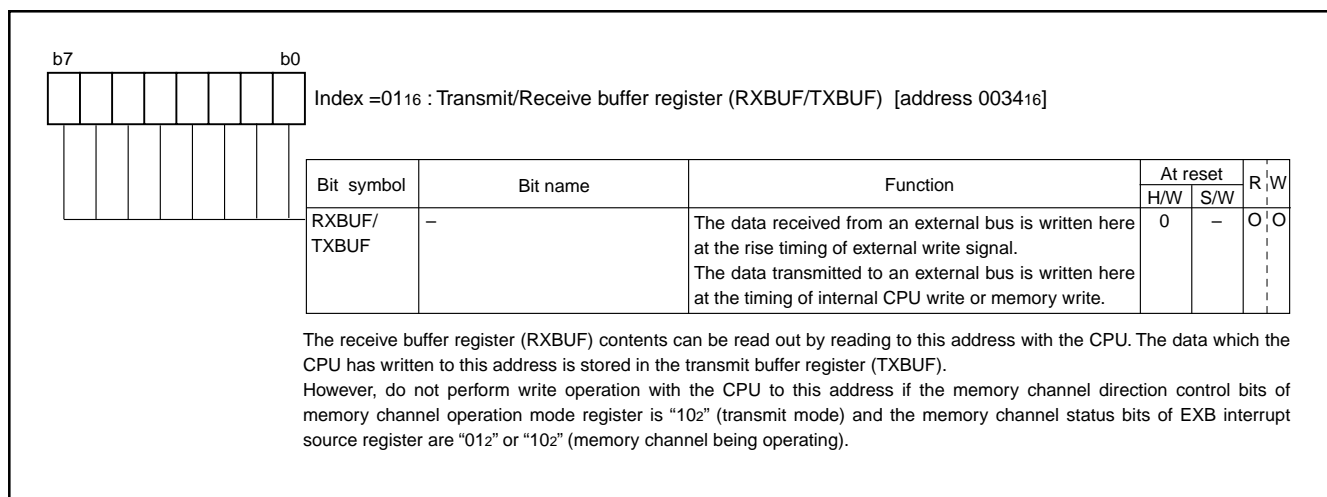


Fig. 86 Index01[low]; Structure of Transmit/Receive buffer register

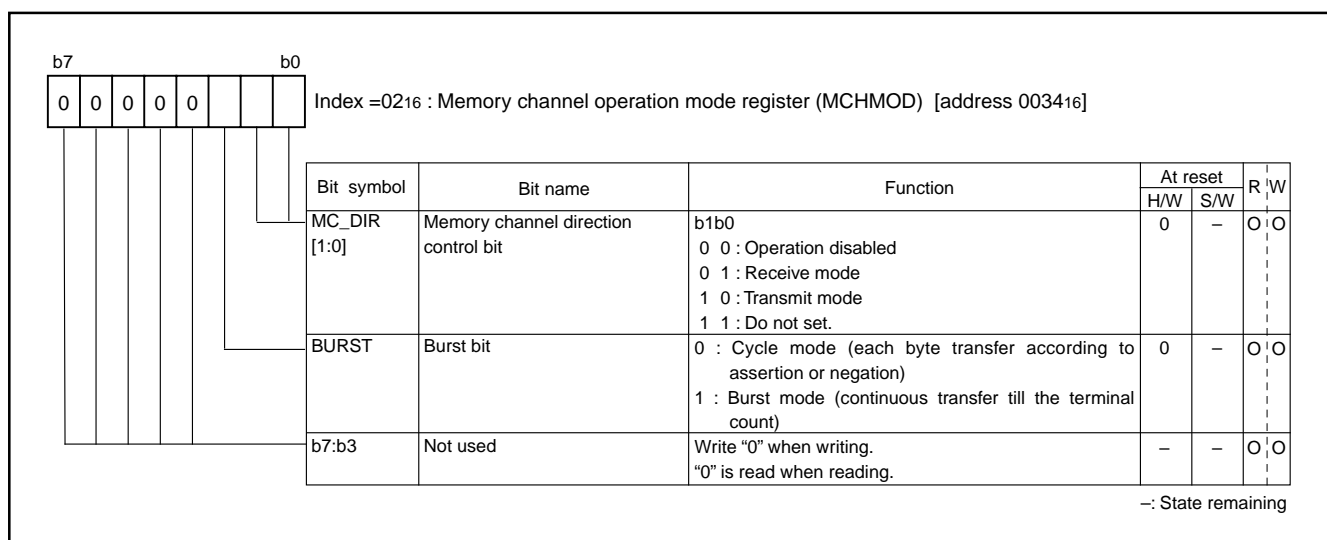


Fig. 87 Index02[low]; Structure of Memory channel operation mode register

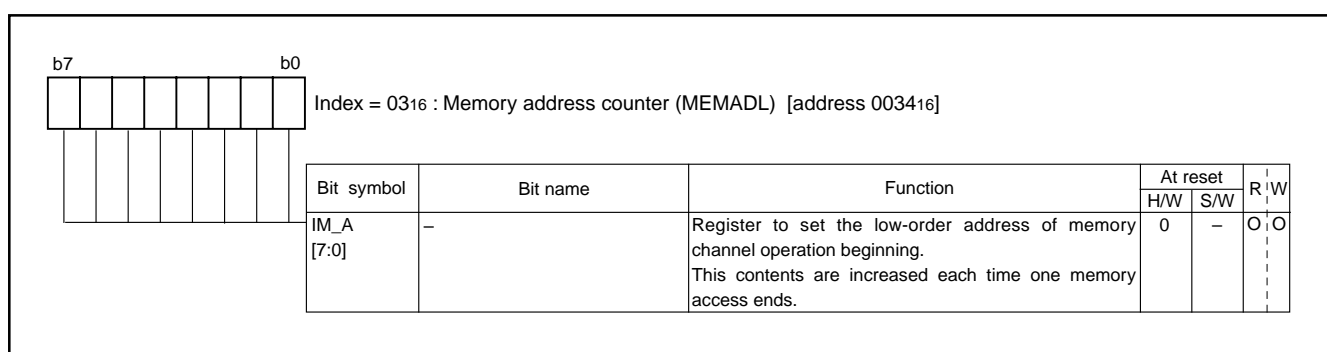


Fig. 88 Index03[low]; Structure of Memory address counter

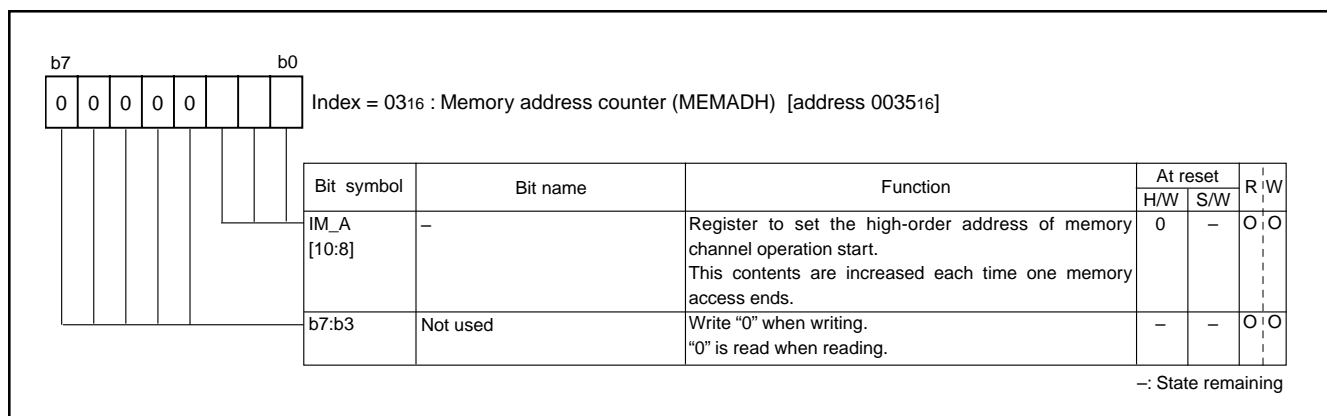


Fig. 89 Index03[high]; Structure of Memory address counter

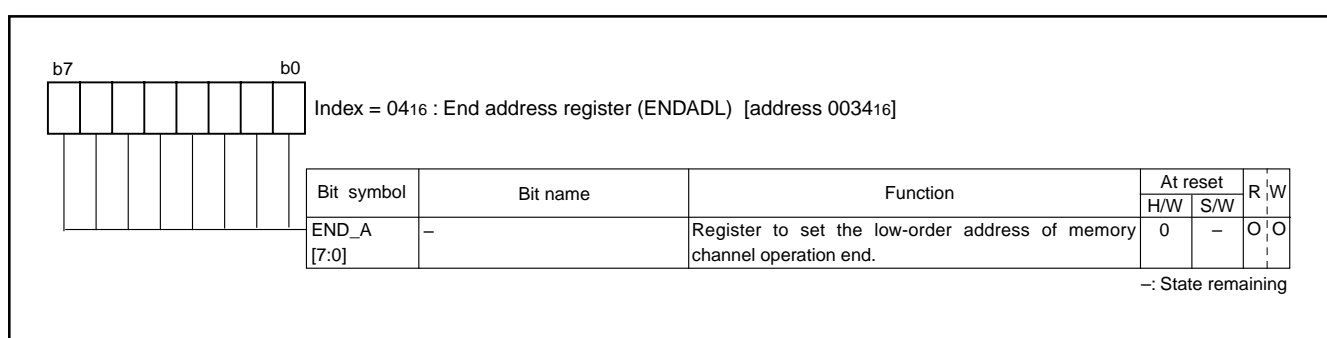


Fig. 90 Index04[low]; Structure of End address register

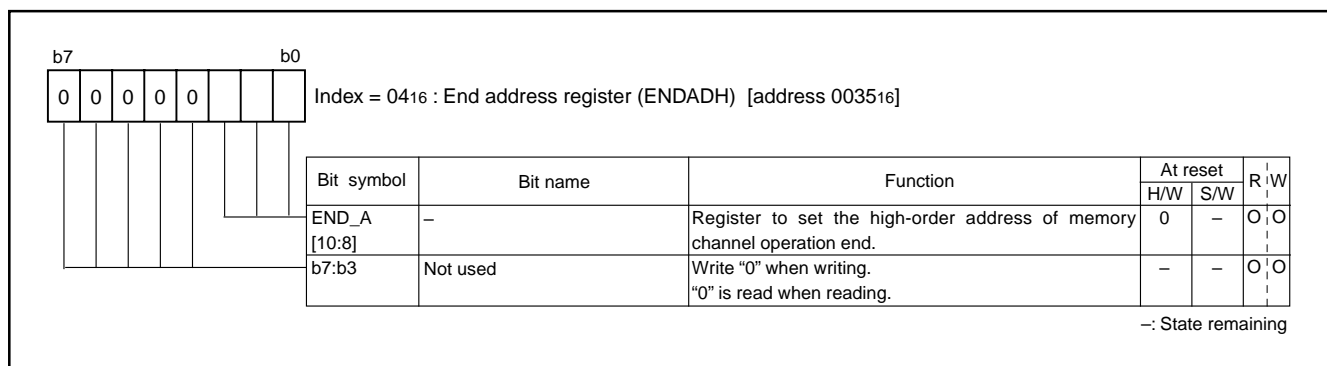


Fig. 91 Index04[high]; Structure of End address register

HARDWARE

FUNCTIONAL DESCRIPTION

EXB Operation Timing Diagram

(1) CPU Channel Receiving Operation

CPU channel receiving operation is shown below.

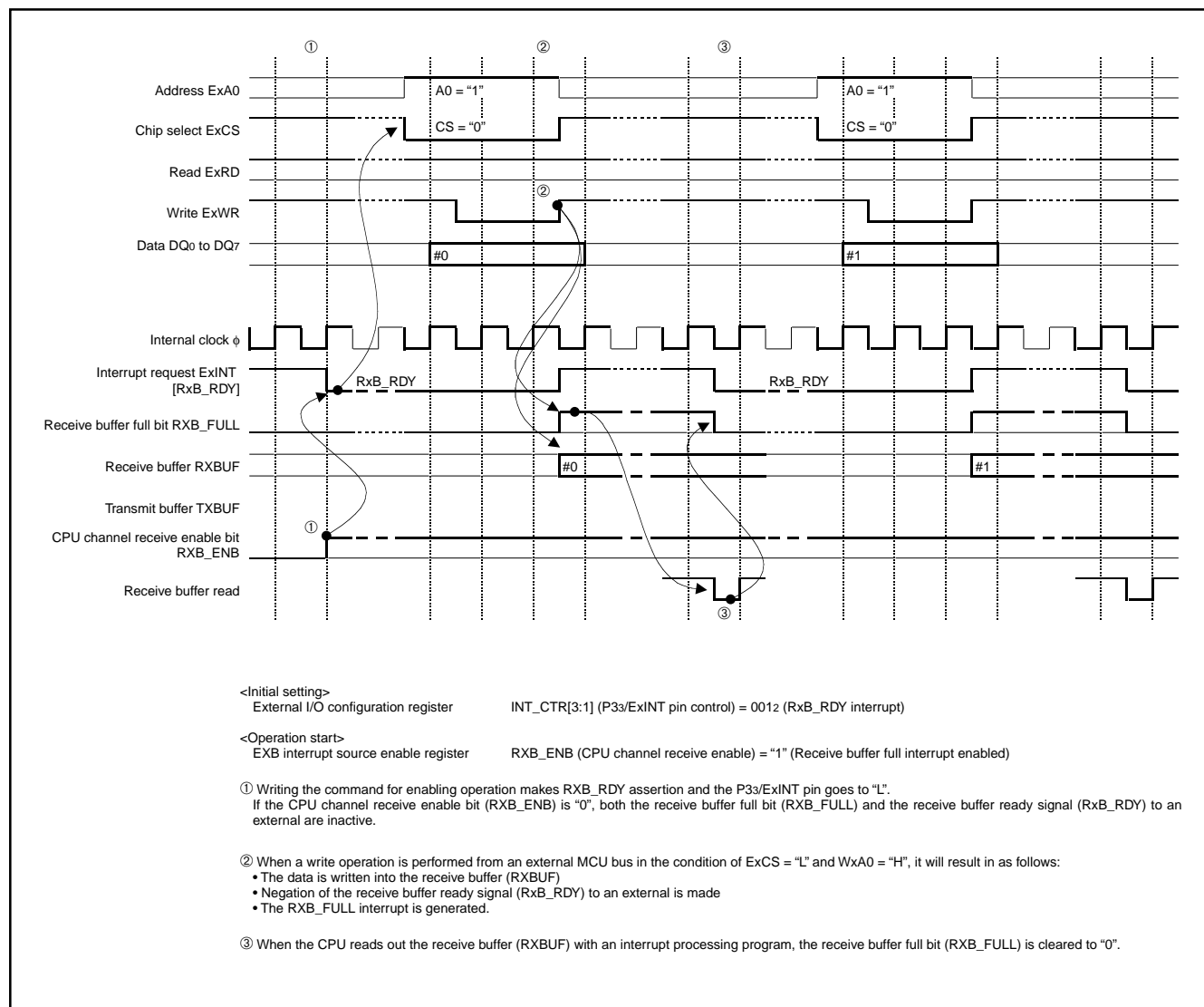


Fig. 92 CPU channel receiving operation

(2) CPU Channel Transmitting Operation

CPU channel transmitting operation is shown bellow.

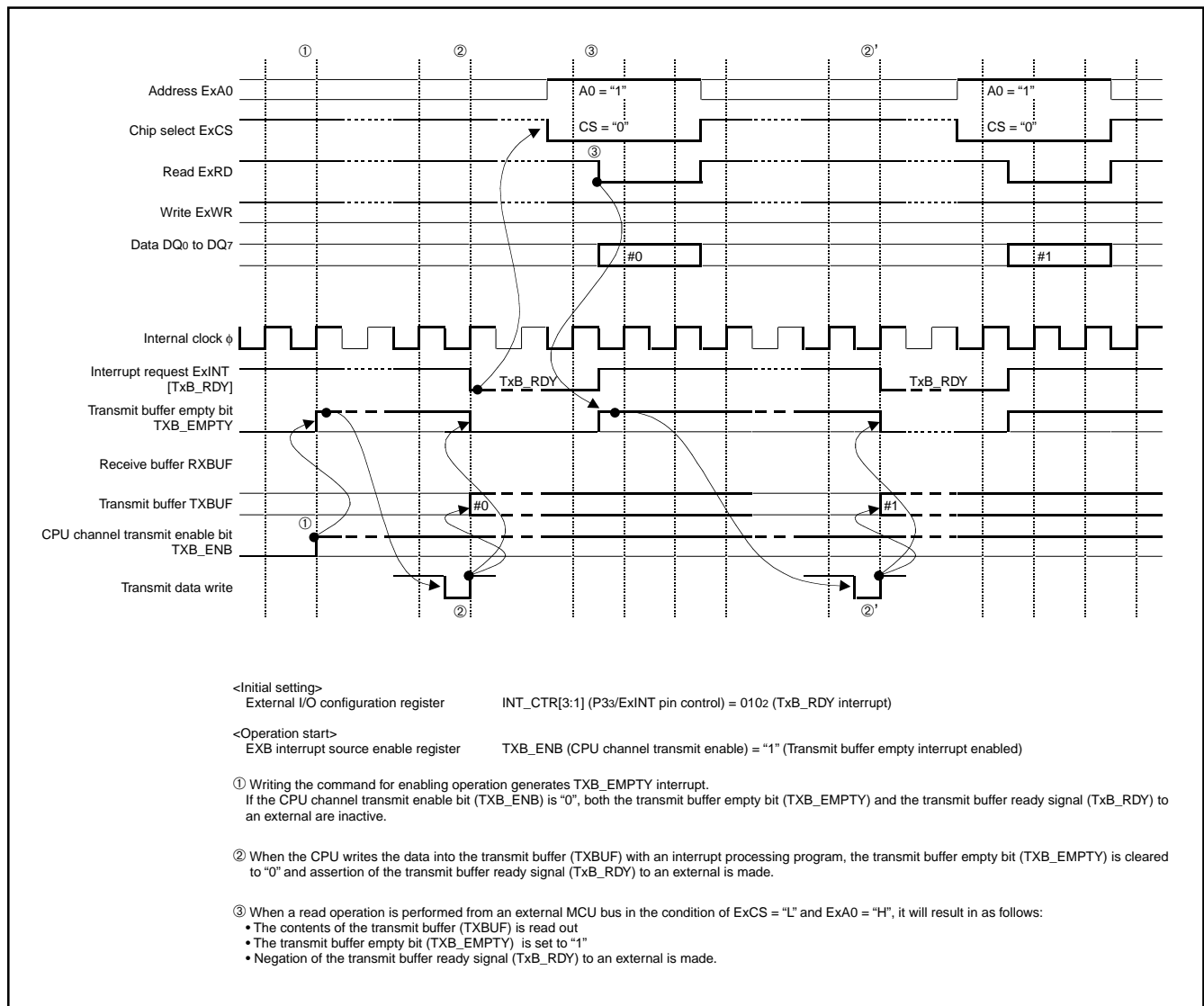


Fig. 93 CPU channel transmitting operation

HARDWARE

FUNCTIONAL DESCRIPTION

(3) Memory Channel Receiving Operation (1)- Cycle Mode

Memory channel receiving operation (1) is shown below.

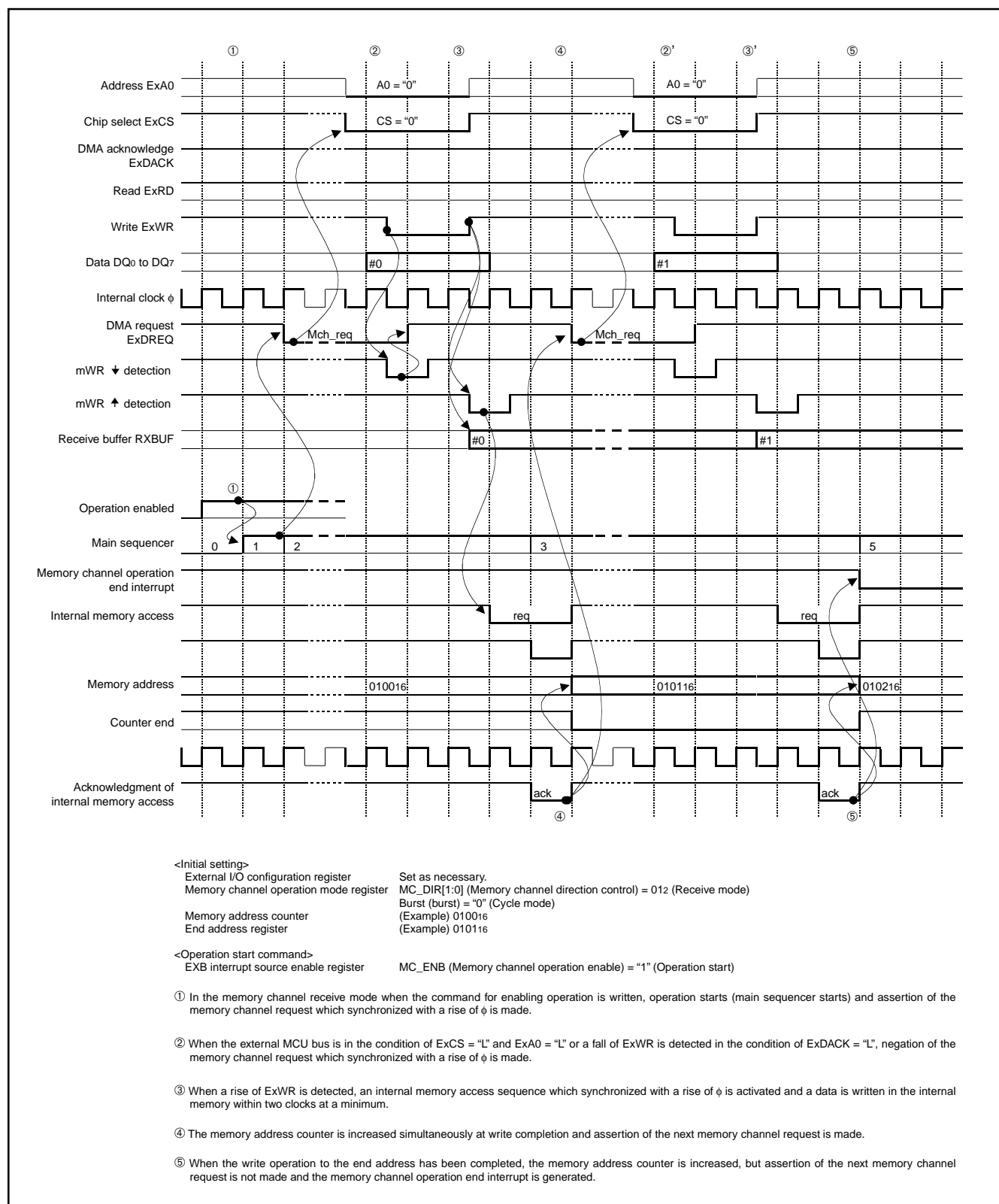


Fig. 94 Memory channel receiving operation (1)

(4) Memory Channel Receiving Operation (2)-Burst Mode

Memory channel receiving operation (2) is shown below.

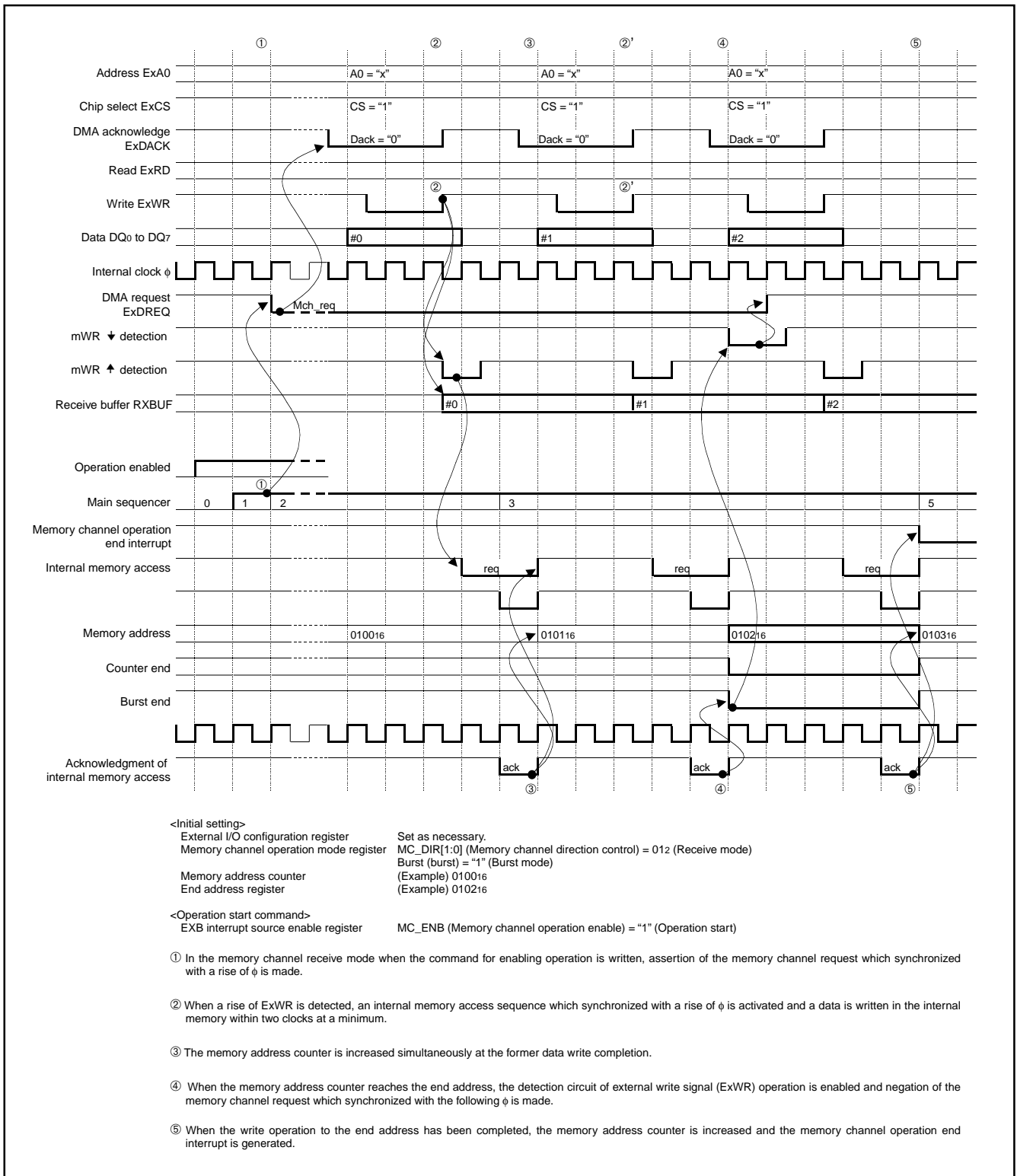


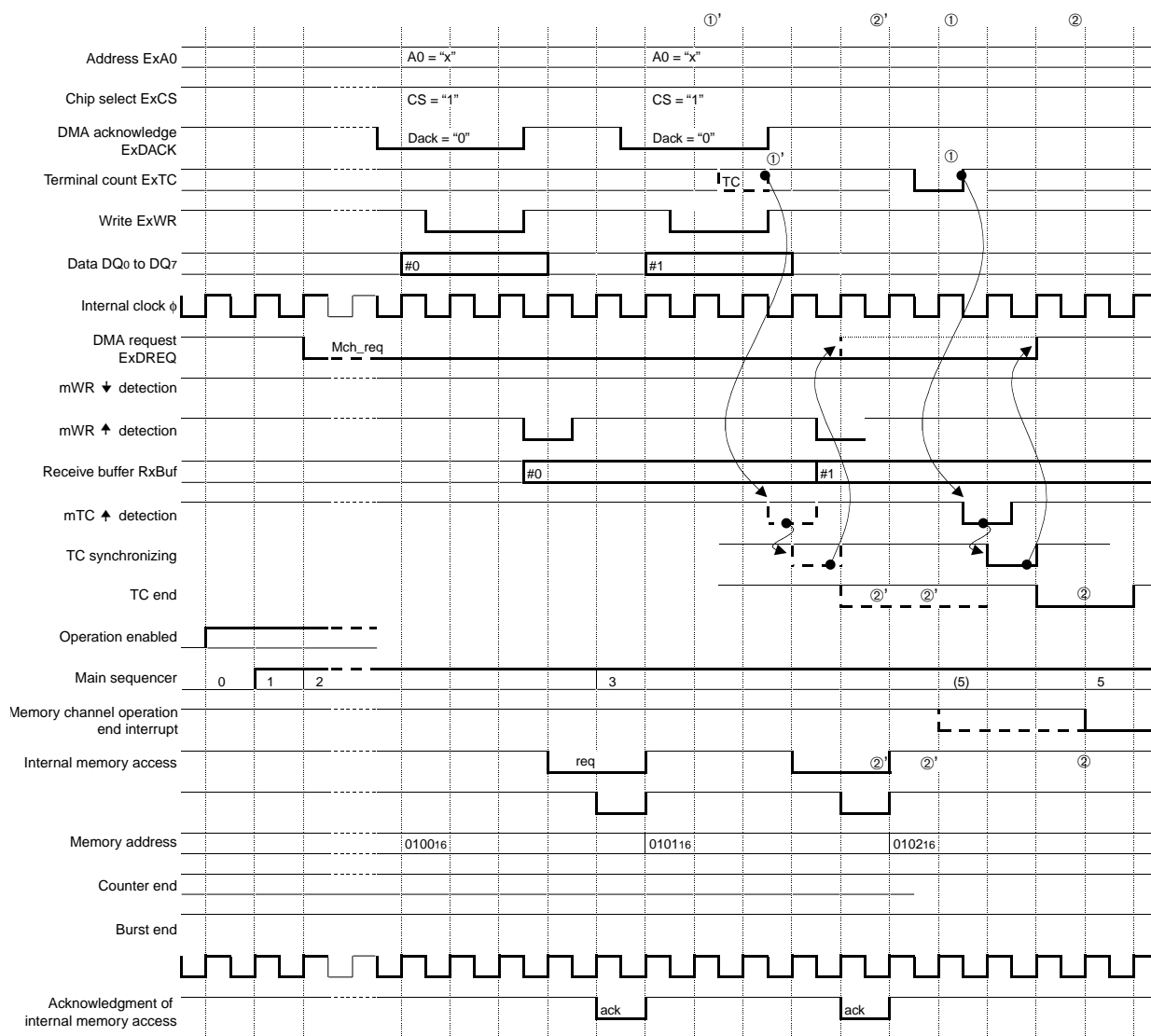
Fig. 95 Memory channel receiving operation (2)

HARDWARE

FUNCTIONAL DESCRIPTION

(5) Memory Channel Receiving Operation (3)- Burst Mode (Terminal Count)

Memory channel receiving operation (3) is shown below.



<Initial setting>
 External I/O configuration register Set as necessary.
 Memory channel operation mode register MC_DIR[1:0] (Memory channel direction control) = 012 (Receive mode)
 Burst (burst) = "1" (Burst mode)
 Memory address counter (Example) 0100₁₆
 End address register (Example) 0107₁₆

<Operation start command>
 EXB interrupt source enable register MC_ENB (Memory channel operation enable) = "1" (Operation start)

① When a rise of TC is detected, negation of the memory channel request which synchronized with a rise of ϕ is made.

② When the write operation to the end address has been completed, the memory channel operation end interrupt is generated.

Fig. 96 Memory channel receiving operation (3)

(6) Memory Channel Transmitting Operation

(1)-Cycle Mode

Memory channel transmitting operation (1) is shown below.

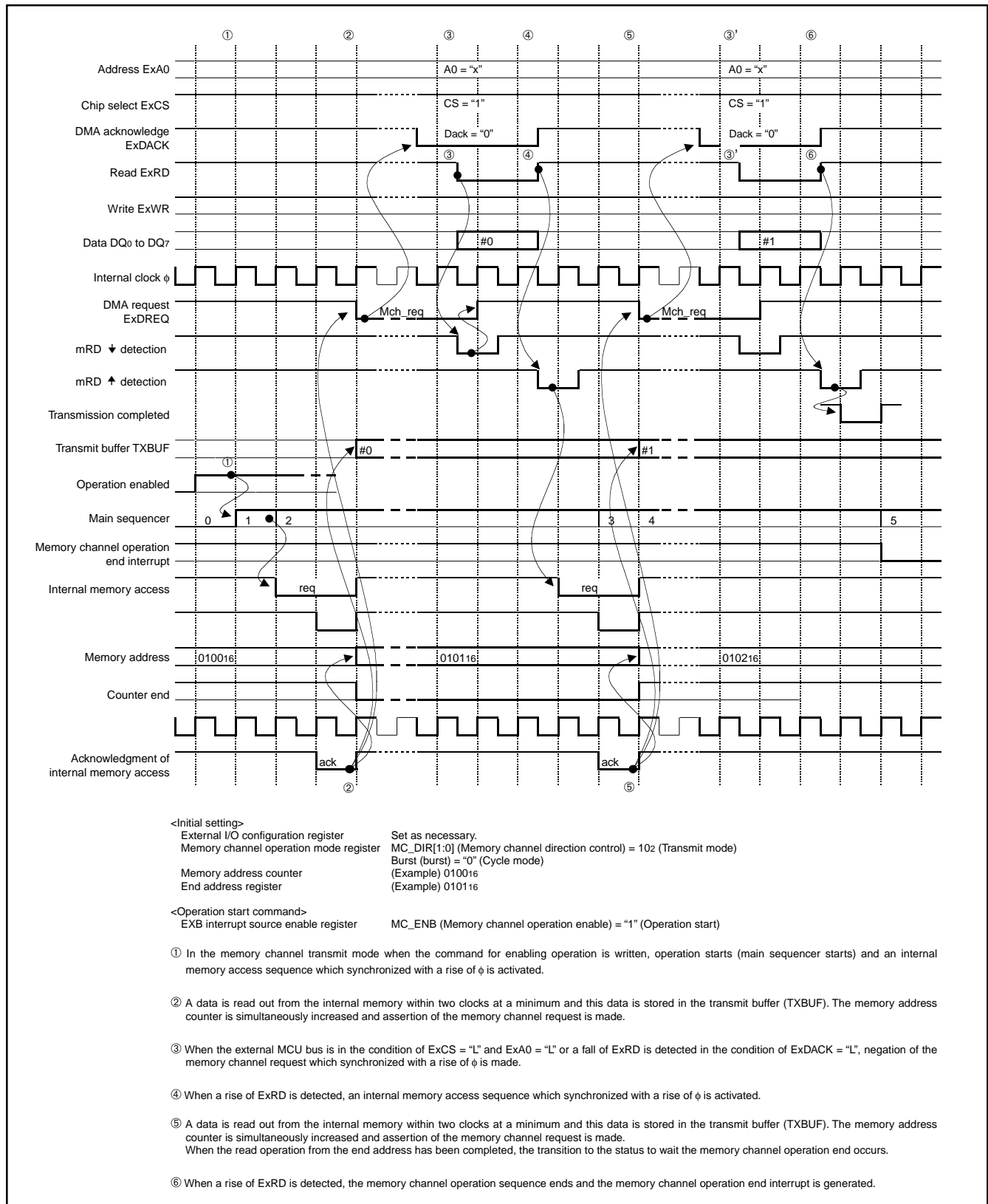


Fig. 97 Memory channel transmitting operation (1)

HARDWARE

FUNCTIONAL DESCRIPTION

(7) Memory Channel Transmitting Operation (2)-Burst Mode

Memory channel transmitting operation (2) is shown bellow.

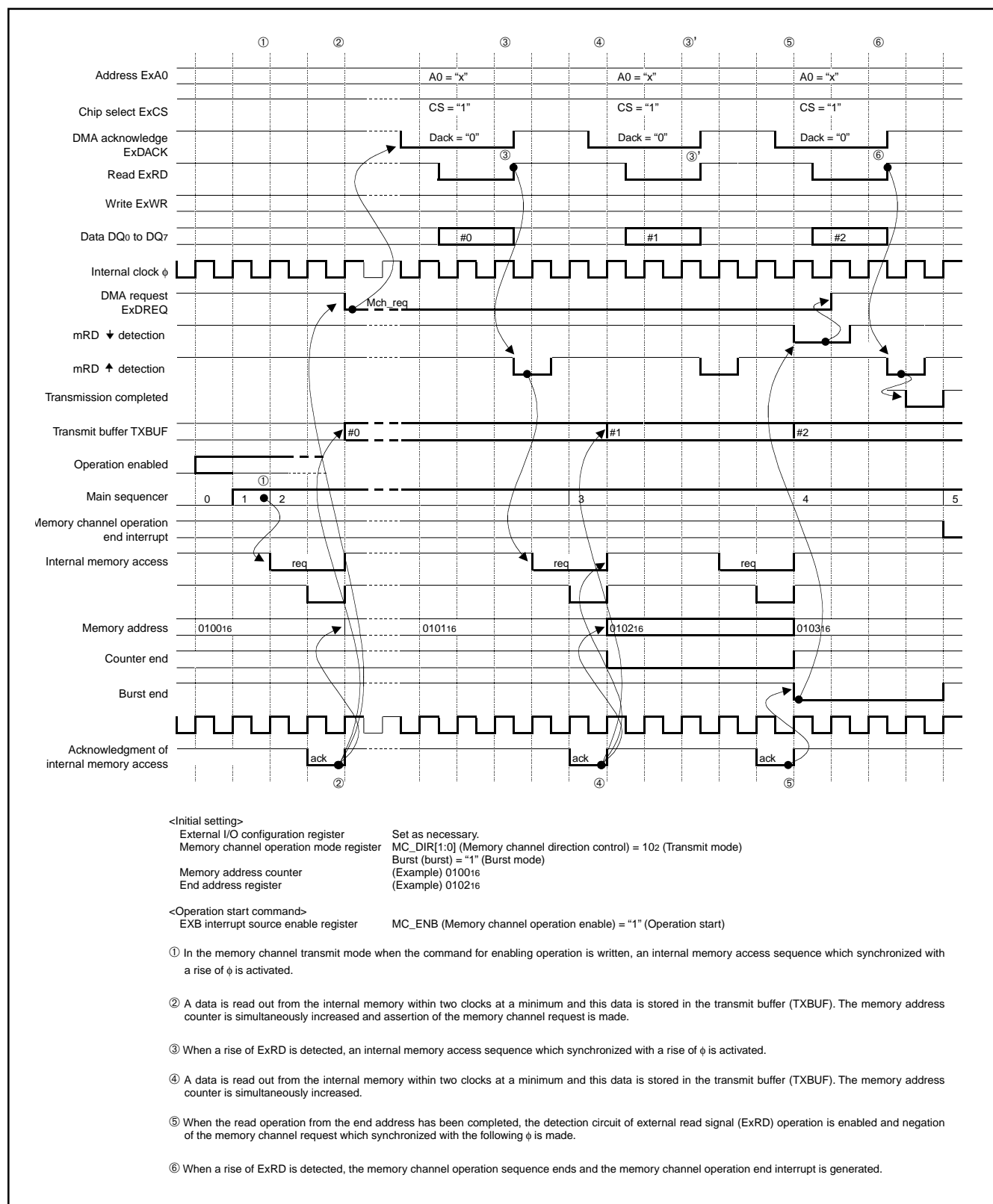


Fig. 98 Memory channel transmitting operation (2)

The multichannel RAM controls access from CPU, USB and EXB, synchronizing control with ϕ . The USB transfer rate is about 1.5 Mbytes/second. Access to the multichannel RAM is performed at every about 5.3 clocks in $\phi = 8$ MHz, or at every about 4 clocks in $\phi = 6$ MHz. The USB's access has priority to the EXB's.

If the multichannel RAM is outputting ONW signal while the CPU is in the state of reading/writing for the RAM area, the CPU read cycle or write cycle is extended by 1 period of ϕ .



HARDWARE

FUNCTIONAL DESCRIPTION

Multichannel RAM Operation Example

The multichannel RAM operation example is shown below.

This example shows the case that an external MCU uses the 38K0 group as a peripheral LSI (USB controller).

The following explains that the external MCU reads out the data which is received via the USB.

- ① The data which is received via the USB is written into the multichannel RAM.
- ② Receive completion is propagated to the CPU.
- ③ The external bus interface is activated owing to the CPU.
- ④ (1) The external bus interface sets the data which is read from the multichannel RAM into the internal data buffer.
(2) The external MCU reads out the data bus buffer of the external bus interface.
(3) The above operation is repeated by the number of the received bytes. After that, the data transfer is completed.

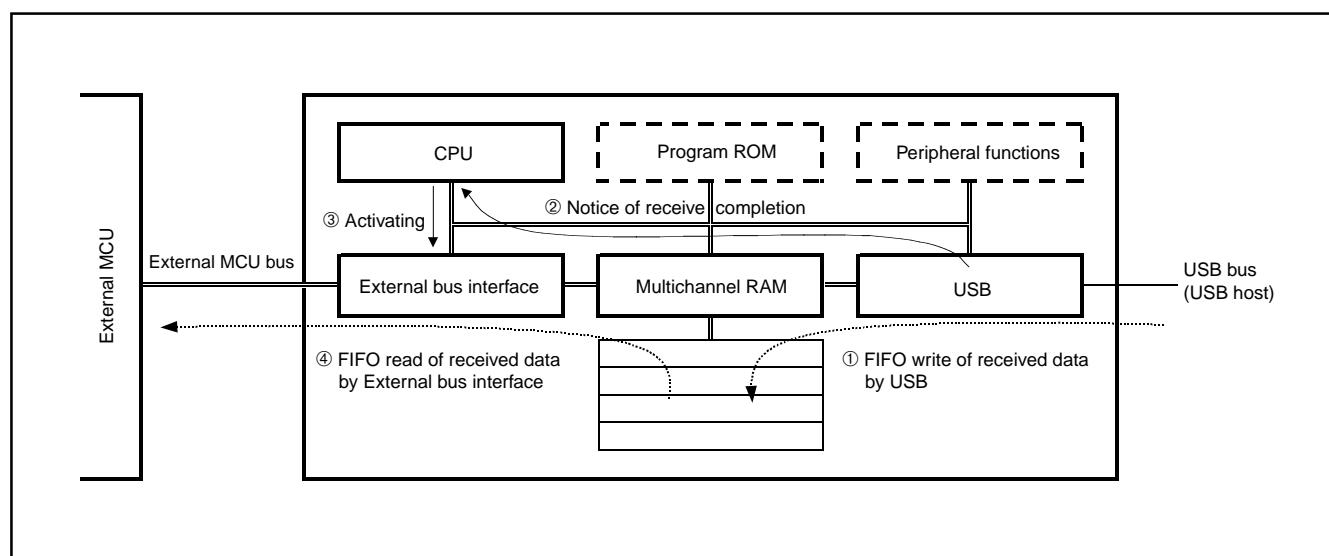


Fig. 101 Multichannel RAM operation example

A-D CONVERTER

The functional blocks of the A-D converter are described below.

[A-D Conversion Register 1, 2 (AD1, AD2)] 003716, 003816

The A-D conversion register is a read-only register that stores the result of an A-D conversion. When reading this register during an A-D conversion, the previous conversion result is read.

Bit 7 of the A-D conversion register 2 must be set to "0". Not only 10-bit reading but also only high-order 8-bit reading of conversion result can be performed by selecting the reading procedure of the A-D conversion registers 1, 2 after A-D conversion is completed (in Figure 103).

The 8-bit reading inclined to MSB is performed when reading the A-D converter register 1 after A-D conversion is started or reset; and when the A-D converter register 1 is read after reading the A-D converter register 2, the 8-bit reading inclined to LSB is performed.

[A-D Control Register (ADCON)] 003616

The A-D control register controls the A-D conversion process. Bits 0 to 2 select a specific analog input pin. Bit 3 signals the completion of an A-D conversion. The value of this bit remains at "0" during an A-D conversion, and changes to "1" when an A-D conversion ends. Writing "0" to this bit starts the A-D conversion.

Comparison Voltage Generator

The comparison voltage generator divides the voltage between VREF and AVSS into 1024, and that outputs the comparison voltage.

The A-D converter successively compares the comparison voltage Vref in each mode, dividing the VREF voltage (see below), with the input voltage.

• 10-bit reading

$$V_{ref} = \frac{V_{REF}}{1024} \times n \quad (n = 0-1023)$$

• 8-bit reading

$$V_{ref} = \frac{V_{REF}}{256} \times n \quad (n = 0-255)$$

Channel Selector

The channel selector selects one of the input ports P17/AN7-P10/AN0.

Comparator and Control Circuit

The comparator and control circuit compares an analog input voltage with the comparison voltage, and then stores the result in the A-D conversion registers 1, 2. When an A-D conversion is completed, the control circuit sets the AD conversion completion bit and the AD interrupt request bit to "1".

Note that because the comparator consists of a capacitor coupling, set f(system clock) to 500 kHz or more during an A-D conversion.

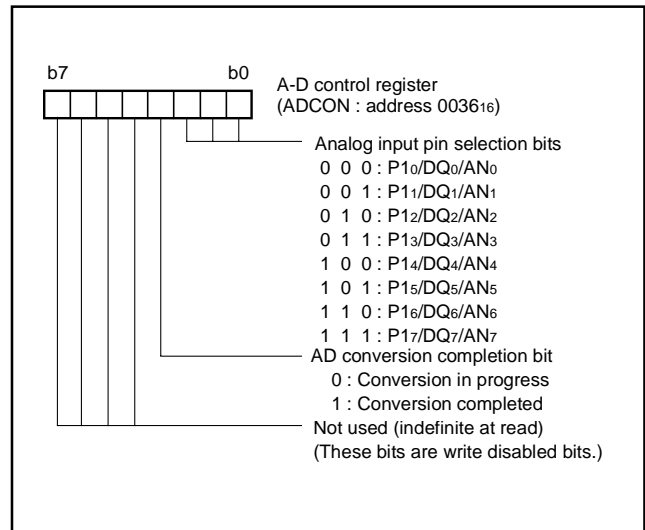


Fig. 102 Structure of A-D control register

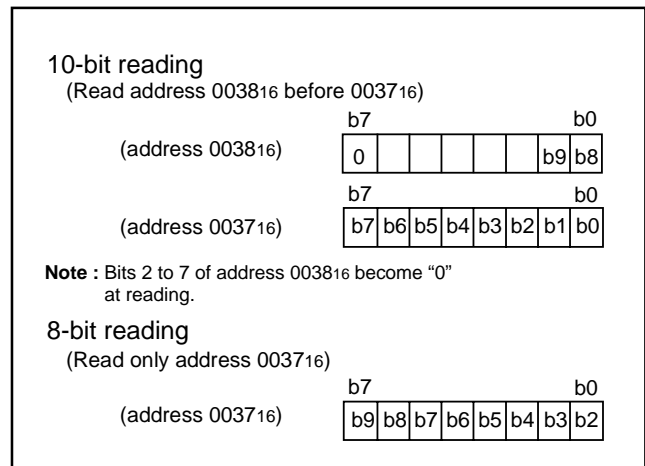


Fig. 103 10-bit A-D mode reading

HARDWARE

FUNCTIONAL DESCRIPTION

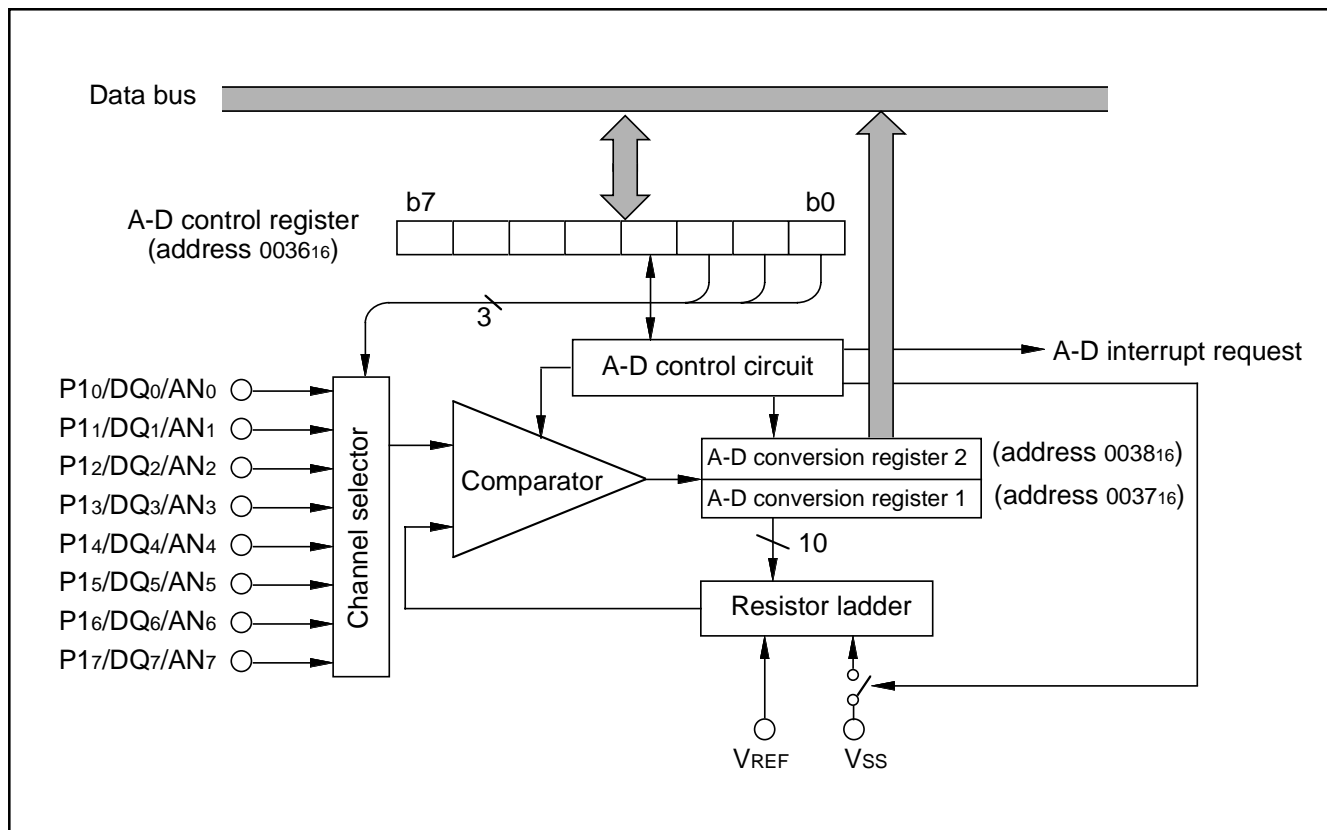


Fig. 104 A-D converter block diagram

WATCHDOG TIMER

The watchdog timer gives a mean of returning to the reset status when a program cannot run on a normal loop (for example, because of a software run-away). The watchdog timer consists of an 8-bit watchdog timer L and an 8-bit watchdog timer H.

Standard Operation of Watchdog Timer

When any data is not written into the watchdog timer control register (address 0039₁₆) after resetting, the watchdog timer is in the stop state. The watchdog timer starts to count down by writing an optional value into the watchdog timer control register (address 0039₁₆) and an internal reset occurs at an underflow of the watchdog timer H.

Accordingly, programming is usually performed so that writing to the watchdog timer control register (address 0039₁₆) may be started before an underflow. When the watchdog timer control register (address 0039₁₆) is read, the values of the high-order 6 bits of the watchdog timer H, STP instruction disable bit (bit 6), and watchdog timer H count source selection bit (bit 7) are read.

Initial Value of Watchdog Timer

At reset or writing to the watchdog timer control register (address 0039₁₆), each watchdog timer H and L is set to "FF₁₆."

● Watchdog timer H count source selection bit operation

Bit 7 of the watchdog timer control register (address 0039₁₆) permits selecting a watchdog timer H count source. When this bit is set to "0", the count source becomes the underflow signal of watchdog timer L. The detection time is set to 131.072 ms at system clock 8 MHz frequency.

When this bit is set to "1", the count source becomes the system clock divided by 16. The detection time in this case is set to 512 μ s at system clock 8 MHz frequency. This bit is cleared to "0" after resetting.

● Operation of STP instruction disable bit

Bit 6 of the watchdog timer control register (address 0039₁₆) permits disabling the STP instruction when the watchdog timer is in operation.

When this bit is "0", the STP instruction is enabled.

When this bit is "1", the STP instruction is disabled.

Once the STP instruction is executed, an internal reset occurs. When this bit is set to "1", it cannot be rewritten to "0" by program. This bit is cleared to "0" after resetting.

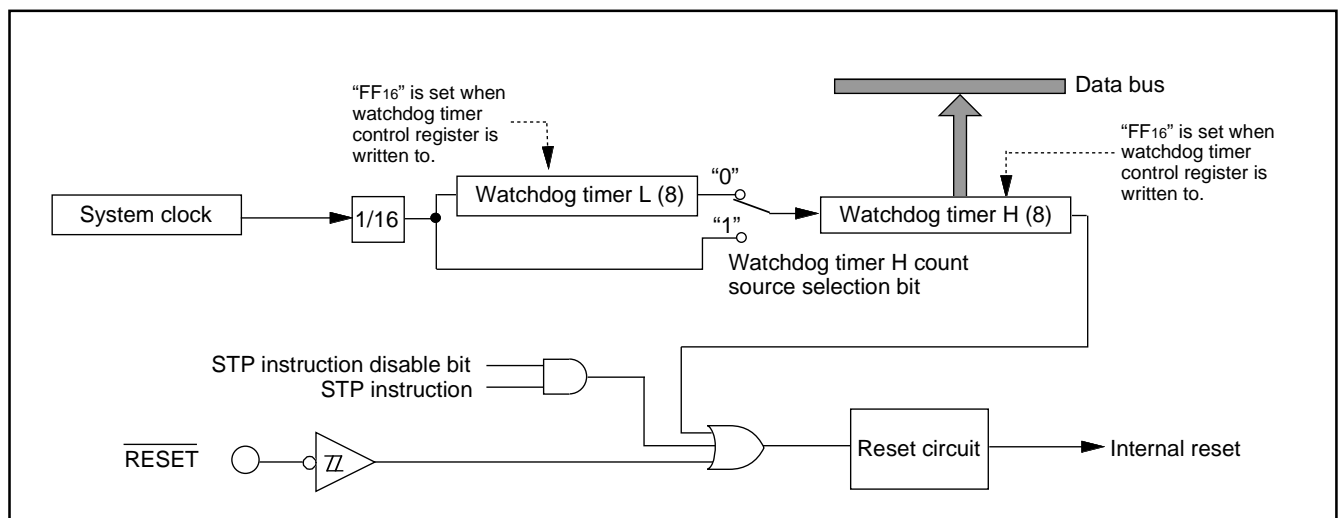


Fig. 105 Block diagram of Watchdog timer

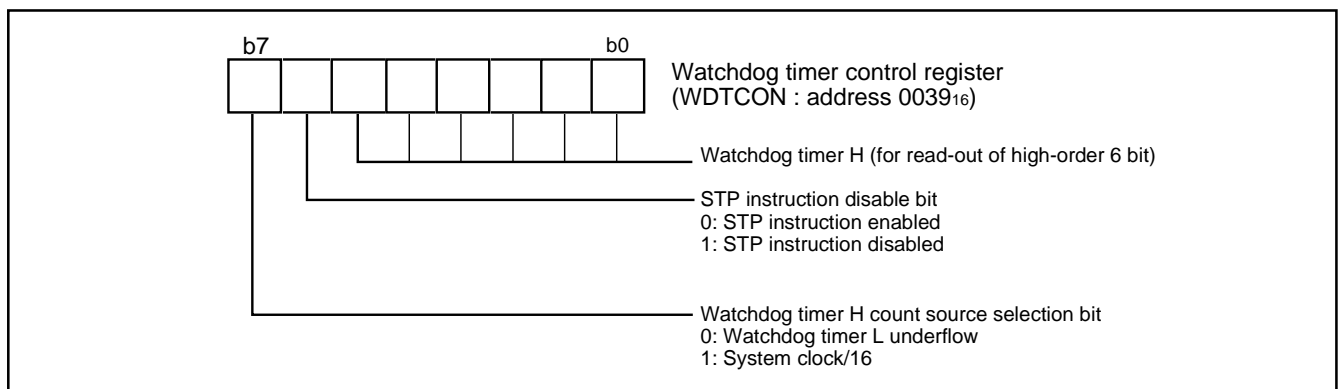


Fig. 106 Structure of Watchdog timer control register

HARDWARE

FUNCTIONAL DESCRIPTION

RESET CIRCUIT

To reset the microcomputer, $\overline{\text{RESET}}$ pin should be held at an "L" level for 16 cycles or more of X_{IN} . Then the $\overline{\text{RESET}}$ pin is returned to an "H" level (the power source voltage should be between 4.0 V and 5.25 V for Standard or between 3.0 V and 5.25 V for L version, and the oscillation should be stable), reset is released. After the reset is completed, the program starts from the address contained in address FFFD_{16} (high-order byte) and address FFFC_{16} (low-order byte). Make sure that the reset input voltage is 0.8 V for V_{CC} of 4.0 V (Standard), it is 0.6 V for V_{CC} of 3.0 V (L version).

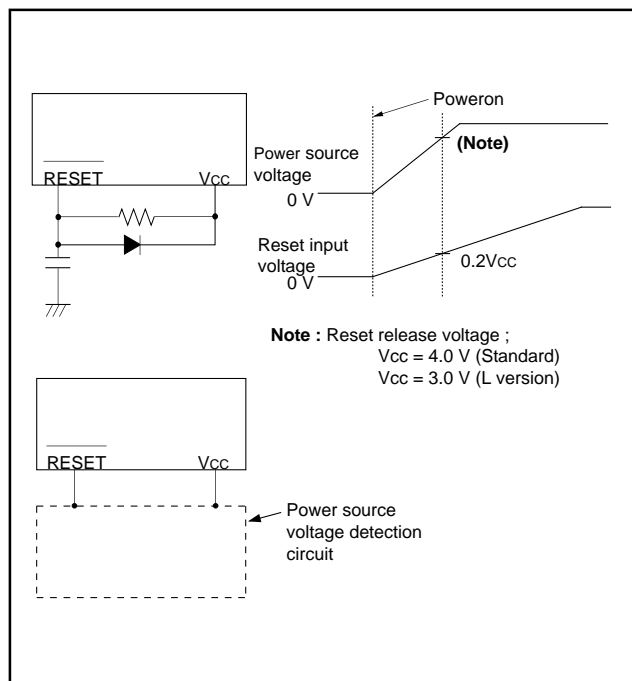


Fig. 107 Example of reset circuit

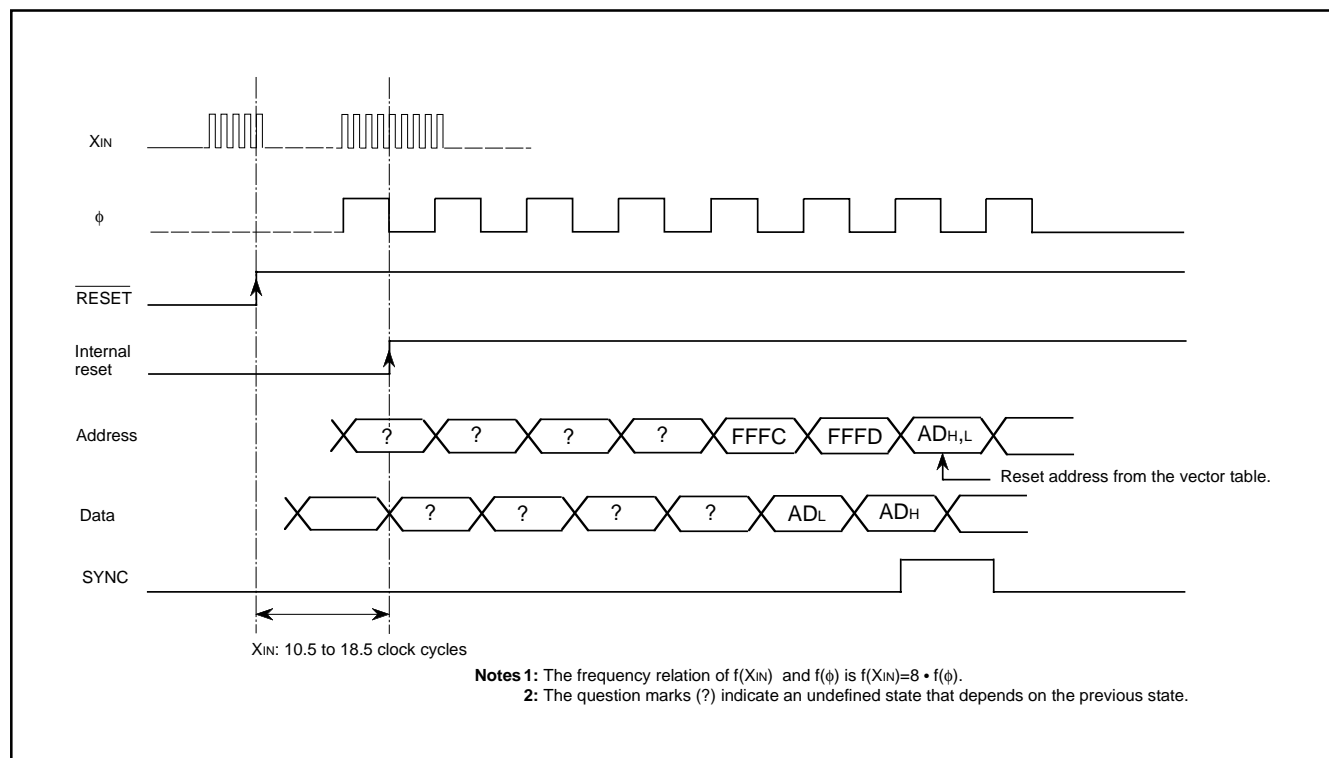


Fig. 108 Reset sequence

PLL CIRCUIT (FREQUENCY SYNTHESIZER)

The PLL circuit generates f_{VCO} (PLL output clock), which is required for f_{USB} (USB clock) and f_{SYN} (f_{USB} division clock), from $f(X_{IN})$ (external input reference clock). Figure 109 shows the PLL circuit block diagram.

It is possible to input 6 or 12 MHz clock from the externals as a standard clock input. When using the USB function, set the PLL operation mode selection bit so that f_{VCO} may be set to 48 MHz.

The PLL circuit operates by setting the PLL operation enable bit to "1". When supplying f_{VCO} to the USB block, wait for the oscillation stable time (1ms or less) of PLL before selecting f_{VCO} with the USB clock selection bit.

According to the setting of the USB clock division ratio selection bit, the division clock of f_{USB} is supplied to f_{SYN} . When using this clock as system clock, set the USB clock division ratio selection bit so that it may be set to 6 MHz, 8 MHz or 12 MHz. (However, using it only when f_{USB} is 48MHz is recommended).

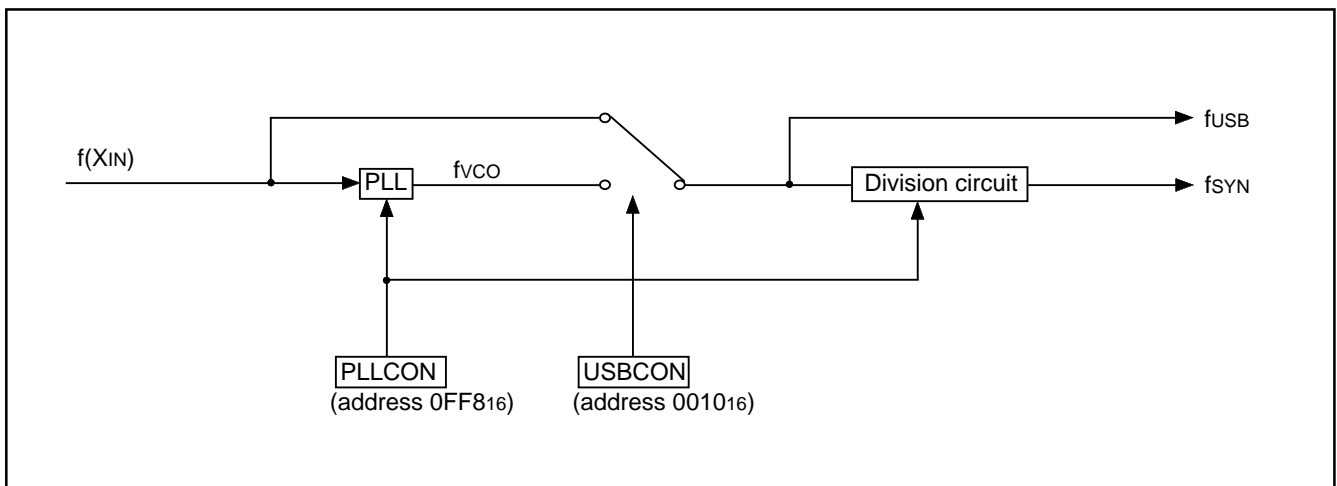


Fig. 109 Block diagram of PLL circuit

HARDWARE

FUNCTIONAL DESCRIPTION

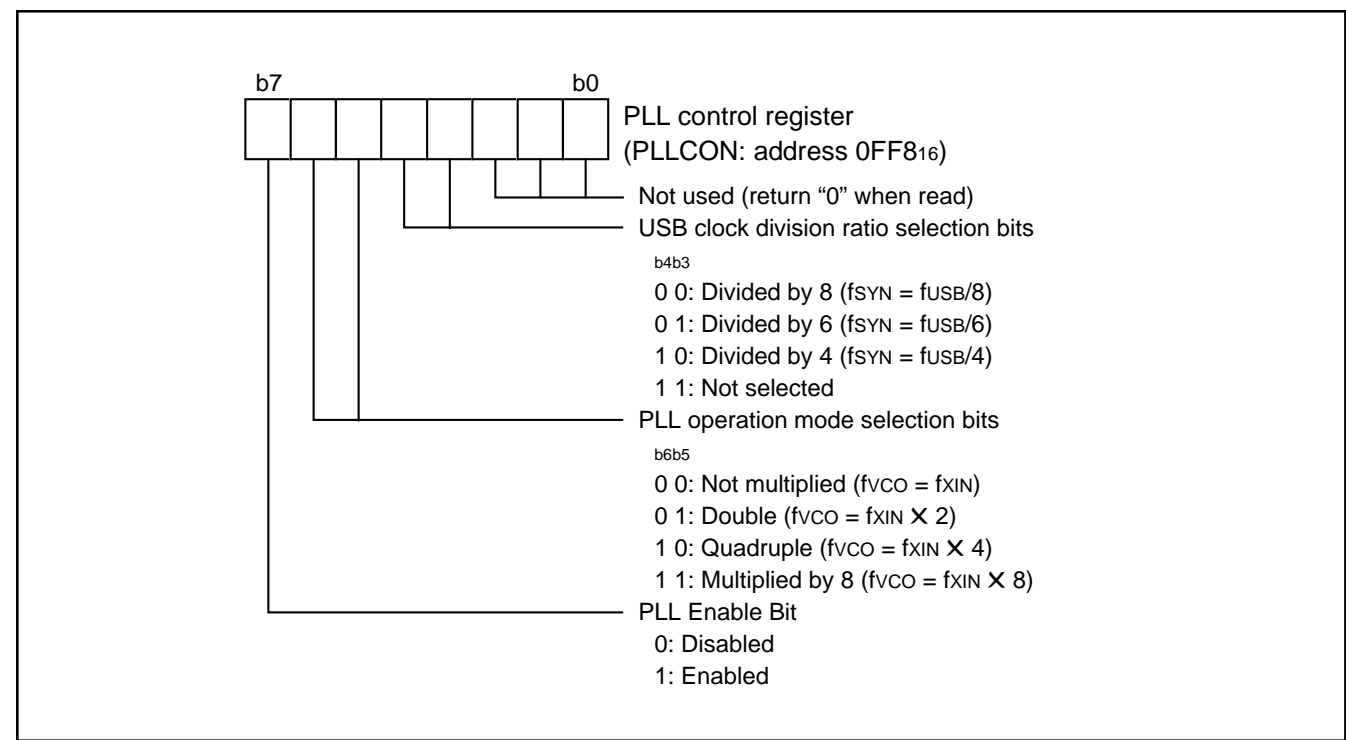


Fig. 110 Structure of PLL control register

CLOCK GENERATING CIRCUIT

An oscillation circuit can be formed by connecting a resonator between XIN and XOUT. Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between XIN and XOUT since a feed-back resistor exists on-chip.

Frequency Control

Either f_{SYN} or f(XIN) can be selected as an internal system clock. Furthermore, the frequency of internal clock ϕ can be selected by the system clock division ratio selection bit.

(1) f_{SYN} clock

f_{SYN} clock is generated by the PLL circuit. f(XIN) or f_{VCO} can be selected as an input clock. When using as an internal system clock, there is restriction on use. Refer to the clause of "PLL CIRCUIT".

(2) f(XIN) clock

The frequency applied to the XIN pin is used as an internal system clock frequency.

Oscillation Control

(1) Stop mode

If the STP instruction is executed, the internal clock ϕ stops at an "H" level, and the XIN oscillator stops. When the oscillation stabilizing time set after STP instruction released bit is "0," the prescaler 12 is set to "FF16" and timer 1 is set to "0116." When the oscillation stabilizing time set after STP instruction released bit is "1," set the sufficient time for oscillation of used oscillator to stabilize since nothing is set to the prescaler 12 and timer 1. XIN divided by 16 is compulsorily connected to the input of the prescaler 12. Oscillator restarts when an external interrupt (including USB resume interrupt) is received, but the internal clock ϕ remains at "H" until timer 1 underflows. The internal clock ϕ is not supplied until timer 1 underflows. Because the sufficient time is required for the oscillation to stabilize when a ceramic resonator etc. is used. When the oscillator is restarted by reset, apply "L" level to the $\overline{\text{RESET}}$ pin until the oscillation is stable since a wait time will not be generated automatically.

(2) Wait mode

If the WIT instruction is executed, the internal clock ϕ stops at an "H" level, but the oscillator does not stop. The internal clock ϕ restarts at reset or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

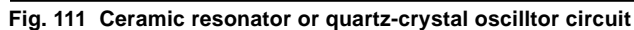
To ensure that the interrupts will be received to release the STP or WIT state, their interrupt enable bits must be set to "1" before executing of the STP or WIT instruction.

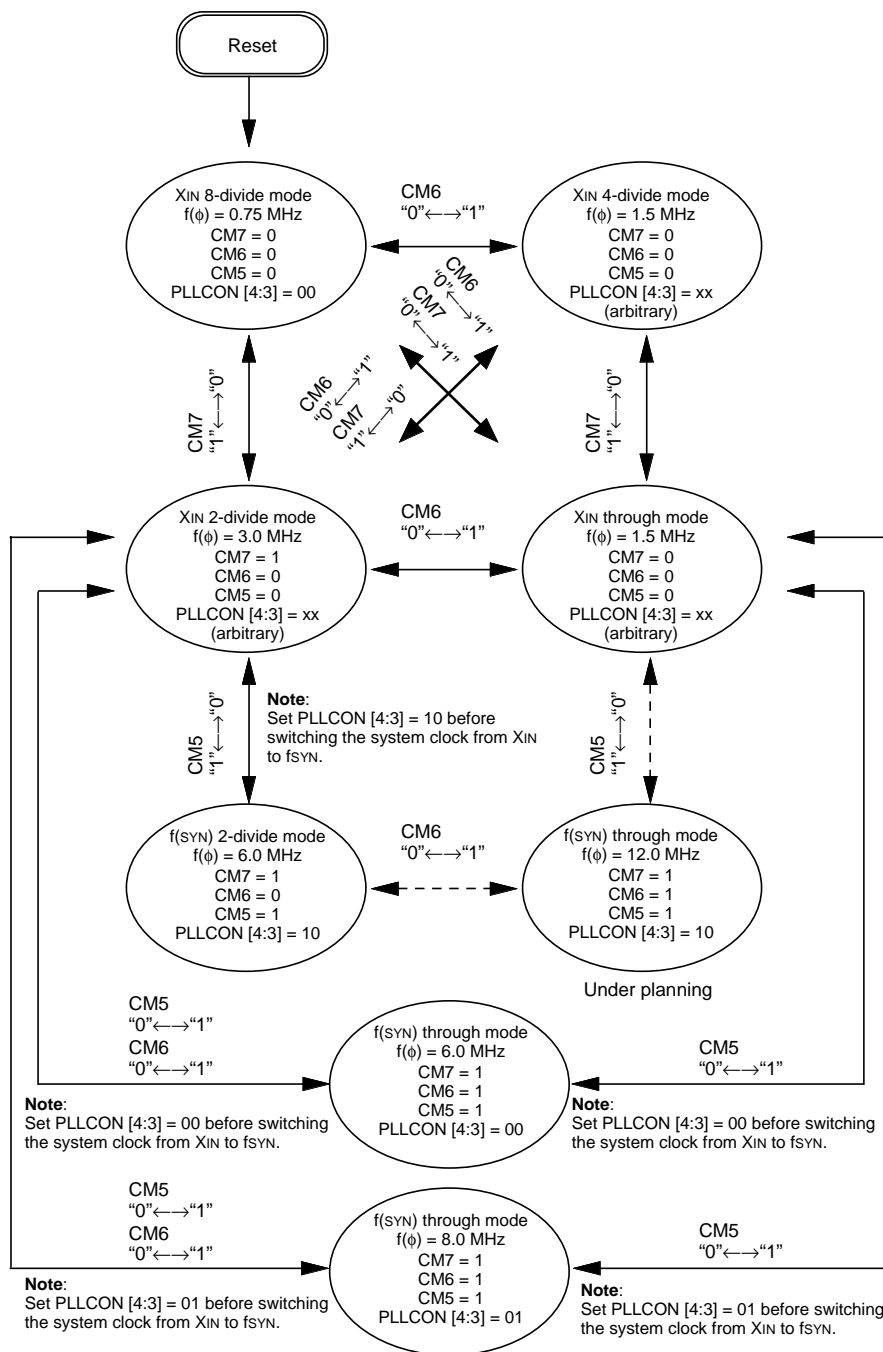
When releasing the STP state, the prescaler 12 and timer 1 will start counting the clock XIN divided by 16. Accordingly, set the timer 1 interrupt enable bit to "0" before executing the STP instruction.

■Note

When using the oscillation stabilizing time set after STP instruction released bit set to "1", evaluate time to stabilize oscillation of the used oscillator and set the value to the timer 1 and prescaler 12.

FUNCTIONAL DESCRIPTION





- Notes 1 :** Switch the mode by the allows shown between the mode blocks. (Do not switch between the modes directly without an allow.)
- 2 :** Set the USB clock (fUSB) to 48 MHz when switching the system clock to fSYN.
- 3 :** Do not change a division ratio of USB clock when using fSYN as the system clock.
- 4 :** See section "PLL CIRCUIT" in details for enabling/disabling PLL operation and usage notes of fSYN.
- 5 :** Set the system clock to XIN when entering STOP mode.
- 6 :** In all modes, switching to WAIT mode is possible. When it is released, the MCU returns to the original mode. In WAIT mode the timers can operate.

Remarks : This diagram assumes that the 6 MHz signals are applied to XIN pin.

Fig. 115 State transitions of clock

HARDWARE

FUNCTIONAL DESCRIPTION

FLASH MEMORY MODE

The 38K0 group's flash memory version has an internal new DINOR (DlVided bit line NOR) flash memory that can be rewritten with a single power source when Vcc is 4.5 to 5.25 V, and 2 power sources when Vcc is 3.0 to 4.5 V.

For this flash memory, three flash memory modes are available in which to read, program, and erase: the parallel I/O and standard serial I/O modes in which the flash memory can be manipulated using a programmer and the CPU rewrite mode in which the flash memory can be manipulated by the Central Processing Unit (CPU).

Summary

Table 9 lists the summary of the 38K0 group's flash memory version.

This flash memory version has some blocks on the flash memory as shown in Figure 116 and each block can be erased. The flash memory is divided into User ROM area and Boot ROM area.

In addition to the ordinary User ROM area to store the MCU operation control program, the flash memory has a Boot ROM area that is used to store a program to control rewriting in CPU rewrite and standard serial I/O modes. This Boot ROM area has had a standard serial I/O mode control program stored in it when shipped from the factory. However, the user can write a rewrite control program in this area that suits the user's application system. This Boot ROM area can be rewritten in only parallel I/O mode.

Table 9 Summary of 38K0 group's flash memory version

Item		Specifications
Power source voltage (Vcc)		4.00 – 5.25 V (Standard), 3.00 – 5.25 V (L version) (Program and erase in 4.00 to 5.25 V of Vcc.) 3.00 – 4.00 V(only L version) (Program and erase in 3.00 to 5.25 V of Vcc.)
Program/Erase VPP voltage (VPP)		4.50 – 5.25 V
Flash memory mode		3 modes; Flash memory can be manipulated as follows: •CPU rewrite mode: Manipulated by the Central Processing Unit (CPU). •Parallel I/O mode: Manipulated using an external programmer (Note 1) •Standard serial I/O mode: Manipulated using an external programmer (Note 1)
Erase block division	User ROM area	1 block (32 Kbytes)
	Boot ROM area	1 block (4 Kbytes) (Note 2)
Program method		Byte program
Erase method		Batch erasing
Program/Erase control method		Program/Erase control by software command
Number of commands		6 commands
Number of program/Erase times		100 times
Data retention period		10 years
ROM code protection		Available in parallel I/O mode and standard serial I/O mode

Notes 1: In the parallel I/O mode or the standard serial I/O mode, use the exclusive external equipment flash programmer which supports the 38K0 Group (flash memory version).

2: The Boot ROM area has had a standard serial I/O mode control program stored in it when shipped from the factory. This Boot ROM area can be rewritten in only parallel I/O mode.

(1) CPU Rewrite Mode

In CPU rewrite mode, the internal flash memory can be operated on (read, program, or erase) under control of the Central Processing Unit (CPU).
In CPU rewrite mode, only the User ROM area shown in Figure 116 can be rewritten; the Boot ROM area cannot be rewritten. Make sure the program and block erase commands are issued for only the User ROM area and each block area.
The control program for CPU rewrite mode can be stored in either User ROM or Boot ROM area. In the CPU rewrite mode, because the flash memory cannot be read from the CPU, the rewrite control program must be transferred to internal RAM area to be executed before it can be executed.

Microcomputer Mode and Boot Mode

The control program for CPU rewrite mode must be written into the User ROM or Boot ROM area in parallel I/O mode beforehand. (If the control program is written into the Boot ROM area, the standard serial I/O mode becomes unusable.)
See Figure 116 for details about the Boot ROM area.
Normal microcomputer mode is entered when the microcomputer is reset with pulling CNVss pin low. In this case, the CPU starts operating using the control program in the User ROM area.
When the microcomputer is reset by pulling the P16 (CE) pin high, the CNVss pin high, the CPU starts operating using the control program in the Boot ROM area. This mode is called the "Boot" mode.

Block Address

Block addresses refer to the maximum address of each block. These addresses are used in the block erase command.

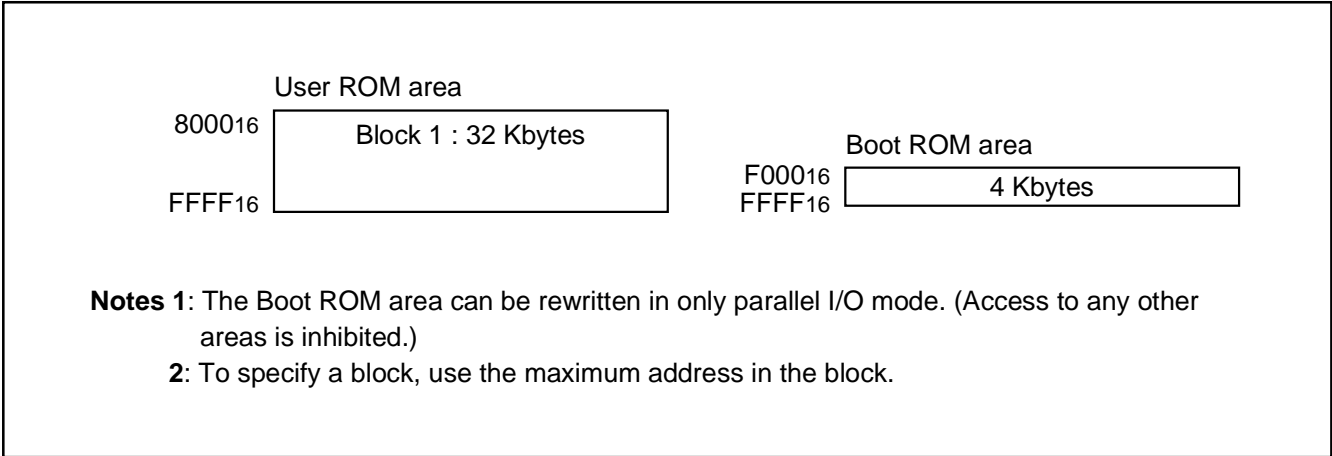


Fig. 116 Block diagram of built-in flash memory

HARDWARE

FUNCTIONAL DESCRIPTION

Outline Performance (CPU Rewrite Mode)

CPU rewrite mode is usable in the single-chip or Boot mode. The only User ROM area can be rewritten in CPU rewrite mode.

In CPU rewrite mode, the CPU erases, programs and reads the internal flash memory as instructed by software commands. This rewrite control program must be transferred to a memory such as the internal RAM before it can be executed.

The MCU enters CPU rewrite mode by applying 4.50 V to 5.25 V to the CNVSS pin and setting "1" to the CPU Rewrite Mode Select Bit (bit 1 of address 0FFE₁₆). Software commands are accepted once the mode is entered.

Use software commands to control program and erase operations. Whether a program or erase operation has terminated normally or in error can be verified by reading the status register.

Figure 117 shows the flash memory control register.

Bit 0 is the RY/ $\overline{\text{BY}}$ status flag used exclusively to read the operating status of the flash memory. During programming and erase operations, it is "0" (busy). Otherwise, it is "1" (ready). This is equivalent to the RY/ $\overline{\text{BY}}$ pin function in parallel I/O mode.

Bit 1 is the CPU Rewrite Mode Select Bit. When this bit is set to "1", the MCU enters CPU rewrite mode. Software commands are accepted once the mode is entered. In CPU rewrite mode, the

CPU becomes unable to access the internal flash memory directly. Therefore, use the control program in a memory other than internal flash memory for write to bit 1. To set this bit to "1", it is necessary to write "0" and then write "1" in succession. The bit can be set to "0" by only writing "0".

Bit 2 is the CPU Rewrite Mode Entry Flag. This flag indicates "1" in CPU rewrite mode, so that reading this flag can check whether CPU rewrite mode has been entered or not.

Bit 3 is the flash memory reset bit used to reset the control circuit of internal flash memory. This bit is used when exiting CPU rewrite mode and when flash memory access has failed. When the CPU Rewrite Mode Select Bit is "1", setting "1" for this bit resets the control circuit. To set this bit to "1", it is necessary to write "0" and then write "1" in succession. To release the reset, it is necessary to set this bit to "0".

Bit 4 is the User Area/Boot Area Select Bit. When this bit is set to "1", Boot ROM area is accessed, and CPU rewrite mode in Boot ROM area is available. In Boot mode, this bit is set to "1" automatically. Reprogramming of this bit must be in a memory other than internal flash memory.

Figure 118 shows a flowchart for setting/releasing CPU rewrite mode.

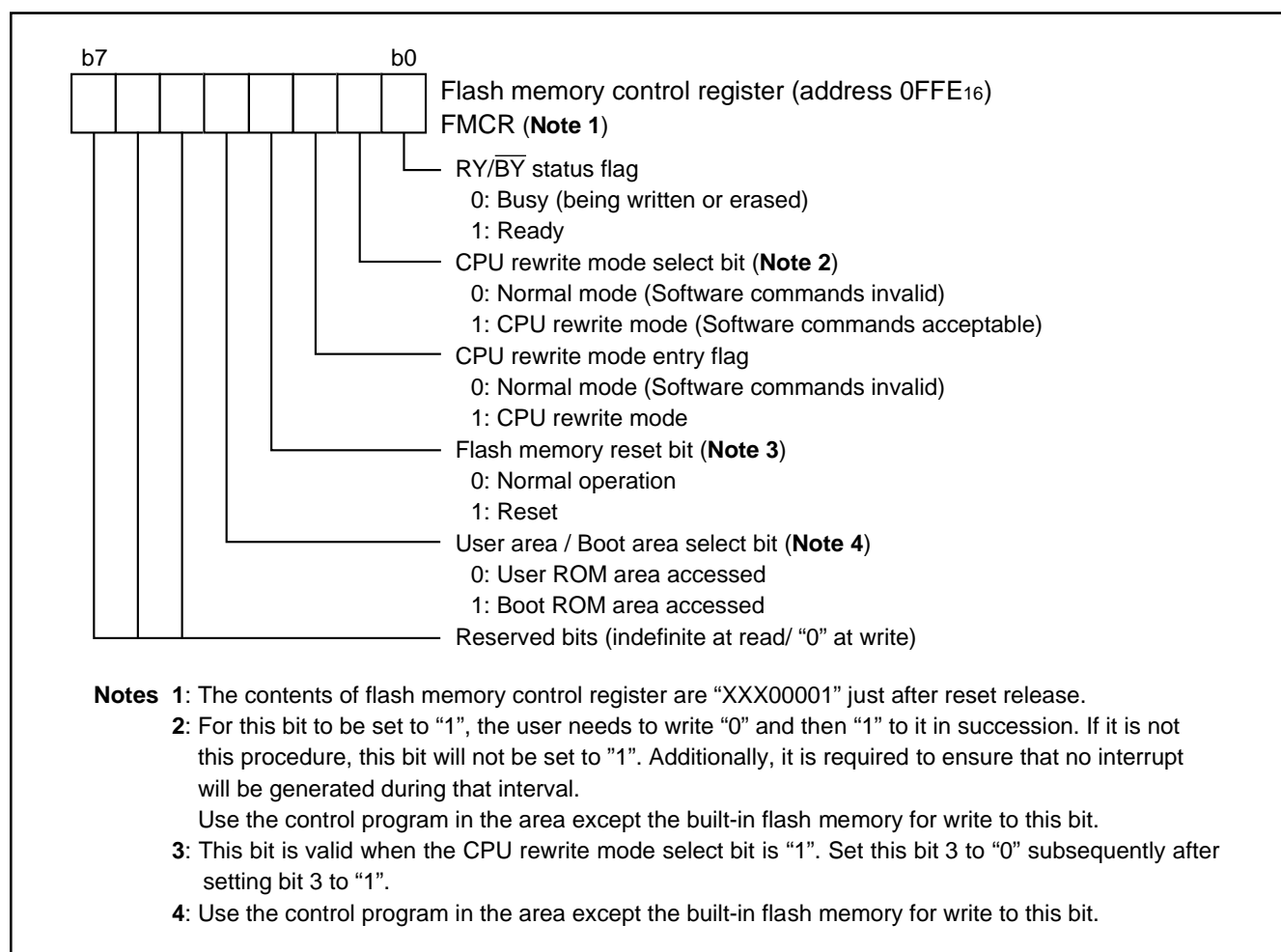
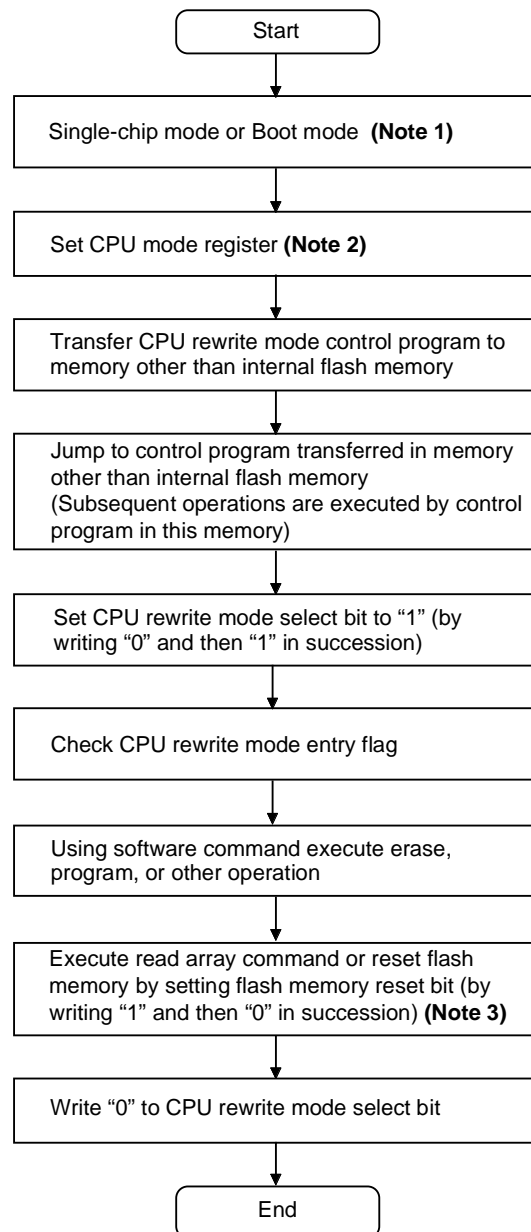


Fig. 117 Structure of flash memory control register



- Notes**
- 1:** When starting the MCU in the single-chip mode or memory expansion mode, supply 4.5 V to 5.25 V to the CNVss pin until checking the CPU rewrite mode entry flag.
 - 2:** Set the system clock division ration selection bits of CPU mode register (bits 6 and 7 at address 003B16).
 - 3:** Before exiting the CPU rewrite mode after completing erase or program operation, always be sure to execute the read array command or reset the flash memory.

Fig. 118 CPU rewrite mode set/release flowchart

HARDWARE

FUNCTIONAL DESCRIPTION

Notes on CPU Rewrite Mode

Take the notes described below when rewriting the flash memory in CPU rewrite mode.

●Operation speed

During CPU rewrite mode, set the internal clock ϕ to 1.5 MHz or less using the system clock division ratio selection bits (bits 6 and 7 of address 003B₁₆).

●Instructions inhibited against use

The instructions which refer to the internal data of the flash memory cannot be used during CPU rewrite mode .

●Interrupts inhibited against use

The interrupts cannot be used during CPU rewrite mode because they refer to the internal data of the flash memory.

●Watchdog timer

If the watchdog timer has been already activated, internal reset due to an underflow will not occur because the watchdog timer is surely cleared during program or erase.

●Reset

Reset is always valid. The MCU is activated using the boot mode at release of reset in the condition of CNVss = "H", so that the program will begin at the address which is stored in addresses FFFC₁₆ and FFFD₁₆ of the boot ROM area.

Software Commands

Table 10 lists the software commands.

After setting the CPU Rewrite Mode Select Bit to "1", write a software command to specify an erase or program operation.

Each software command is explained below.

●Read Array Command (FF₁₆)

The read array mode is entered by writing the command code "FF₁₆" in the first bus cycle. When an address to be read is input in one of the bus cycles that follow, the contents of the specified address are read out at the data bus (D₀ to D₇).

The read array mode is retained intact until another command is written.

●Read Status Register Command (70₁₆)

When the command code "70₁₆" is written in the first bus cycle, the contents of the status register are read out at the data bus (D₀ to D₇) by a read in the second bus cycle.

The status register is explained in the next section.

●Clear Status Register Command (50₁₆)

This command is used to clear the bits SR₄ and SR₅ of the status register after they have been set. These bits indicate that operation has ended in an error. To use this command, write the command code "50₁₆" in the first bus cycle.

●Program Command (40₁₆)

Program operation starts when the command code "40₁₆" is written in the first bus cycle. Then, if the address and data to program are written in the 2nd bus cycle, the control circuit of flash memory (data programming and verification) will start a program.

Whether the write operation is completed can be confirmed by reading the status register or the RY/BY Status Flag. When the program starts, the read status register mode is entered automatically and the contents of the status register is read at the data bus (D₀ to D₇). The status register bit 7 (SR₇) is set to "0" at the same time the write operation starts and is returned to "1" upon completion of the write operation. In this case, the read status register mode remains active until the read array command (FF₁₆) is written.

During the program movement, The RY/BY Status Flag of flash memory control register is set to "0". When the program completes, it becomes "1".

At program end, program results can be checked by reading the status register.

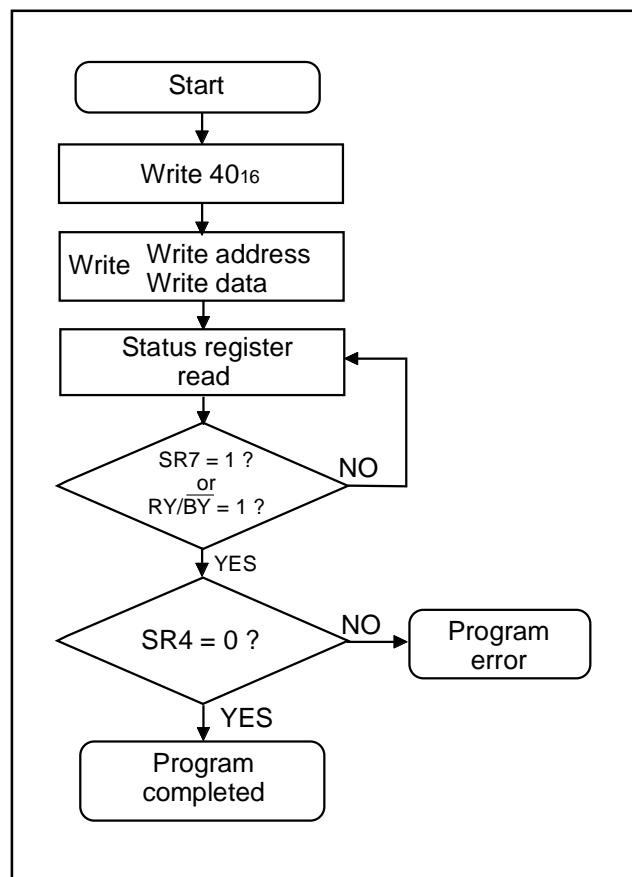


Fig. 119 Program flowchart

Table 10 List of software commands (CPU rewrite mode)

Command	Cycle number	First bus cycle			Second bus cycle		
		Mode	Address	Data (D ₀ to D ₇)	Mode	Address	Data (D ₀ to D ₇)
Read array	1	Write	X (Note 4)	FF ₁₆			
Read status register	2	Write	X	70 ₁₆	Read	X	SRD (Note 1)
Clear status register	1	Write	X	50 ₁₆			
Program	2	Write	X	40 ₁₆	Write	WA (Note 2)	WD (Note 2)
Erase all blocks	2	Write	X	20 ₁₆	Write	X	20 ₁₆
Block erase	2	Write	X	20 ₁₆	Write	BA (Note 3)	D0 ₁₆

Notes 1: SRD = Status Register Data

2: WA = Write Address, WD = Write Data

3: BA = Block Address to be erased (Input the maximum address of each block.)

4: X denotes a given address in the User ROM area .

HARDWARE

FUNCTIONAL DESCRIPTION

●Erase All Blocks Command (20₁₆/20₁₆)

By writing the command code "20₁₆" in the first bus cycle and the confirmation command code "20₁₆" in the second bus cycle that follows, the operation of erase all blocks (erase and erase verify) starts.

Whether the erase all blocks command is terminated can be confirmed by reading the status register or the RY/B \bar{Y} Status Flag of flash memory control register. When the erase all blocks operation starts, the read status register mode is entered automatically and the contents of the status register can be read out at the data bus (D₀ to D₇). The status register bit 7 (SR7) is set to "0" at the same time the erase operation starts and is returned to "1" upon completion of the erase operation. In this case, the read status register mode remains active until the read array command (FF₁₆) is written.

The RY/B \bar{Y} Status Flag is "0" during erase operation and "1" when the erase operation is completed as is the status register bit 7.

After the erase all blocks end, erase results can be checked by reading the status register. For details, refer to the section where the status register is detailed.

●Block Erase Command (20₁₆/D0₁₆)

By writing the command code "20₁₆" in the first bus cycle and the confirmation command code "D0₁₆" and the block address in the second bus cycle that follows, the block erase (erase and erase verify) operation starts for the block address of the flash memory to be specified.

Whether the block erase operation is completed can be confirmed by reading the status register or the RY/B \bar{Y} Status Flag of flash memory control register. At the same time the block erase operation starts, the read status register mode is automatically entered, so that the contents of the status register can be read out. The status register bit 7 (SR7) is set to "0" at the same time the block erase operation starts and is returned to "1" upon completion of the block erase operation. In this case, the read status register mode remains active until the read array command (FF₁₆) is written.

The RY/B \bar{Y} Status Flag is "0" during block erase operation and "1" when the block erase operation is completed as is the status register bit 7.

After the block erase ends, erase results can be checked by reading the status register. For details, refer to the section where the status register is detailed.

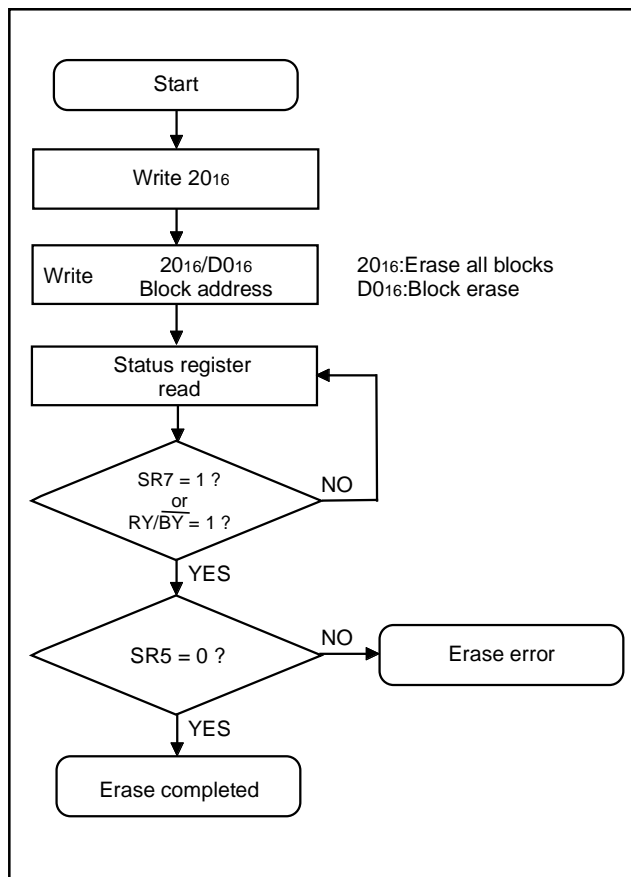


Fig. 120 Erase flowchart

Status Register (SRD)

The status register shows the operating status of the flash memory and whether erase operations and programs ended successfully or in error. It can be read in the following ways:

- (1) By reading an arbitrary address from the User ROM area after writing the read status register command (70₁₆)
- (2) By reading an arbitrary address from the User ROM area in the period from when the program starts or erase operation starts to when the read array command (FF₁₆) is input.

Also, the status register can be cleared by writing the clear status register command (50₁₆).

After reset, the status register is set to "80₁₆".

Table 11 shows the status register. Each bit in this register is explained below.

•Sequencer status (SR7)

The sequencer status indicates the operating status of the flash memory. This bit is set to "0" (busy) during write or erase operation and is set to "1" when these operations ends.

After power-on, the sequencer status is set to "1" (ready).

•Erase status (SR5)

The erase status indicates the operating status of erase operation. If an erase error occurs, it is set to "1". When the erase status is cleared, it is set to "0".

•Program status (SR4)

The program status indicates the operating status of write operation. When a write error occurs, it is set to "1".

The program status is set to "0" when it is cleared.

If "1" is written for any of the SR5 and SR4 bits, the program, erase all blocks, and block erase commands are not accepted. Before executing these commands, execute the clear status register command (50₁₆) and clear the status register.

Table 11 Definition of each bit in status register

Each bit of SRD0 bits	Status name	Definition	
		"1"	"0"
SR7 (bit7)	Sequencer status	Ready	Busy
SR6 (bit6)	Reserved	-	-
SR5 (bit5)	Erase status	Terminated in error	Terminated normally
SR4 (bit4)	Program status	Terminated in error	Terminated normally
SR3 (bit3)	Reserved	-	-
SR2 (bit2)	Reserved	-	-
SR1 (bit1)	Reserved	-	-
SR0 (bit0)	Reserved	-	-

HARDWARE

FUNCTIONAL DESCRIPTION

Full Status Check

By performing full status check, it is possible to know the execution results of erase and program operations. Figure 121 shows a full status check flowchart and the action to be taken when each error occurs.

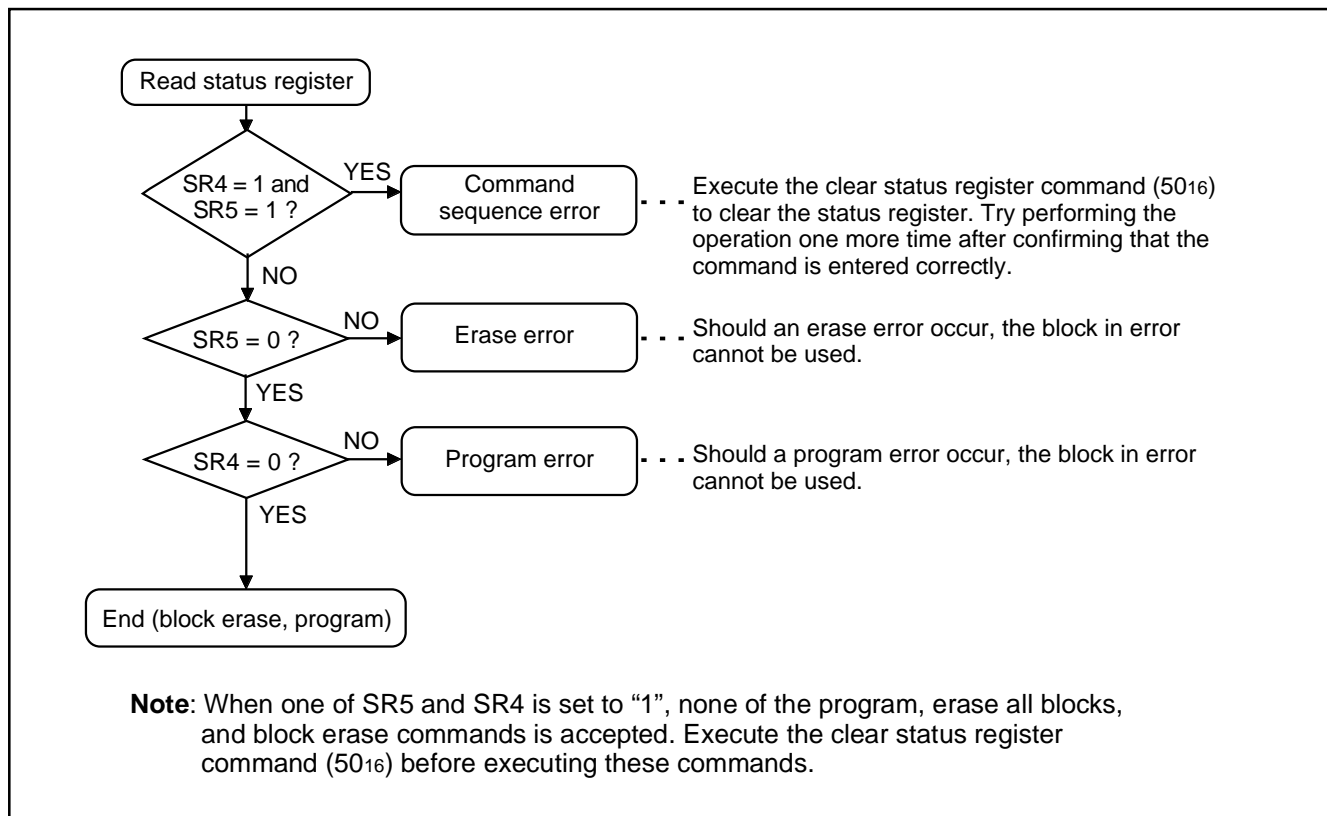


Fig. 121 Full status check flowchart and remedial procedure for errors

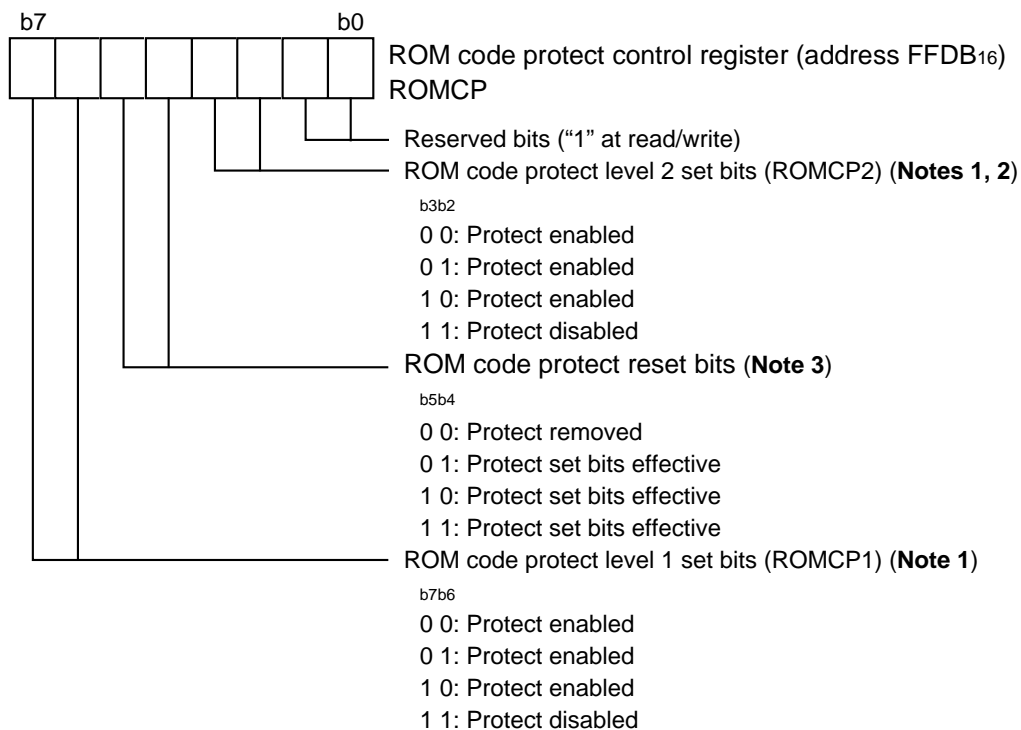
Functions To Inhibit Rewriting Flash Memory Version

To prevent the contents of internal flash memory from being read out or rewritten easily, this MCU incorporates a ROM code protect function for use in parallel I/O mode and an ID code check function for use in standard serial I/O mode.

●ROM Code Protect Function

The ROM code protect function is the function to inhibit reading out or modifying the contents of internal flash memory by using the ROM code protect control register (address FFDB₁₆) in parallel I/O mode. Figure 122 shows the ROM code protect control register (address FFDB₁₆). (This address exists in the User ROM area.)

If one or both of the pair of ROM Code Protect Bits is set to "0", the ROM code protect is turned on, so that the contents of internal flash memory are protected against readout and modification. The ROM code protect is implemented in two levels. If level 2 is selected, the flash memory is protected even against readout by a shipment inspection LSI tester, etc. When an attempt is made to select both level 1 and level 2, level 2 is selected by default. If both of the two ROM Code Protect Reset Bits are set to "00", the ROM code protect is turned off, so that the contents of internal flash memory can be read out or modified. Once the ROM code protect is turned on, the contents of the ROM Code Protect Reset Bits cannot be modified in parallel I/O mode. Use the serial I/O or CPU rewrite mode to rewrite the contents of the ROM Code Protect Reset Bits.



- Notes**
- 1:** When ROM code protect is turned on, the internal flash memory is protected against readout or modification in parallel I/O mode.
 - 2:** When ROM code protect level 2 is turned on, ROM code readout by a shipment inspection LSI tester, etc. also is inhibited.
 - 3:** The ROM code protect reset bits can be used to turn off ROM code protect level 1 and ROM code protect level 2. However, since these bits cannot be modified in parallel I/O mode, they need to be rewritten in serial I/O mode or CPU rewrite mode.

Fig. 122 Structure of ROM code protect control register

HARDWARE

FUNCTIONAL DESCRIPTION

ID Code Check Function

Use this function in standard serial I/O mode. When the contents of the flash memory are not blank, the ID code sent from the programmer is compared with the ID code written in the flash memory to see if they match. If the ID codes do not match, the commands sent from the programmer are not accepted. The ID code consists of 8-bit data, and its areas are FFD4₁₆ to FFDA₁₆. Write a program which has had the ID code preset at these addresses to the flash memory.

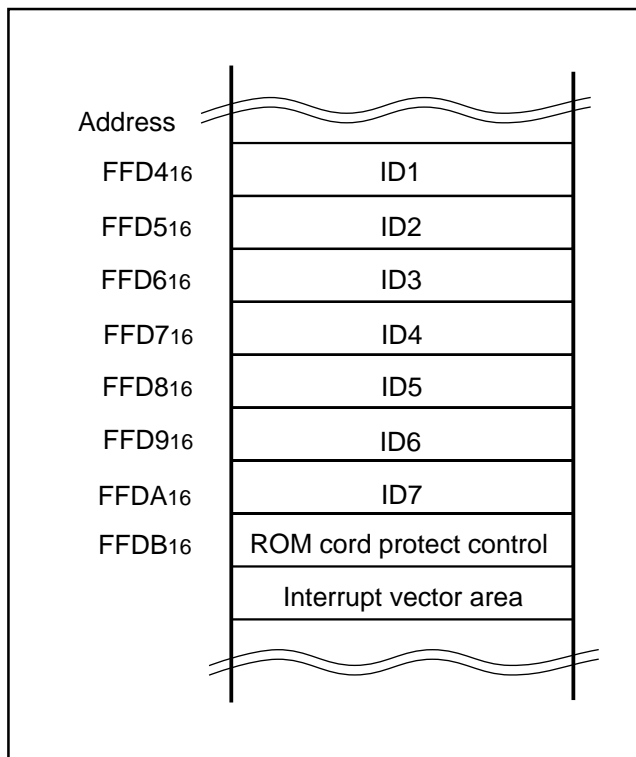


Fig. 123 ID code store addresses

(2) Parallel I/O Mode

Parallel I/O mode is the mode which parallel output and input software command, address, and data required for the operations (read, program, erase, etc.) to a built-in flash memory. Use the exclusive external equipment flash programmer which supports the 38K0 Group (flash memory version). Refer to each programmer maker's handling manual for the details of the usage.

User ROM and Boot ROM Areas

In parallel I/O mode, the user ROM and boot ROM areas shown in Figure 116 can be rewritten. Both areas of flash memory can be operated on in the same way.

The boot ROM area is 4 Kbytes in size. It is located at addresses F000₁₆ through FFFF₁₆. Make sure program and block erase operations are always performed within this address range. (Access to any location outside this address range is prohibited.)

In the Boot ROM area, an erase block operation is applied to only one 4 Kbyte block.

The boot ROM area has had a standard serial I/O mode control program stored in it when shipped from the Mitsubishi factory. Therefore, using the device in standard serial I/O mode, you must perform program and block erase in the user ROM area.

HARDWARE

FUNCTIONAL DESCRIPTION

(3) Standard Serial I/O Mode

The standard serial I/O mode inputs and outputs the software commands, addresses and data needed to operate (read, program, erase, etc.) the internal flash memory. This I/O is clock synchronized serial. This mode requires a purpose-specific peripheral unit. The standard serial I/O mode is different from the parallel I/O mode in that the CPU controls flash memory rewrite (uses the CPU rewrite mode), rewrite data input and so forth. The standard serial I/O mode is started by connecting "H" to the P16 (CE) pin and "H" to the P42 (SCLK) pin and "H" to the CNVSS (VPP) pin (apply 4.5 V to 5.25 V to Vpp from an external source), and releasing the reset operation. (In the ordinary microcomputer mode, set CNVss pin to "L" level.)

This control program is written in the Boot ROM area when the product is shipped from Mitsubishi. Accordingly, make note of the fact that the standard serial I/O mode cannot be used if the Boot ROM area is rewritten in parallel I/O mode. Figure 124 shows the pin connections for the standard serial I/O mode.

In standard serial I/O mode, serial data I/O uses the four serial I/O pins SCLK, RxD, TxD and SRDY (BUSY). The SCLK pin is the transfer clock input pin through which an external transfer clock is input. The TxD pin is for CMOS output. The SRDY (BUSY) pin outputs "L" level when ready for reception and "H" level when reception starts.

Serial data I/O is transferred serially in 8-bit units.

In standard serial I/O mode, only the User ROM area shown in Figure 116 can be rewritten. The Boot ROM area cannot.

In standard serial I/O mode, a 7-byte ID code is used. When there is data in the flash memory, commands sent from the peripheral unit (programmer) are not accepted unless the ID code matches.

Outline Performance (Standard Serial I/O Mode)

In standard serial I/O mode, software commands, addresses and data are input and output between the MCU and peripheral units (serial programmer, etc.) using 4-wire clock-synchronized serial I/O. In reception, software commands, addresses and program data are synchronized with the rise of the transfer clock that is input to the SCLK pin, and are then input to the MCU via the RxD pin. In transmission, the read data and status are synchronized with the fall of the transfer clock, and output from the TxD pin.

The TxD pin is for CMOS output. Transfer is in 8-bit units with LSB first.

When busy, such as during transmission, reception, erasing or program execution, the SRDY (BUSY) pin is "H" level. Accordingly, always start the next transfer after the SRDY (BUSY) pin is "L" level.

Also, data and status registers in a memory can be read after inputting software commands. Status, such as the operating state of the flash memory or whether a program or erase operation ended successfully or not, can be checked by reading the status register. Here following explains software commands, status registers, etc.

Table 12 Description of pin function (Standard Serial I/O Mode)

Pin name	Signal name	I/O	Function
VCC,VSS	Power supply		Apply 4.00 to 5.25 V (Standard) or 3.00 to 5.25 V (L version) to the Vcc pin and 0 V to the Vss pin.
VCC_E	Power supply		Connect this pin to Vcc.
CNVSS	VPP	I	Connect this pin to VPP (VPP = 4.50 to 5.25 V).
CNVSS2	CNVSS2	I	Connect this pin to Vss.
VREF	Analog reference voltage	I	Connect this pin to Vcc when not using.
DVCC, PVCC	Analog power supply		Connect this pin to Vcc.
PVSS	Analog power supply		Connect this pin to Vss.
RESET	Reset input	I	To reset, input "L" level for 20 cycles or longer clocks of ϕ .
XIN	Clock input	I	Connect a ceramic or crystal resonator between the XIN and XOUT pins. When entering an externally driven clock, enter it from XIN and leave XOUT open.
XOUT	Clock output	O	
USBVREF	USB reference voltage input		Connect this pin to Vcc when not using.
TrON	USB reference voltage output	O	Leave this pin open when not using.
D0+,D0-	USB upstream input	I/O	Input "L" level when not using.
P00 to P07	Input port P0	I	Input "L" or "H" level, or keep open.
P10 to P15	Input port P1	I	Input "L" or "H" level, or keep open.
P16	Input port P1	I	Input "L" or "H" level, or keep open. Input "H" level only at release of reset.
P17	Input port P1	I	Input "L" or "H" level, or keep open.
P20 to P27	Input port P2	I	Input "L" or "H" level, or keep open.
P30 to P37	Input port P3	I	Input "L" or "H" level, or keep open.
P40	RxD input	I	This is a serial data input pin.
P41	TxD output	O	This is a serial data output pin.
P42	SCLK input	I	This is a serial clock input pin. Input "H" level only at release of reset.
P43	BUSY output	O	This is a BUSY output pin.
P50 to P57	Input port P5	I	Input "L" or "H" level, or keep open.
P60 to P63	Input port P6	I	Input "L" or "H" level, or keep open.

HARDWARE

FUNCTIONAL DESCRIPTION

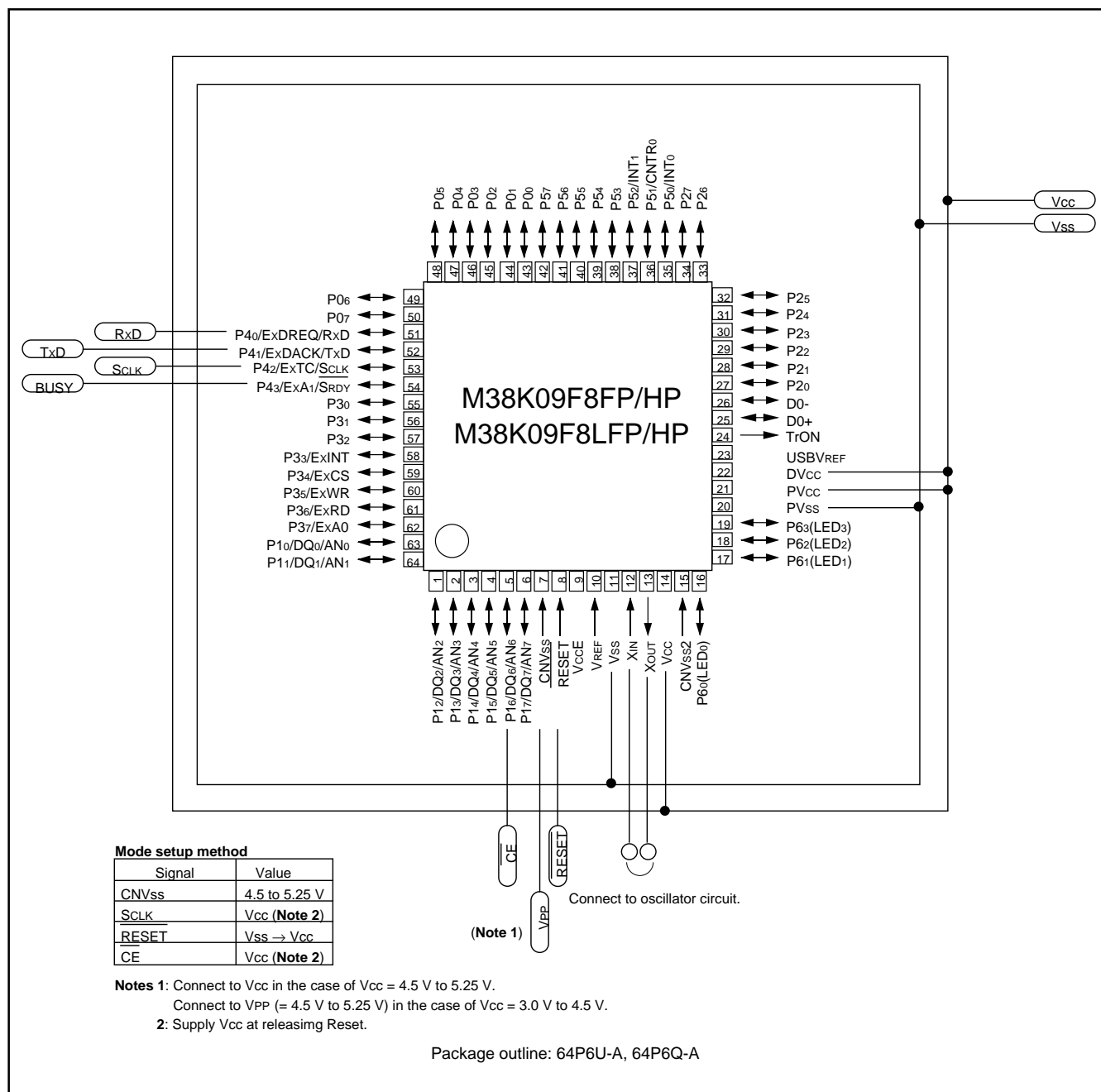


Fig. 124 Pin connection diagram in standard serial I/O mode (1)

Software Commands

Table 13 lists software commands. In standard serial I/O mode, erase, program and read are controlled by transferring software commands via the RxD pin. Software commands are explained

here below. Basically, the software commands of the standard serial I/O mode are the same as that of the parallel I/O mode, but the block erase function is excluded, and 4 commands are added: ID check, download, version data output and Boot ROM area output functions.

Table 13 Software commands (Standard serial I/O mode)

Control command	1st byte transfer	2nd byte	3rd byte	4th byte	5th byte	6th byte	When ID is not verified
1 Page read	FF ₁₆	Address (middle)	Address (high)	Data output	Data output	Data output	Data output to 259th byte	Not acceptable
2 Page program	41 ₁₆	Address (middle)	Address (high)	Data input	Data input	Data input	Data input to 259th byte	Not acceptable
3 Erase all blocks	A7 ₁₆	D0 ₁₆						Not acceptable
4 Read status register	70 ₁₆	SRD output	SRD1 output					Acceptable
5 Clear status register	50 ₁₆							Not acceptable
6 ID check function	F5 ₁₆	Address (low)	Address (middle)	Address (high)	ID size	ID1	To ID7	Acceptable
7 Download function	FA ₁₆	Size (low)	Size (high)	Check-sum	Data input	To required number of times		Not acceptable
8 Version data output function	FB ₁₆	Version data output	Version data output	Version data output	Version data output	Version data output	Version data output to 9th byte	Acceptable
9 Boot ROM area output function	FC ₁₆	Address (middle)	Address (high)	Data output	Data output	Data output	Data output to 259th byte	Not acceptable

Notes1: Shading indicates transfer from the internal flash memory microcomputer to a programmer. All other data is transferred from a programmer to the internal flash memory microcomputer.

2: SRD refers to status register data. SRD1 refers to status register 1 data.

3: All commands can be accepted when the flash memory is totally blank.

4: Address low is A0 to A7; Address middle is A8 to A15; Address high is A16 to A23. Address-high A16 to A23 are always "0016".

HARDWARE

FUNCTIONAL DESCRIPTION

The contents of software commands are explained as follows.

●Page Read Command

This command reads the specified page (256 bytes) in the flash memory sequentially one byte at a time. Execute the page read command as explained here following.

- (1) Transfer the “FF16” command code with the 1st byte.
- (2) Transfer addresses A8 to A15 and A16 to A23 with the 2nd and 3rd bytes respectively.
- (3) From the 4th byte onward, data (D0 to D7) for the page (256 bytes) specified with addresses A8 to A23 will be output sequentially from the smallest address first synchronized with the fall of the clock.

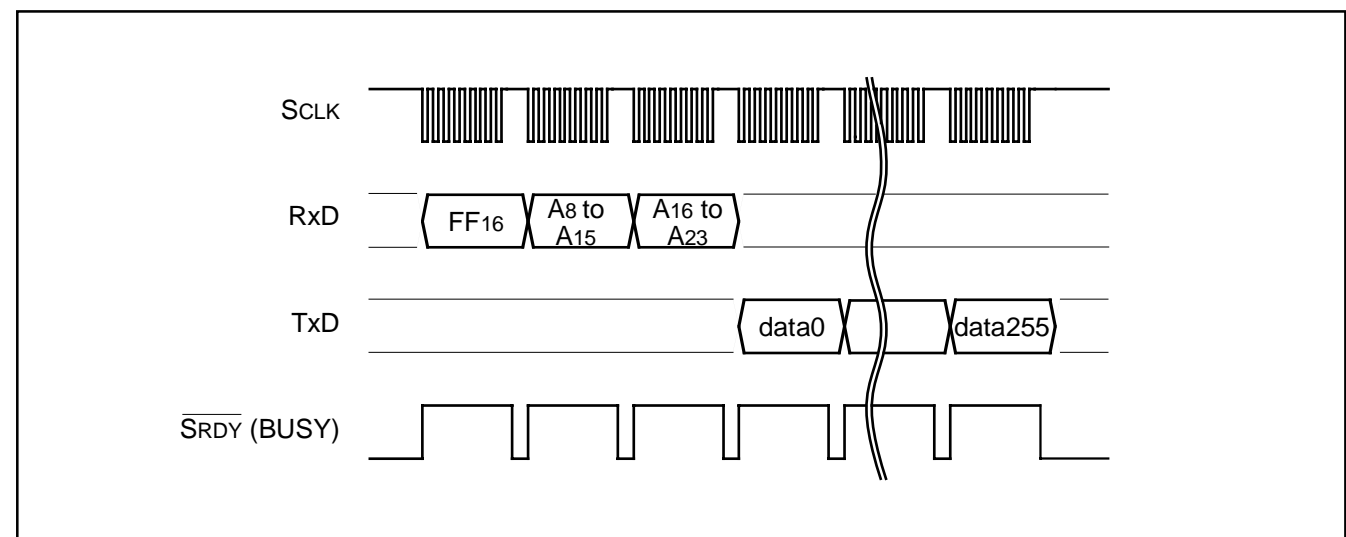


Fig. 125 Timing for page read

●Read Status Register Command

This command reads status information. When the “7016” command code is transferred with the 1st byte, the contents of the status register (SRD) with the 2nd byte and the contents of status register 1 (SRD1) with the 3rd byte are read.

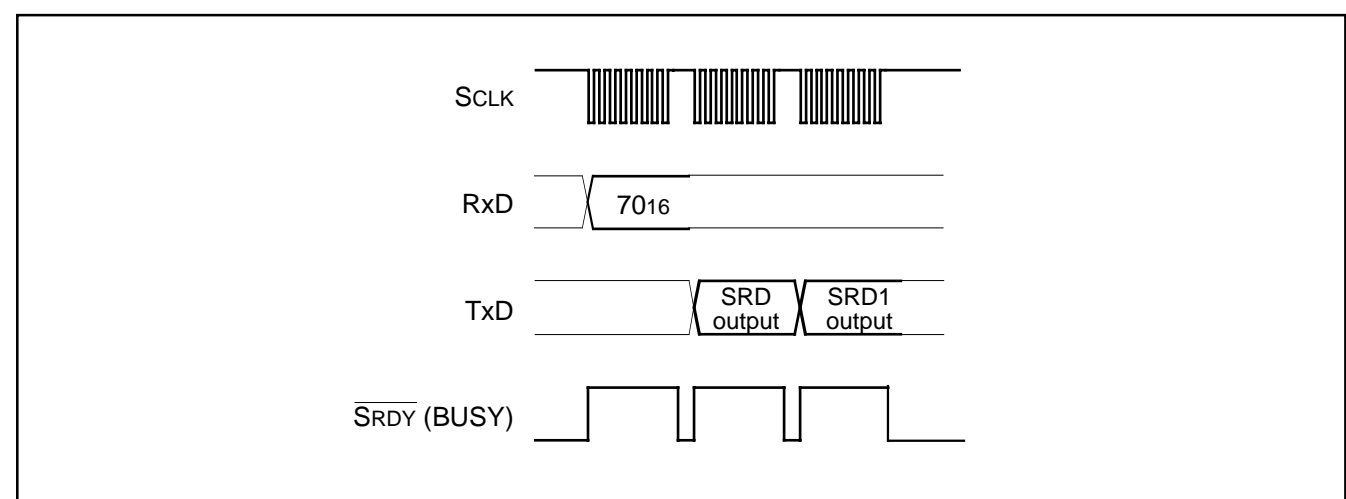


Fig. 126 Timing for reading status register

●Clear Status Register Command

This command clears the bits (SR3 to SR5) which are set when the status register operation ends in error. When the "5016" command code is sent with the 1st byte, the aforementioned bits are cleared. When the clear status register operation ends, the $\overline{\text{SRDY}}$ (BUSY) signal changes from "H" to "L" level.

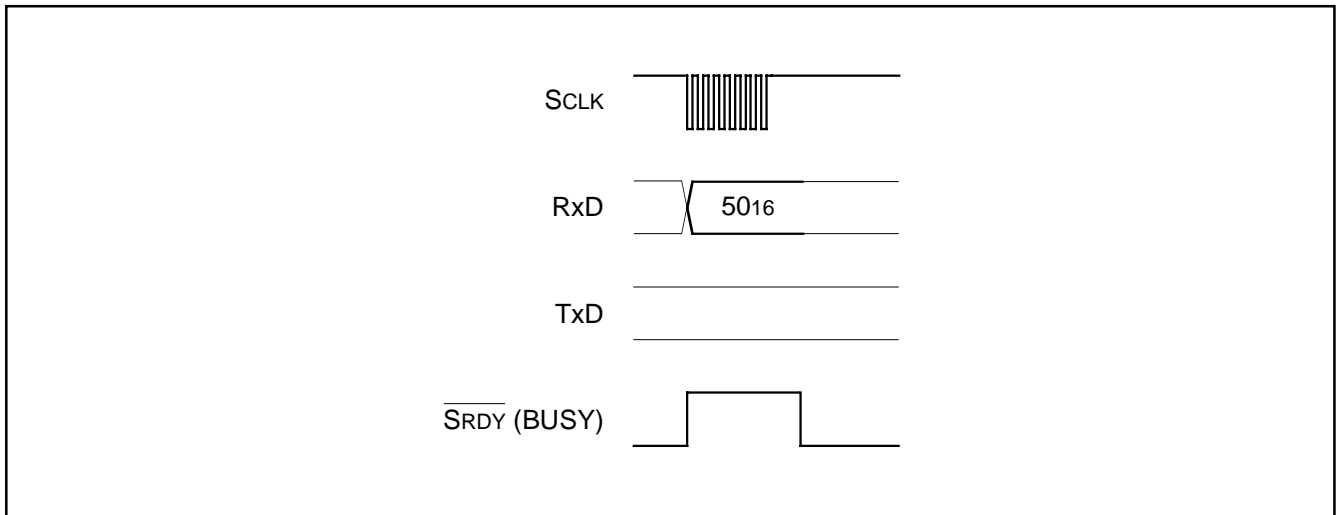


Fig. 127 Timing for clear status register

●Page Program Command

This command writes the specified page (256 bytes) in the flash memory sequentially one byte at a time. Execute the page program command as explained here following.

- (1) Transfer the "4116" command code with the 1st byte.
- (2) Transfer addresses A8 to A15 and A16 to A23 with the 2nd and 3rd bytes respectively.

- (3) From the 4th byte onward, as write data (D0 to D7) for the page (256 bytes) specified with addresses A8 to A23 is input sequentially from the smallest address first, that page is automatically written.

When reception setup for the next 256 bytes ends, the $\overline{\text{SRDY}}$ (BUSY) signal changes from "H" to "L" level. The result of the page program can be known by reading the status register. For more information, see the section on the status register.

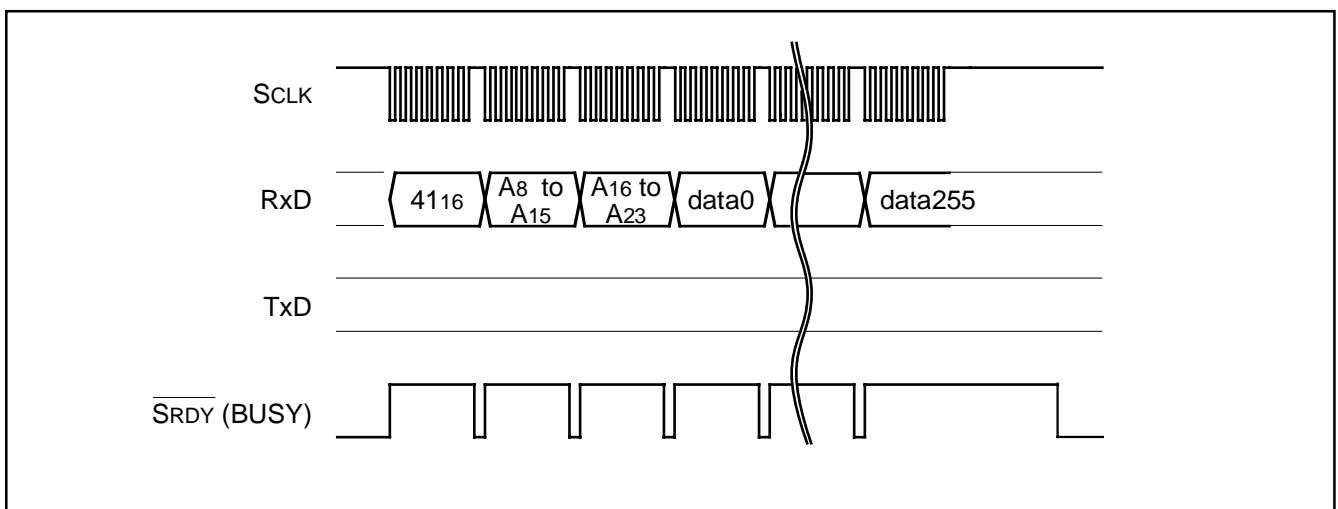


Fig. 128 Timing for page program

HARDWARE

FUNCTIONAL DESCRIPTION

●Erase All Blocks Command

This command erases the contents of all blocks. Execute the erase all blocks command as explained here following.

- (1) Transfer the "A716" command code with the 1st byte.
- (2) Transfer the verify command code "D016" with the 2nd byte.

With the verify command code, the erase operation will start and continue for all blocks in the flash memory.

When erase all blocks end, the $\overline{\text{SRDY}}$ (BUSY) signal changes from "H" to "L" level. The result of the erase operation can be known by reading the status register.

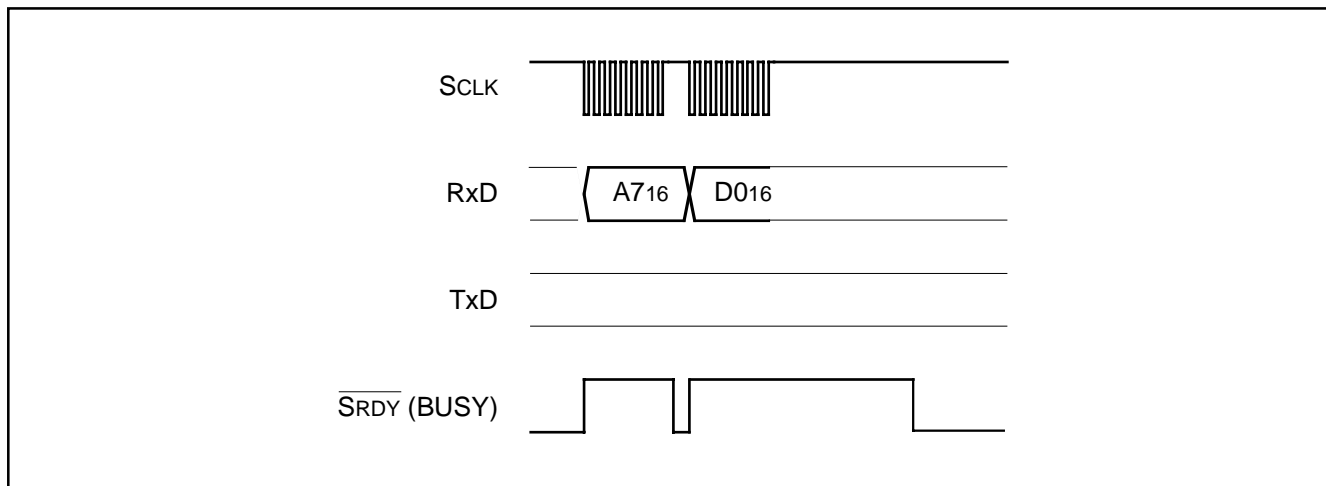


Fig. 129 Timing for erase all blocks

●Download Command

This command downloads a program to the RAM for execution.

Execute the download command as explained here following.

- (1) Transfer the "FA16" command code with the 1st byte.
- (2) Transfer the program size with the 2nd and 3rd bytes.
- (3) Transfer the check sum with the 4th byte. The check sum is added to all data sent with the 5th byte onward.
- (4) The program to execute is sent with the 5th byte onward.

When all data has been transmitted, if the check sum matches, the downloaded program is executed. The size of the program will vary according to the internal RAM.

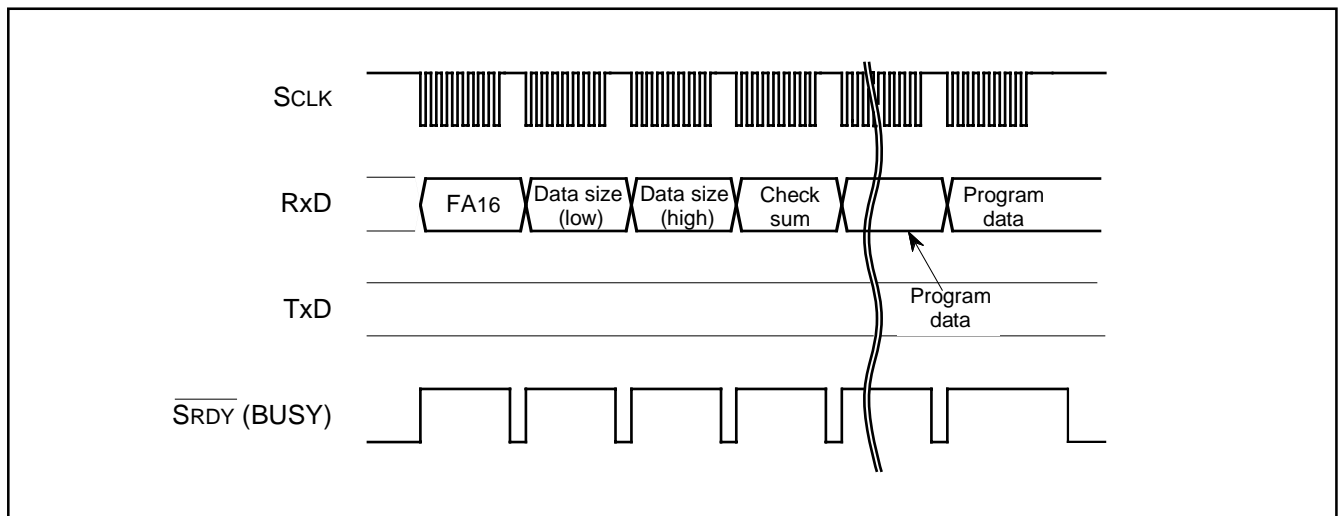


Fig. 130 Timing for download

HARDWARE

FUNCTIONAL DESCRIPTION

●Version Information Output Command

This command outputs the version information of the control program stored in the Boot ROM area. Execute the version information output command as explained here following.

- (1) Transfer the "FB16" command code with the 1st byte.
- (2) The version information will be output from the 2nd byte onward.

This data is composed of 8 ASCII code characters.

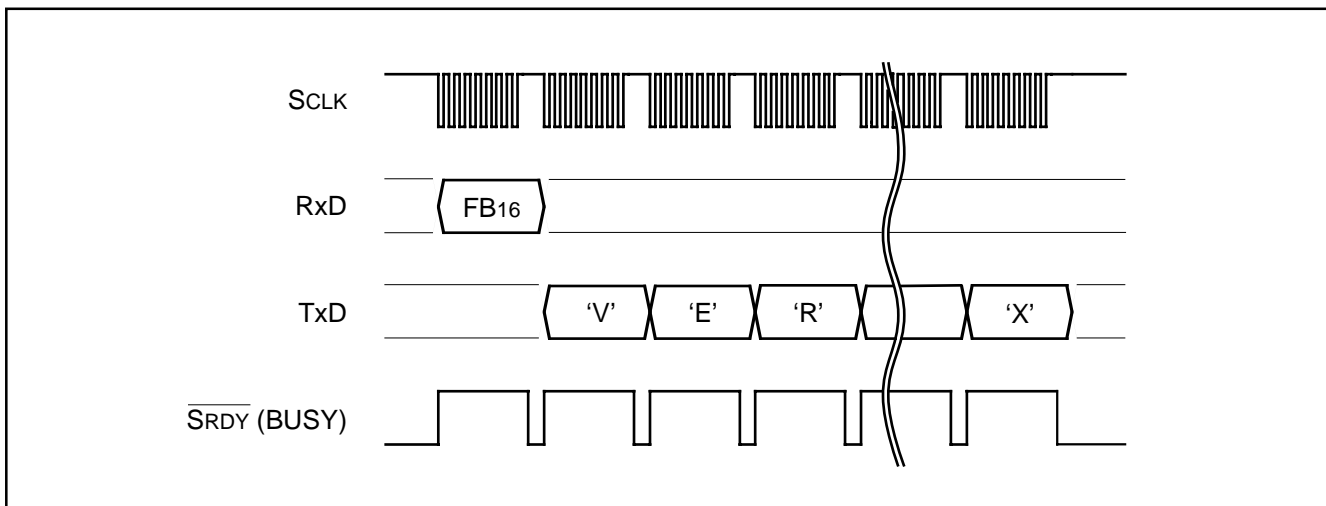


Fig. 131 Timing for version information output

●Boot ROM Area Output Command

This command reads the control program stored in the Boot ROM area in page (256 bytes) unit. Execute the Boot ROM area output command as explained here following.

- (1) Transfer the "FC16" command code with the 1st byte.
- (2) Transfer addresses A8 to A15 and A16 to A23 with the 2nd and 3rd bytes respectively.
- (3) From the 4th byte onward, data (D0 to D7) for the page (256 bytes) specified with addresses A8 to A23 will be output sequentially from the smallest address first synchronized with the fall of the clock.

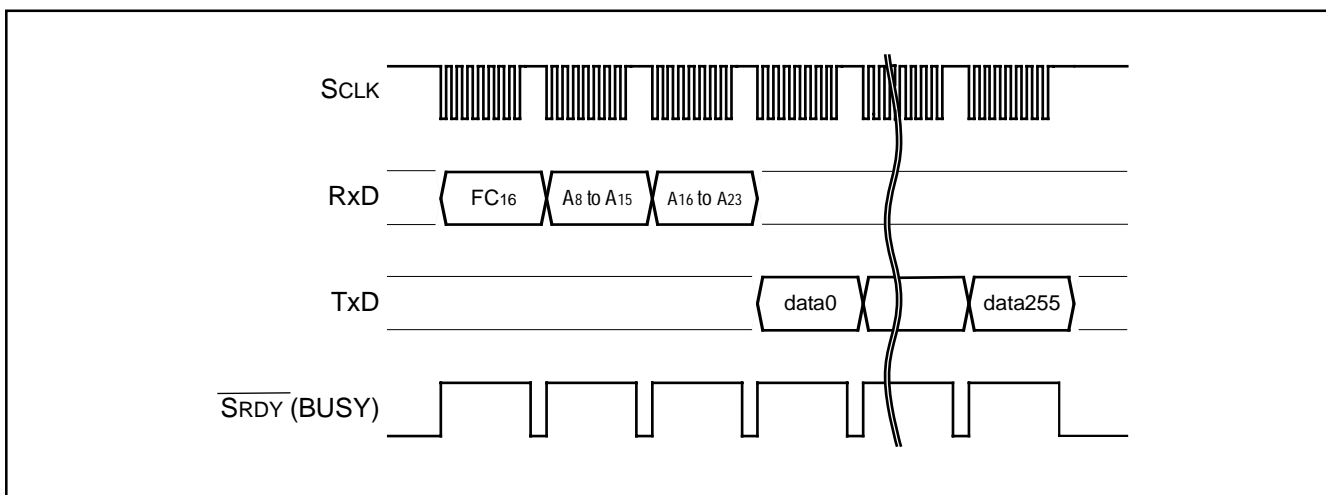


Fig. 132 Timing for Boot ROM area output

●ID Check

This command checks the ID code. Execute the boot ID check command as explained here following.

- (1) Transfer the “F5₁₆” command code with the 1st byte.
- (2) Transfer addresses A0 to A7, A8 to A15 and A16 to A23 (“00₁₆”) of the 1st byte of the ID code with the 2nd, 3rd and 4th respectively.
- (3) Transfer the number of data sets of the ID code with the 5th byte.
- (4) Transfer the ID code with the 6th byte onward, starting with the 1st byte of the code.

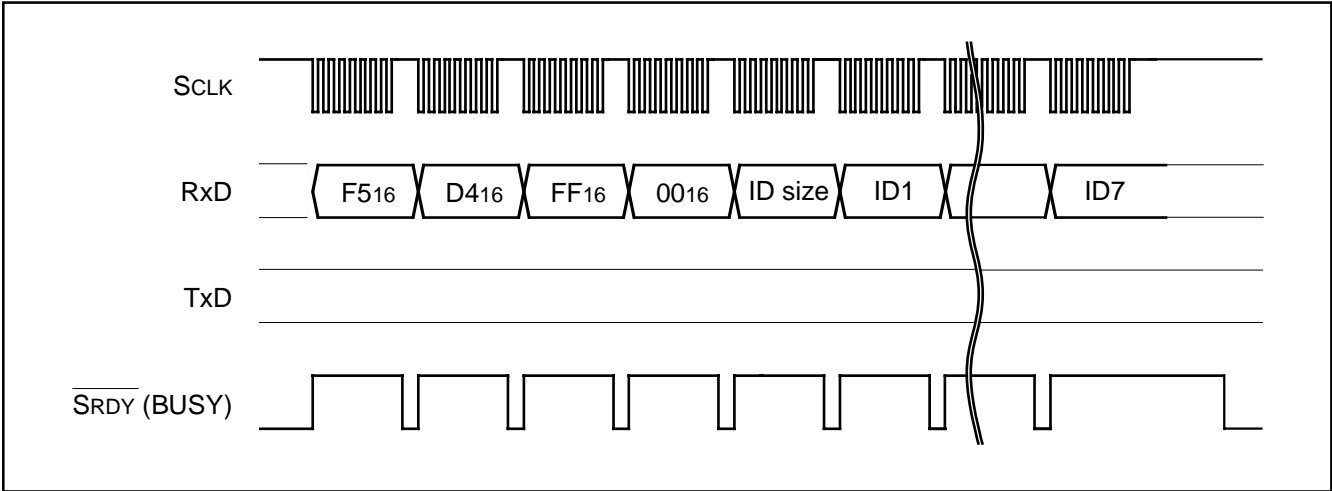


Fig. 133 Timing for ID check

●ID Code

When the flash memory is not blank, the ID code sent from the serial programmer and the ID code written in the flash memory are compared to see if they match. If the codes do not match, the command sent from the serial programmer is not accepted. An ID code contains 8 bits of data. Area is, from the 1st byte, addresses FFD4₁₆ to FFDA₁₆. Write a program into the flash memory, which already has the ID code set for these addresses.

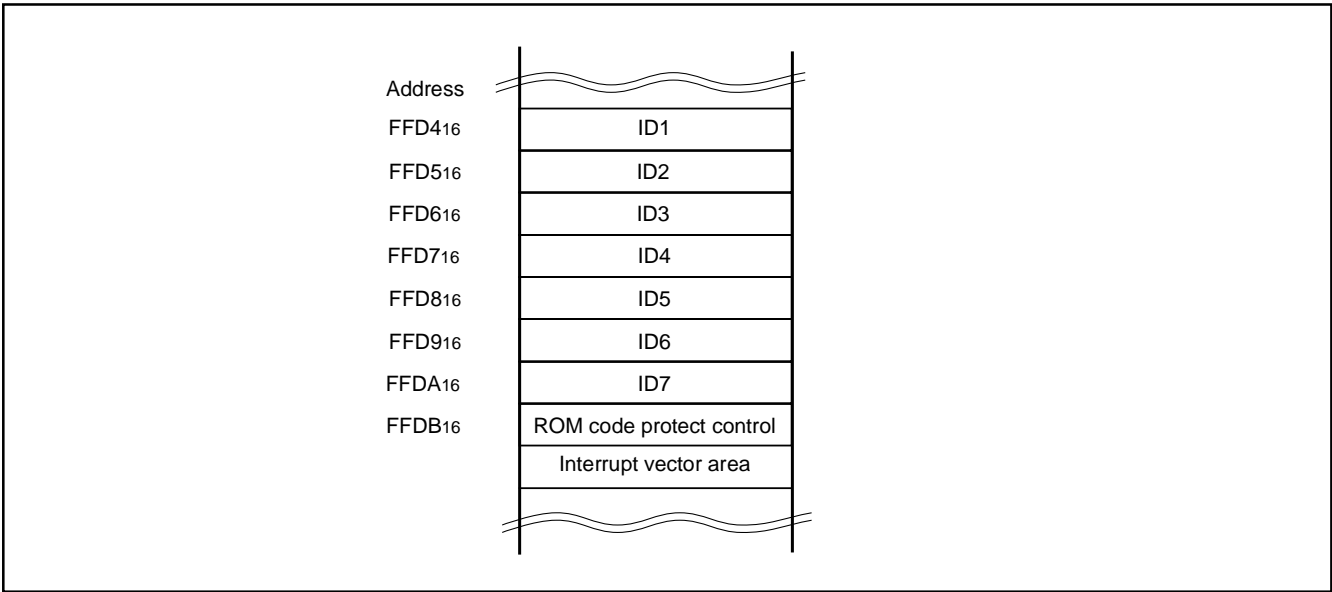


Fig. 134 ID code storage addresses

HARDWARE

FUNCTIONAL DESCRIPTION

●Status Register (SRD)

The status register indicates operating status of the flash memory and status such as whether an erase operation or a program ended successfully or in error. It can be read by writing the read status register command (70₁₆). Also, the status register is cleared by writing the clear status register command (50₁₆).

Table 14 lists the definition of each status register bit. After releasing the reset, the status register becomes "80₁₆".

•Sequencer status (SR7)

The sequencer status indicates the operating status of the flash memory.

After power-on and recover from deep power down mode, the sequencer status is set to "1" (ready).

This status bit is set to "0" (busy) during write or erase operation and is set to "1" upon completion of these operations.

•Erase status (SR5)

The erase status indicates the operating status of erase operation. If an erase error occurs, it is set to "1". When the erase status is cleared, it is set to "0".

•Program status (SR4)

The program status indicates the operating status of write operation. If a write error occurs, it is set to "1". When the program status is cleared, it is set to "0".

Table 14 Status register (SRD)

SRD0 bits	Status name	Definition	
		"1"	"0"
SR7 (bit7)	Sequencer status	Ready	Busy
SR6 (bit6)	Reserved	-	-
SR5 (bit5)	Erase status	Terminated in error	Terminated normally
SR4 (bit4)	Program status	Terminated in error	Terminated normally
SR3 (bit3)	Reserved	-	-
SR2 (bit2)	Reserved	-	-
SR1 (bit1)	Reserved	-	-
SR0 (bit0)	Reserved	-	-

●Status Register 1 (SRD1)

The status register 1 indicates the status of serial communications, results from ID checks and results from check sum comparisons. It can be read after the SRD by writing the read status register command (70₁₆). Also, status register 1 is cleared by writing the clear status register command (50₁₆).

Table 15 lists the definition of each status register 1 bit. This register becomes "00₁₆" when power is turned on and the flag status is maintained even after the reset.

•Boot update completed bit (SR15)

This flag indicates whether the control program was downloaded to the RAM or not, using the download function.

•Check sum consistency bit (SR12)

This flag indicates whether the check sum matches or not when a program, is downloaded for execution using the download function.

•ID check completed bits (SR11 and SR10)

These flags indicate the result of ID checks. Some commands cannot be accepted without an ID check.

•Data reception time out (SR9)

This flag indicates when a time out error is generated during data reception. If this flag is attached during data reception, the received data is discarded and the MCU returns to the command wait state.

Table 15 Status register 1 (SRD1)

SRD1 bits	Status name	Definition	
		"1"	"0"
SR15 (bit7)	Boot update completed bit	Update completed	Not Update
SR14 (bit6)	Reserved	-	-
SR13 (bit5)	Reserved	-	-
SR12 (bit4)	Checksum match bit	Match	Mismatch
SR11 (bit3)	ID check completed bits	00	Not verified
SR10 (bit2)		01	Verification mismatch
		10	Reserved
		11	Verified
SR9 (bit1)	Data reception time out	Time out	Normal operation
SR8 (bit0)	Reserved	-	-

HARDWARE

FUNCTIONAL DESCRIPTION

Full Status Check

Results from executed erase and program operations can be known by running a full status check. Figure 135 shows a flow-chart of the full status check and explains how to remedy errors which occur.

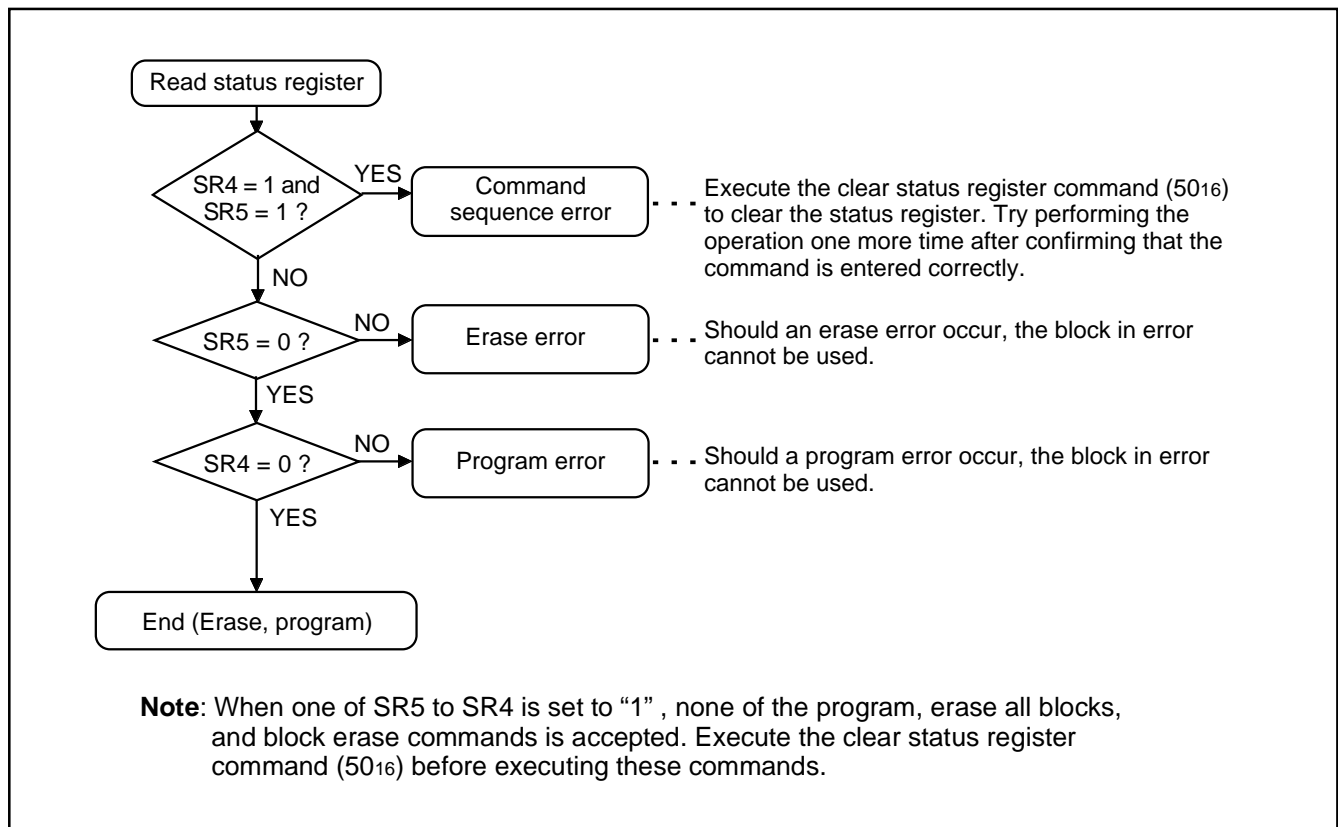


Fig. 135 Full status check flowchart and remedial procedure for errors

Example Circuit Application for Standard Serial I/O Mode

Figure 136 shows a circuit application for the standard serial I/O mode. Control pins will vary according to a programmer, therefore see a programmer manual for more information.

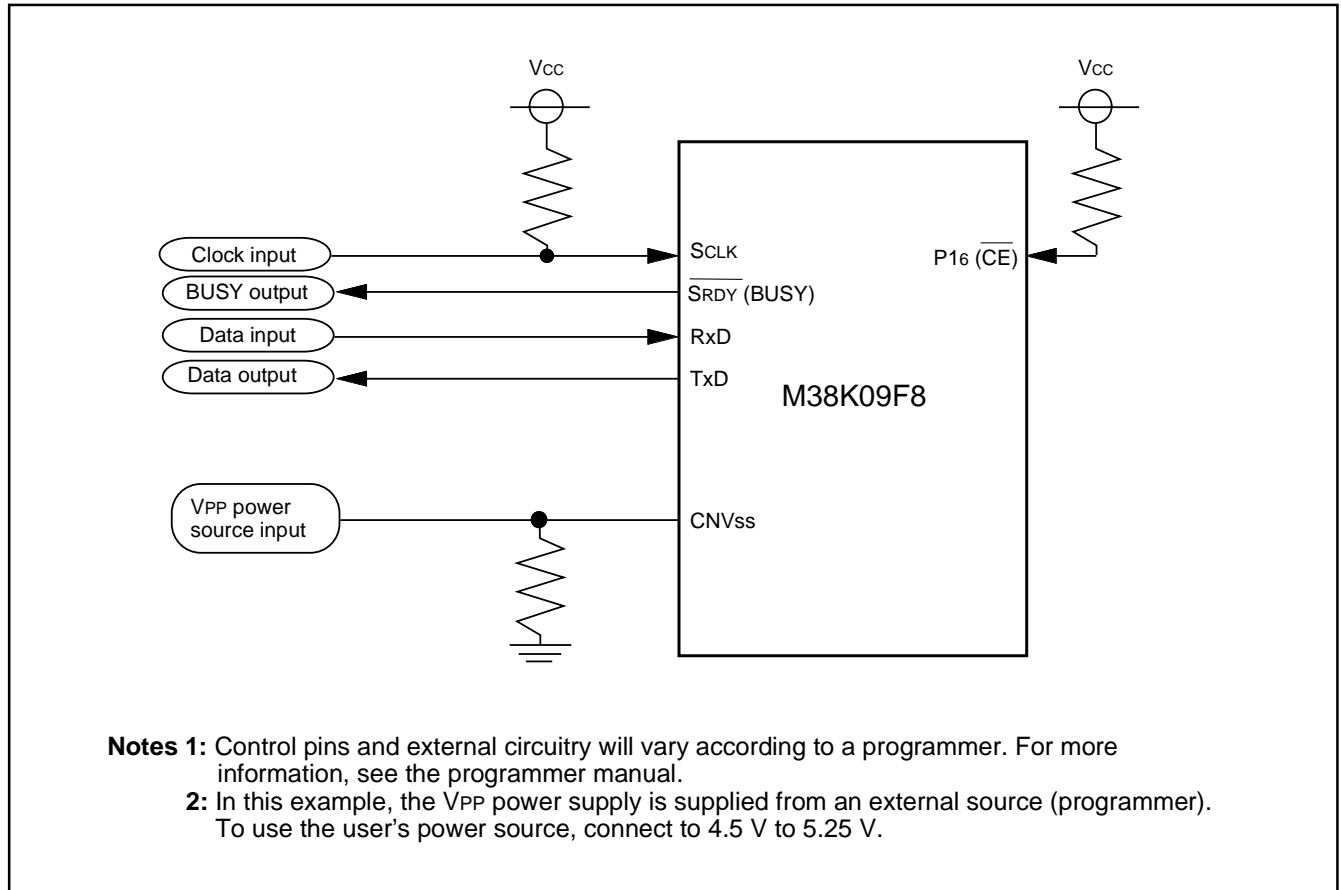


Fig. 136 Example circuit application for standard serial I/O mode

HARDWARE

NOTES ON PROGRAMMING

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1." After a reset, initialize flags which affect program execution. In particular, it is essential to initialize the index X mode (T) and the decimal mode (D) flags because of their effect on calculations.

Interrupts

The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

Decimal Calculations

- To calculate in decimal notation, set the decimal mode flag (D) to "1", then execute an ADC or SBC instruction. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.
- In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

Timers

- When n (0 to 255) is written to a timer latch, the frequency division ratio is $1/(n+1)$.
- When a count source of timer X is switched, stop a count of timer X.

Multiplication and Division Instructions

- The index X mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.
- The execution of these instructions does not change the contents of the processor status register.

Ports

The contents of the port direction registers cannot be read. The following cannot be used:

- The data transfer instruction (LDA, etc.)
- The operation instruction when the index X mode flag (T) is "1"
- The addressing mode which uses the value of a direction register as an index
- The bit-test instruction (BBC or BBS, etc.) to a direction register
- The read-modify-write instructions (ROR, CLB, or SEB, etc.) to a direction register.

Use instructions such as LDM and STA, etc., to set the port direction registers.

A-D Converter

The comparator uses capacitive coupling amplifier whose charge will be lost if the clock frequency is too low.

Therefore, make sure that f(system clock) in the middle/high-speed mode is at least on 500 kHz during an A-D conversion.

Do not execute the STP or WIT instruction during an A-D conversion.

Instruction Execution Time

The instruction execution time is obtained by multiplying the frequency of the internal clock ϕ by the number of cycles needed to execute an instruction. However, When using the USB function or EXB function, an occurrence of one-wait due to the multichannel RAM will double an internal clock ϕ cycle.

Definition of A-D Conversion Accuracy

The A-D conversion accuracy is defined below (refer to Figure 137).

•Relative accuracy

① Zero transition voltage (V_{OT})

This means an analog input voltage when the actual A-D conversion output data changes from “0” to “1.”

② Full-scale transition voltage (V_{FST})

This means an analog input voltage when the actual A-D conversion output data changes from “1023” to “1022.”

③ Non-linearity error

This means a deviation from the line between V_{OT} and V_{FST} of a converted value between V_{OT} and V_{FST}.

④ Differential non-linearity error

This means a deviation from the input potential difference required to change a converted value between V_{OT} and V_{FST} by 1 LSB of the 1 LSB at the relative accuracy.

•Absolute accuracy

This means a deviation from the ideal characteristics between 0 to V_{REF} of actual A-D conversion characteristics.

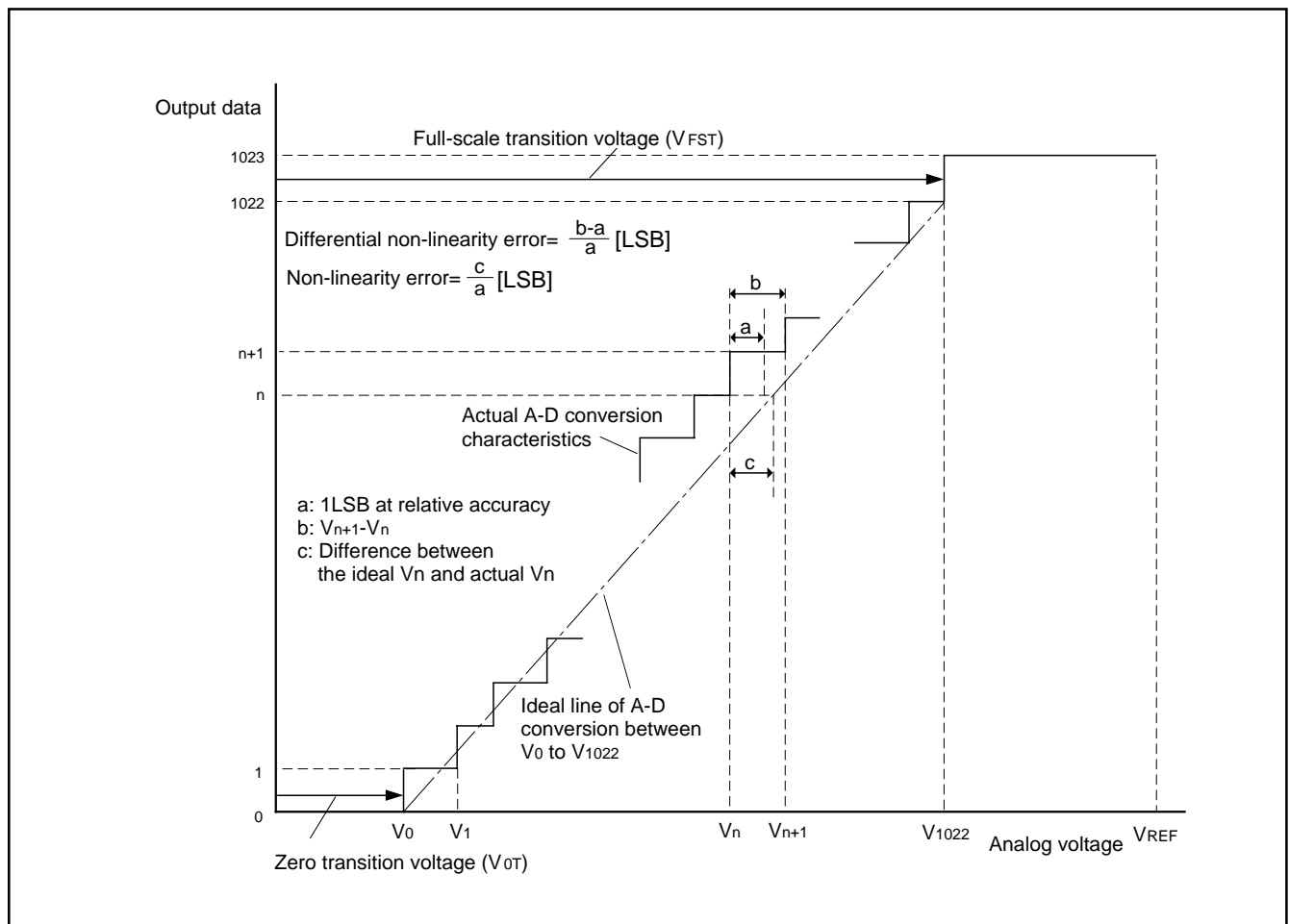


Fig. 137 Definition of A-D conversion accuracy

V_n: Analog input voltage when the output data changes from “n” to “n + 1” (n = 0 to 1022)

• 1 LSB at relative accuracy $\rightarrow \frac{V_{FST} - V_{OT}}{1022}$ (V)

• 1 LSB at absolute accuracy $\rightarrow \frac{V_{REF}}{1024}$ (V)

HARDWARE

NOTES ON USAGE/DATA REQUIRED FOR MASK ORDERS

NOTES ON USAGE

Handling of Power Source Pin

In order to avoid a latch-up occurrence, connect a capacitor suitable for high frequencies as bypass capacitor between power source pin (Vcc pin) and GND pin (Vss pin). Besides, connect the capacitor to as close as possible. For bypass capacitor which should not be located too far from the pins to be connected, a ceramic or electrolytic capacitor of 1.0 μ F is recommended.

USB Port Pins (D0+, D0-) Treatment

- The USB specification requires a driver-impedance 28 to 44 Ω . In order to meet the USB specification impedance requirements, connect a resistor (27 Ω recommended) in series to the USB port pins.

In addition, in order to reduce the ringing and control the falling/rising timing and a crossover point, connect a capacitor between the USB port pins and the Vss pin if necessary.

The values and structure of those peripheral elements depend on the impedance characteristics and the layout of the printed circuit board. Accordingly, evaluate your system and observe waveforms before actual use and decide use of elements and the values of resistors and capacitors.

- Make sure the USB D+/D- lines do not cross any other wires. Keep a large GND area to protect the USB lines. Also, make sure you use a USB specification compliant connector for the connection.

USBVREF pin Treatment (Noise Elimination)

- Connect a capacitor between the USBVREF pin and the Vss pin. The capacitor should have a 2.2 μ F capacitor (electrolytic capacitor) and a 0.1 μ F capacitor (ceramic type capacitor) connected in parallel.

- In Vcc = 3.0 to 3.6 V operation, connect the USBVREF pin directly to the Vcc pin in order to supply power to the USB port circuit. In addition, you will need to disable the built-in USB reference voltage circuit in this operation (set bit 4 of the USB control register to "0".) If you are using the bus powered supply in this condition, the DC-DC converter must be placed outside the MCU.

- In Vcc = 4.00 to 5.25 V operation, do not connect the external DC-DC converter to the USBVREF pin. Use the built-in USB reference voltage circuit.

Flash Memory Version

The CNVss pin is connected to the internal memory circuit block by a low-ohmic resistance, since it has the multiplexed function to be a programmable power source pin (VPP pin) as well.

To improve the noise reduction, connect a track between CNVss pin and Vss pin or Vcc pin with 1 to 10 k Ω resistance.

The mask ROM version track of CNVss pin has no operational interference even if it is connected to Vss pin or Vcc pin via a resistor.

Electric Characteristic Differences Between Mask ROM and Flash Memory Version MCUs

There are differences in electric characteristics, operation margin, noise immunity, and noise radiation between Mask ROM and Flash Memory version MCUs due to the difference in the manufacturing processes.

When manufacturing an application system with the Flash Memory version and then switching to use of the Mask ROM version, please perform sufficient evaluations for the commercial samples of the Mask ROM version.

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

1. Mask ROM Order Confirmation Form*
2. Mark Specification Form*
3. Data to be written to ROM, in EPROM form (three identical copies) or one floppy disk.

* Mask ROM Confirmation Forms/Mark Specification Forms
<http://www.infocom.maec.co.jp/>

FUNCTIONAL DESCRIPTION SUPPLEMENT

A-D Converter

A-D conversion is started by setting AD conversion completion bit to "0." During A-D conversion, internal operations are performed as follows.

1. After the start of A-D conversion, A-D conversion register goes to "0016."
2. The highest-order bit of A-D conversion register is set to "1," and the comparison voltage V_{ref} is input to the comparator. Then, V_{ref} is compared with analog input voltage V_{IN} .
3. As a result of comparison, when $V_{ref} < V_{IN}$, the highest-order bit of A-D conversion register becomes "1." When $V_{ref} > V_{IN}$, the highest-order bit becomes "0."

By repeating the above operations up to the lowest-order bit of the A-D conversion register, an analog value converts into a digital value.

A-D conversion completes at 122 clock cycles (15.25 μ s at system clock = 8 MHz, Through mode) after it is started, and the result of the conversion is stored into the A-D conversion register.

Concurrently with the completion of A-D conversion, A-D conversion interrupt request occurs, so that the AD conversion interrupt request bit is set to "1."

Table 16 Relative formula for a reference voltage V_{REF} of A-D converter and V_{ref}

When $n = 0$	$V_{ref} = 0$
When $n = 1$ to 1023	$V_{ref} = \frac{V_{REF}}{1024} \times n$

n : Value of A-D converter (decimal numeral)

Table 17 Change of A-D conversion register during A-D conversion

	Change of A-D conversion register	Value of comparison voltage (V_{ref})
At start of conversion	0 0 0 0 0 0 0 0 0 0 0 0	0
First comparison	1 0 0 0 0 0 0 0 0 0 0 0	$\frac{V_{REF}}{2}$
Second comparison	*1 1 0 0 0 0 0 0 0 0 0 0	$\frac{V_{REF}}{2} \pm \frac{V_{REF}}{4}$
Third comparison	*1 *2 1 0 0 0 0 0 0 0 0 0	$\frac{V_{REF}}{2} \pm \frac{V_{REF}}{4} \pm \frac{V_{REF}}{8}$
≈		≈
After completion of tenth comparison	A result of A-D conversion *1 *2 *3 *4 *5 *6 *7 *8 *9 *10	$\frac{V_{REF}}{2} \pm \frac{V_{REF}}{4} \pm \dots \pm \frac{V_{REF}}{1024}$

*1–*10: A result of the first comparison to the tenth comparison

HARDWARE

FUNCTIONAL DESCRIPTION SUPPLEMENT

Figures 138 shows the A-D conversion equivalent circuit, and Figure 139 shows the A-D conversion timing chart.

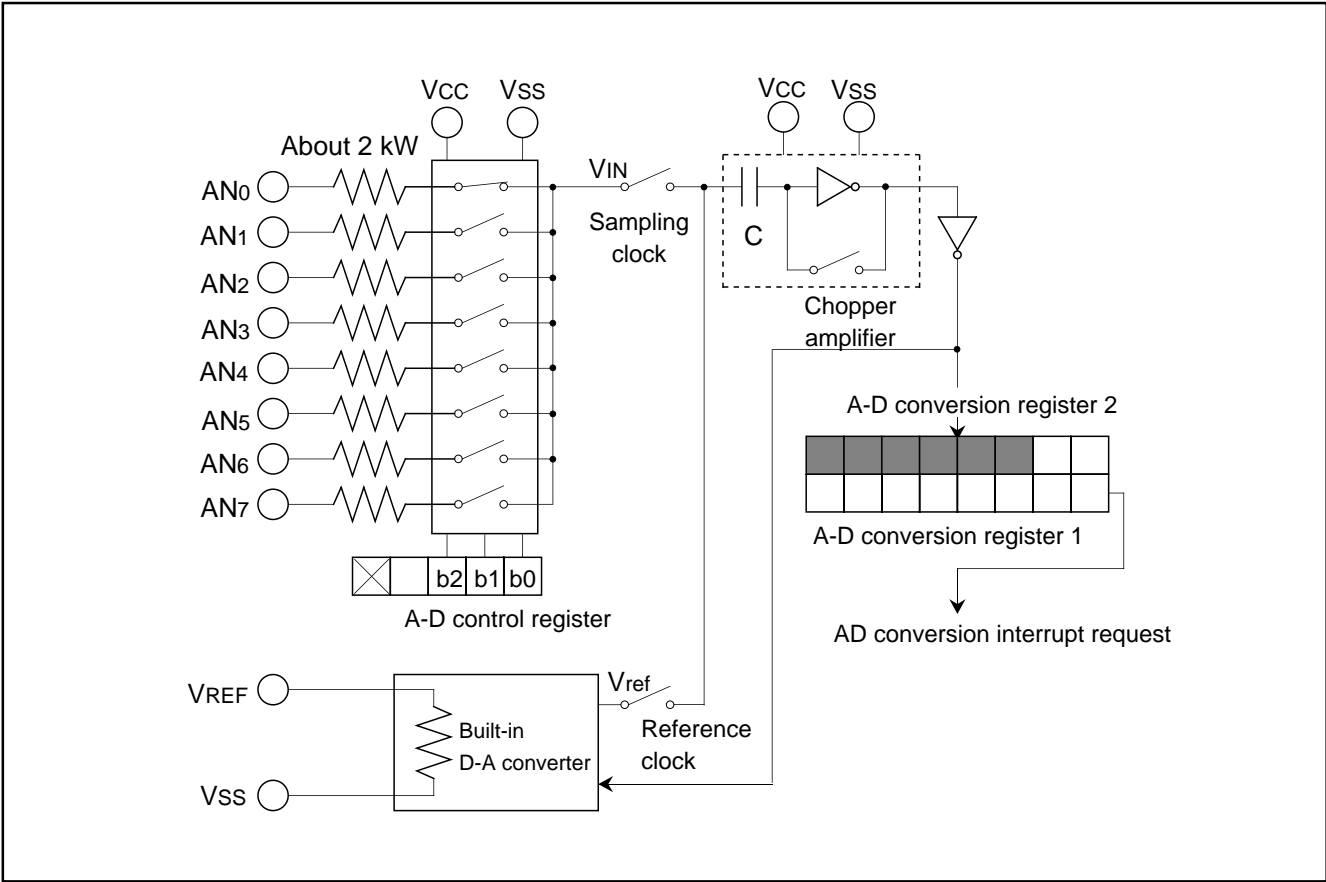


Fig. 138 A-D conversion equivalent circuit

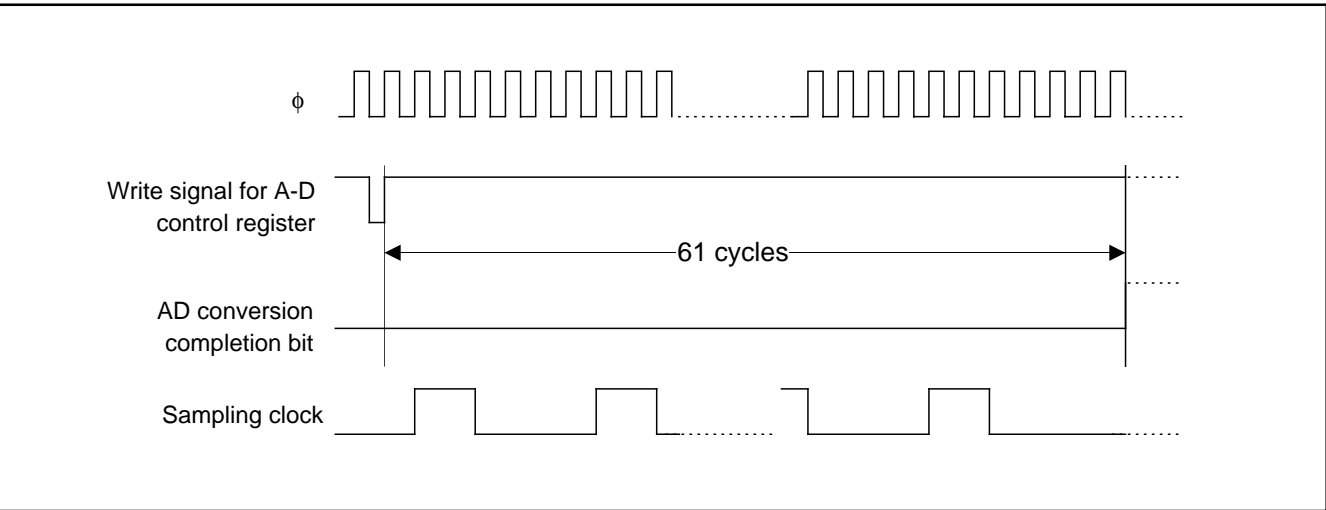


Fig. 139 A-D conversion timing chart

CHAPTER 2

APPLICATION

- 2.1 I/O port
- 2.2 Interrupt
- 2.3 Timer
- 2.4 Serial I/O
- 2.5 USB function
- 2.6 External bus interface (EXB)
- 2.7 A-D converter
- 2.8 Watchdog timer
- 2.9 Reset
- 2.10 Frequency synthesizer (PLL)
- 2.11 Clock generating circuit
- 2.12 Standby function
- 2.13 Flash memory

APPLICATION

2.1 I/O port

2.1 I/O port

This paragraph explains the registers setting method and the notes related to the I/O ports.

2.1.1 Memory map

0000 ₁₆	Port P0 (P0)
0001 ₁₆	Port P0 direction register (P0D)
0002 ₁₆	Port P1 (P1)
0003 ₁₆	Port P1 direction register (P1D)
0004 ₁₆	Port P2 (P2)
0005 ₁₆	Port P2 direction register (P2D)
0006 ₁₆	Port P3 (P3)
0007 ₁₆	Port P3 direction register (P3D)
0008 ₁₆	Port P4 (P4)
0009 ₁₆	Port P4 direction register (P4D)
000A ₁₆	Port P5 (P5)
000B ₁₆	Port P5 direction register (P5D)
000C ₁₆	Port P6 (P6)
000D ₁₆	Port P6 direction register (P6D)
⋮	⋮
0FF0 ₁₆	Port P0 pull-up control register (PULL0)
⋮	⋮
0FF2 ₁₆	Port P5 pull-up control register (PULL5)

Fig. 2.1.1 Memory map of registers related to I/O port

2.1.2 Related registers

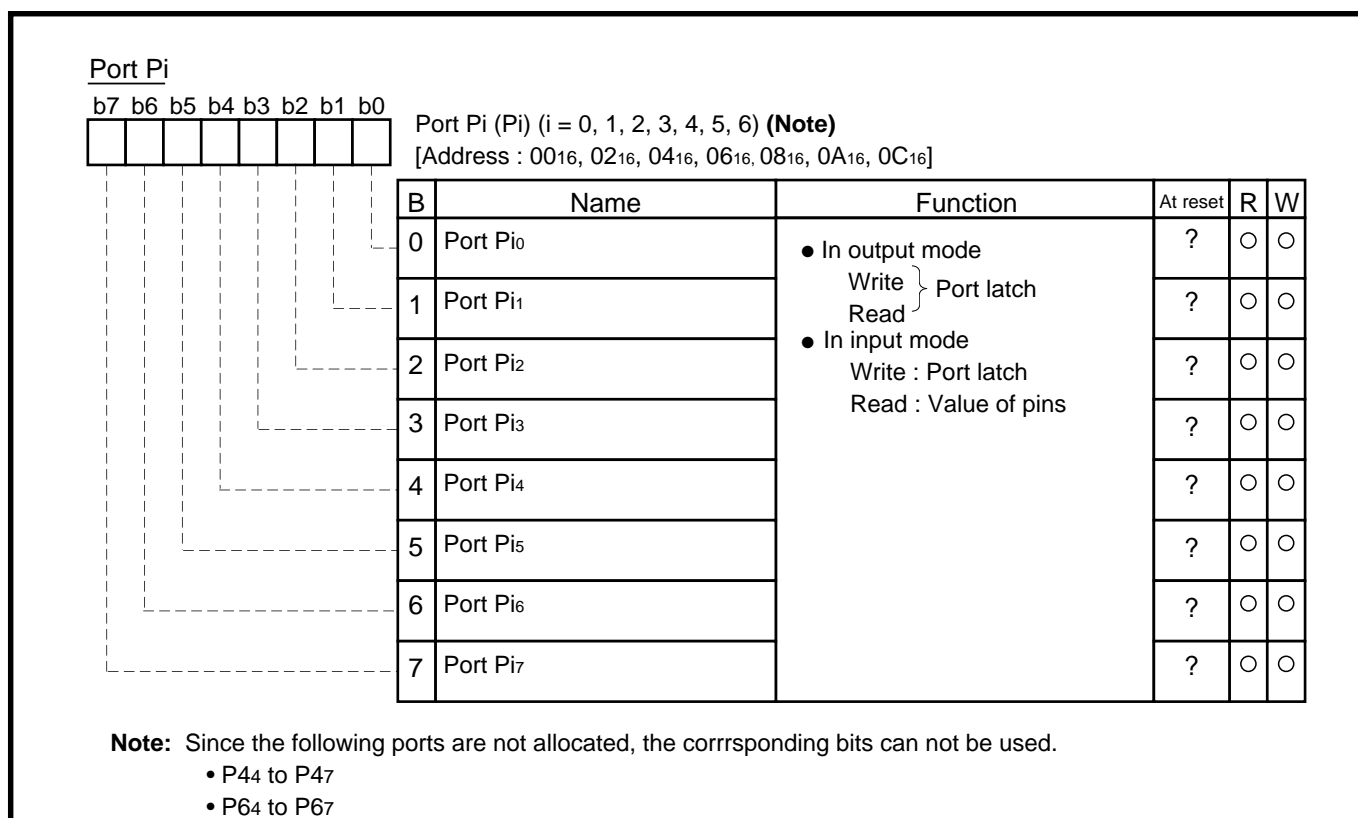


Fig. 2.1.2 Structure of Port Pi (i = 0 to 6)

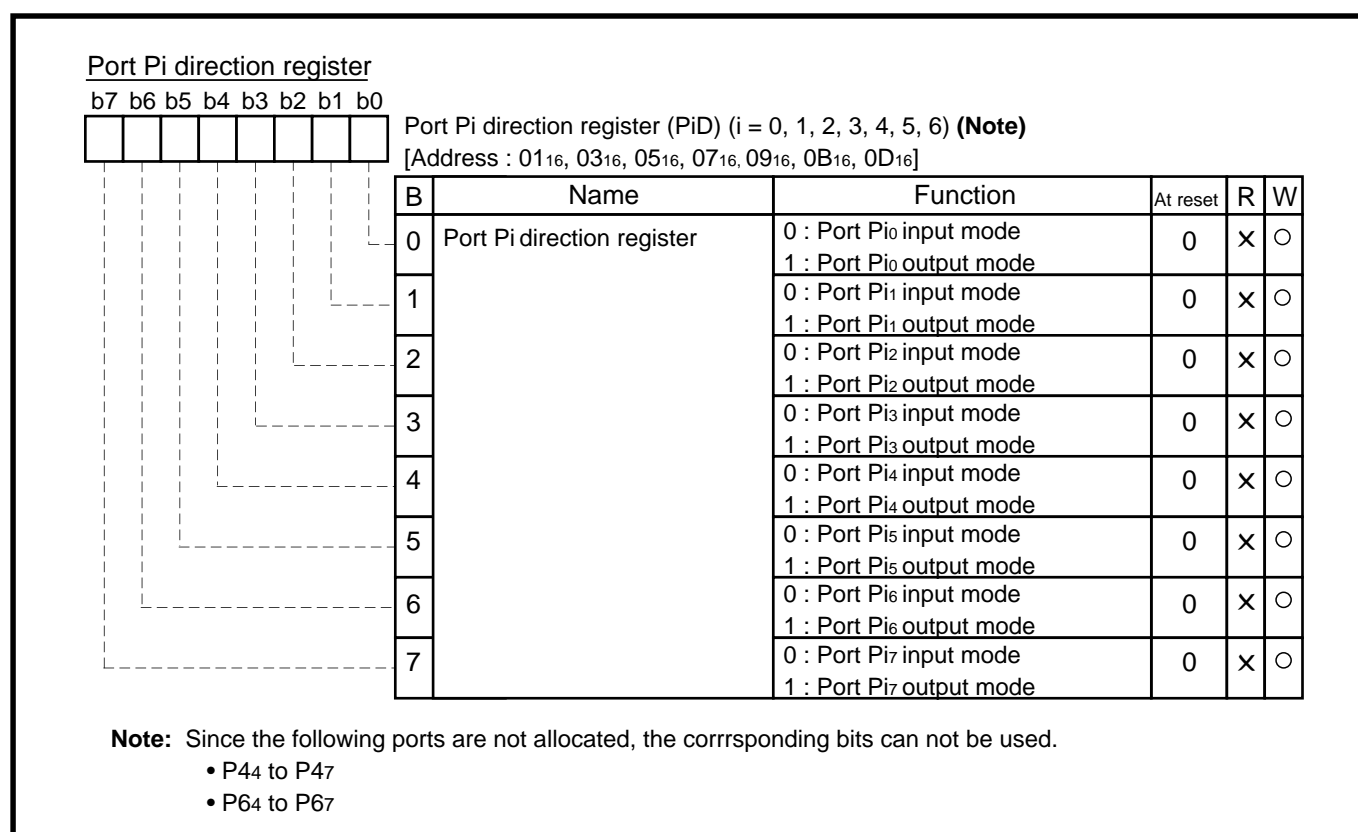


Fig. 2.1.3 Structure of Port Pi direction register (i = 0 to 6)

APPLICATION

2.1 I/O port

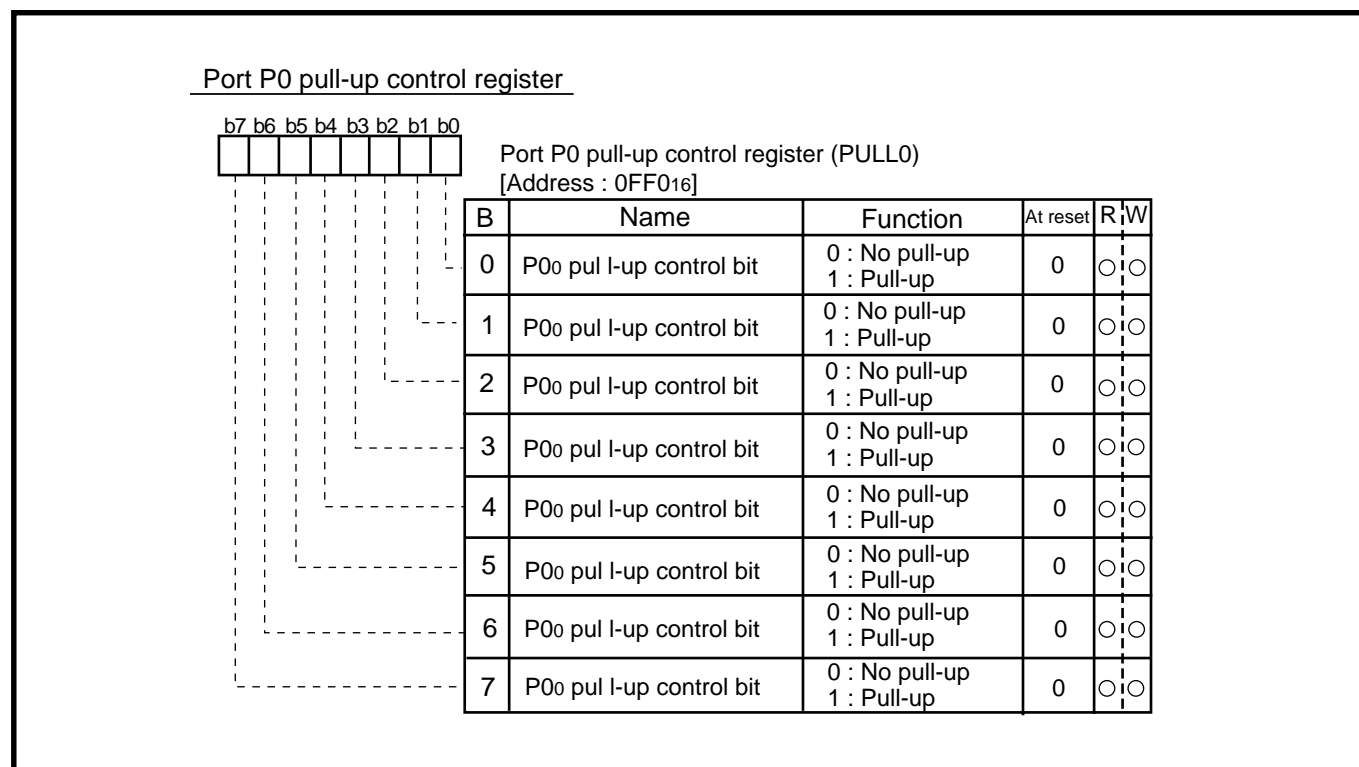


Fig. 2.1.4 Structure of Port P0 pull-up control register

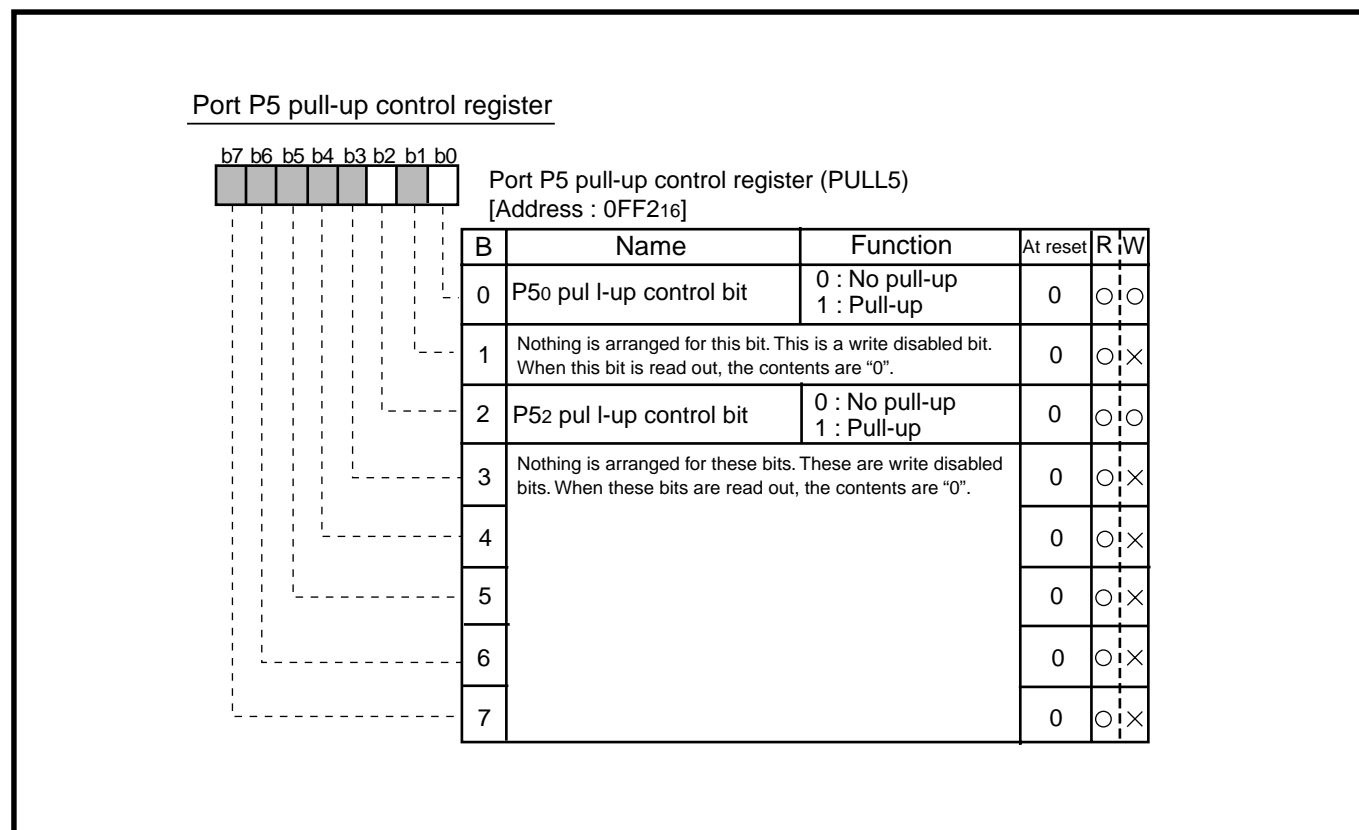


Fig. 2.1.5 Structure of Port P5 pull-up control register

2.1.3 Handling of unused pins

Table 2.1.1 Handling of unused pins

Pins/Ports name	Handling
P0, P1, P2, P3, P4, P5, P6	<ul style="list-style-type: none">•Set to the input mode and connect each to Vcc or Vss through a resistor of 1 kΩ to 10 kΩ.•Set to the output mode and open at “L” or “H” level.
V _{REF}	<ul style="list-style-type: none">•Connect to Vss (GND).
X _{OUT}	<ul style="list-style-type: none">•Open, only when using an external clock.
USBV _{REF}	<ul style="list-style-type: none">•Connect to Vcc
TrON	<ul style="list-style-type: none">•Open
D0+, D0-	<ul style="list-style-type: none">•Connect each to Vss through a resistor of 1 kΩ to 10 kΩ.

APPLICATION

2.1 I/O port

2.1.4 Notes on input and output pins

(1) Modifying output data with bit managing instruction

When the port latch of an I/O port is modified with the bit managing instruction^{*1}, the value of the unspecified bit may be changed.

● Reason

The bit managing instructions are read-modify-write form instructions for reading and writing data by a byte unit. Accordingly, when these instructions are executed on a bit of the port latch of an I/O port, the following is executed to all bits of the port latch.

- As for a bit which is set for an input port :
The pin state is read in the CPU, and is written to this bit after bit managing.
- As for a bit which is set for an output port :
The bit value of the port latch is read in the CPU, and is written to this bit after bit managing.

Note the following :

- Even when a port which is set as an output port is changed for an input port, its port latch holds the output data.
- As for a bit of the port latch which is set for an input port, its value may be changed even when not specified with a bit managing instruction in case where the pin state differs from its port latch contents.

^{*1} bit managing instructions : **SEB**, and **CLB** instructions

2.1.5 Termination of unused pins

(1) Terminate unused pins

① I/O ports :

- Set the I/O ports for the input mode and connect them to Vcc or Vss through each resistor of 1 k Ω to 10 k Ω . With regard to ports which can select the built-in pull-up resistor, the built-in pull-up resistor can be used.

Set the I/O ports for the output mode and open them at "L" or "H".

- When opening them in the output mode, the input mode of the initial status remains until the mode of the ports is switched over to the output mode by the program after reset. Thus, the potential at these pins is undefined and the power source current may increase in the input mode. With regard to an effects on the system, thoroughly perform system evaluation on the user side.
- Since the direction register setup may be changed because of a program runaway or noise, set direction registers by program periodically to increase the reliability of program.

(2) Termination remarks

① I/O ports :

Do not open in the input mode.

● Reason

- The power source current may increase depending on the first-stage circuit.
- An effect due to noise may be easily produced as compared with proper termination shown in (1).

② I/O ports :

When setting for the input mode, do not connect to Vcc or Vss directly.

● Reason

If the direction register setup changes for the output mode because of a program runaway or noise, a short circuit may occur between a port and Vcc (or Vss).

③ I/O ports :

When setting for the input mode, do not connect multiple ports in a lump to Vcc or Vss through a resistor.

● Reason

If the direction register setup changes for the output mode because of a program runaway or noise, a short circuit may occur between ports.

- At the termination of unused pins, perform wiring at the shortest possible distance (20 mm or less) from microcomputer pins.

APPLICATION

2.2 Interrupt

2.2 Interrupt

This paragraph explains the registers setting method and the notes related to the interrupt.

2.2.1 Memory map

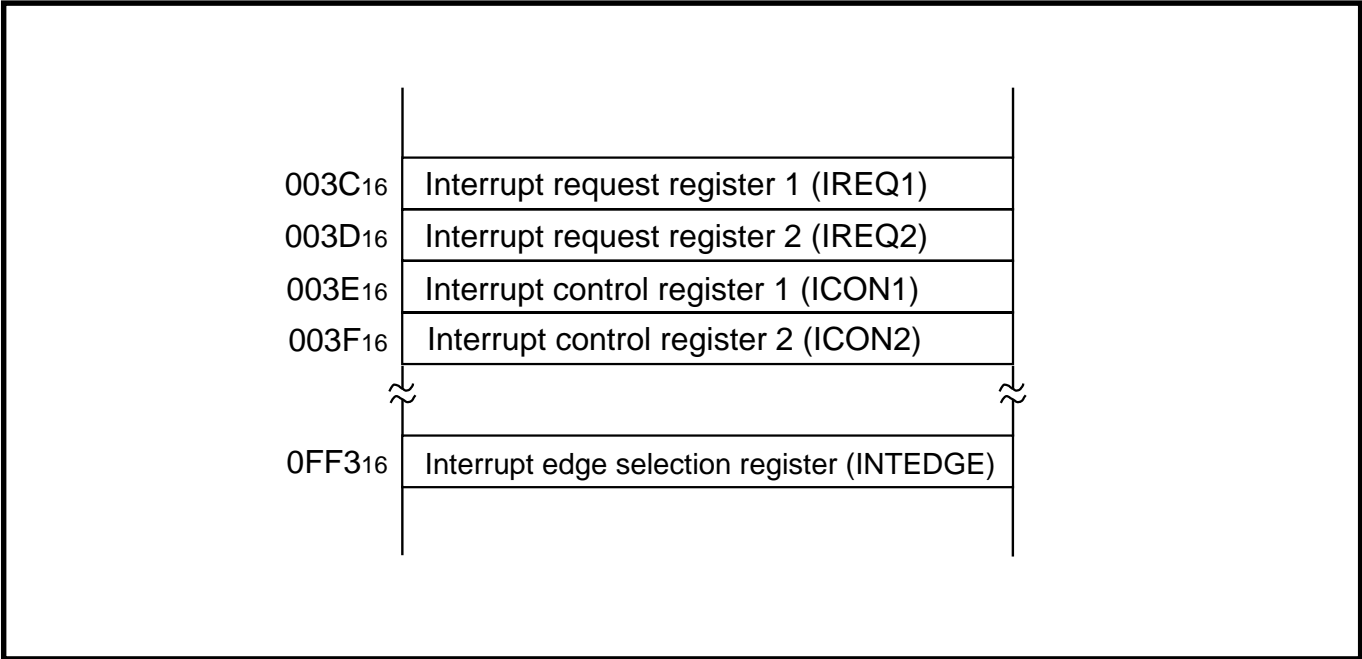


Fig. 2.2.1 Memory map of registers related to interrupt

2.2.2 Related registers

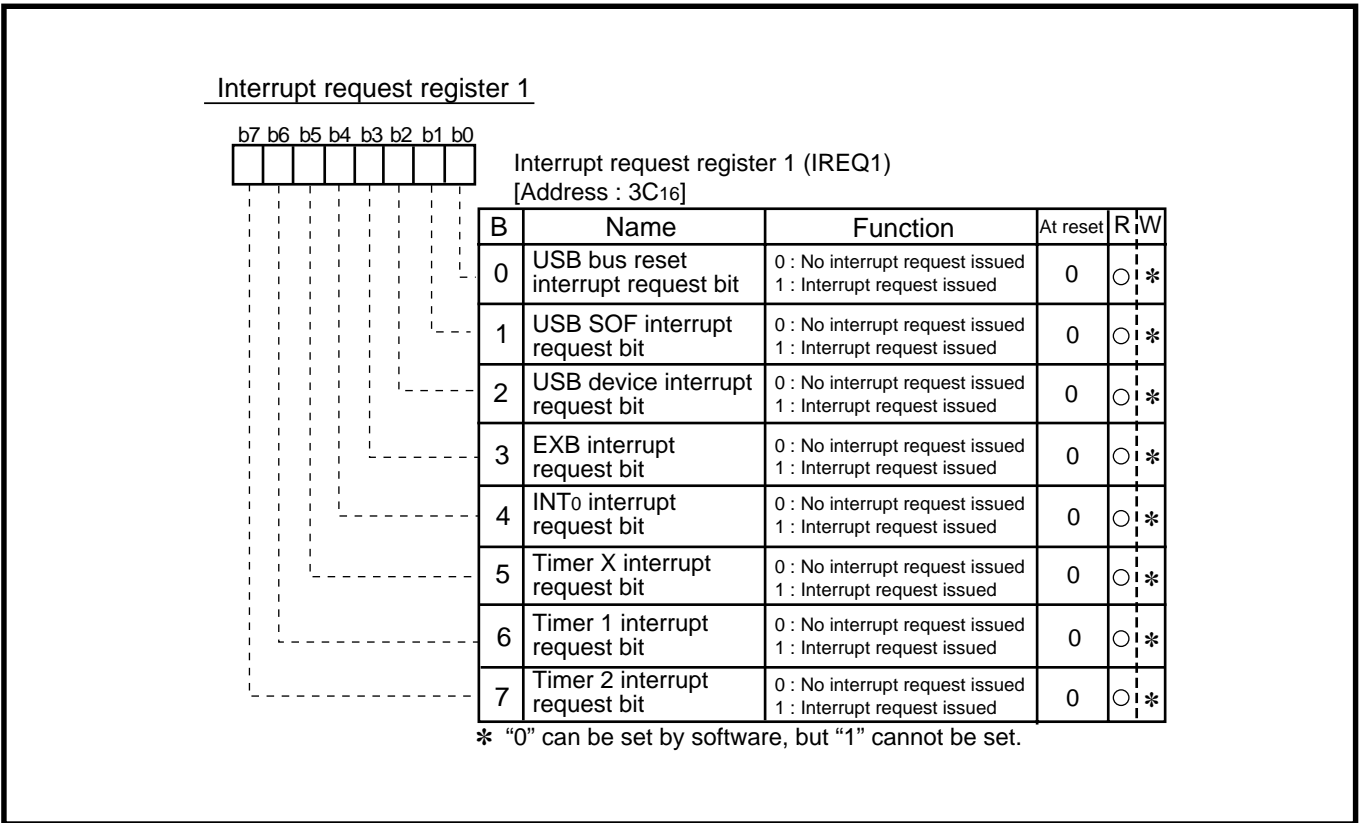
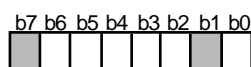


Fig. 2.2.2 Structure of Interrupt request register 1

Interrupt request register 2



Interrupt request register 2 (IREQ2)

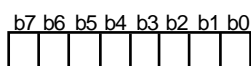
[Address : 3D16]

B	Name	Function	At reset	R	W
0	INT1 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	*
1	Nothing is arranged for this bits. This is a write disabled bit. When this bit is read out, the contents are "0".		0	○	×
2	Serial I/O receive interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	*
3	Serial I/O transmit interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	*
4	CNTR0 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	*
5	Key-on wake-up interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	*
6	A/D conversion interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	*
7	Nothing is arranged for this bits. This is a write disabled bit. When this bit is read out, the contents are "0".		0	○	×

* "0" can be set by software, but "1" cannot be set.

Fig. 2.2.3 Structure of Interrupt request register 2

Interrupt control register 1



Interrupt control register 1 (ICON1)

[Address : 3E16]

B	Name	Function	At reset	R	W
0	USB bus reset interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
1	USB SOF interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
2	USB device interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
3	EXB interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
4	INT0 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
5	Timer X interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
6	Timer 1 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
7	Timer 2 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○

Fig. 2.2.4 Structure of Interrupt control register 1

APPLICATION

2.2 Interrupt

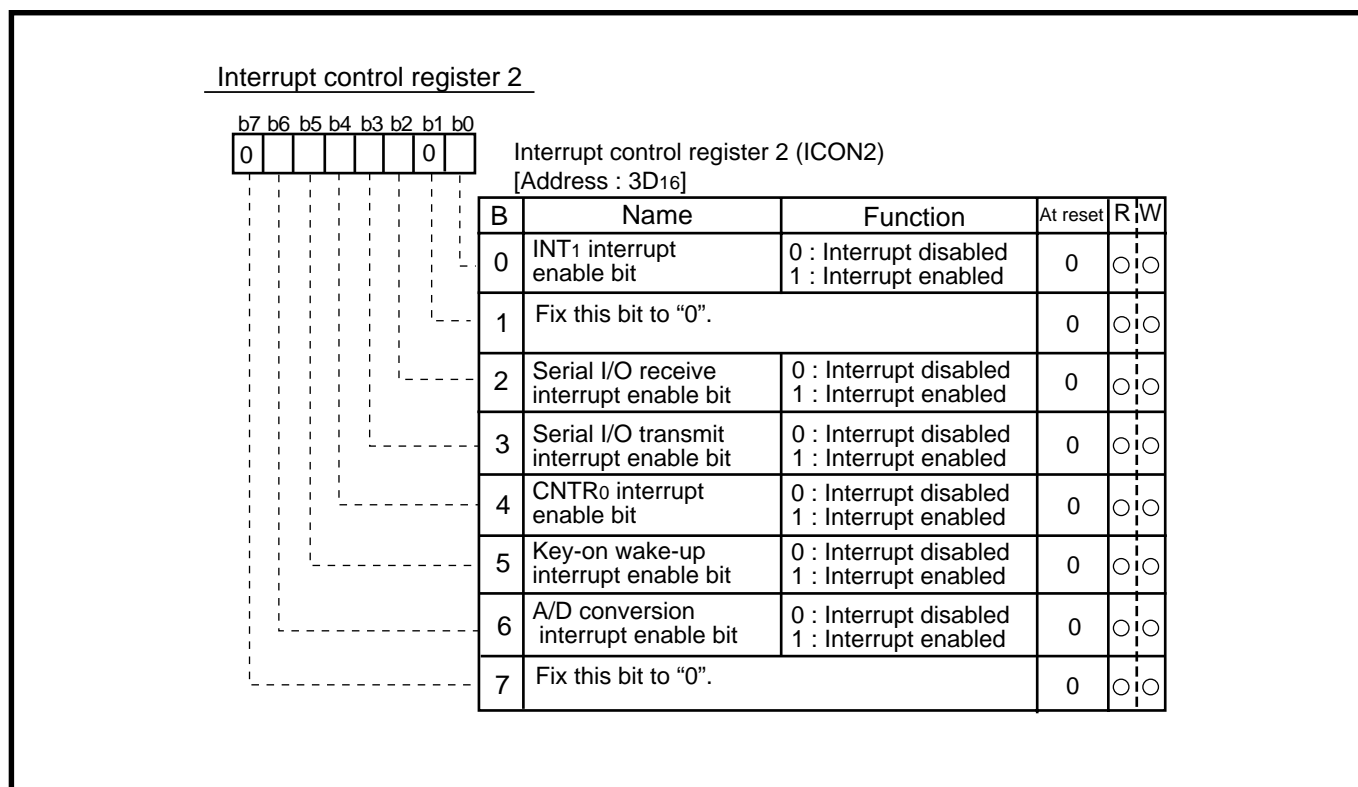


Fig. 2.2.5 Structure of Interrupt control register 2

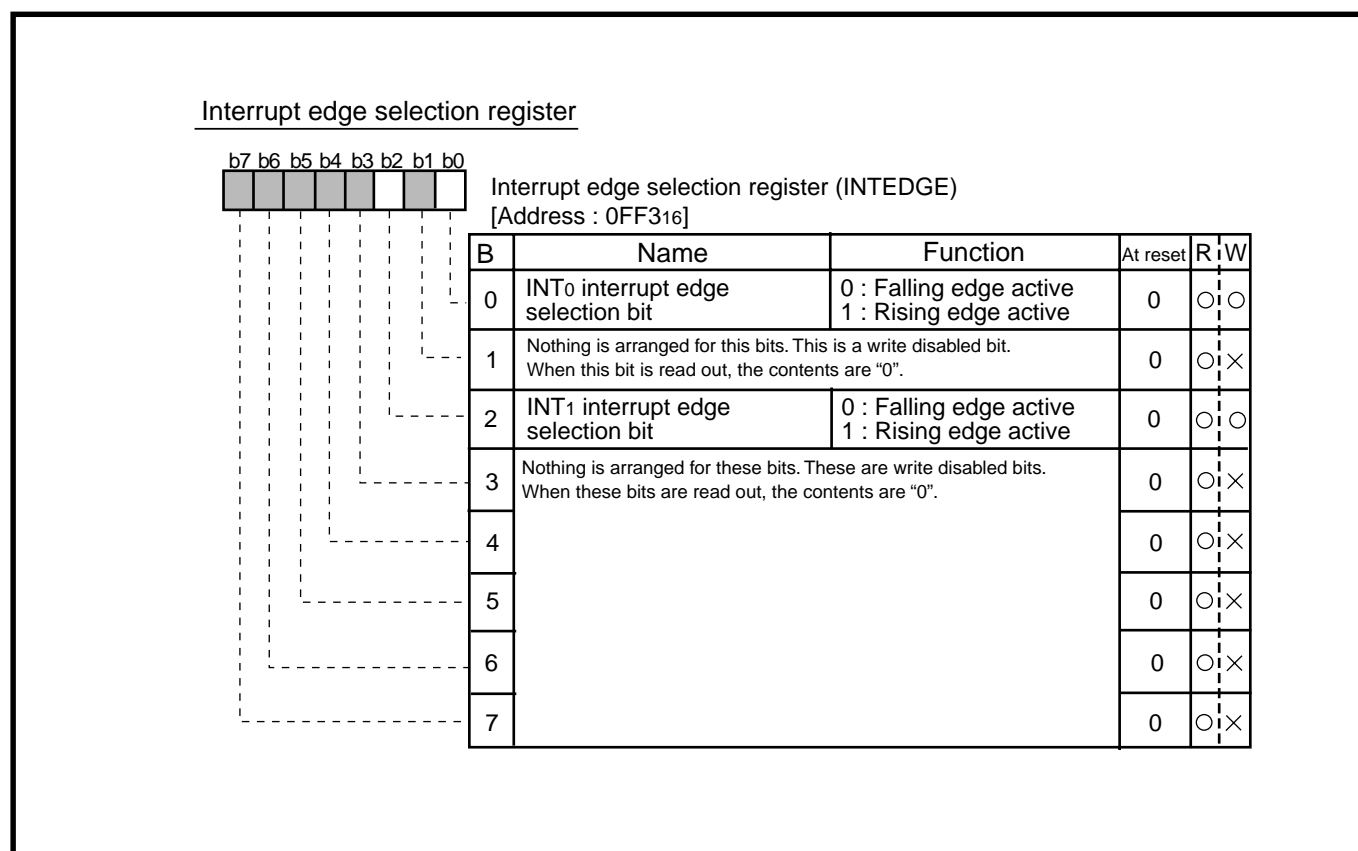


Fig. 2.2.6 Structure of Interrupt edge selection register

2.2.3 Interrupt source

The 38K0 group permits interrupts of 15 sources. These are vector interrupts with a fixed priority system. Accordingly, when two or more interrupt requests occur during the same sampling, the higher-priority interrupt is accepted first. This priority is determined by hardware, but a variety of priority processing can be performed by software, using an interrupt enable bit and an interrupt disable flag.

For interrupt sources, vector addresses and interrupt priority, refer to Table 2.2.1.

Table 2.2.1 Interrupt sources, vector addresses and priority of 38K0 group

Interrupt Source	Priority	Vector Addresses (Note 1)		Interrupt Request Generating Conditions	Remarks
		High	Low		
Reset (Note 2)	1	FFFD ₁₆	FFFC ₁₆	At reset	Non-maskable
USB bus reset	2	FFFB ₁₆	FFFA ₁₆	At detection of USB bus reset signal (2.5 μ s interval SE0)	Valid when USB mode
USB SOF	3	FFF9 ₁₆	FFF8 ₁₆	At detection of USB SOF signal	Valid when USB mode
USB device	4	FFF7 ₁₆	FFF6 ₁₆	At detection of resume signal (K state or SE0) or suspend signal (3 ms interval bus idle), or at completion of transaction	Valid when USB mode
External bus	5	FFF5 ₁₆	FFF4 ₁₆	At completion of reception or transmission or at completion of DMA transmission	Valid when external bus is selected
INT ₀	6	FFF3 ₁₆	FFF2 ₁₆	At detection of either rising or falling edge of INT ₀ input	External interrupt (active edge selectable)
Timer X	7	FFF1 ₁₆	FFF0 ₁₆	At timer X underflow	
Timer 1	8	FFEF ₁₆	FFEE ₁₆	At timer 1 underflow	STP release timer underflow
Timer 2	9	FFED ₁₆	FFEC ₁₆	At timer 2 underflow	
INT ₁	10	FFEB ₁₆	FFEA ₁₆	At detection of either rising or falling edge of INT ₁ input	External interrupt (active edge selectable)
(Note 3)	—	FFE9 ₁₆	FFE8 ₁₆	(Note 4)	(Note 4)
Serial I/O reception	11	FFE7 ₁₆	FFE6 ₁₆	At completion of serial I/O data reception	Valid when serial I/O is selected
Serial I/O transmission	12	FFE5 ₁₆	FFE4 ₁₆	At completion of serial I/O data transmission	Valid when serial I/O is selected
CNTR ₀	13	FFE3 ₁₆	FFE2 ₁₆	At detection of either rising or falling edge of CNTR ₀ input	External interrupt (active edge selectable)
Key-on wake up	14	FFE1 ₁₆	FFE0 ₁₆	At falling of conjunction of input level for port P0 (at input mode)	External interrupt (active edge selectable)
A-D conversion	15	FFDF ₁₆	FFDE ₁₆	At completion of A-D conversion	
BRK instruction	16	FFDD ₁₆	FFDC ₁₆	At BRK instruction execution	Non-maskable software interrupt

Notes 1: Vector addresses contain interrupt jump destination addresses.

2: Reset function in the same way as an interrupt with the highest priority.

3: Nothing is arranged in these vector addresses.

4: Fix bit 1 of interrupt control register 2 (address 003F₁₆) to "0".

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2.2 Interrupt

2.2.4 Interrupt operation

When an interrupt request is accepted, the contents of the following registers just before acceptance of the interrupt requests is automatically pushed onto the stack area in the order of ①, ② and ③.

- ① High-order contents of program counter (PC_H)
- ② Low-order contents of program counter (PC_L)
- ③ Contents of processor status register (PS)

After the contents of the above registers are pushed onto the stack area, the accepted interrupt vector address enters the program counter and consequently the interrupt processing routine is executed.

When the RTI instruction is executed at the end of the interrupt processing routine, the contents of the above registers pushed onto the stack area are restored to the respective registers in the order of ③, ② and ①; and the microcomputer resumes the processing executed just before acceptance of the interrupts. Figure 2.2.7 shows an interrupt operation diagram.

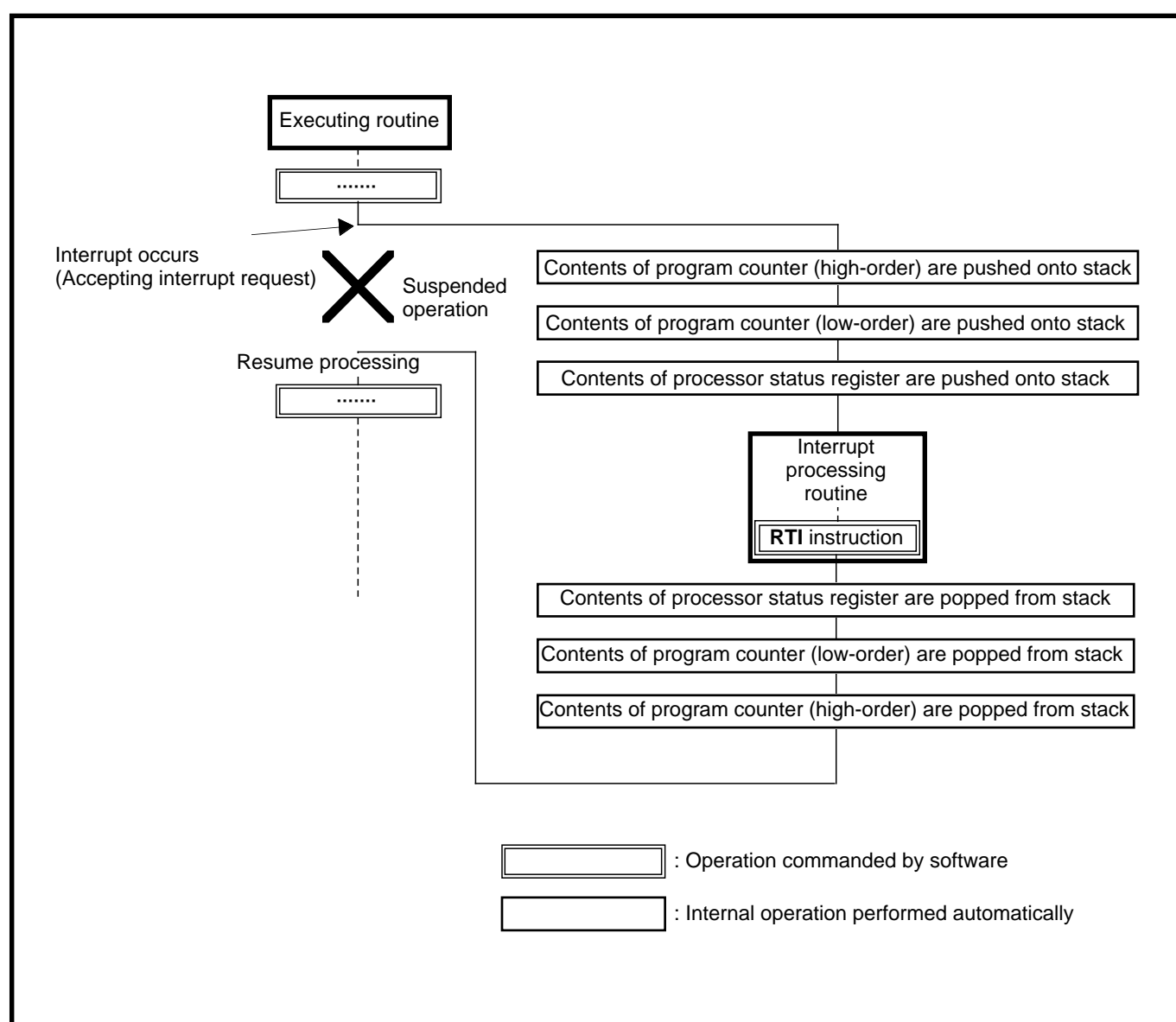


Fig. 2.2.7 Interrupt operation diagram

(1) Processing upon acceptance of interrupt request

Upon acceptance of an interrupt request, the following operations are automatically performed.

- ① The processing being executed is stopped.
- ② The contents of the program counter and the processor status register are pushed onto the stack area. Figure 2.2.8 shows the changes of the stack pointer and the program counter upon acceptance of an interrupt request.
- ③ Concurrently with the push operation, the jump destination address (the beginning address of the interrupt processing routine) of the occurring interrupt stored in the vector address is set in the program counter, then the interrupt processing routine is executed.
- ④ After the interrupt processing routine is started, the corresponding interrupt request bit is automatically cleared to "0". The interrupt disable flag is set to "1" so that multiple interrupts are disabled.

Accordingly, for executing the interrupt processing routine, it is necessary to set the jump destination address in the vector area corresponding to each interrupt.

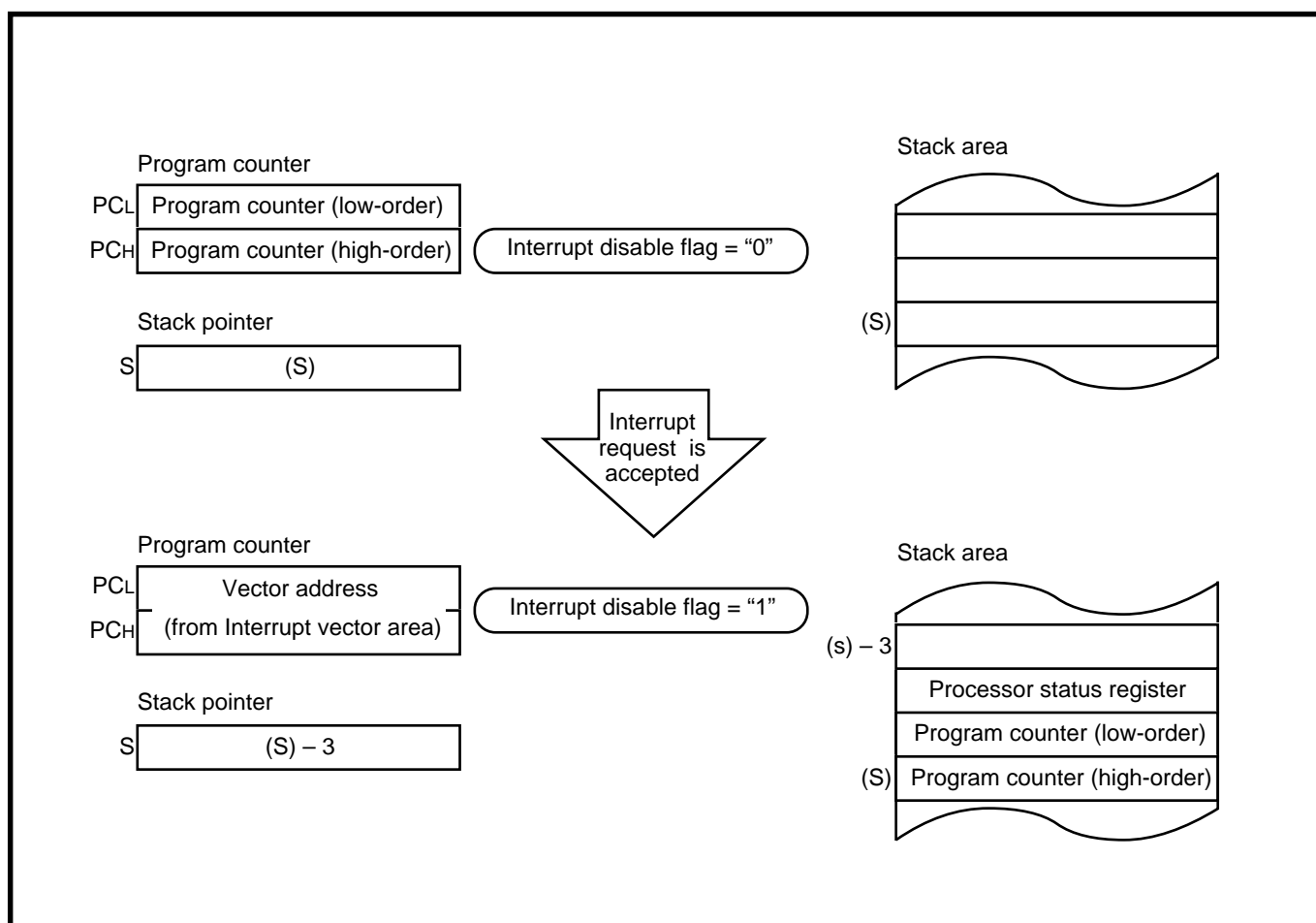


Fig. 2.2.8 Changes of stack pointer and program counter upon acceptance of interrupt request

APPLICATION

2.2 Interrupt

(2) Timing after acceptance of interrupt request

The interrupt processing routine begins with the machine cycle following the completion of the instruction that is currently being executed.

Figure 2.2.9 shows the time up to execution of interrupt processing routine and Figure 2.2.10 shows the timing chart after acceptance of interrupt request.

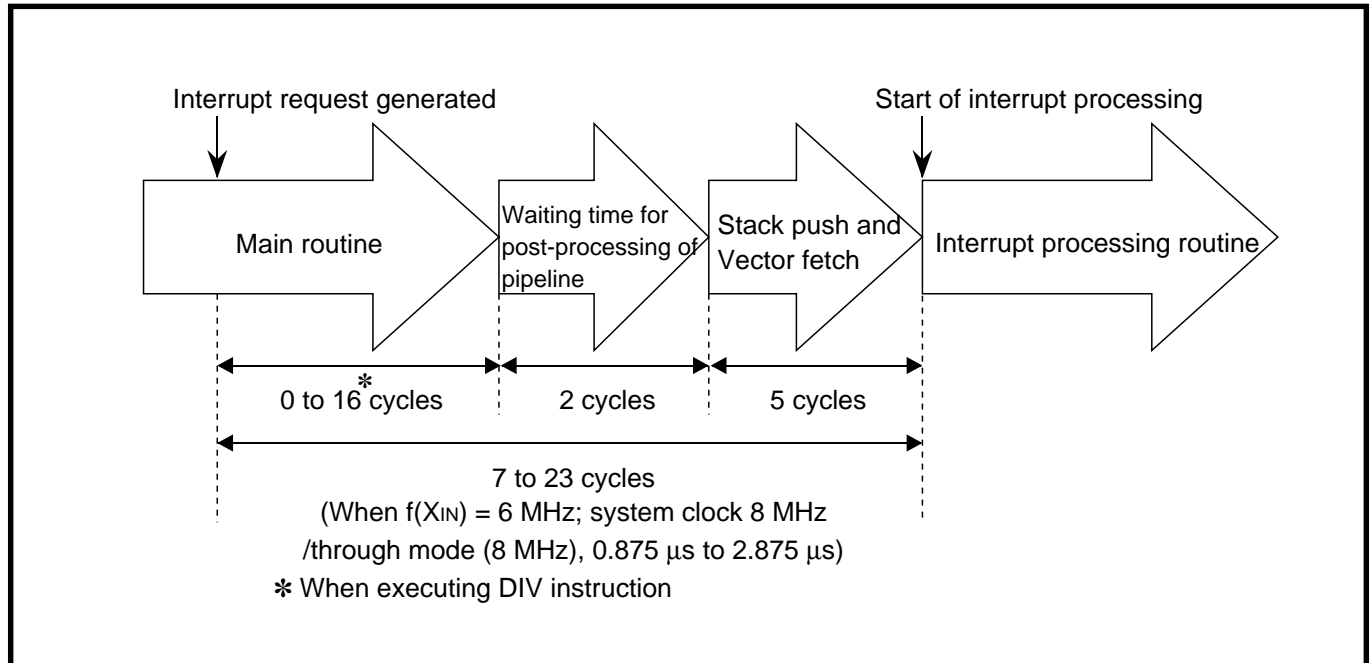


Fig. 2.2.9 Time up to execution of interrupt processing routine

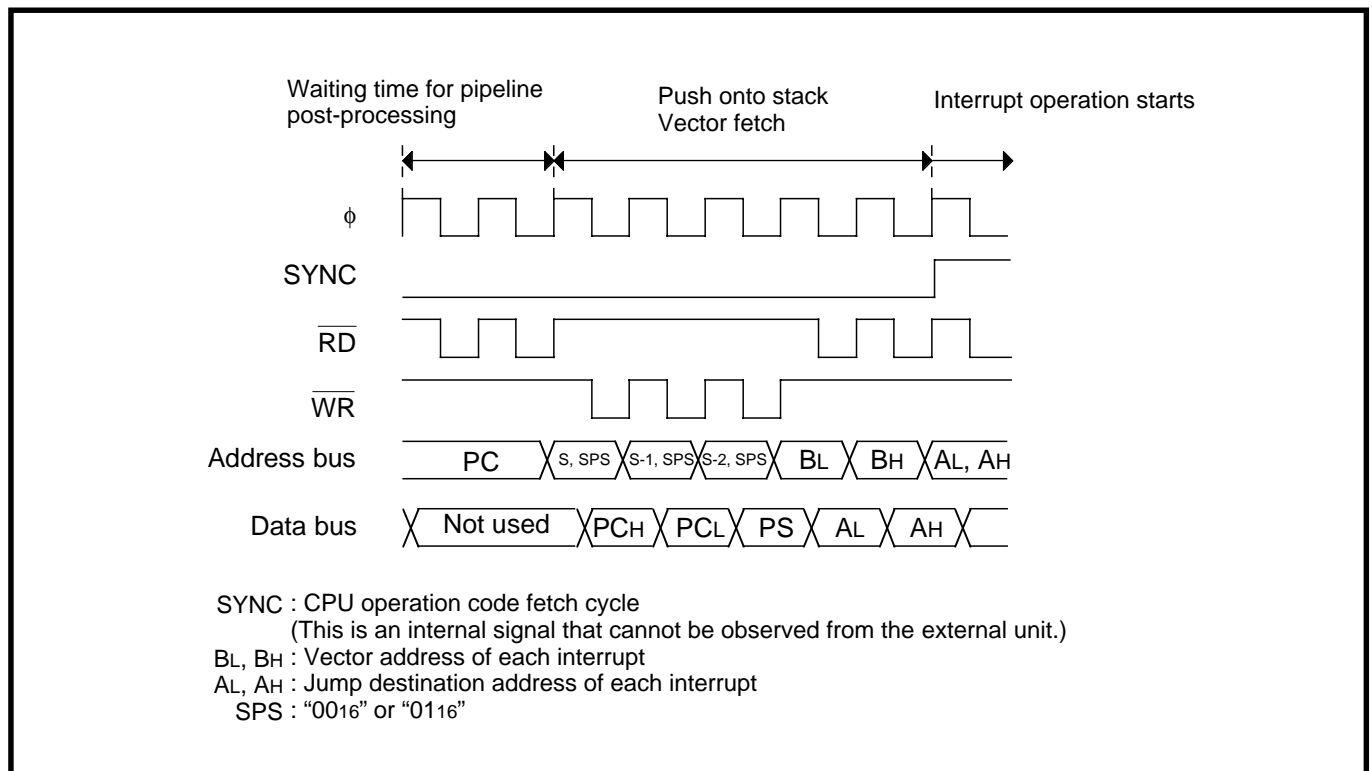


Fig. 2.2.10 Timing chart after acceptance of interrupt request

2.2.5 Interrupt control

The acceptance of all interrupts, excluding the BRK instruction interrupt, can be controlled by the interrupt request bit, interrupt enable bit, and an interrupt disable flag, as described in detail below. Figure 2.2.11 shows an interrupt control diagram.

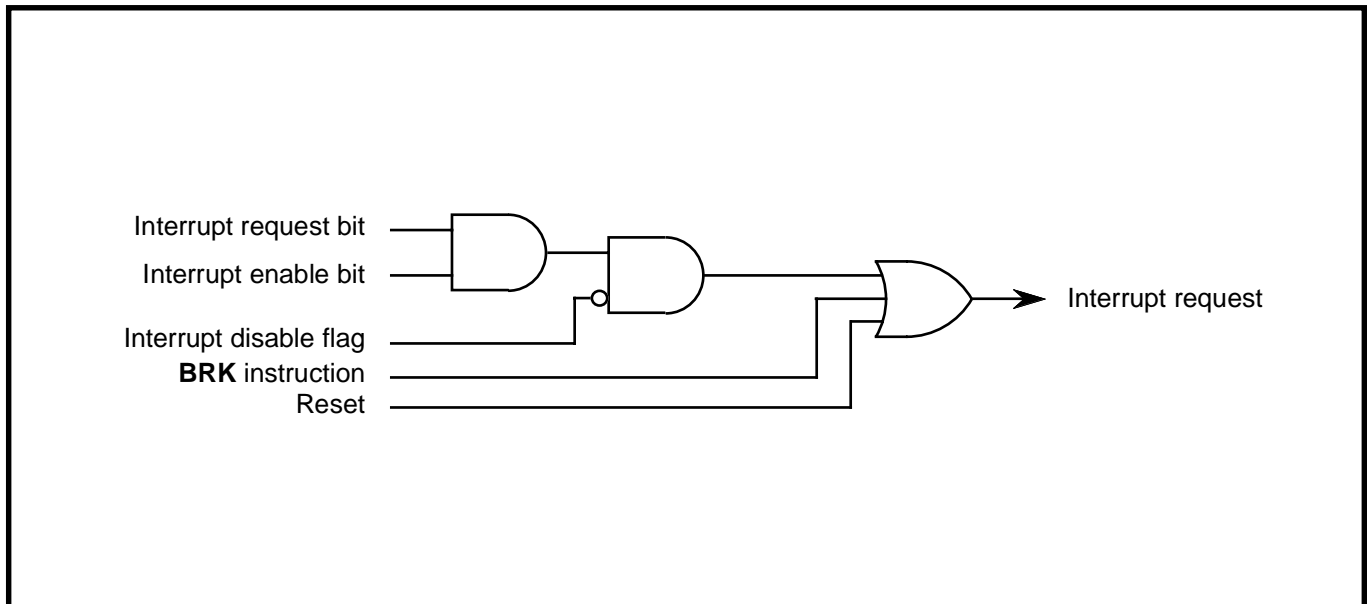


Fig. 2.2.11 Interrupt control diagram

The interrupt request bit, interrupt enable bit and interrupt disable flag function independently and do not affect each other. An interrupt is accepted when all the following conditions are satisfied.

- Interrupt request bit "1"
- Interrupt enable bit "1"
- Interrupt disable flag "0"

Though the interrupt priority is determined by hardware, a variety of priority processing can be performed by software using the above bits and flag. Table 2.2.2 shows a list of interrupt control bits according to the interrupt source.

(1) Interrupt request bits

The interrupt request bits are allocated to the interrupt request register 1 (address 3C₁₆) and interrupt request register 2 (address 3D₁₆).

The occurrence of an interrupt request causes the corresponding interrupt request bit to be set to "1". The interrupt request bit is held in the "1" state until the interrupt is accepted. When the interrupt is accepted, this bit is automatically cleared to "0".

Each interrupt request bit can be set to "0", but cannot be set to "1", by software.

(2) Interrupt enable bits

The interrupt enable bits are allocated to the interrupt control register 1 (address 003E₁₆) and the interrupt control register 2 (address 3F₁₆).

The interrupt enable bits control the acceptance of the corresponding interrupt request.

When an interrupt enable bit is "0", the corresponding interrupt request is disabled. If an interrupt request occurs when this bit is "0", the corresponding interrupt request bit is set to "1" but the interrupt is not accepted. In this case, unless the interrupt request bit is set to "0" by software, the interrupt request bit remains in the "1" state.

When an interrupt enable bit is "1", the corresponding interrupt is enabled. If an interrupt request occurs when this bit is "1", the interrupt is accepted (when interrupt disable flag = "0").

Each interrupt enable bit can be set to "0" or "1" by software.

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2.2 Interrupt

(3) Interrupt disable flag

The interrupt disable flag is allocated to bit 2 of the processor status register. The interrupt disable flag controls the acceptance of interrupt request except BRK instruction.

When this flag is “1”, the acceptance of interrupt requests is disabled. When the flag is “0”, the acceptance of interrupt requests is enabled. This flag is set to “1” with the SEI instruction and is set to “0” with the CLI instruction.

When a main routine branches to an interrupt processing routine, this flag is automatically set to “1”, so that multiple interrupts are disabled. To use multiple interrupts, set this flag to “0” with the CLI instruction within the interrupt processing routine. Figure 2.2.12 shows an example of multiple interrupts.

Table 2.2.2 List of interrupt bits according to interrupt source

Interrupt source	Interrupt enable bit		Interrupt request bit	
	Address	Bit	Address	Bit
USB bus reset	003E ₁₆	b0	003C ₁₆	b0
USB SOF	003E ₁₆	b1	003C ₁₆	b1
USB device	003E ₁₆	b2	003C ₁₆	b2
External bus	003E ₁₆	b3	003C ₁₆	b3
INT ₀	003E ₁₆	b4	003C ₁₆	b4
Timer X	003E ₁₆	b5	003C ₁₆	b5
Timer 1	003E ₁₆	b6	003C ₁₆	b6
Timer 2	003E ₁₆	b7	003C ₁₆	b7
INT ₁	003F ₁₆	b0	003D ₁₆	b0
Serial I/O receive	003F ₁₆	b2	003D ₁₆	b2
Serial I/O transmit	003F ₁₆	b3	003D ₁₆	b3
CNTR ₀	003F ₁₆	b4	003D ₁₆	b4
Key-on wake-up	003F ₁₆	b5	003D ₁₆	b5
A-D converter	003F ₁₆	b6	003D ₁₆	b6

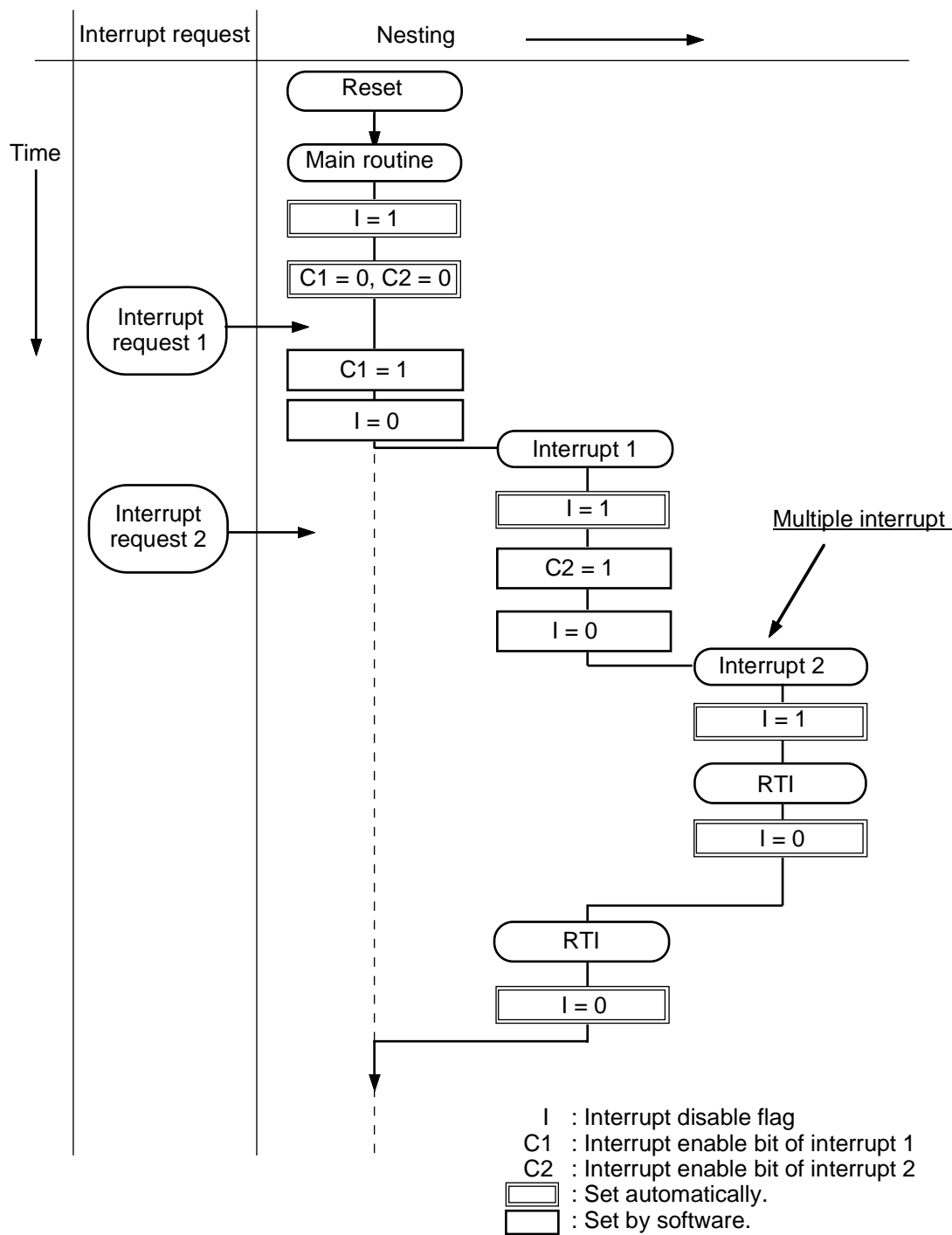


Fig. 2.2.12 Example of multiple interrupts

APPLICATION

2.2 Interrupt

2.2.6 INT interrupt

The INT interrupt requests is generated when the microcomputer detects a level change of each INT pin (INT₀, INT₁).

(1) Active edge selection

INT₀ and INT₁ can be selected from either a falling edge or rising edge detection as an active edge by the interrupt edge selection register. In the “0” state, the falling edge of the corresponding pin is detected. In the “1” state, the rising edge of the corresponding pin is detected.

2.2.7 Key input interrupt

A key input interrupt request is generated by applying “L” level to any port P0 pin that has been set to the input mode. In other words, it is generated when AND of the input level goes from “1” to “0”.

(1) Connection example when Key input interrupt is used

When using the Key input interrupt, compose an active-low key matrix which inputs to port P0. Figure 2.2.13 shows a connection example and the port P0 block diagram when using a key input interrupt. In the connection example in Figure 2.2.13, a key input interrupt request is generated by pressing one of the keys corresponding to ports P0₀ to P0₃.

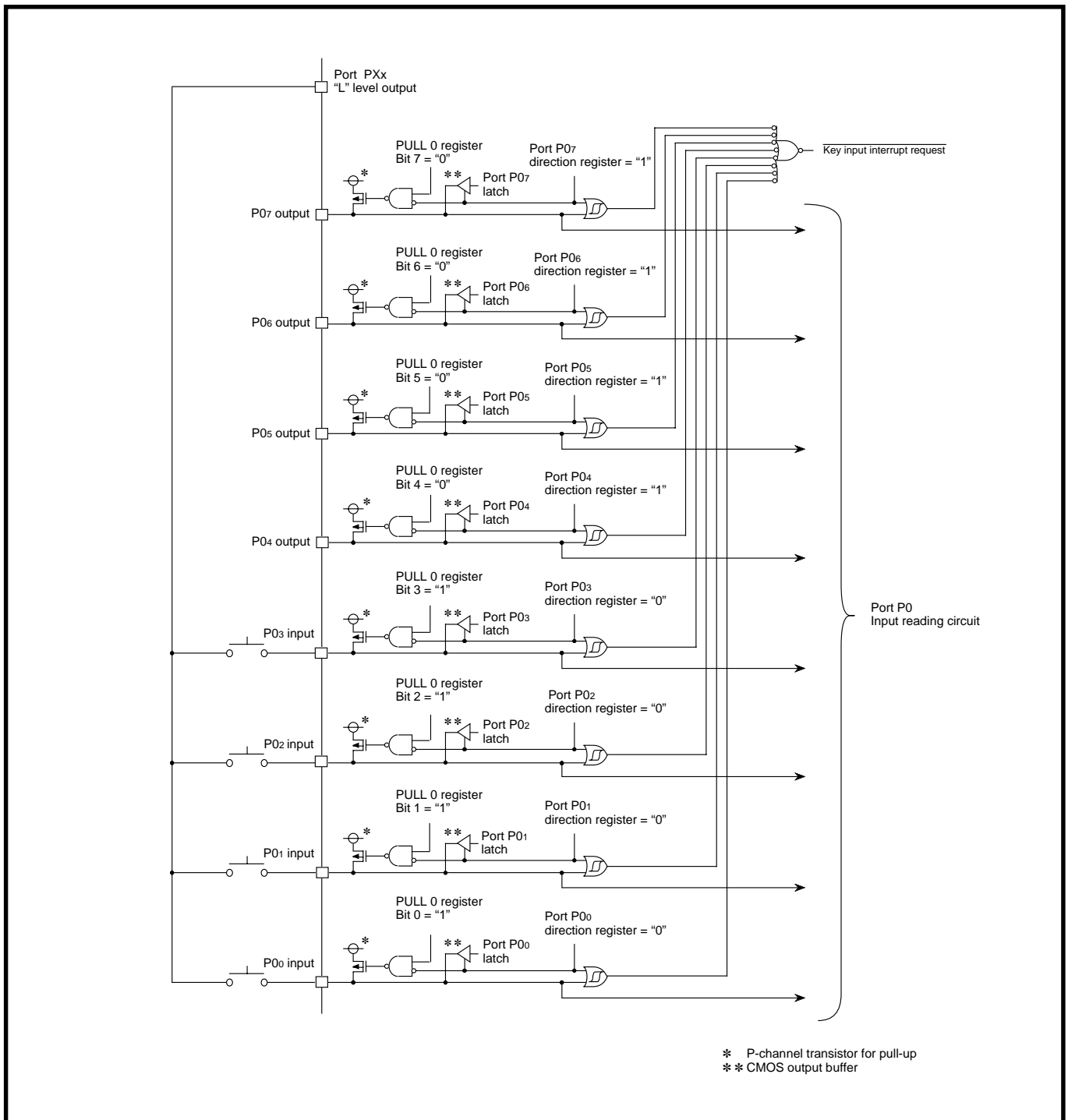


Fig. 2.2.13 Connection example and port P0 block diagram when using key input interrupt

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2.2 Interrupt

(2) Related registers setting

Figure 2.2.14 shows the related registers setting (corresponding to Figure 2.2.13).

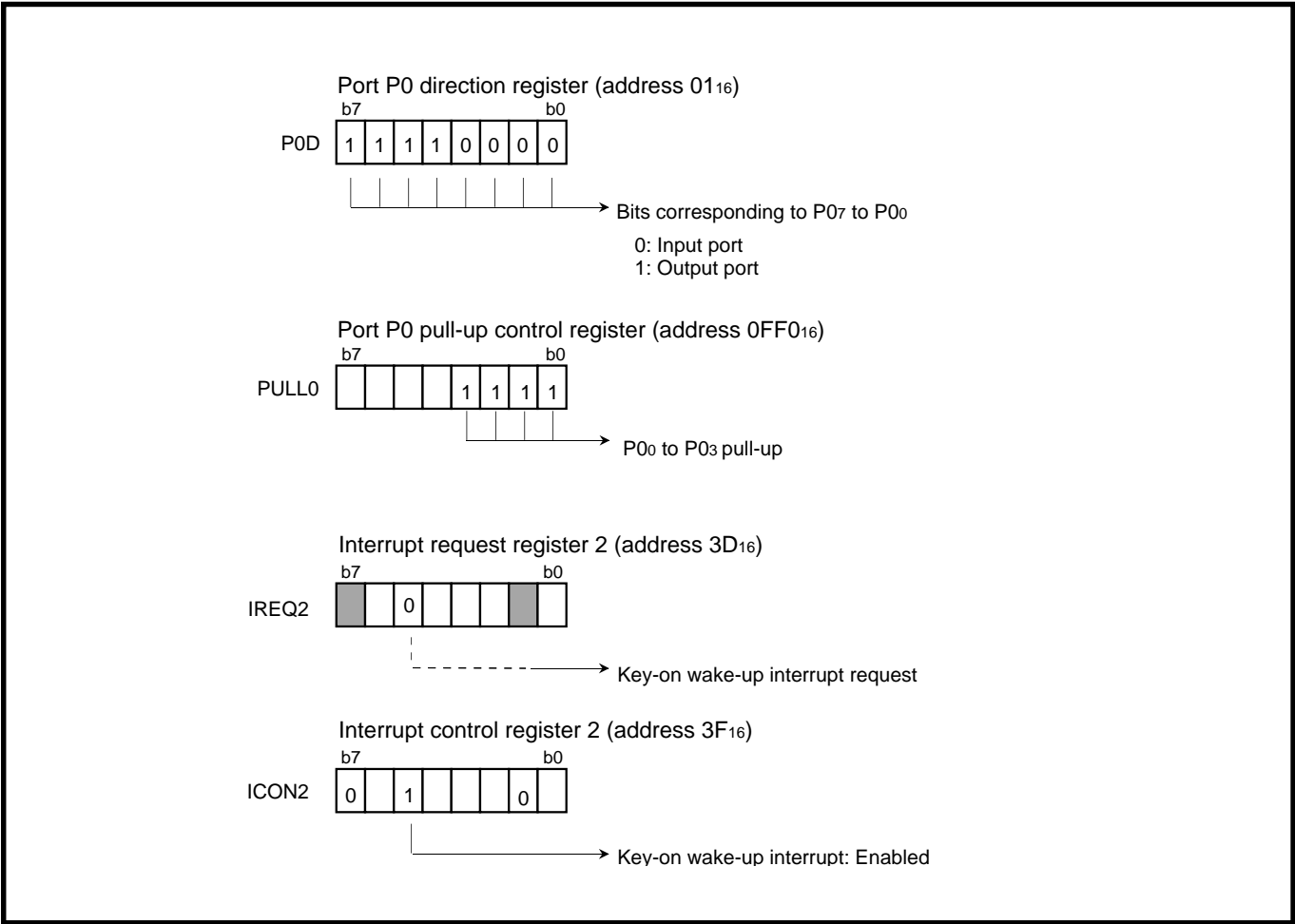


Fig. 2.2.14 Registers setting related to key input interrupt (corresponding to Figure 2.2.13)

2.2.8 Notes on interrupts

(1) Change of relevant register settings

When the setting of the following registers or bits is changed, the interrupt request bit may be set to "1". When not requiring the interrupt occurrence synchronized with these setting, take the following sequence.

- Interrupt edge selection register (address $0FF3_{16}$)
- Timer X mode register (address 23_{16})

Set the above listed registers or bits as the following sequence.

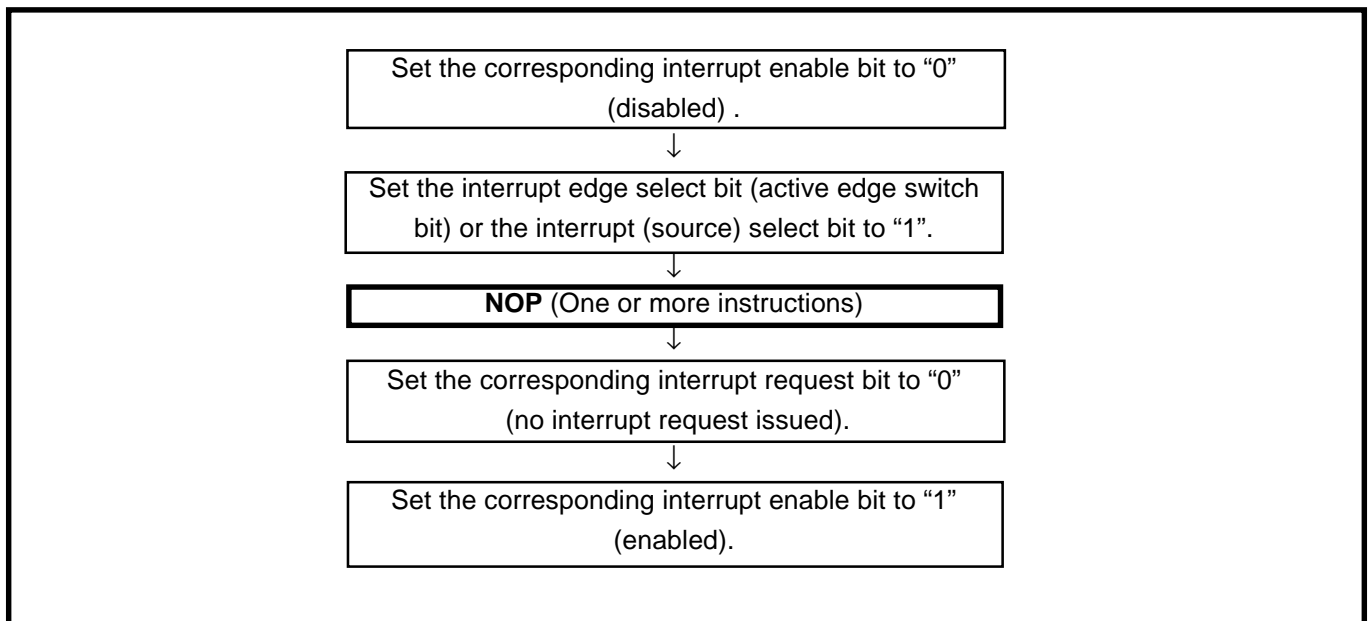


Fig. 2.2.15 Sequence of changing relevant register

■ Reason

When setting the following, the interrupt request bit may be set to "1".

- When setting external interrupt active edge

Concerned register: Interrupt edge selection register (address $0FF3_{16}$)

Timer X mode register (address 23_{16})

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2.2 Interrupt

(2) Check of interrupt request bit

- When executing the **BBC** or **BBS** instruction to an interrupt request bit of an interrupt request register immediately after this bit is set to "0" by using a data transfer instruction, execute one or more instructions before executing the **BBC** or **BBS** instruction.

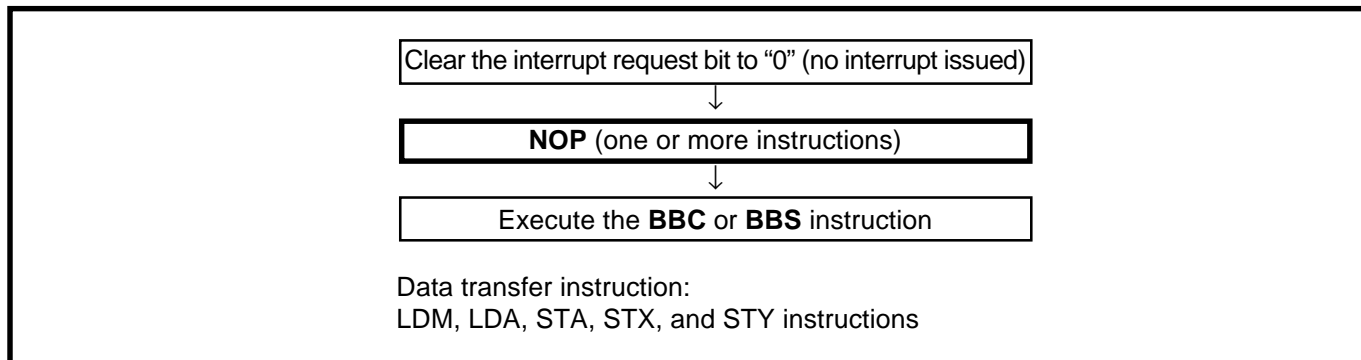


Fig. 2.2.16 Sequence of check of interrupt request bit

■ Reason

If the BBC or BBS instruction is executed immediately after an interrupt request bit of an interrupt request register is cleared to "0", the value of the interrupt request bit before being cleared to "0" is read.

2.3 Timer

This paragraph explains the registers setting method and the notes related to the timers.

2.3.1 Memory map

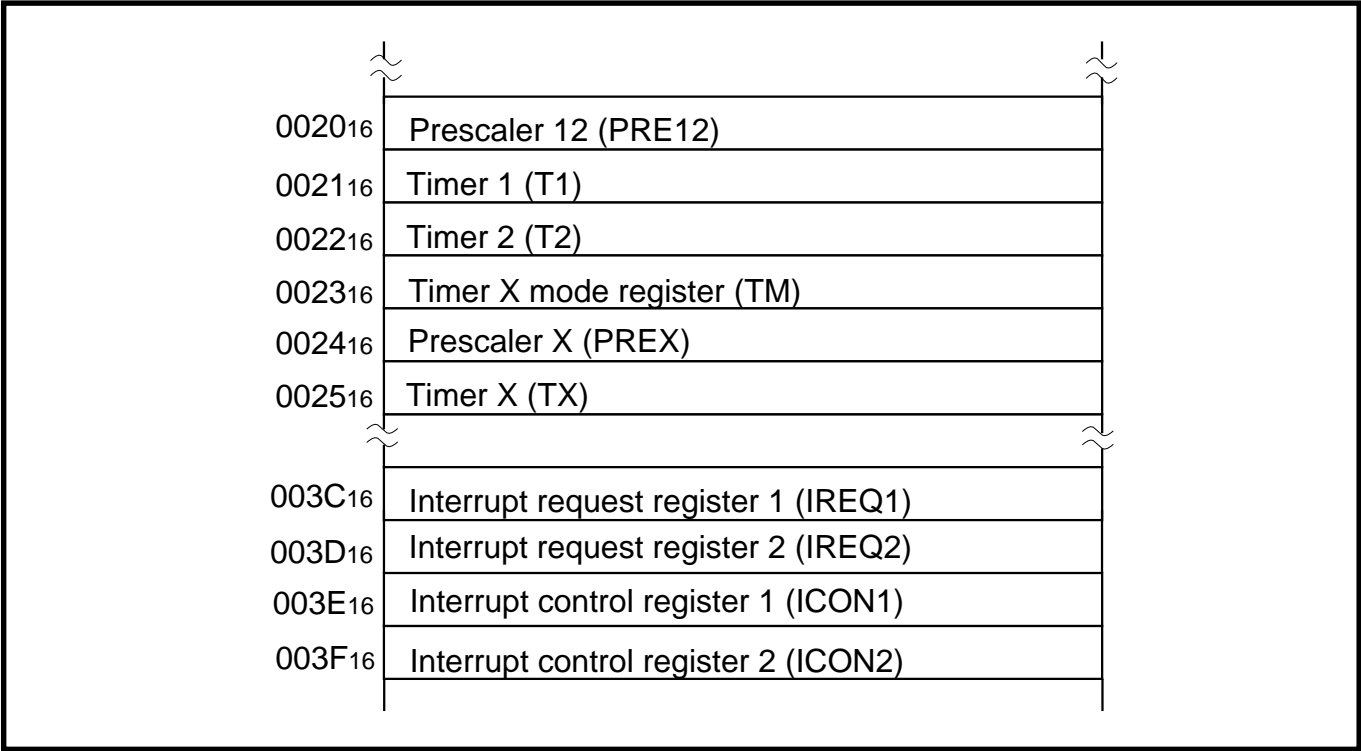


Fig. 2.3.1 Memory map of registers related to timers

2.3.2 Related registers

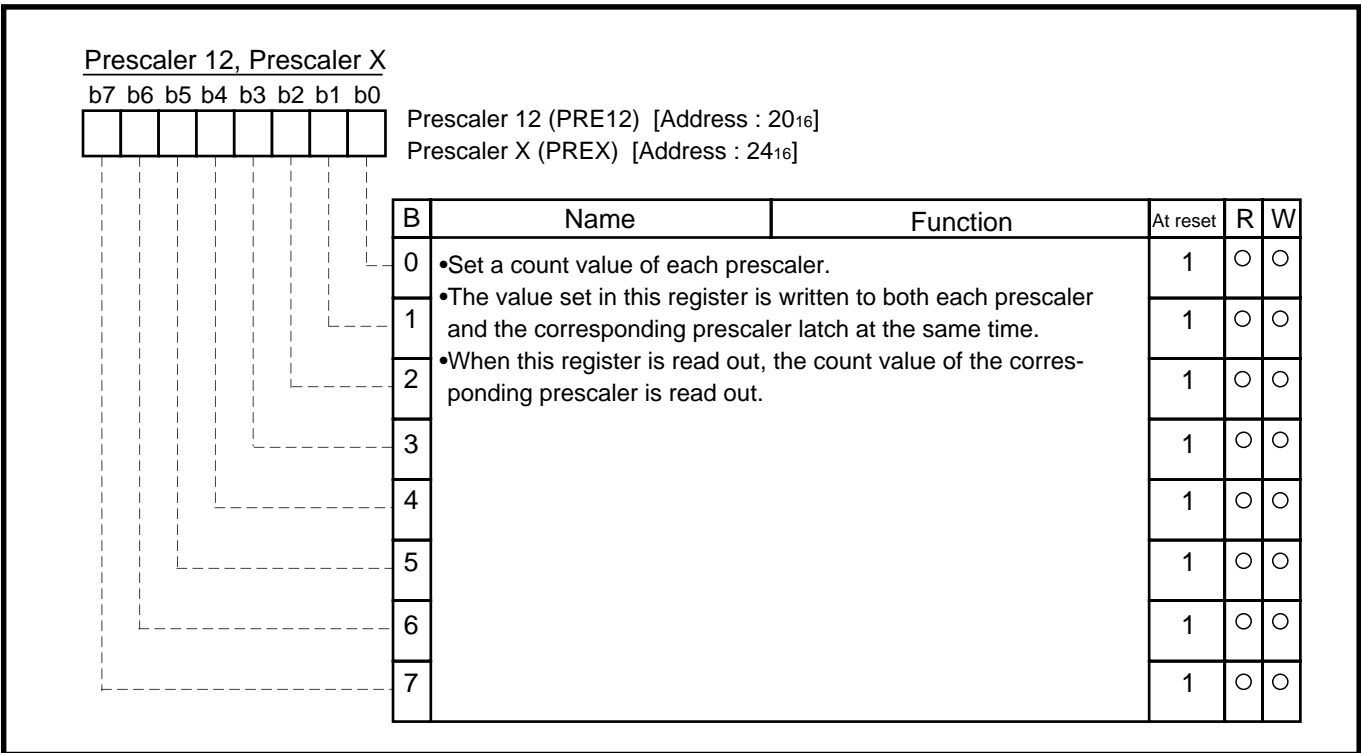


Fig. 2.3.2 Structure of Prescaler 12, Prescaler X

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2.3 Timer

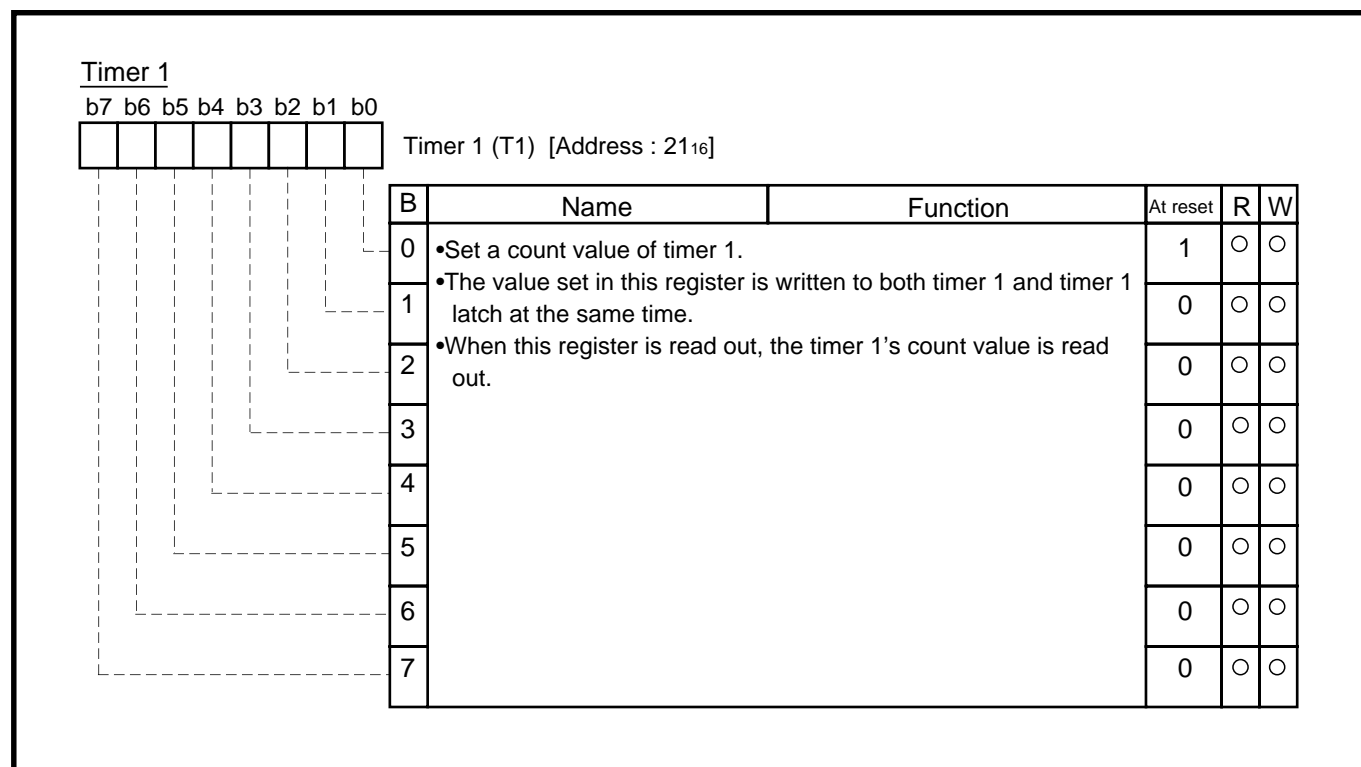


Fig. 2.3.3 Structure of Timer 1

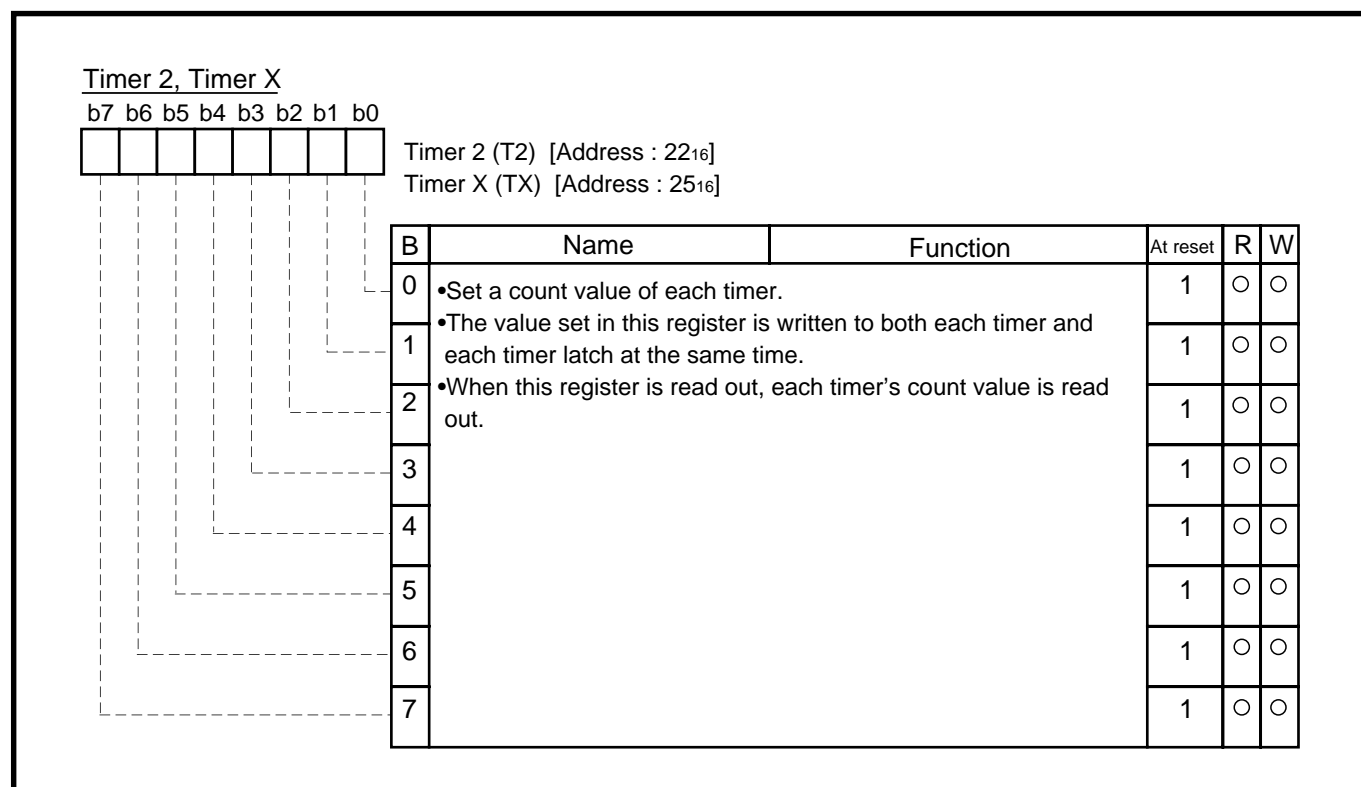


Fig. 2.3.4 Structure of Timer 2, Timer X

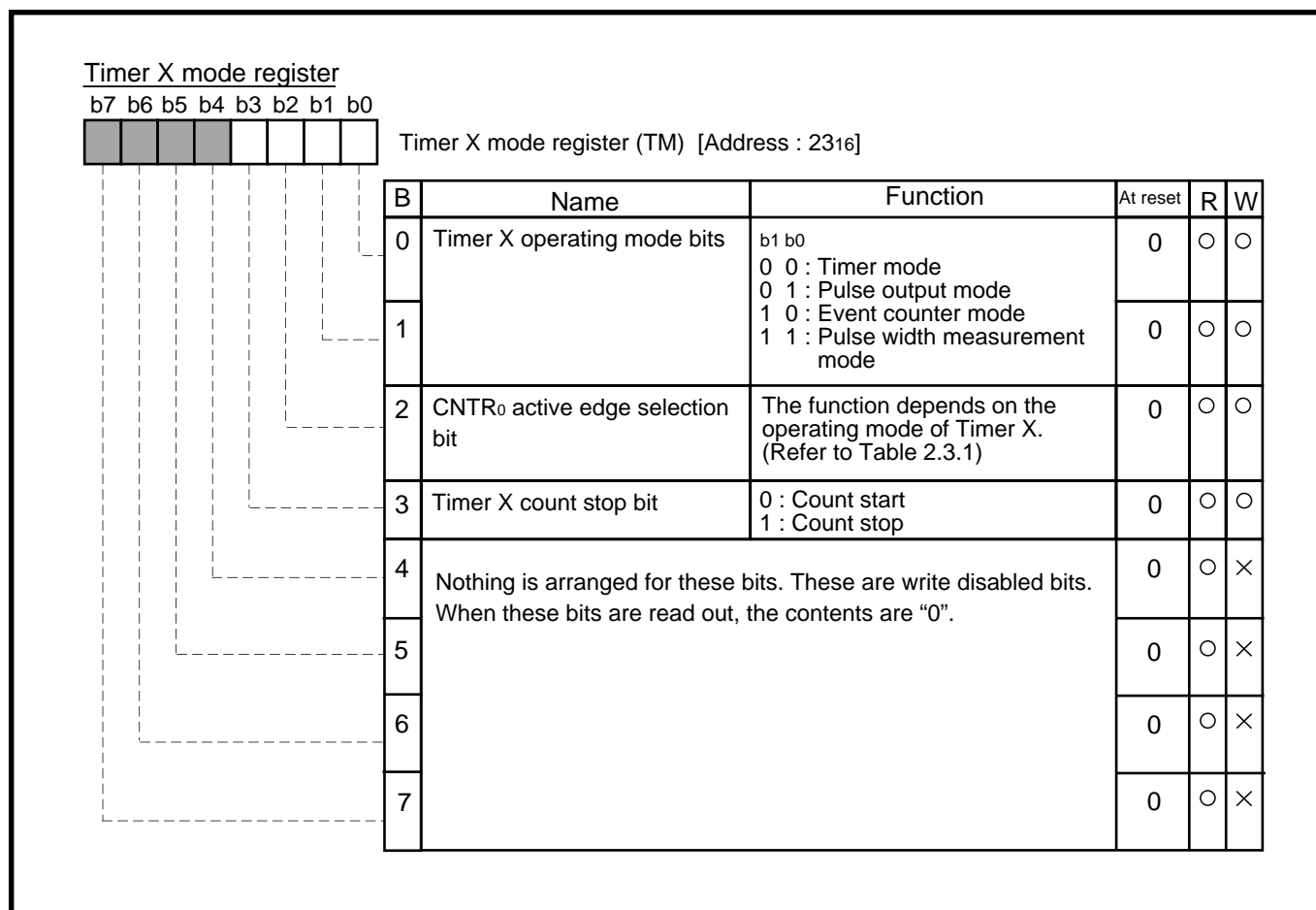


Fig. 2.3.5 Structure of Timer X mode register

Table 2.3.1 CNTR₀ active edge selection bit function

Timer X operation modes	CNTR ₀ active edge selection bit (bits 2 of address 23 ₁₆) contents	
Timer mode	"0"	CNTR ₀ interrupt request occurrence: Falling edge ; No influence to timer count
	"1"	CNTR ₀ interrupt request occurrence: Rising edge ; No influence to timer count
Pulse output mode	"0"	Pulse output start: Beginning at "H" level CNTR ₀ interrupt request occurrence: Falling edge
	"1"	Pulse output start: Beginning at "L" level CNTR ₀ interrupt request occurrence: Rising edge
Event counter mode	"0"	Timer X: Rising edge count CNTR ₀ interrupt request occurrence: Falling edge
	"1"	Timer X: Falling edge count CNTR ₀ interrupt request occurrence: Rising edge
Pulse width measurement mode	"0"	Timer X: "H" level width measurement CNTR ₀ interrupt request occurrence: Falling edge
	"1"	Timer X: "L" level width measurement CNTR ₀ interrupt request occurrence: Rising edge

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2.3 Timer

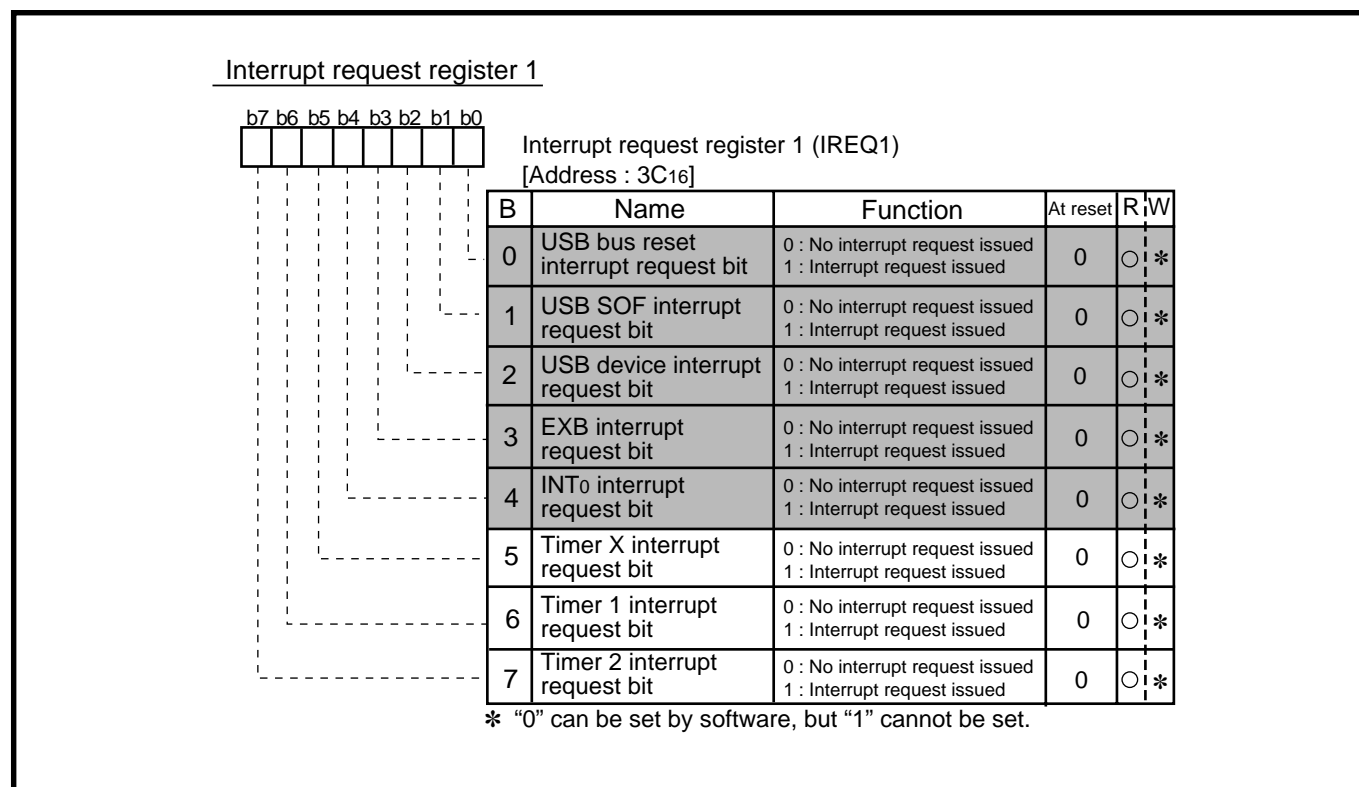


Fig. 2.3.6 Structure of Interrupt request register 1

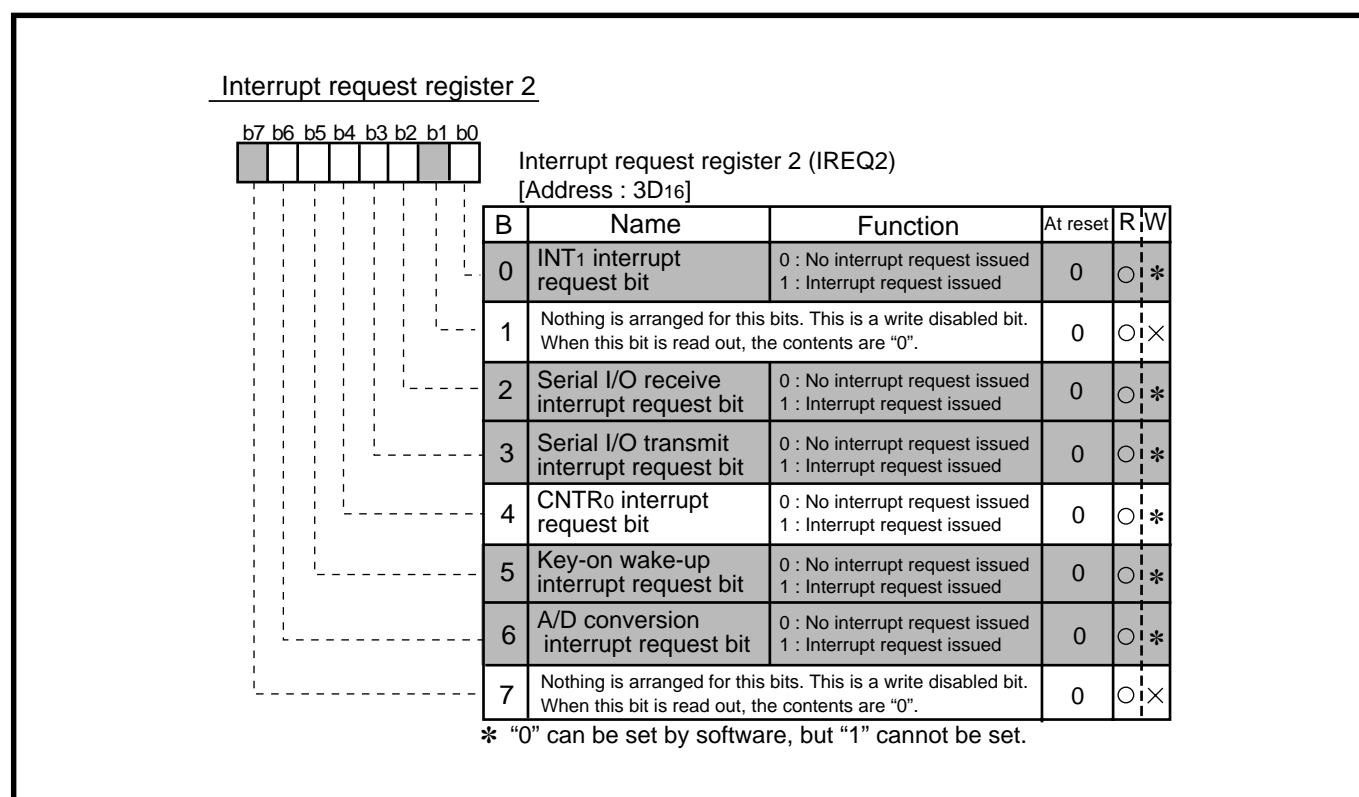
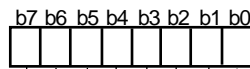


Fig. 2.3.7 Structure of Interrupt request register 2

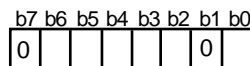
Interrupt control register 1

Interrupt control register 1 (ICON1)
[Address : 3E16]

B	Name	Function	At reset	R	W
0	USB bus reset interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
1	USB SOF interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
2	USB device interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
3	EXB interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
4	INTo interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
5	Timer X interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
6	Timer 1 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
7	Timer 2 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○

Fig. 2.3.8 Structure of Interrupt control register 1

Interrupt control register 2

Interrupt control register 2 (ICON2)
[Address : 3D16]

B	Name	Function	At reset	R	W
0	INT ₁ interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
1	Fix this bit to "0".		0	○	○
2	Serial I/O receive interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
3	Serial I/O transmit interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
4	CNTRo interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
5	Key-on wake-up interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
6	A/D conversion interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○
7	Fix this bit to "0".		0	○	○

Fig. 2.3.9 Structure of Interrupt control register 2

APPLICATION

2.3 Timer

2.3.3 Timer application examples

(1) Basic functions and uses

[Function 1] Control of Event interval (Timer X, Timer 1, Timer 2)

When a certain time, by setting a count value to each timer, has passed, the timer interrupt request occurs.

<Use>

- Generation of an output signal timing
- Generation of a wait time

[Function 2] Control of Cyclic operation (Timer X, Timer 1, Timer 2)

The value of the timer latch is automatically written to the corresponding timer each time the timer underflows, and each timer interrupt request occurs in cycles.

<Use>

- Generation of cyclic interrupts
- Clock function (measurement of 10 ms); see Application example 1
- Control of a main routine cycle

[Function 3] Output of Rectangular waveform (Timer X)

The output level of the CNTR₀ pin is inverted each time the timer underflows (in the pulse output mode).

<Use>

- Piezoelectric buzzer output; see Application example 2
- Generation of the remote control carrier waveforms

[Function 4] Count of External pulses (Timer X)

External pulses input to the CNTR₀ pin are counted as the timer count source (in the event counter mode).

<Use>

- Frequency measurement; see Application example 3
- Division of external pulses
- Generation of interrupts due to a cycle using external pulses as the count source; count of a reel pulse

[Function 5] Measurement of External pulse width (Timer X)

The “H” or “L” level width of external pulses input to CNTR₀ pin is measured (in the pulse width measurement mode).

<Use>

- Measurement of external pulse frequency (measurement of pulse width of FG pulse* for a motor); see Application example 4
- Measurement of external pulse duty (when the frequency is fixed)

FG pulse*: Pulse used for detecting the motor speed to control the motor speed.

(2) Timer application example 1: Clock function (measurement of 10 ms)

Outline: The input clock is divided by the timer so that the clock can count up at 10 ms intervals.

Specifications: •The clock $f(X_{IN}) = 6\text{ MHz}$ is divided by the timer.

- The clock is counted up in the process routine of the timer X interrupt which occurs at 10 ms intervals.

Figure 2.3.10 shows the timers connection and setting of division ratios; Figure 2.3.11 shows the related registers setting; Figure 2.3.12 shows the control procedure.

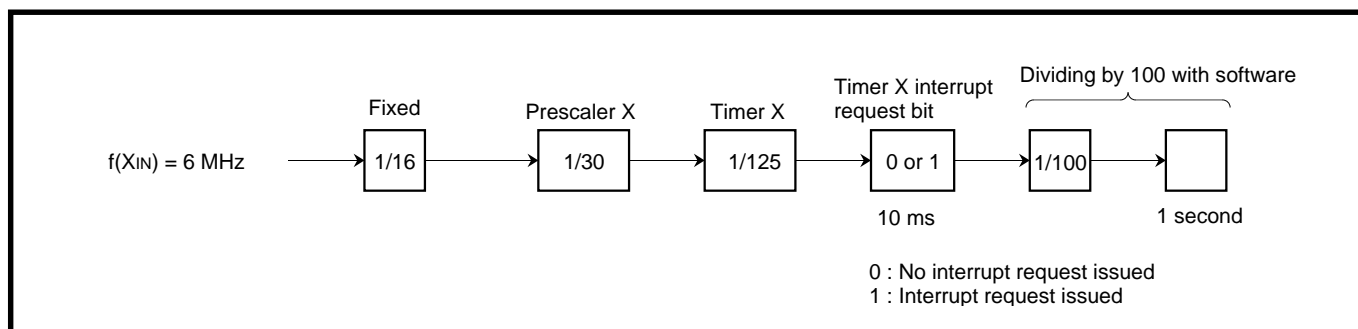


Fig. 2.3.10 Timers connection and setting of division ratios

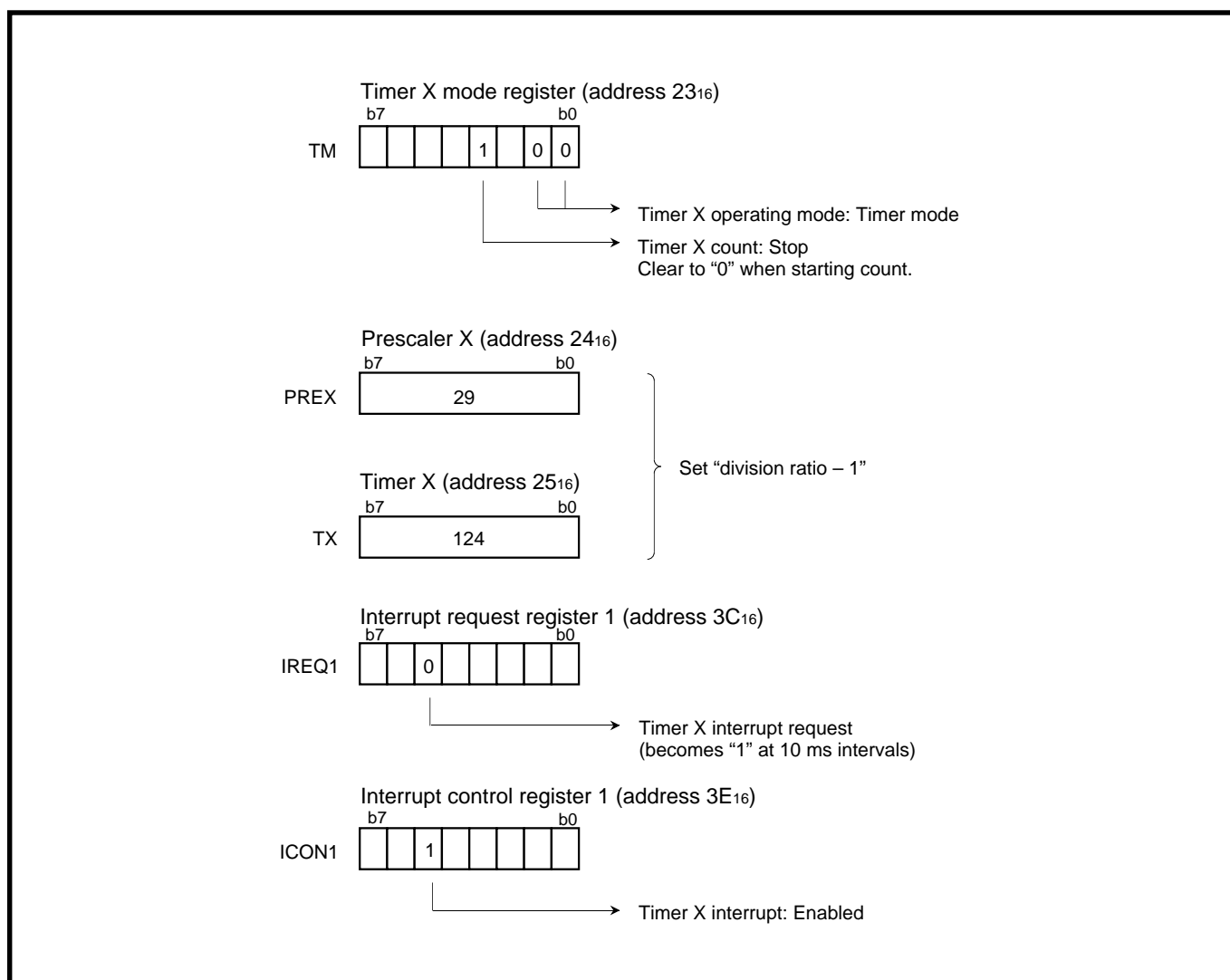


Fig. 2.3.11 Related registers setting

APPLICATION

2.3 Timer

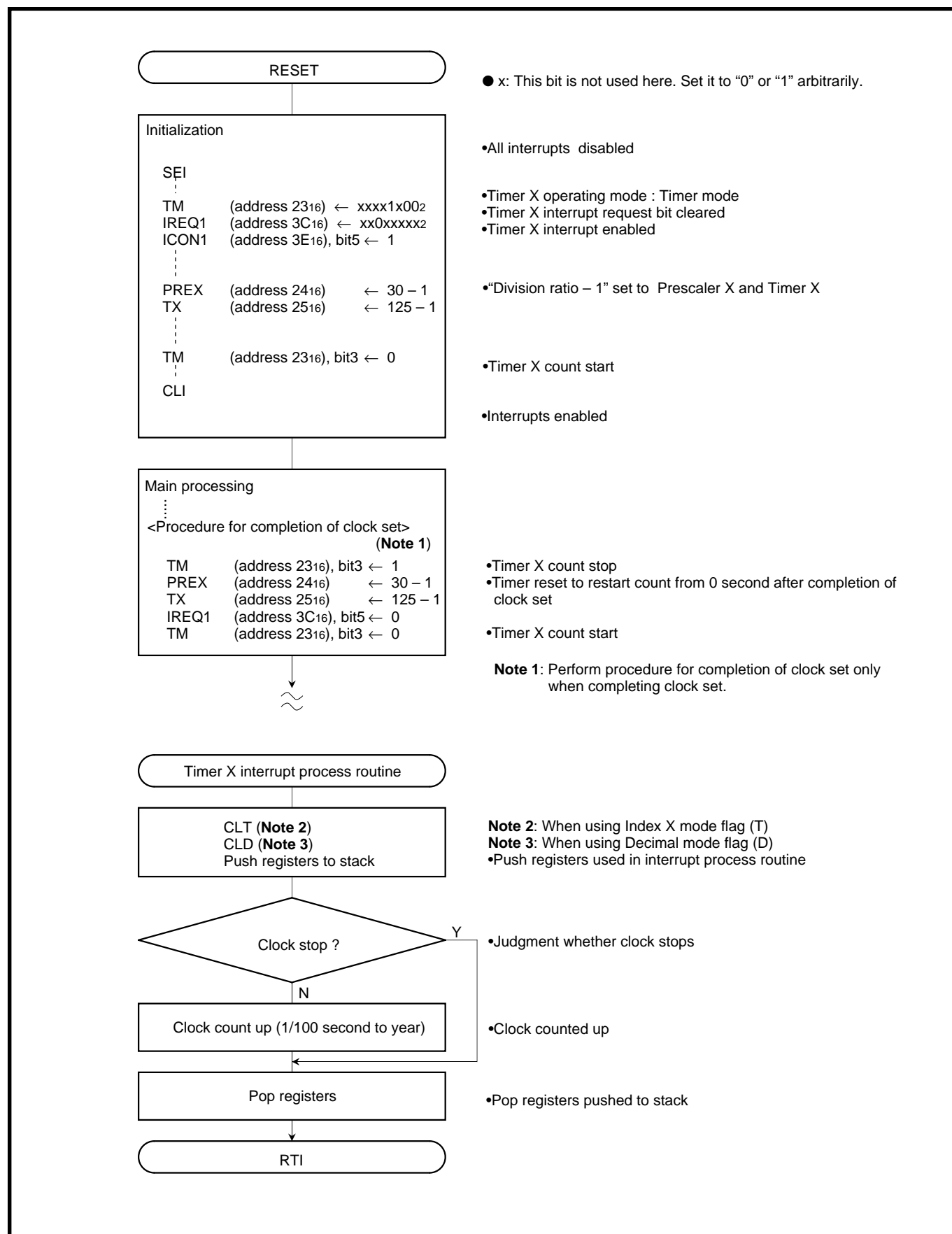


Fig. 2.3.12 Control procedure

(3) Timer application example 2: Piezoelectric buzzer output

Outline: The rectangular waveform output function of the timer is applied for a piezoelectric buzzer output.

Specifications:

- The rectangular waveform, dividing the clock $f(X_{IN}) = 6 \text{ MHz}$ into about 2 kHz (2038 Hz), is output from the P5₁/CNTR₀ pin.
- The level of the P5₁/CNTR₀ pin is fixed to “H” while a piezoelectric buzzer output stops.

Figure 2.3.13 shows a peripheral circuit example, and Figure 2.3.14 shows the timers connection and setting of division ratios. Figures 2.3.15 shows the related registers setting, and Figure 2.3.16 shows the control procedure.

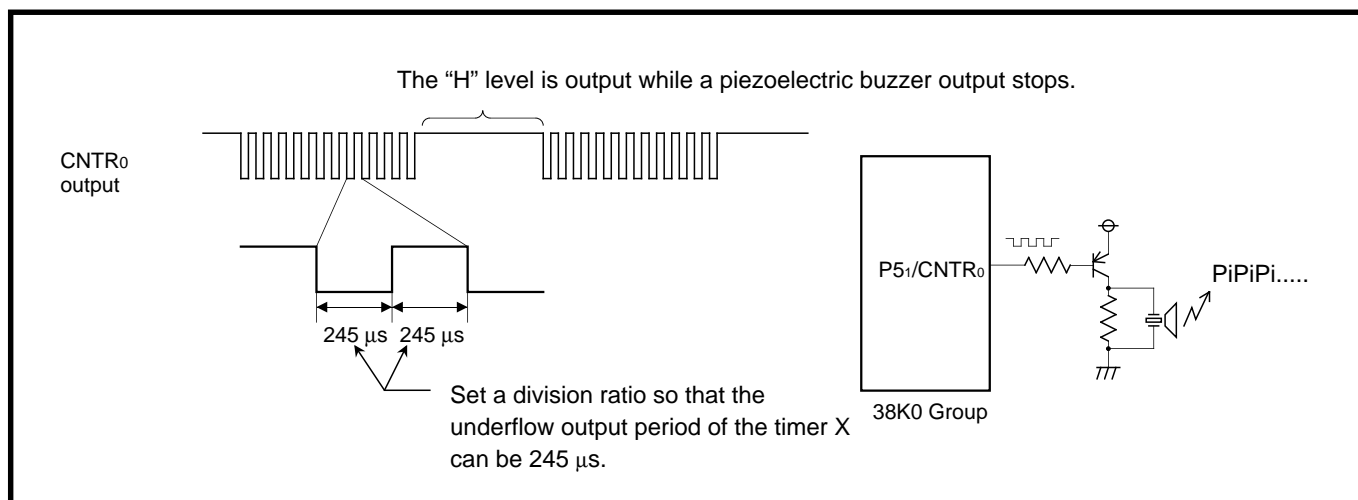


Fig. 2.3.13 Peripheral circuit example

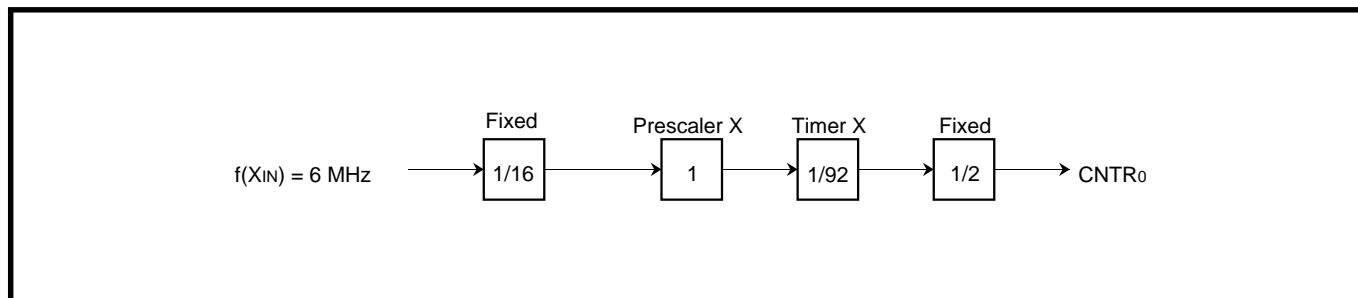


Fig. 2.3.14 Timers connection and setting of division ratios

APPLICATION

2.3 Timer

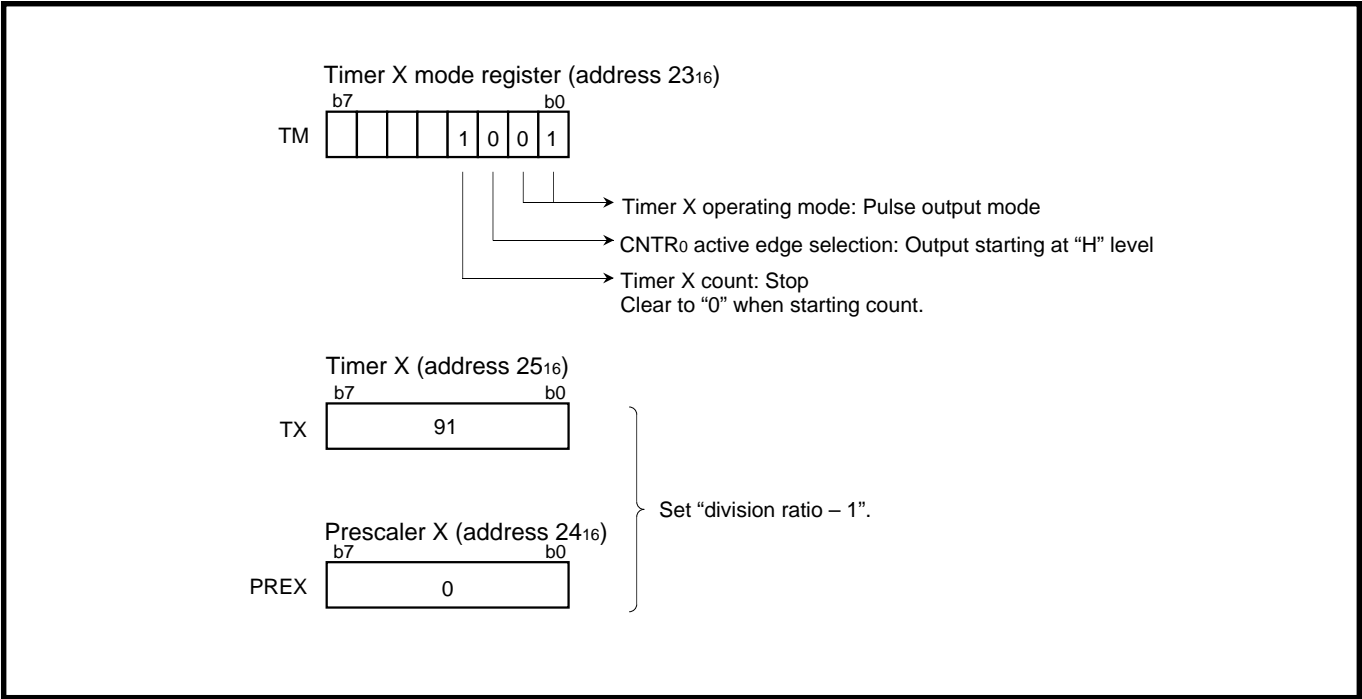


Fig. 2.3.15 Related registers setting

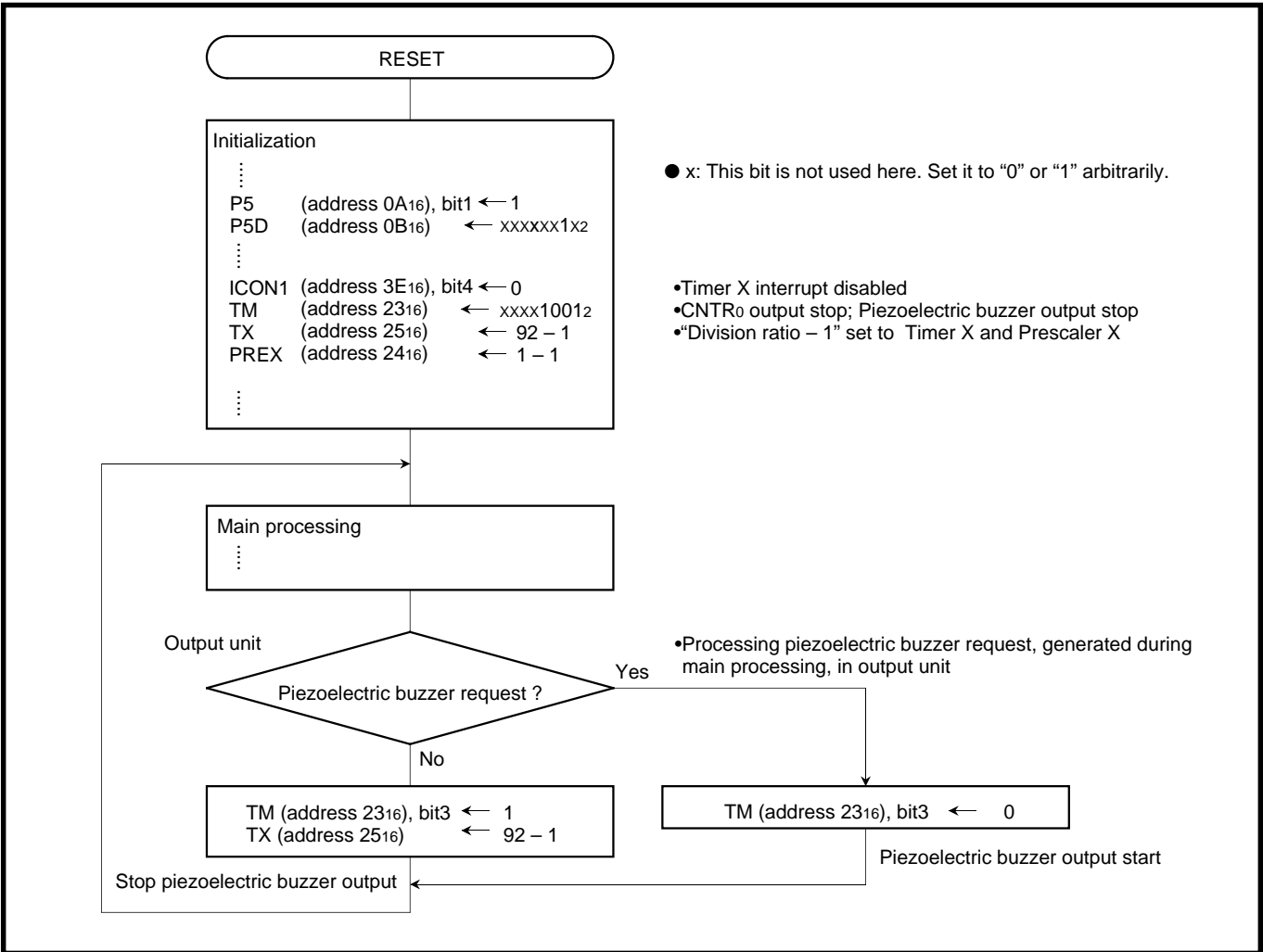


Fig. 2.3.16 Control procedure

(4) Timer application example 3: Frequency measurement

Outline: The following two values are compared to judge whether the frequency is within a valid range.

- A value by counting pulses input to P5₁/CNTR₀ pin with the timer.
- A reference value

Specifications:

- The pulse is input to the P5₁/CNTR₀ pin and counted by the timer X.
- A count value is read out at about 2 ms intervals, the timer 1 interrupt interval. When the count value is 28 to 40, it is judged that the input pulse is valid.
- Because the timer is a down-counter, the count value is compared with 227 to 215 (Note).

Note: 227 to 215 = {255 (initial value of counter) – 28} to {255 – 40}; 28 to 40 means the number of valid value.

Figure 2.3.17 shows the judgment method of valid/invalid of input pulses; Figure 2.3.18 shows the related registers setting; Figure 2.3.19 shows the control procedure.

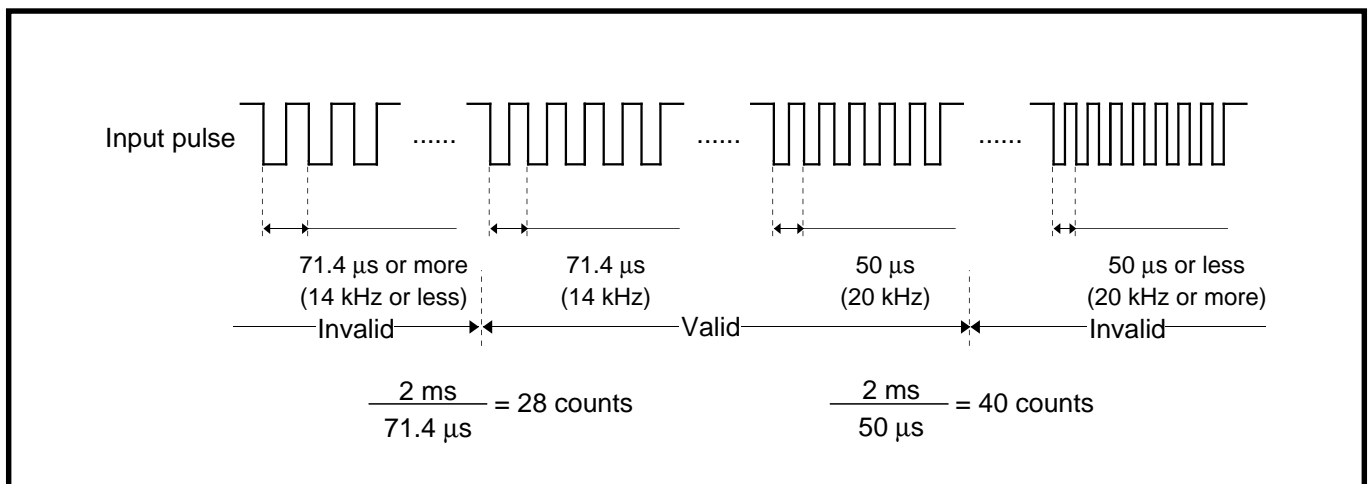


Fig. 2.3.17 Judgment method of valid/invalid of input pulses

APPLICATION

2.3 Timer

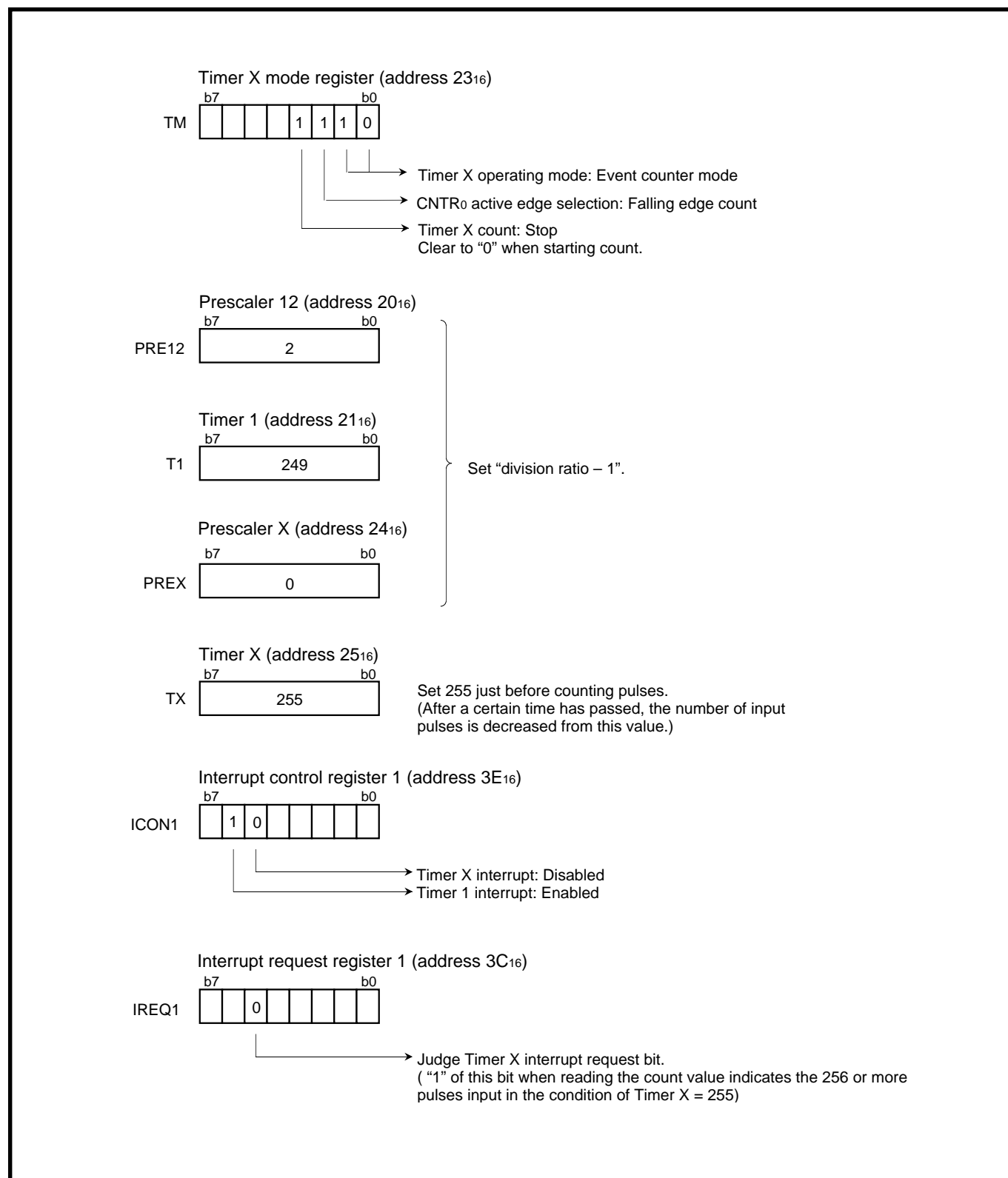


Fig. 2.3.18 Related registers setting

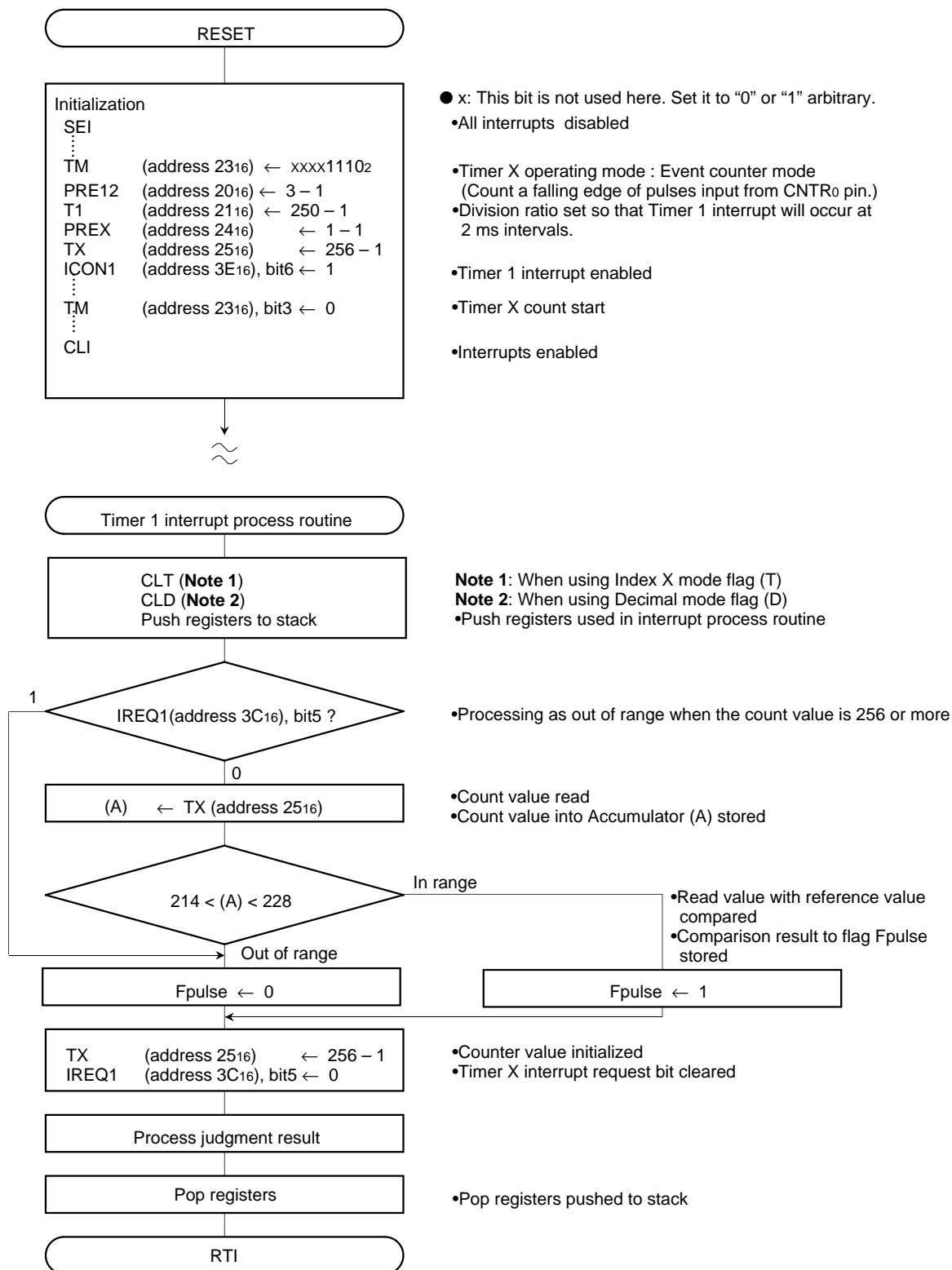


Fig. 2.3.19 Control procedure

APPLICATION

2.3 Timer

(5) Timer application example 4: Measurement of FG pulse width for motor

Outline: The timer X counts the “H” level width of the pulses input to the P5₁/CNTR₀ pin. An underflow is detected by the timer X interrupt and an end of the input pulse “H” level is detected by the CNTR₀ interrupt.

Specifications: •The timer X counts the “H” level width of the FG pulse input to the P5₁/CNTR₀ pin.

<Example>

When the clock frequency is 6 MHz, the count source is 2.67 μ s, which is obtained by dividing the clock frequency by 16. Measurement can be performed to 175 ms in the range of FFFF₁₆ to 0000₁₆.

Figure 2.3.20 shows the timers connection and setting of division ratio; Figure 2.3.21 shows the related registers setting; Figure 2.3.22 shows the control procedure.

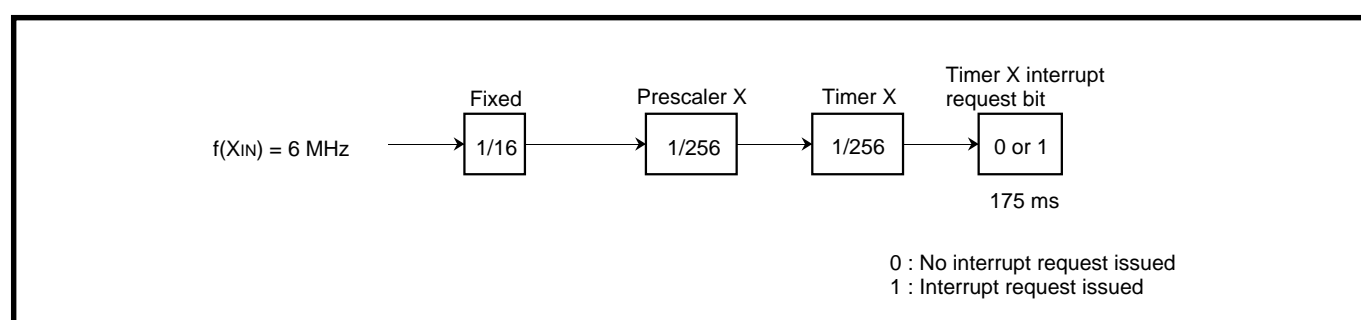


Fig. 2.3.20 Timers connection and setting of division ratios

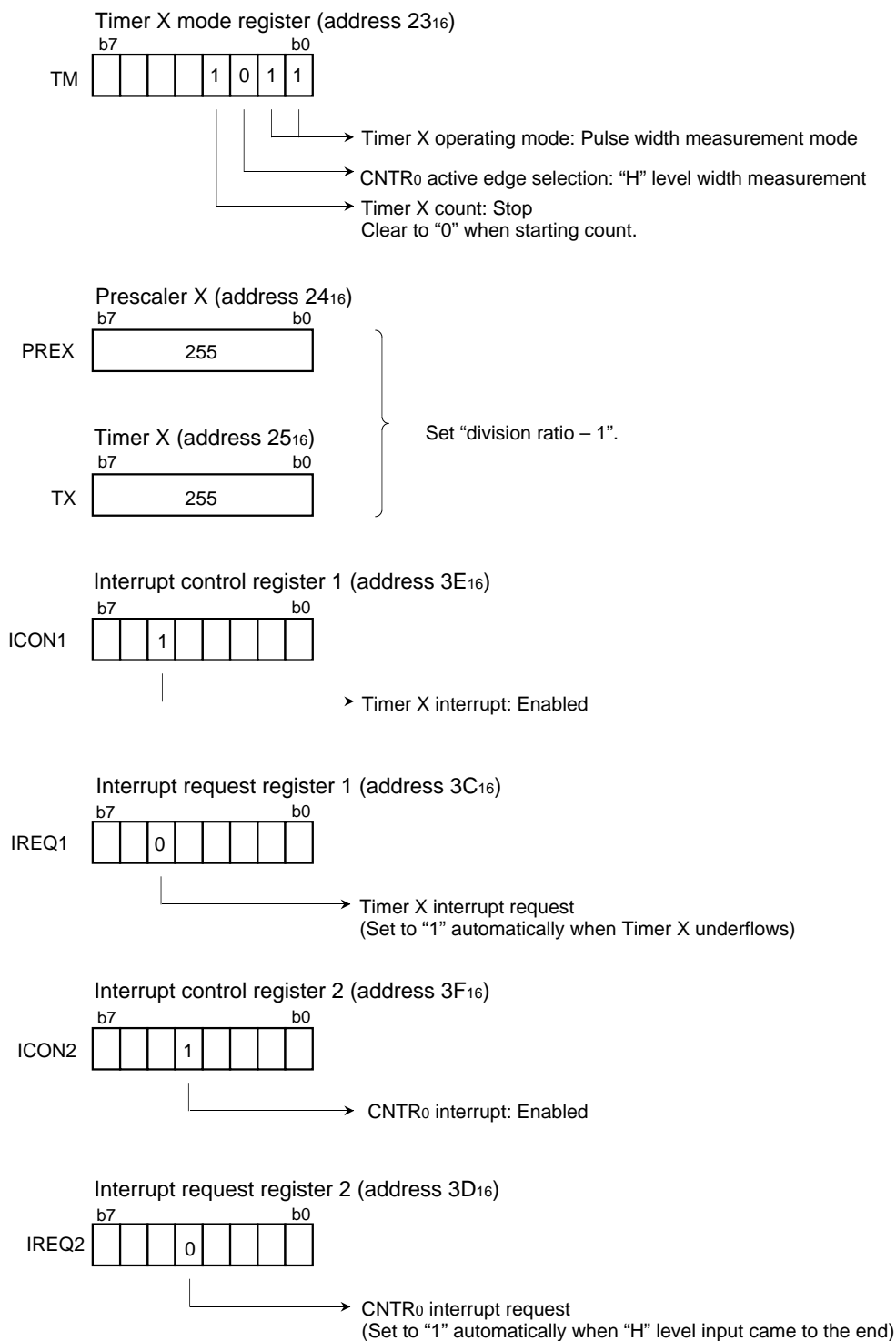


Fig. 2.3.21 Related registers setting

APPLICATION

2.3 Timer

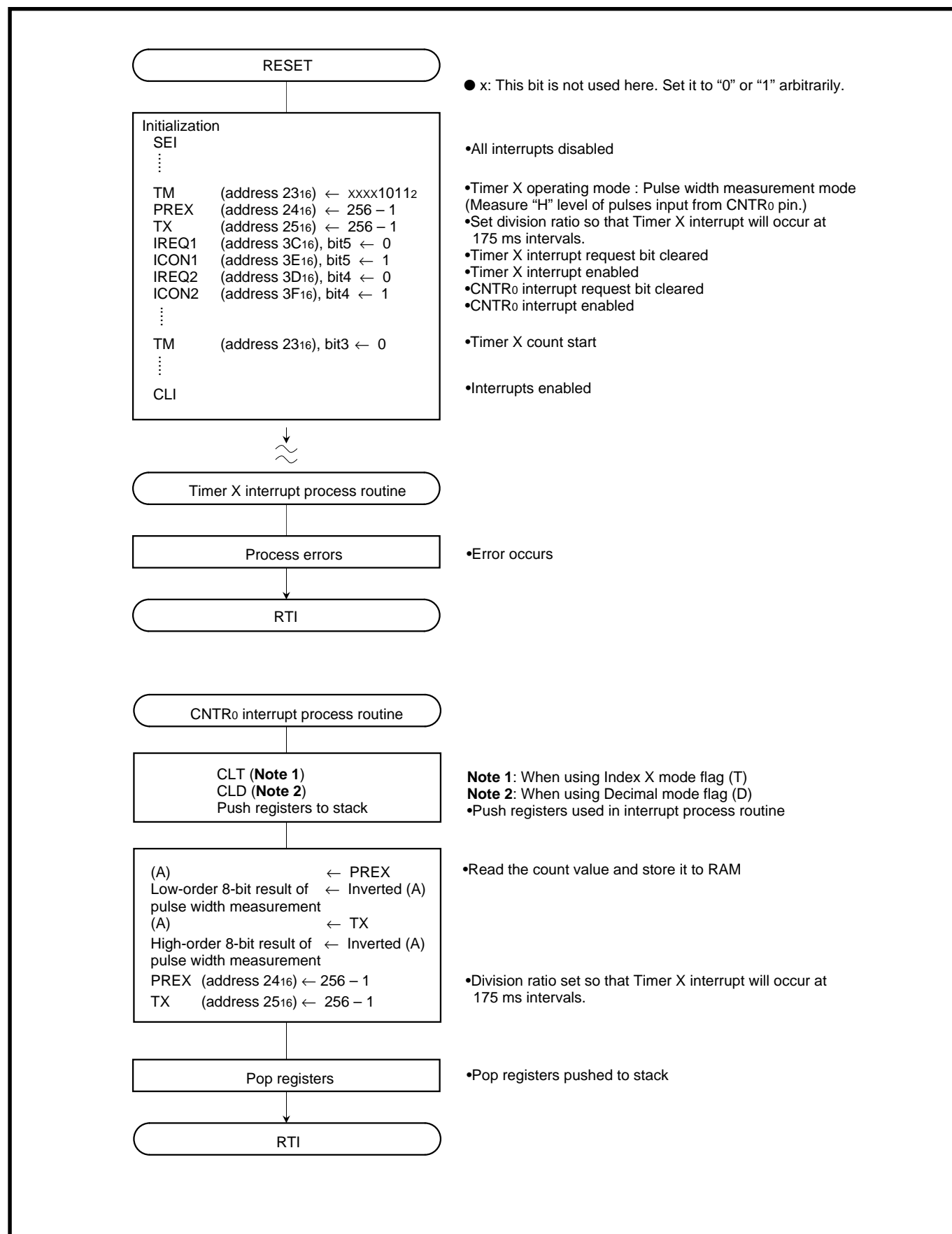


Fig. 2.3.22 Control procedure

2.3.4 Notes on timer

- If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is $1/(n+1)$.
- When switching the count source by the timer X count source selection bit, the value of timer count is altered in unconsiderable amount owing to generating of a thin pulses in the count input signals. Therefore, select the timer count source before set the value to the prescaler and the timer.

APPLICATION

2.4 Serial I/O

2.4 Serial I/O

This paragraph explains the registers setting method and the notes related to the Serial I/O.

2.4.1 Memory map

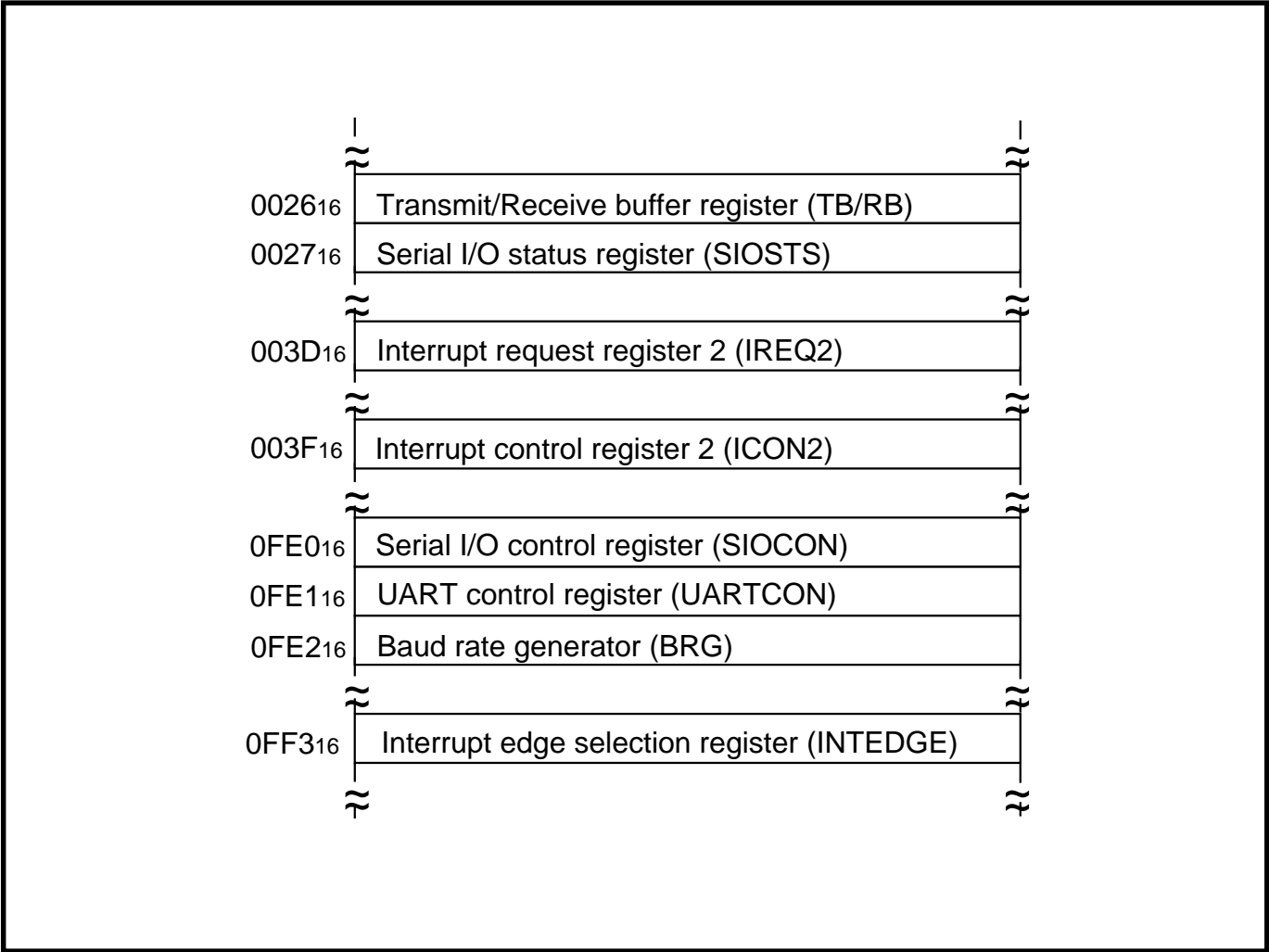
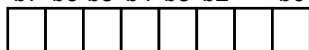


Fig. 2.4.1 Memory map of registers related to Serial I/O

2.4.2 Related registers

Transmit/Receive buffer register

b7 b6 b5 b4 b3 b2 b1 b0

Transmit/Receive buffer register (TB/RB) [Address : 26₁₆]

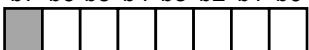
B	Name	Function	At reset	R	W
0		The transmission data is written to or the receive data is read out from this buffer register. • At writing: A data is written to the transmit buffer register. • At reading: The contents of the receive buffer register are read out.	?	○	○
1			?	○	○
2			?	○	○
3			?	○	○
4			?	○	○
5			?	○	○
6			?	○	○
7			?	○	○

Note: The contents of transmit buffer register cannot be read out.
The data cannot be written to the receive buffer register.

Fig. 2.4.2 Structure of Transmit/Receive buffer register

Serial I/O status register

b7 b6 b5 b4 b3 b2 b1 b0

Serial I/O status register (SIOSTS) [Address : 27₁₆]

B	Name	Function	At reset	R	W
0	Transmit buffer empty flag (TBE)	0 : Buffer full 1 : Buffer empty	0	○	×
1	Receive buffer full flag (RBF)	0 : Buffer empty 1 : Buffer full	0	○	×
2	Transmit shift register shift completion flag (TSC)	0 : Transmit shift in progress 1 : Transmit shift completed	0	○	×
3	Overrun error flag (OE)	0 : No error 1 : Overrun error	0	○	×
4	Parity error flag (PE)	0 : No error 1 : Parity error	0	○	×
5	Framing error flag (FE)	0 : No error 1 : Framing error	0	○	×
6	Summing error flag (SE)	0 : (OE) U (PE) U (FE) = 0 1 : (OE) U (PE) U (FE) = 1	0	○	×
7	Nothing is allocated for this bit. This is a write disabled bit. When this bit is read out, the contents are "1".		1	○	×

Fig. 2.4.3 Structure of Serial I/O status register

APPLICATION

2.4 Serial I/O

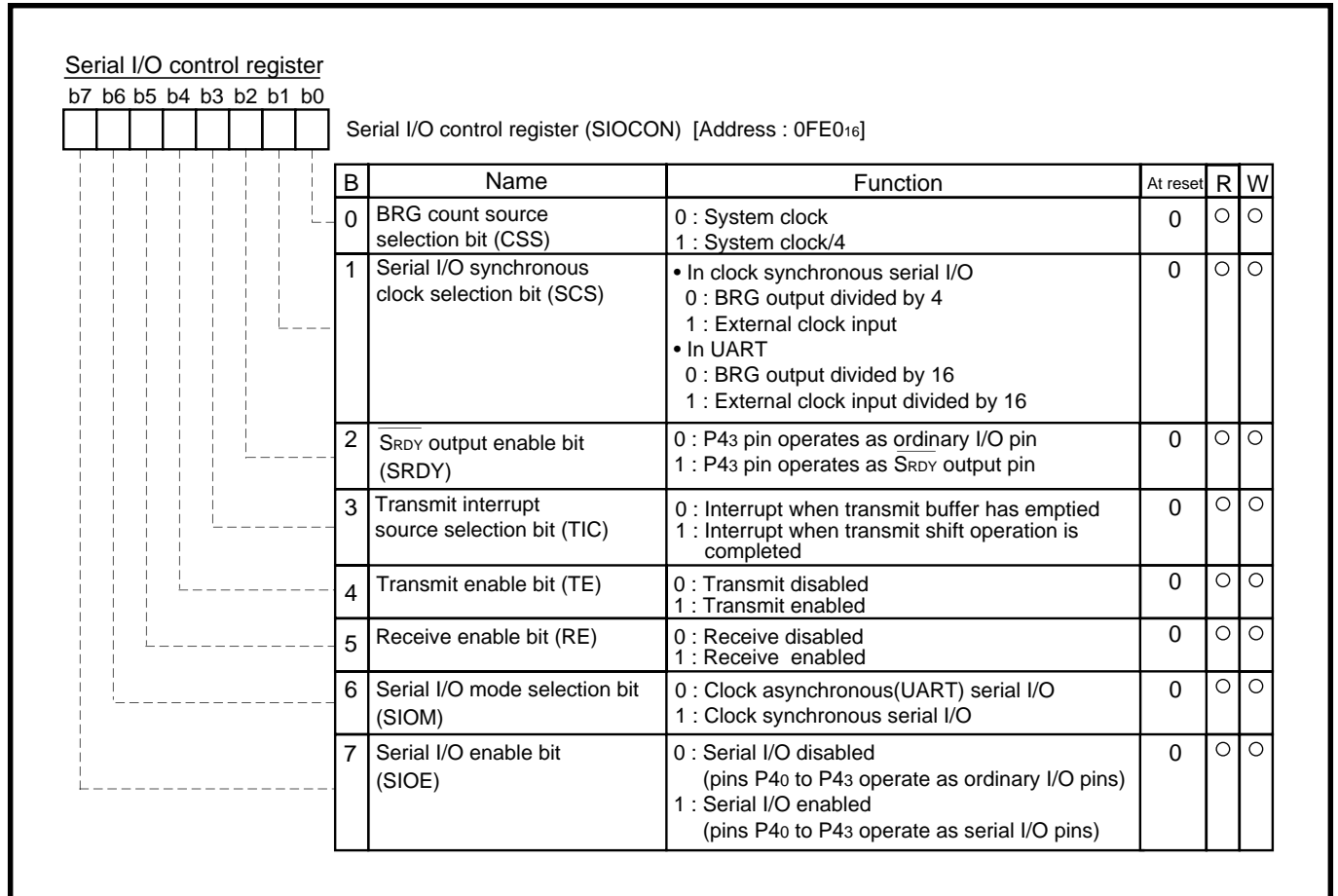


Fig. 2.4.4 Structure of Serial I/O control register

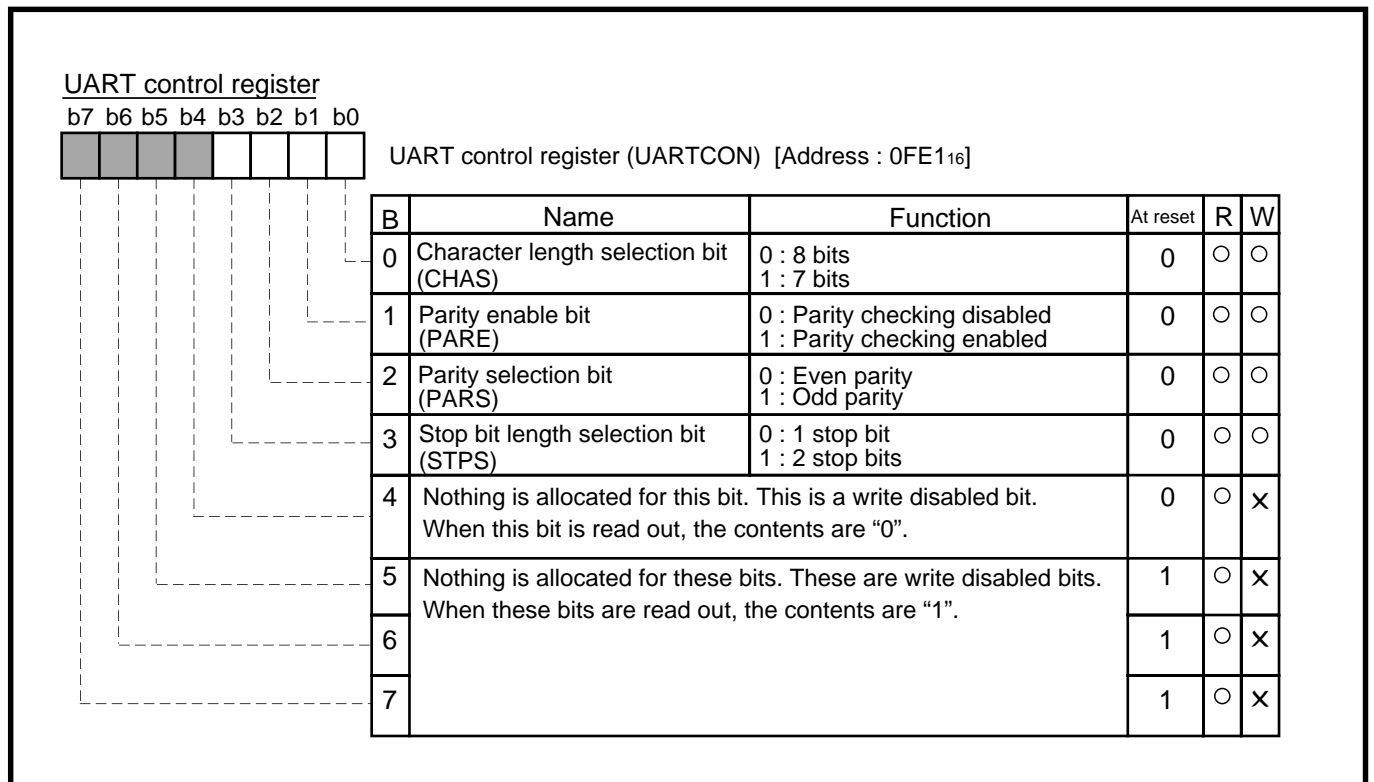
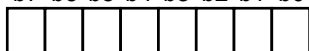


Fig. 2.4.5 Structure of UART control register

Baud rate generator

b7 b6 b5 b4 b3 b2 b1 b0

Baud rate generator (BRG) [Address : 0FE2₁₆]

B	Function	At reset	R	W
0	Set a count value of baud rate generator.	?	○	○
1		?	○	○
2		?	○	○
3		?	○	○
4		?	○	○
5		?	○	○
6		?	○	○
7		?	○	○

Fig. 2.4.6 Structure of Baud rate generator

Interrupt edge selection register

b7 b6 b5 b4 b3 b2 b1 b0



Interrupt edge selection register (INTEDGE)

[Address : 0FF3₁₆]

B	Name	Function	At reset	R	W
0	INT0 interrupt edge selection bit	0 : Falling edge active 1 : Rising edge active	0	○	○
1	Nothing is arranged for this bits. This is a write disabled bit. When this bit is read out, the contents are "0".		0	○	×
2	INT1 interrupt edge selection bit	0 : Falling edge active 1 : Rising edge active	0	○	○
3	Nothing is arranged for this bits. This is a write disabled bit. When this bit is read out, the contents are "0".		0	○	×
4			0	○	×
5			0	○	×
6			0	○	×
7			0	○	×

Fig. 2.4.7 Structure of Interrupt edge selection register

APPLICATION

2.4 Serial I/O

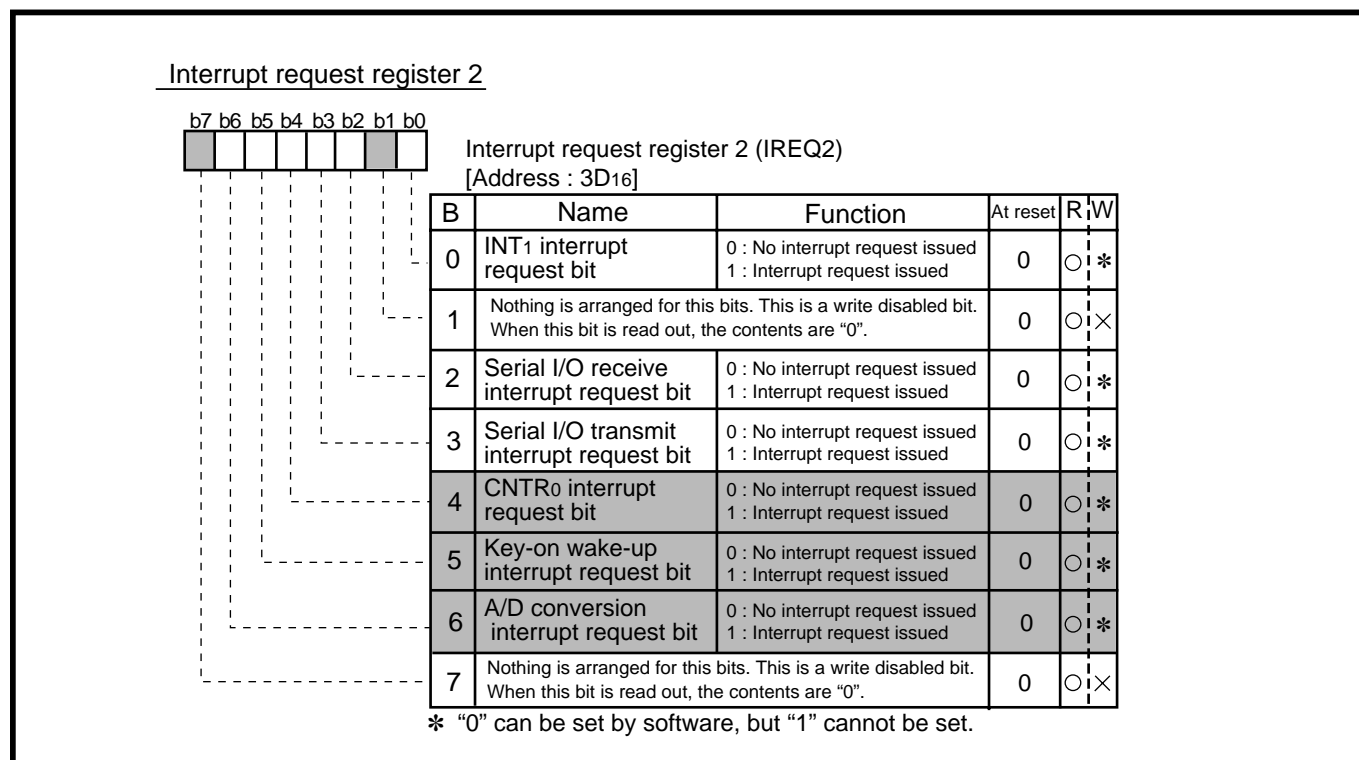


Fig. 2.4.8 Structure of Interrupt request register 2

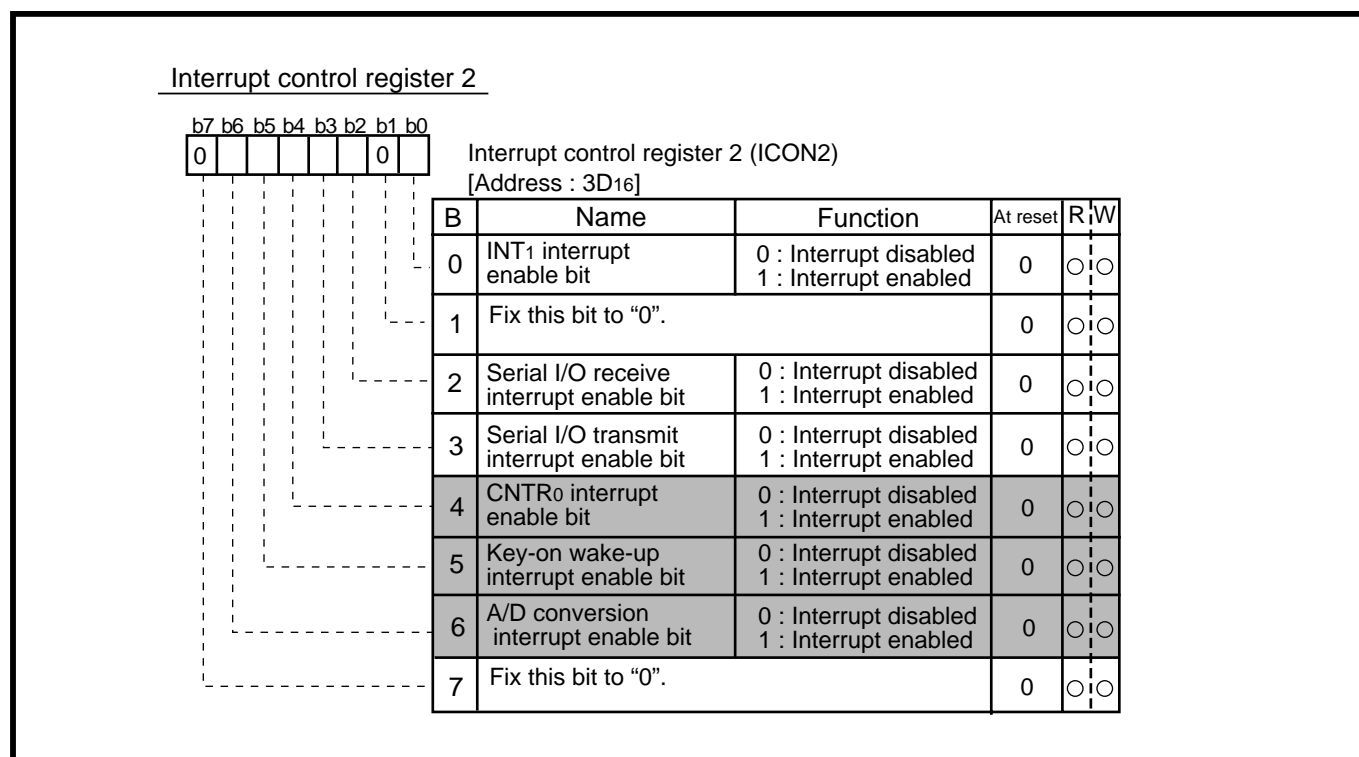


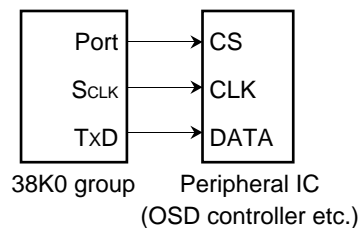
Fig. 2.4.9 Structure of Interrupt control register 2

2.4.3 Serial I/O connection examples

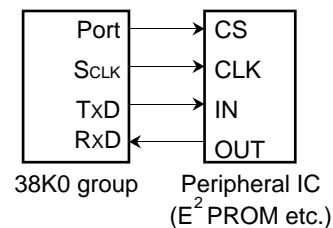
(1) Control of peripheral IC equipped with CS pin

Figure 2.4.10 shows connection examples of a peripheral IC equipped with the CS pin. There are connection examples using a clock synchronous serial I/O mode.

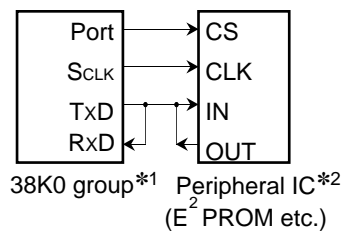
(1) Only transmission
(Using the RxD pin as an I/O port)



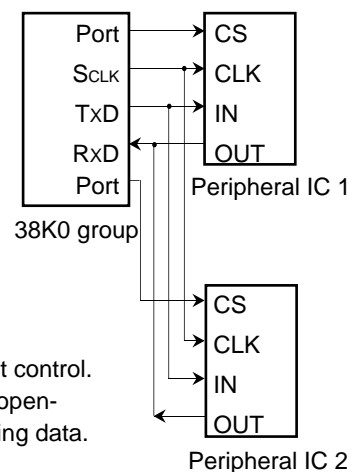
(2) Transmission and reception



(3) Transmission and reception
(When connecting RxD with TxD
(When connecting IN with OUT in
peripheral IC)



(4) Connection of plural IC



*1: Select an N-channel open-drain output for TxD pin output control.

*2: Use the OUT pin of peripheral IC which is an N-channel open-drain output and becomes high impedance during receiving data.

Notes: "Port" means an output port controlled by software.

Fig. 2.4.10 Serial I/O connection examples (1)

APPLICATION

2.4 Serial I/O

(2) Connection with microcomputer

Figure 2.4.11 shows connection examples with another microcomputer.

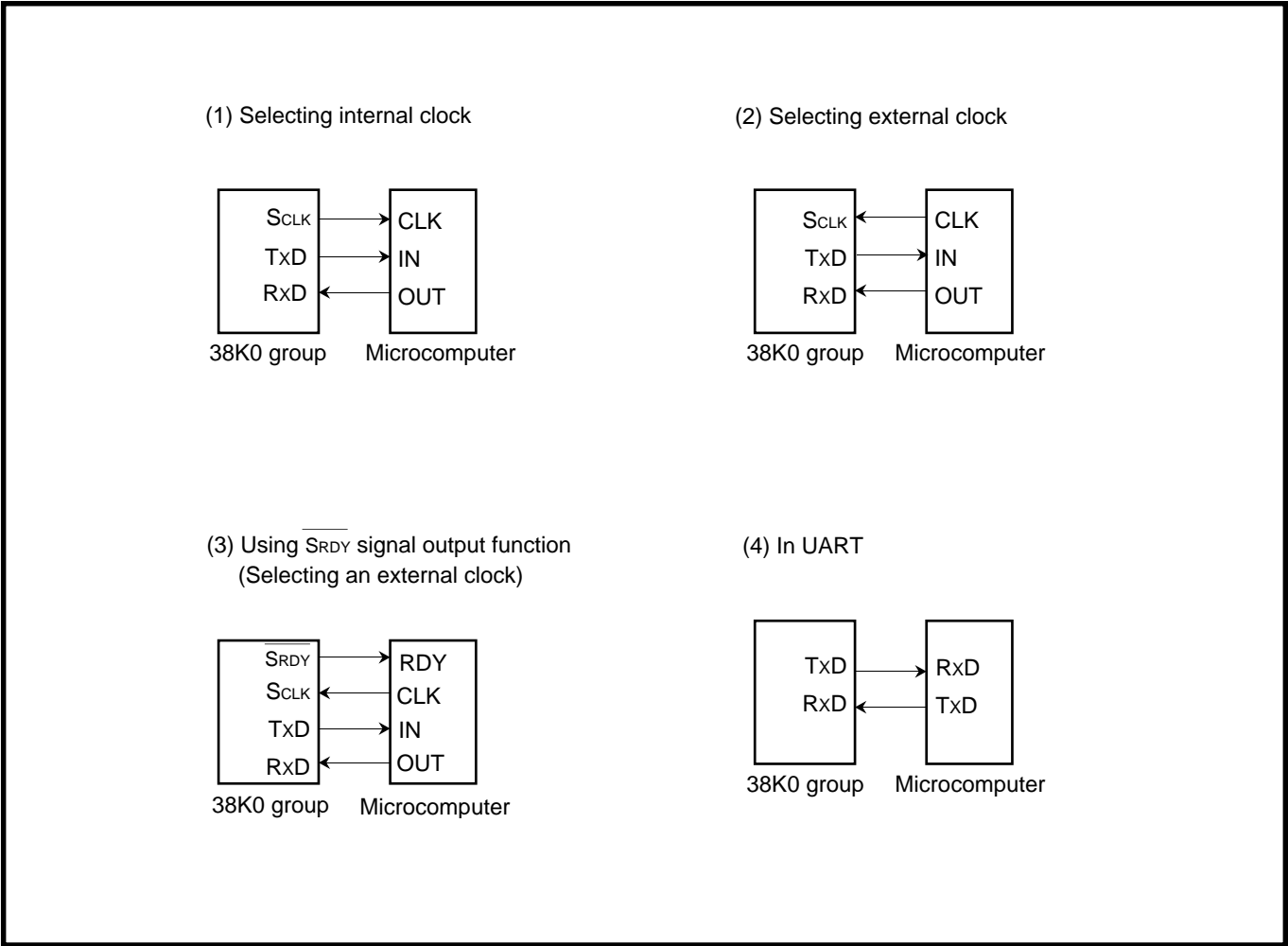


Fig. 2.4.11 Serial I/O connection examples (2)

2.4.4 Setting of serial I/O transfer data format

A clock synchronous or clock asynchronous (UART) can be selected as a data format of Serial I/O. Figure 2.4.12 shows the serial I/O transfer data format.

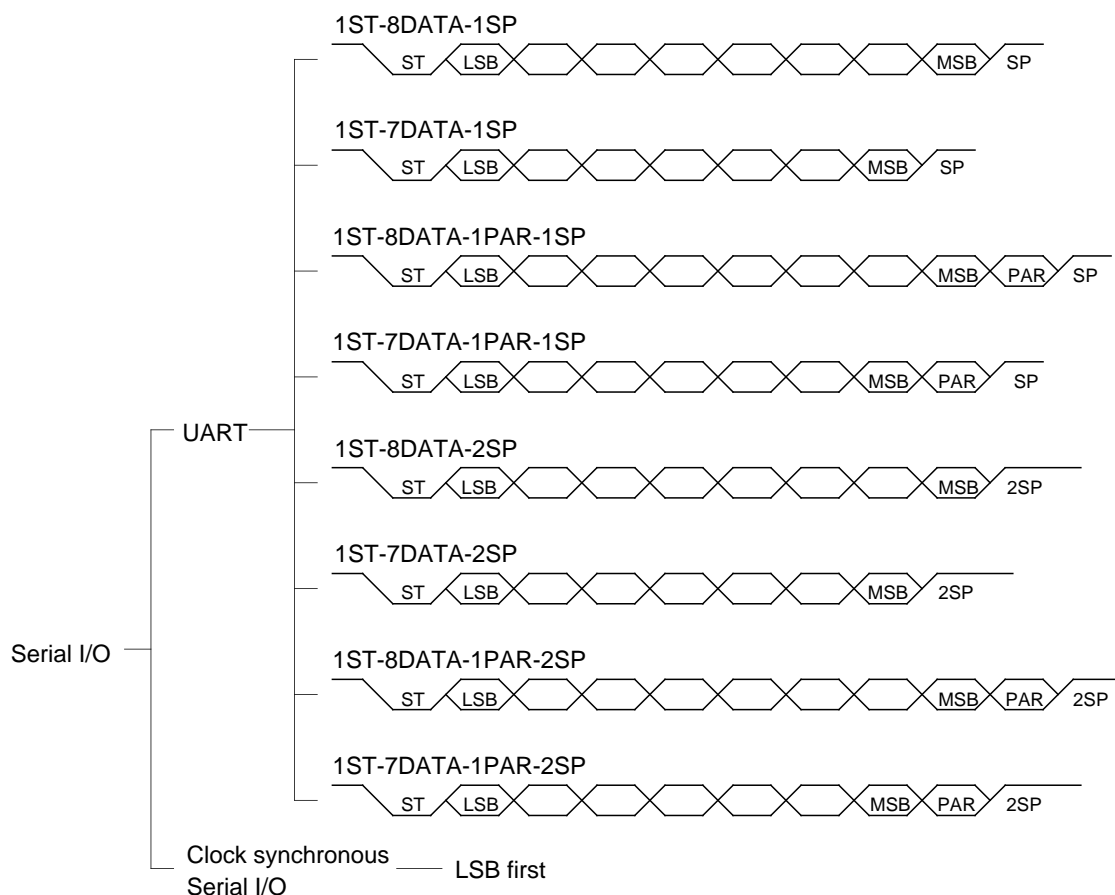


Fig. 2.4.12 Serial I/O transfer data format

APPLICATION

2.4 Serial I/O

2.4.5 Serial I/O application examples

(1) Communication using clock synchronous serial I/O (transmit/receive)

Outline : 2-byte data is transmitted and received, using the clock synchronous serial I/O.
The $\overline{\text{SRDY}}$ signal is used for communication control.

Figure 2.4.13 shows a connection diagram, and Figure 2.4.14 shows a timing chart.
Figure 2.4.15 shows a registers setting related to the transmitting side, and Figure 2.4.16 shows registers setting related to the receiving side.

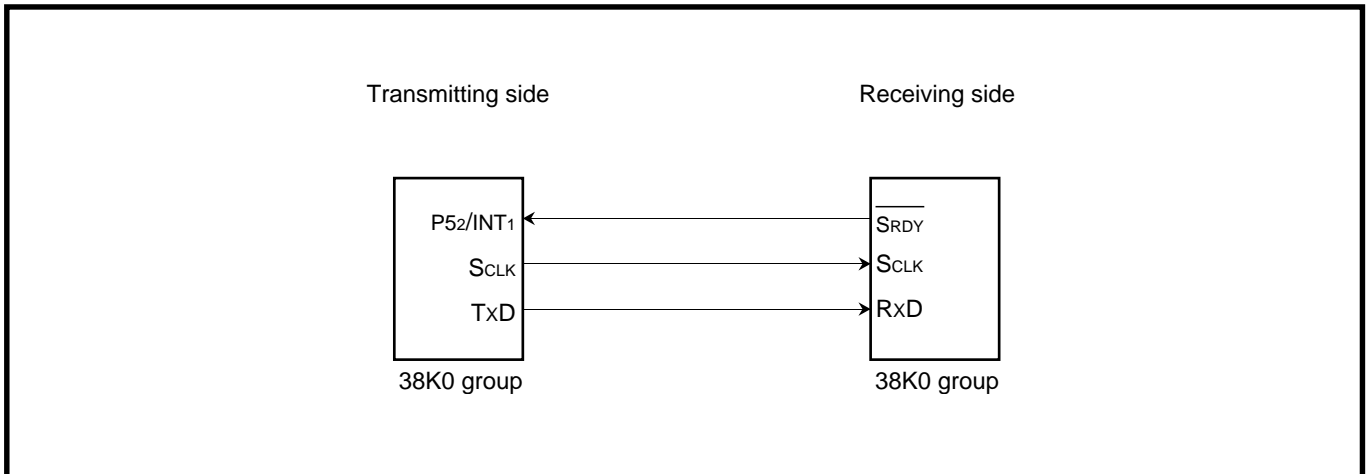


Fig. 2.4.13 Connection diagram

- Specifications :**
- The Serial I/O is used (clock synchronous serial I/O is selected.)
 - Synchronous clock frequency : 125 kHz ($f(\text{X}_{\text{IN}}) = 6 \text{ MHz}$ is divided by 48)
 - The $\overline{\text{SRDY}}$ (receivable signal) is used.
 - The receiving side outputs the $\overline{\text{SRDY}}$ signal at intervals of 2 ms (generated by timer), and 2-byte data is transferred from the transmitting side to the receiving side.

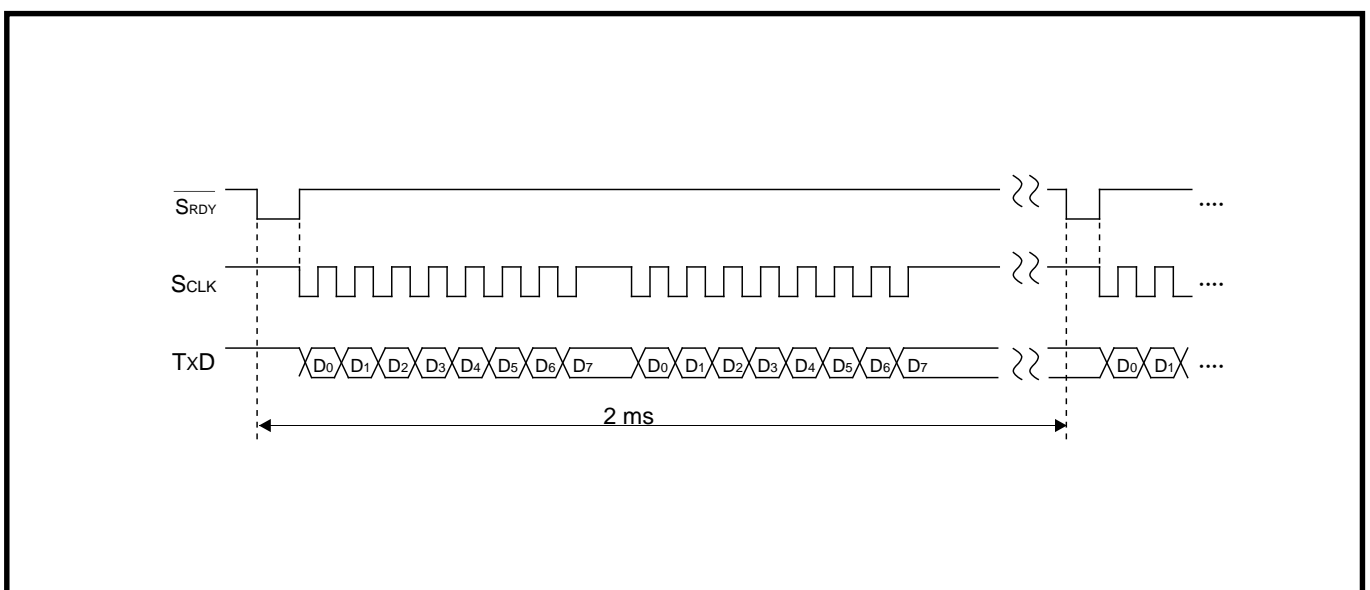


Fig. 2.4.14 Timing chart

Transmitting side

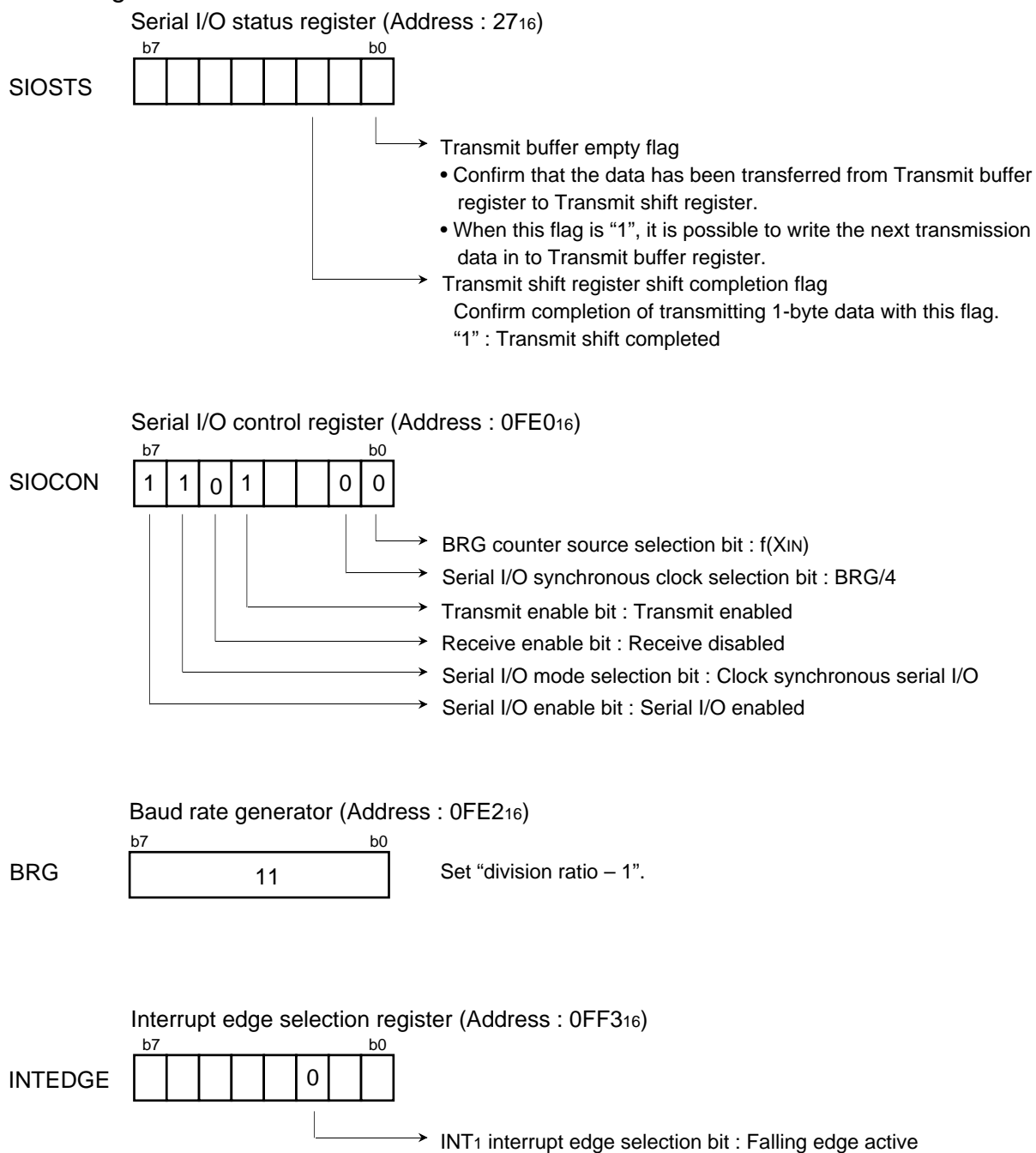


Fig. 2.4.15 Registers setting related to transmitting side

APPLICATION

2.4 Serial I/O

Receiving side

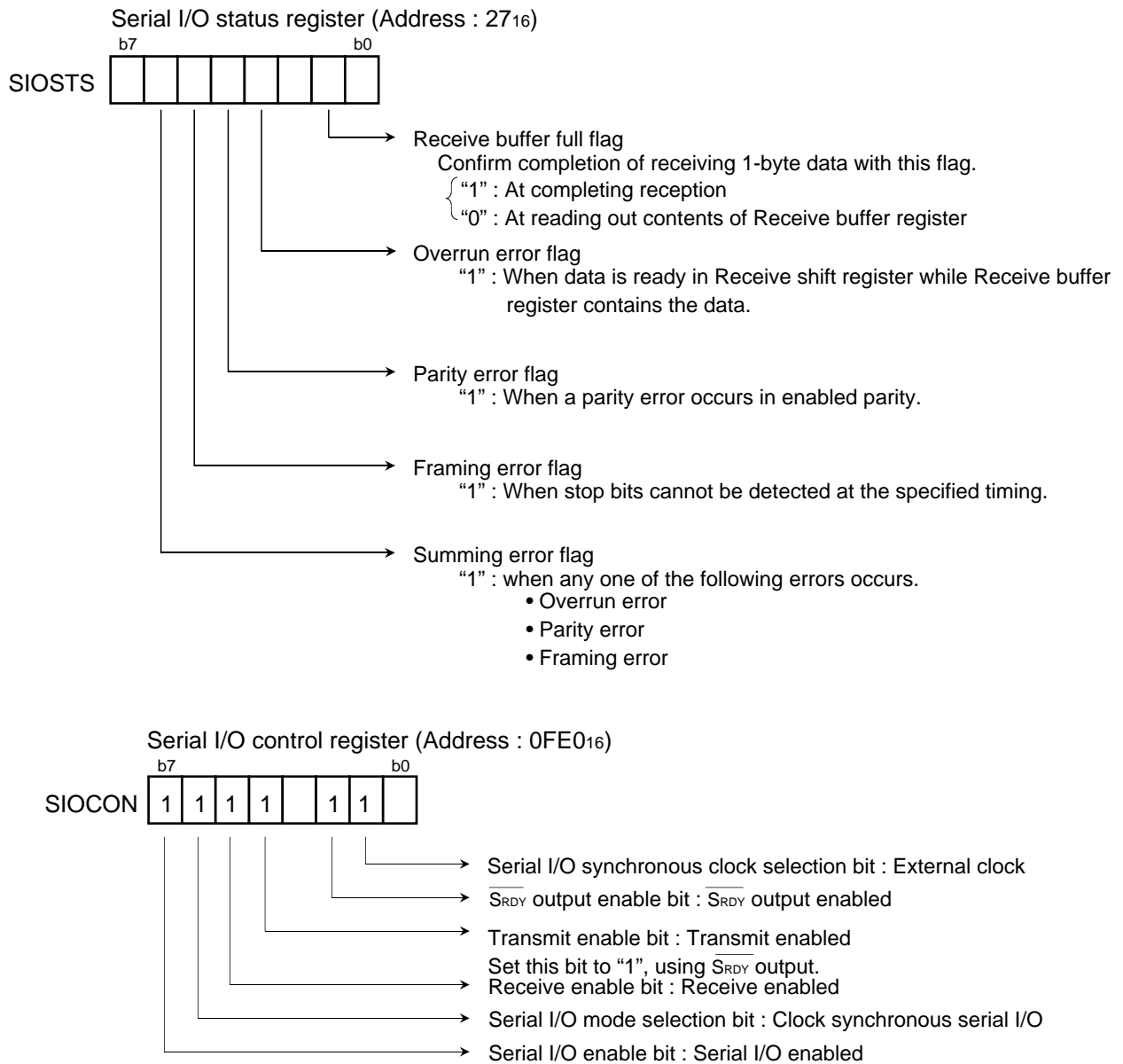


Fig. 2.4.16 Registers setting related to receiving side

Figure 2.4.17 shows a control procedure of the transmitting side, and Figure 2.4.18 shows a control procedure of the receiving side.

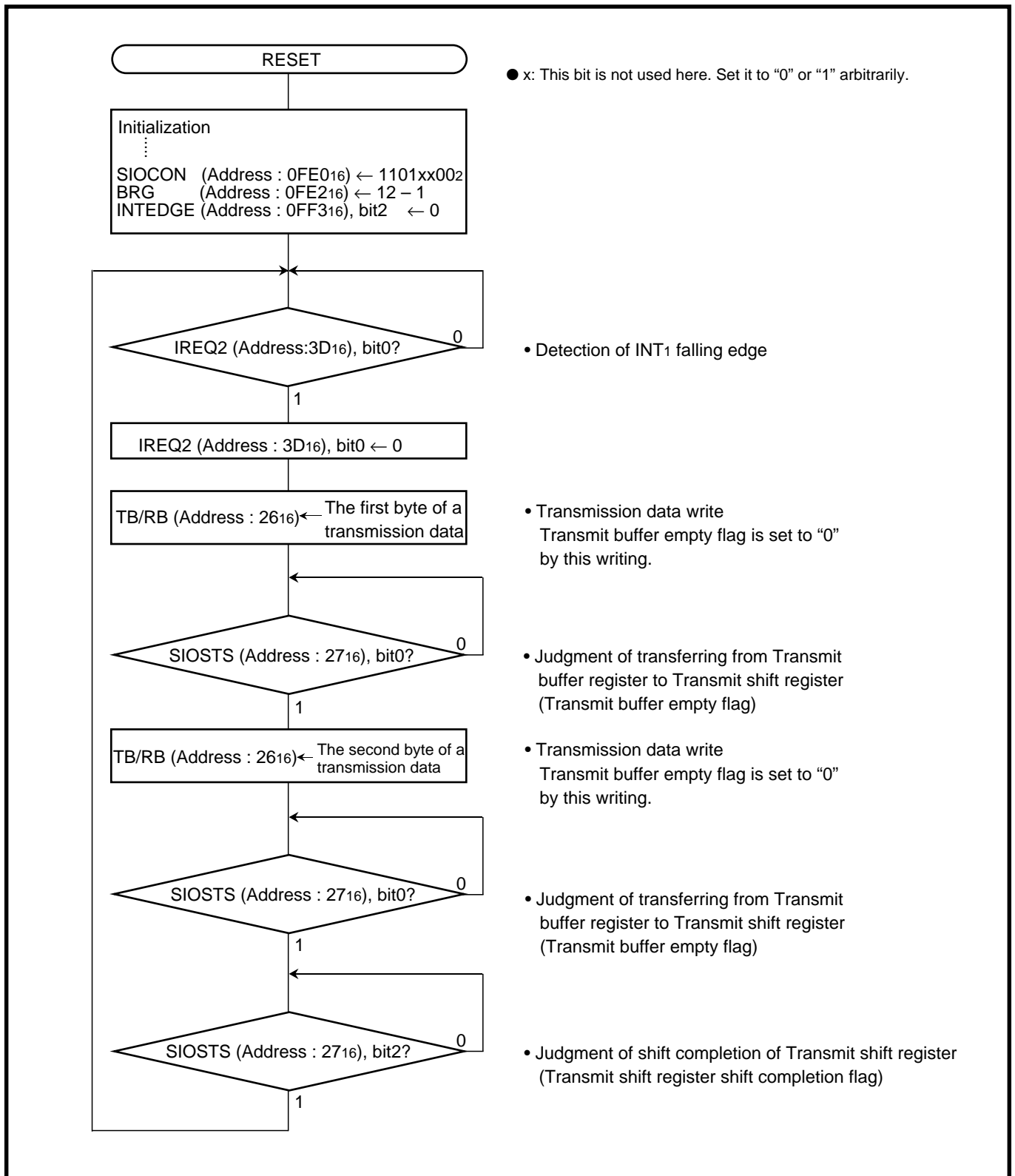


Fig. 2.4.17 Control procedure of transmitting side

APPLICATION

2.4 Serial I/O

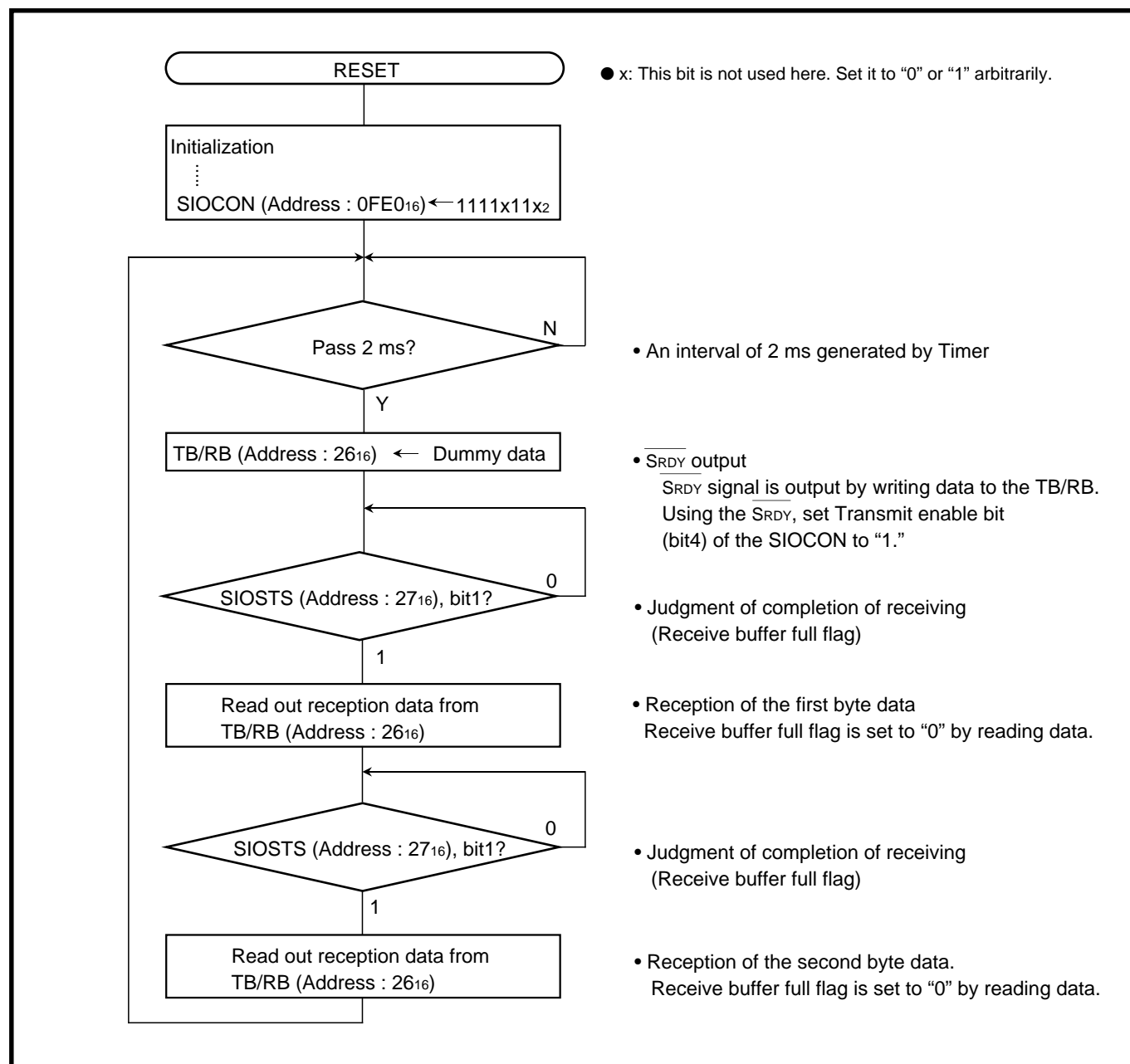


Fig. 2.4.18 Control procedure of receiving side

(2) Output of serial data (control of peripheral IC)

Outline : 4-byte data is transmitted and received, using the clock synchronous serial I/O.
The CS signal is output to a peripheral IC through port P5₃.

The example for using Serial I/O is shown.

Figure 2.4.19 shows a connection diagram, and Figure 2.4.20 shows a timing chart.

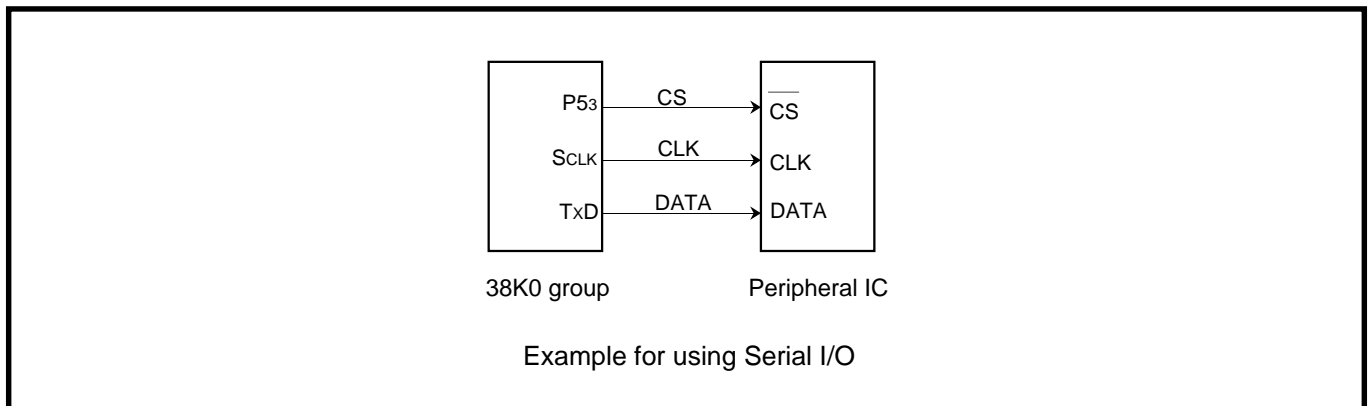


Fig. 2.4.19 Connection diagram

- Specifications :**
- The Serial I/O is used (clock synchronous serial I/O is selected.)
 - Synchronous clock frequency : 125 kHz ($f(X_{IN}) = 6 \text{ MHz}$ is divided by 48)
 - Transfer direction : LSB first
 - The Serial I/O interrupt is not used.
 - Port P5₃ is connected to the \overline{CS} pin ("L" active) of the peripheral IC for transmission control; the output level of port P5₃ is controlled by software.

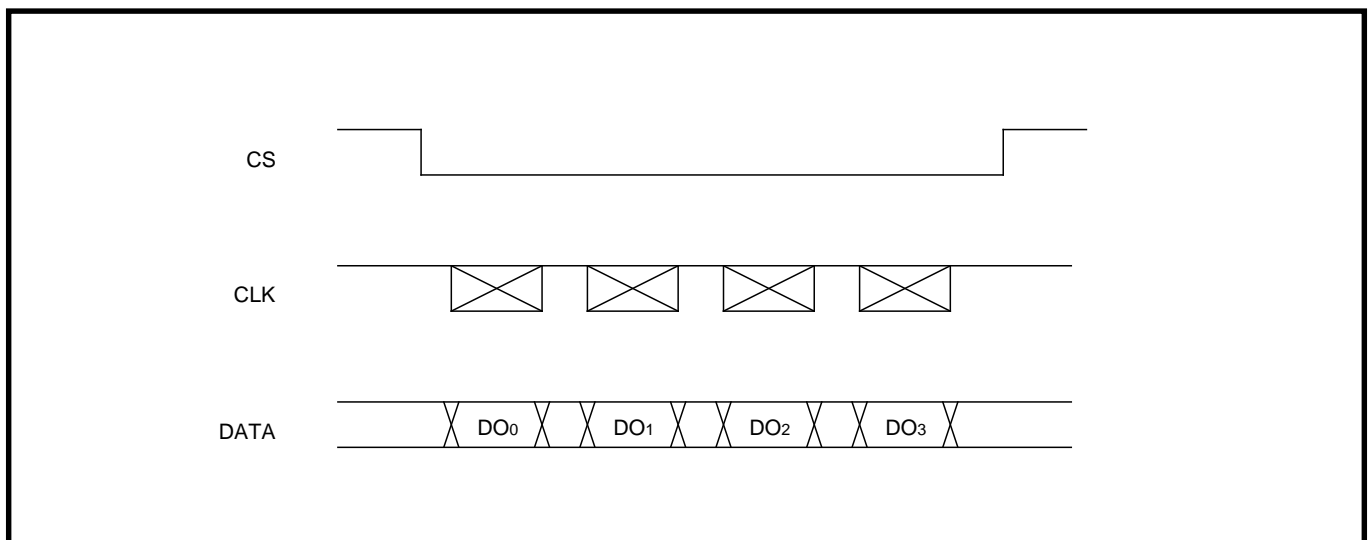


Fig. 2.4.20 Timing chart

APPLICATION

2.4 Serial I/O

Figure 2.4.21 shows registers setting related to Serial I/O, and Figure 2.4.22 shows a setting of serial I/O transmission data.

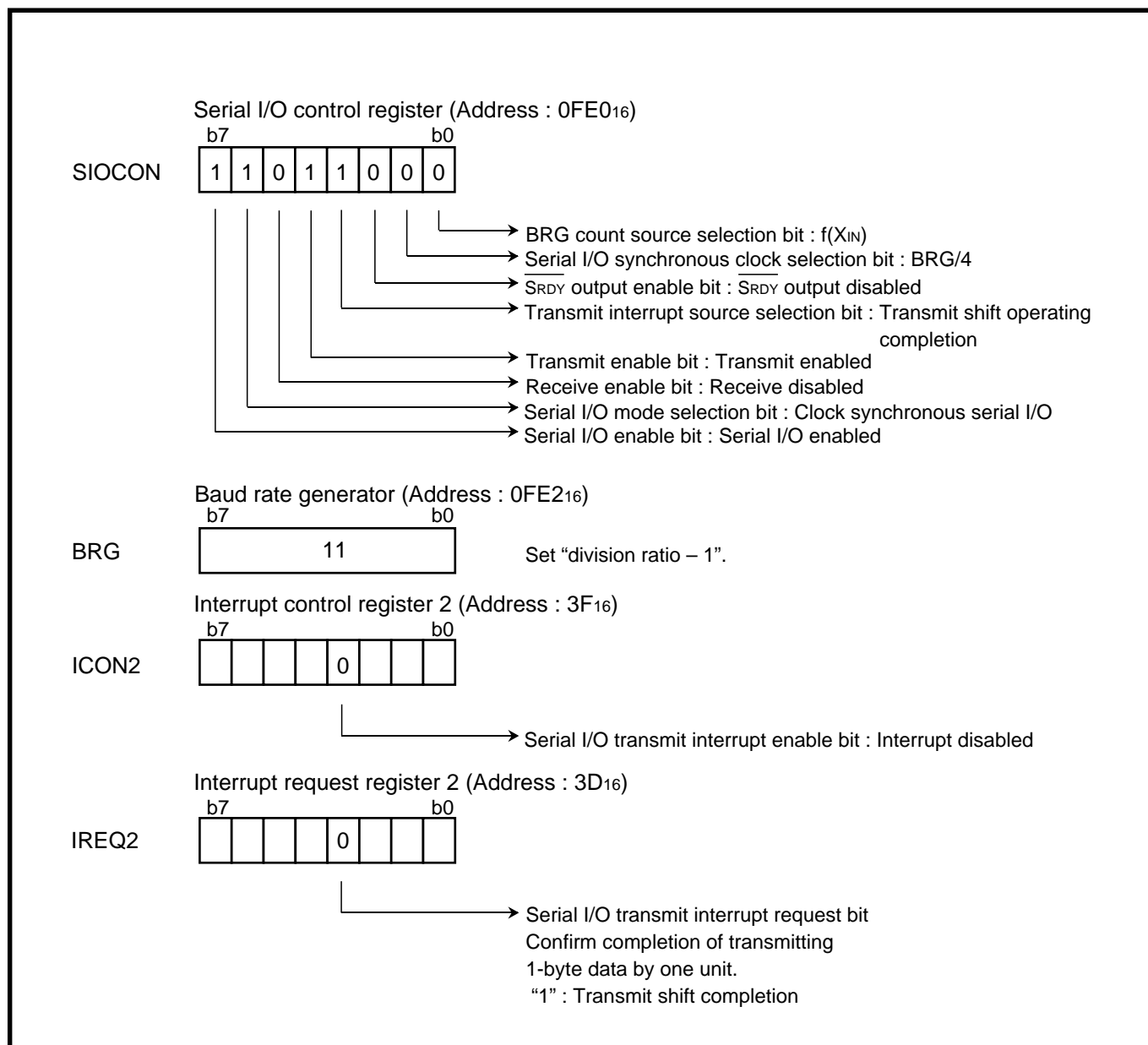


Fig. 2.4.21 Registers setting related to Serial I/O

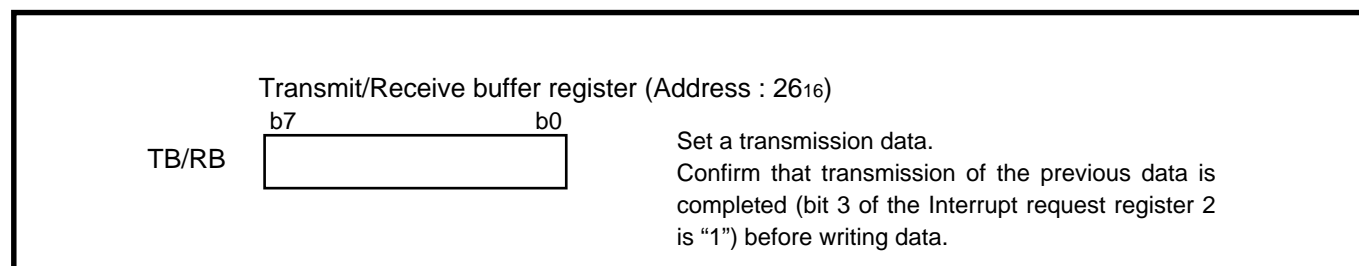


Fig. 2.4.22 Setting of serial I/O transmission data

When the registers are set as shown in Fig. 2.4.21, the Serial I/O can transmit 1-byte data by writing data to the transmit buffer register.

Thus, after setting the CS signal to “L”, write the transmission data to the transmit buffer register by each 1 byte, and return the CS signal to “H” when the target number of bytes has been transmitted. Figure 2.4.23 shows a control procedure of Serial I/O.

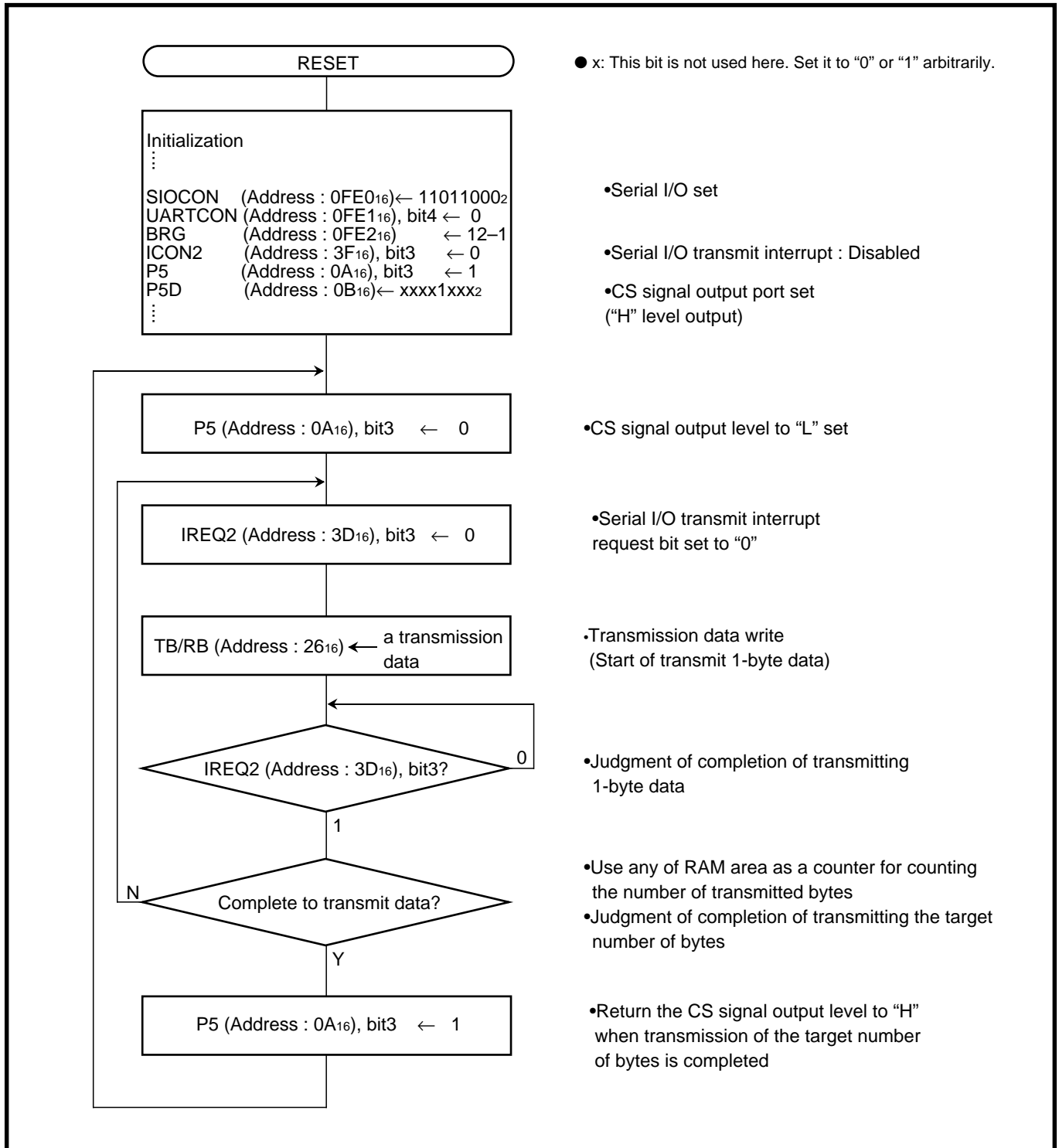


Fig. 2.4.23 Control procedure of Serial I/O

APPLICATION

2.4 Serial I/O

(3) Cyclic transmission or reception of block data (data of specified number of bytes) between two microcomputers

Outline : When the clock synchronous serial I/O is used for communication, synchronization of the clock and the data between the transmitting and receiving sides may be lost because of noise included in the synchronous clock. It is necessary to correct that constantly, using "heading adjustment".

This "heading adjustment" is carried out by using the interval between blocks in this example.

Figure 2.4.24 shows a connection diagram.

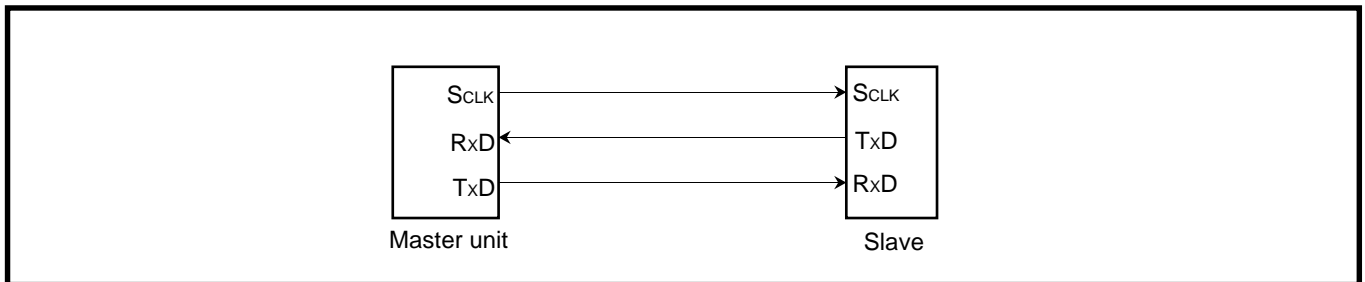


Fig. 2.4.24 Connection diagram

Specifications :

- The serial I/O is used (clock synchronous serial I/O is selected).
- Synchronous clock frequency : 125 kHz ($f(X_{IN}) = 6 \text{ MHz}$ is divided by 48)
- Byte cycle: 488 μs
- Number of bytes for transmission or reception : 8 byte/block
- Block transfer cycle : 16 ms
- Block transfer term : 3.5 ms
- Interval between blocks : 12.5 ms
- Heading adjustment time : 8 ms

Limitations of specifications :

- Reading of the reception data and setting of the next transmission data must be completed within the time obtained from "byte cycle – time for transferring 1-byte data" (in this example, the time taken from generating of the serial I/O receive interrupt request to input of the next synchronous clock is 431 μs).
- "Heading adjustment time < interval between blocks" must be satisfied.

The communication is performed according to the timing shown in Figure 2.4.25. In the slave unit, when a synchronous clock is not input within a certain time (heading adjustment time), the next clock input is processed as the beginning (heading) of a block.

When a clock is input again after one block (8 byte) is received, the clock is ignored.

Figure 2.4.26 shows related registers setting.

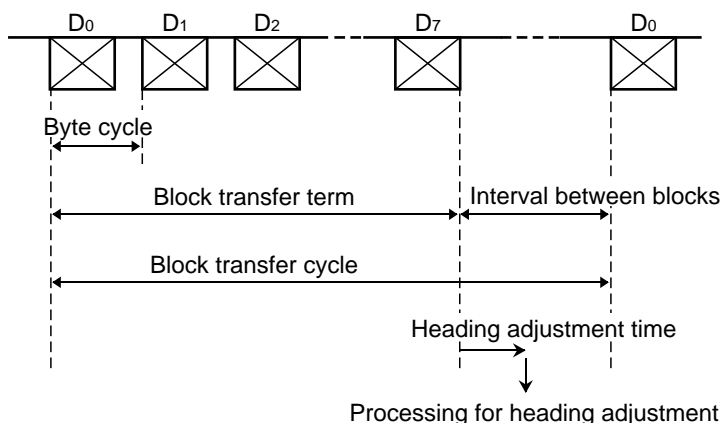


Fig. 2.4.25 Timing chart

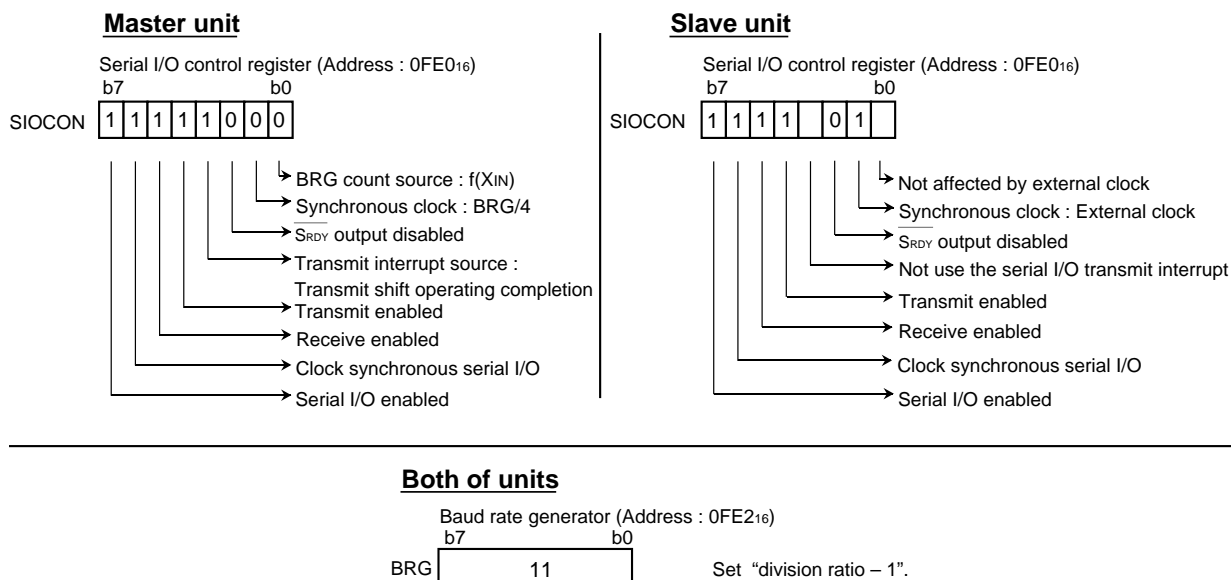


Fig. 2.4.26 Related registers setting

APPLICATION

2.4 Serial I/O

Control procedure :

- Control in the master unit

After setting the related registers shown in Figure 2.4.26, the master unit starts transmission or reception of 1-byte data by writing transmission data to the transmit buffer register.

To perform the communication in the timing shown in Figure 2.4.25, take the timing into account and write transmission data. Additionally, read out the reception data when the serial I/O transmit interrupt request bit is set to "1," or before the next transmission data is written to the transmit buffer register.

Figure 2.4.27 shows a control procedure of the master unit using timer interrupts.

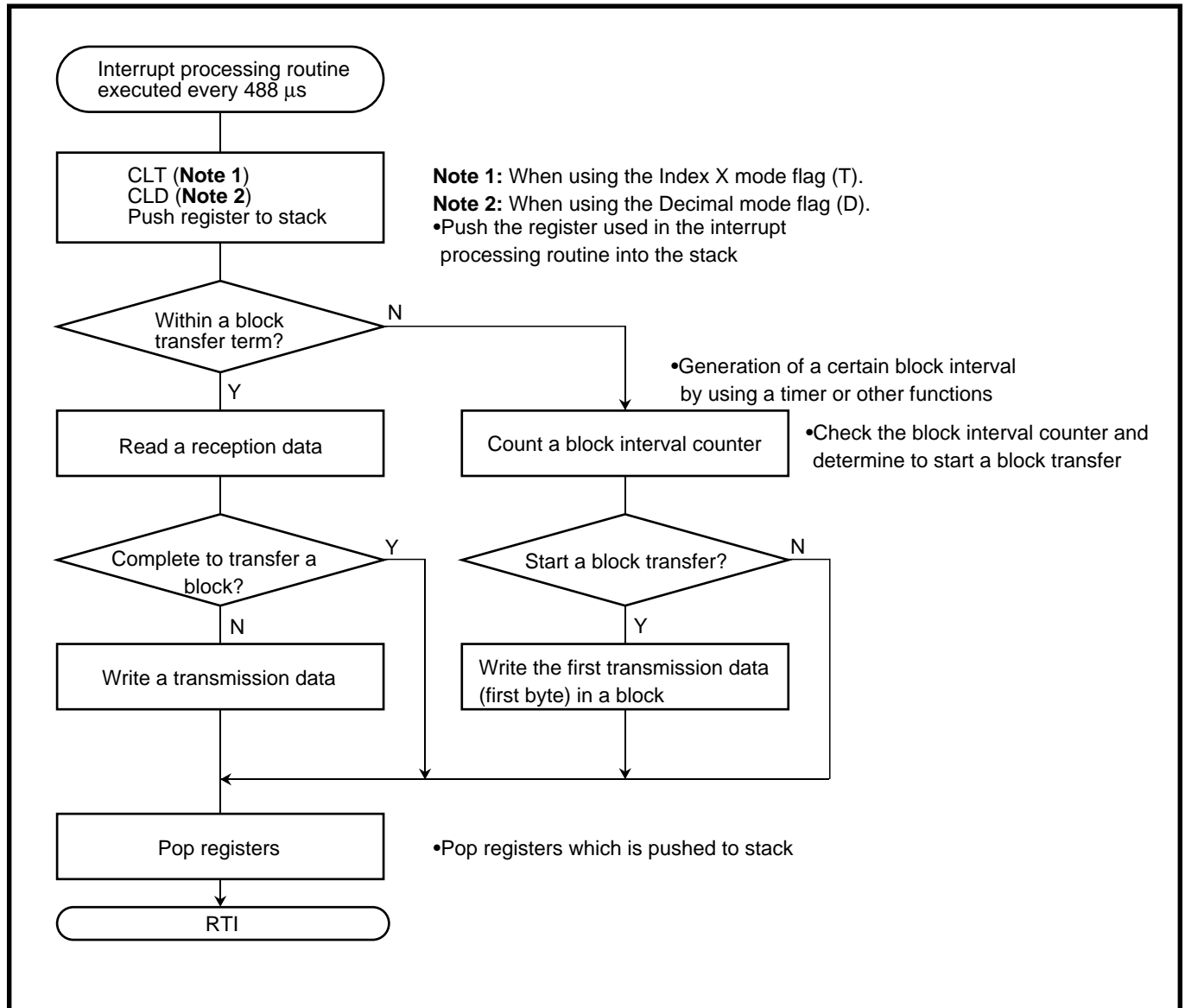


Fig. 2.4.27 Control procedure of master unit

● Control in the slave unit

After setting the related registers as shown in Figure 2.4.26, the slave unit becomes the state where a synchronous clock can be received at any time, and the serial I/O receive interrupt request bit is set to "1" each time an 8-bit synchronous clock is received.

In the serial I/O receive interrupt processing routine, the data to be transmitted next is written to the transmit buffer register after the received data is read out.

However, if no serial I/O receive interrupt occurs for a certain time (heading adjustment time or more), the following processing will be performed.

1. The first 1-byte data of the transmission data in the block is written into the transmit buffer register.
2. The data to be received next is processed as the first 1 byte of the received data in the block.

Figure 2.4.28 shows a control procedure of the slave unit using the serial I/O receive interrupt and any timer interrupt (for heading adjustment).

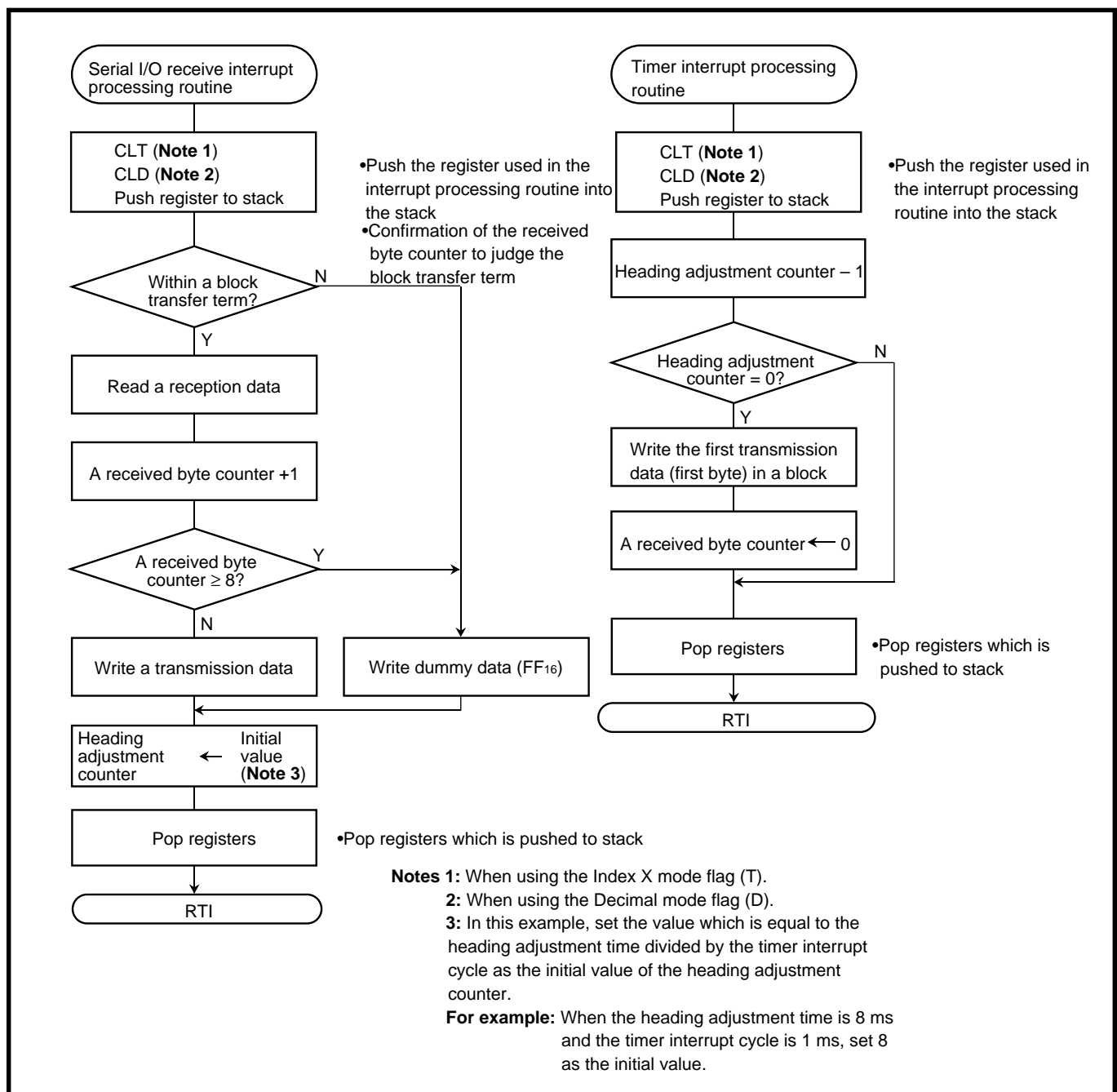


Fig. 2.4.28 Control procedure of slave unit

APPLICATION

2.4 Serial I/O

(4) Communication (transmit/receive) using asynchronous serial I/O (UART)

Outline : 2-byte data is transmitted and received, using the asynchronous serial I/O.
Port P2₀ is used for communication control.

Figure 2.4.29 shows a connection diagram, and Figure 2.4.30 shows a timing chart.

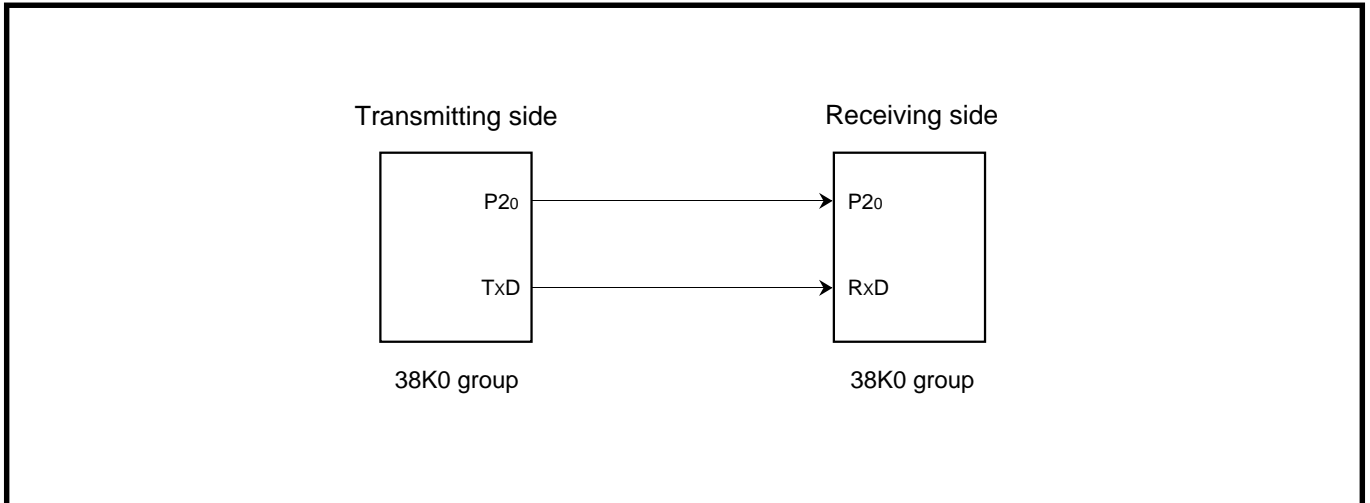


Fig. 2.4.29 Connection diagram (Communication using UART)

- Specifications :**
- The Serial I/O is used (UART is selected).
 - Transfer bit rate : 9600 bps ($f(X_{IN}) = 6 \text{ MHz}$ is divided by 624)
 - Communication control using port P2₀
(The output level of port P2₀ is controlled by software.)
 - 2-byte data is transferred from the transmitting side to the receiving side at intervals of 10 ms generated by the timer.

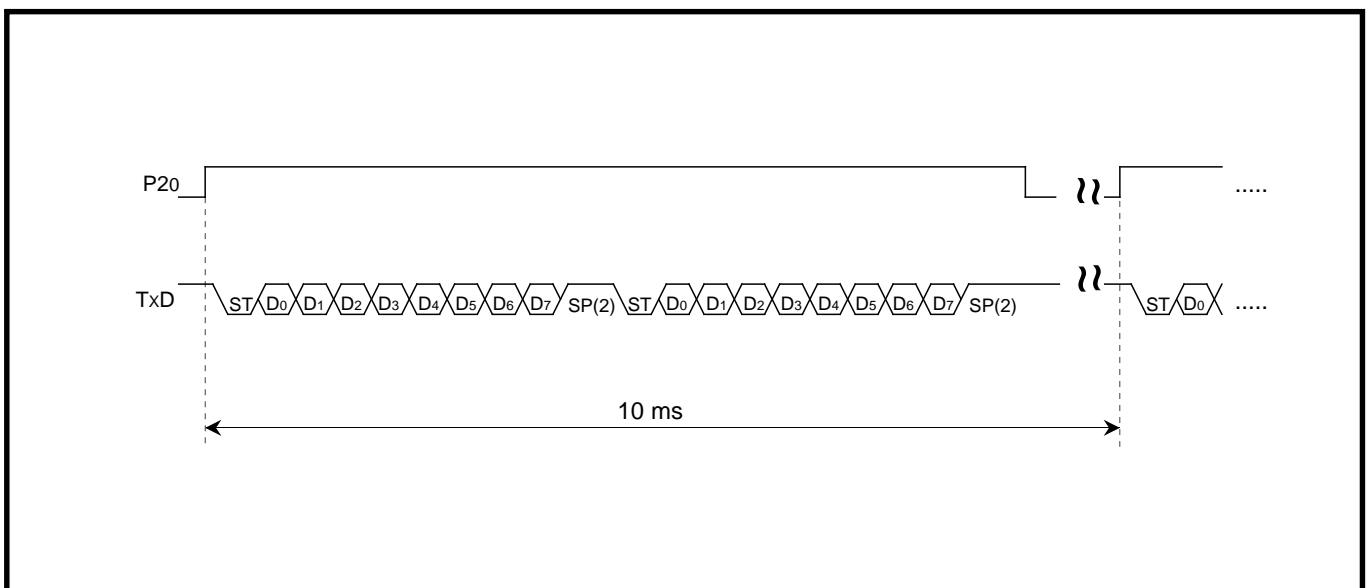


Fig. 2.4.30 Timing chart (using UART)

Table 2.4.1 shows setting examples of the baud rate generator (BRG) values and transfer bit rate values; Figure 2.4.31 shows registers setting related to the transmitting side; Figure 2.4.32 shows registers setting related to the receiving side.

Table 2.4.1 Setting examples of Baud rate generator values and transfer bit rate values

Transfer bit rate (bps) (Note 3)	BRG count source (Note 1)	At f(X _{IN}) = 6 MHz BRG setting value (Note 2)	At f(X _{IN}) = 8 MHz BRG setting value (Note 2)
600	f(X _{IN})/4	155	207
1200	f(X _{IN})/4	77	103
2400	f(X _{IN})	155	207
4800	f(X _{IN})	77	103
9600	f(X _{IN})	38	51
14400	f(X _{IN})	25	34
19200	f(X _{IN})	19	25
38400	f(X _{IN})	9	12
57600	f(X _{IN})	—	8

Notes 1: Select the BRG count source with bit 0 of the serial I/O control register (Address : 0FE016).

2: These are setting values with small errors.

3: Equation of transfer bit rate:

$$\text{Transfer bit rate (bps)} = \frac{f(X_{IN})}{(\text{BRG setting value} + 1) \times 16 \times m^*}$$

*m: When bit 0 of the serial I/O control register (Address : 0FE016) is set to “0”, a value of m is 1.

When bit 0 of the serial I/O control register (Address : 0FE016) is set to “1”, a value of m is 4.

APPLICATION

2.4 Serial I/O

Transmitting side

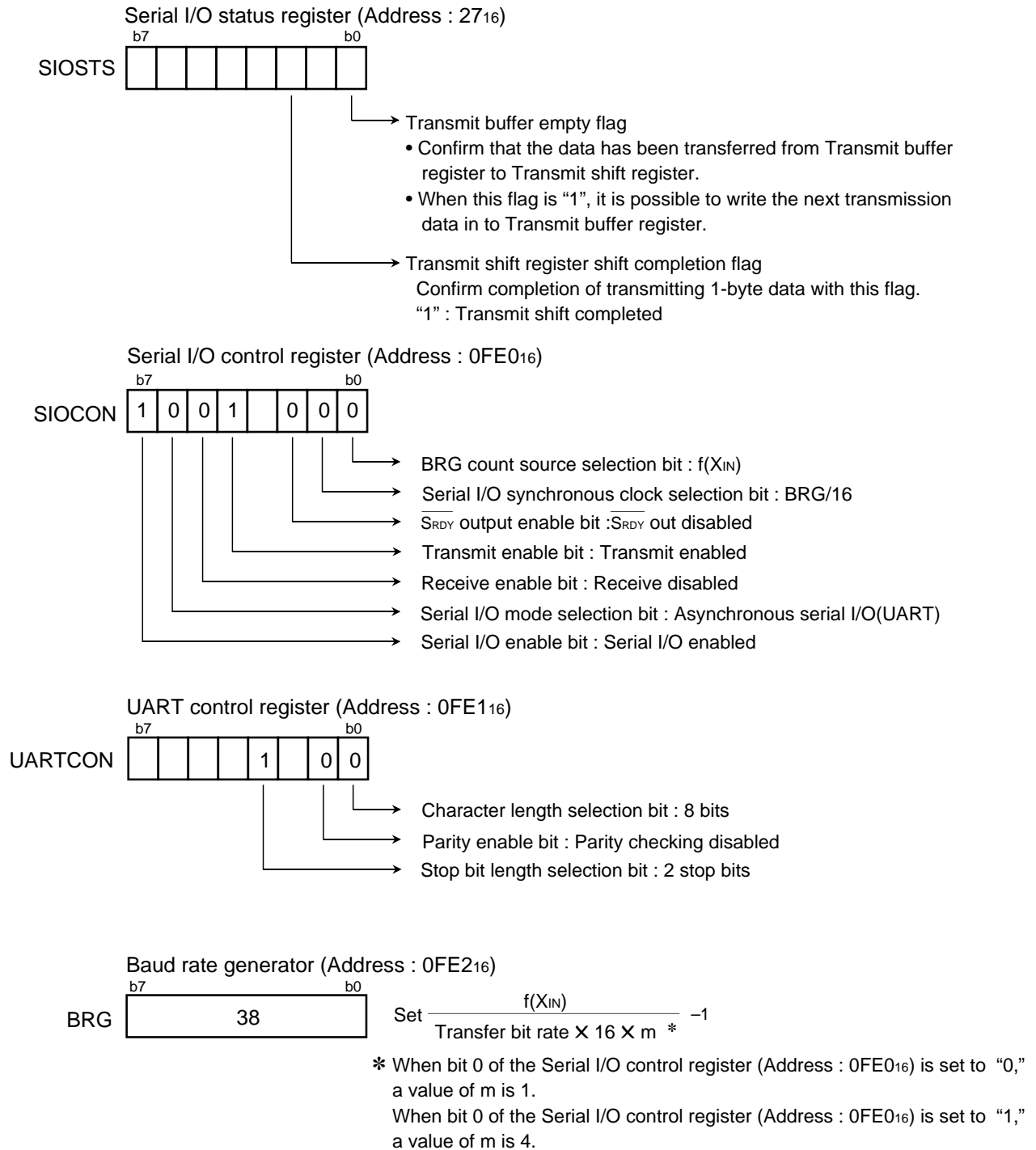


Fig. 2.4.31 Registers setting related to transmitting side

Receiving side

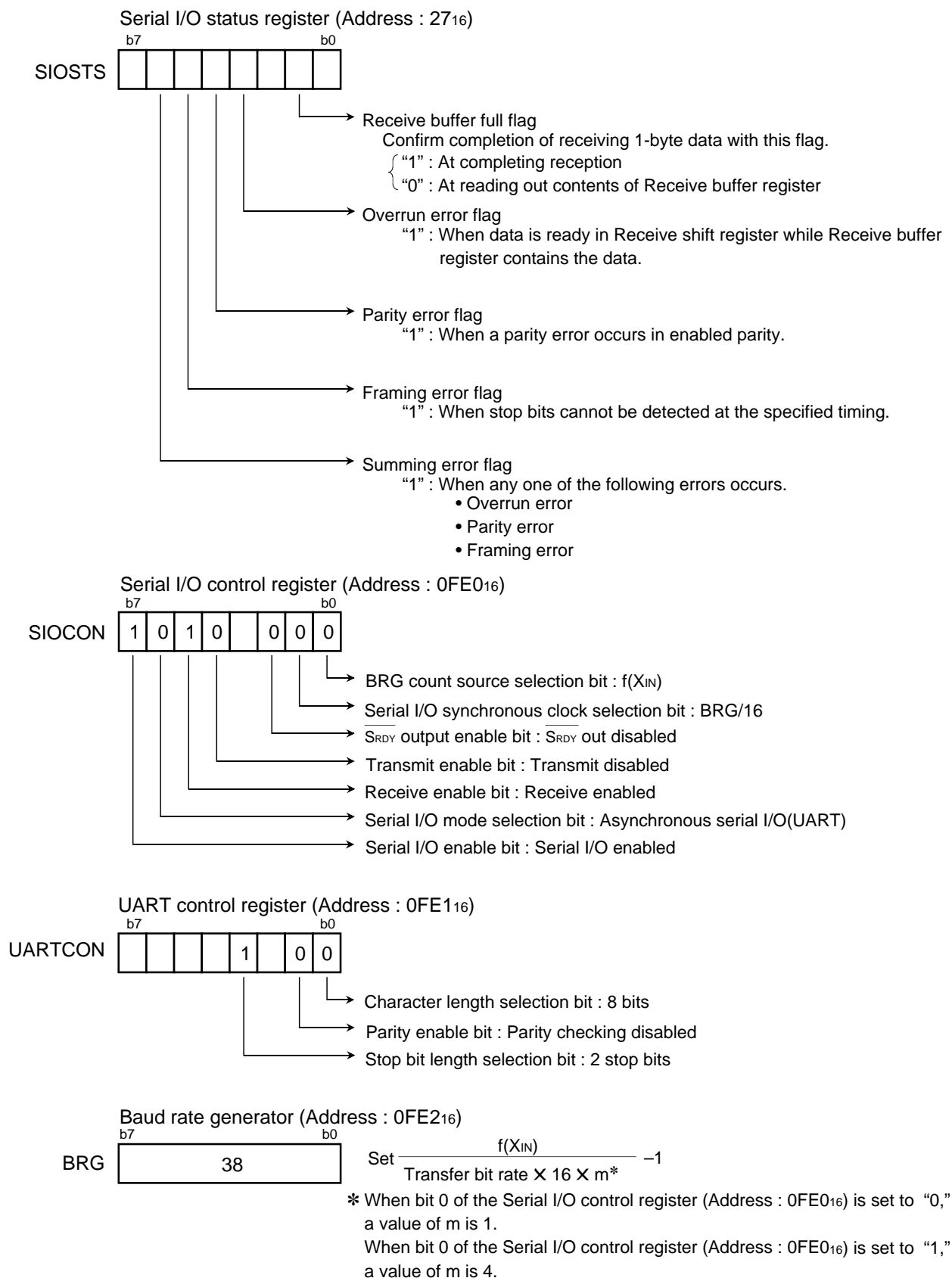


Fig. 2.4.32 Registers setting related to receiving side

APPLICATION

2.4 Serial I/O

Figure 2.4.33 shows a control procedure of the transmitting side, and Figure 2.4.34 shows a control procedure of the receiving side.

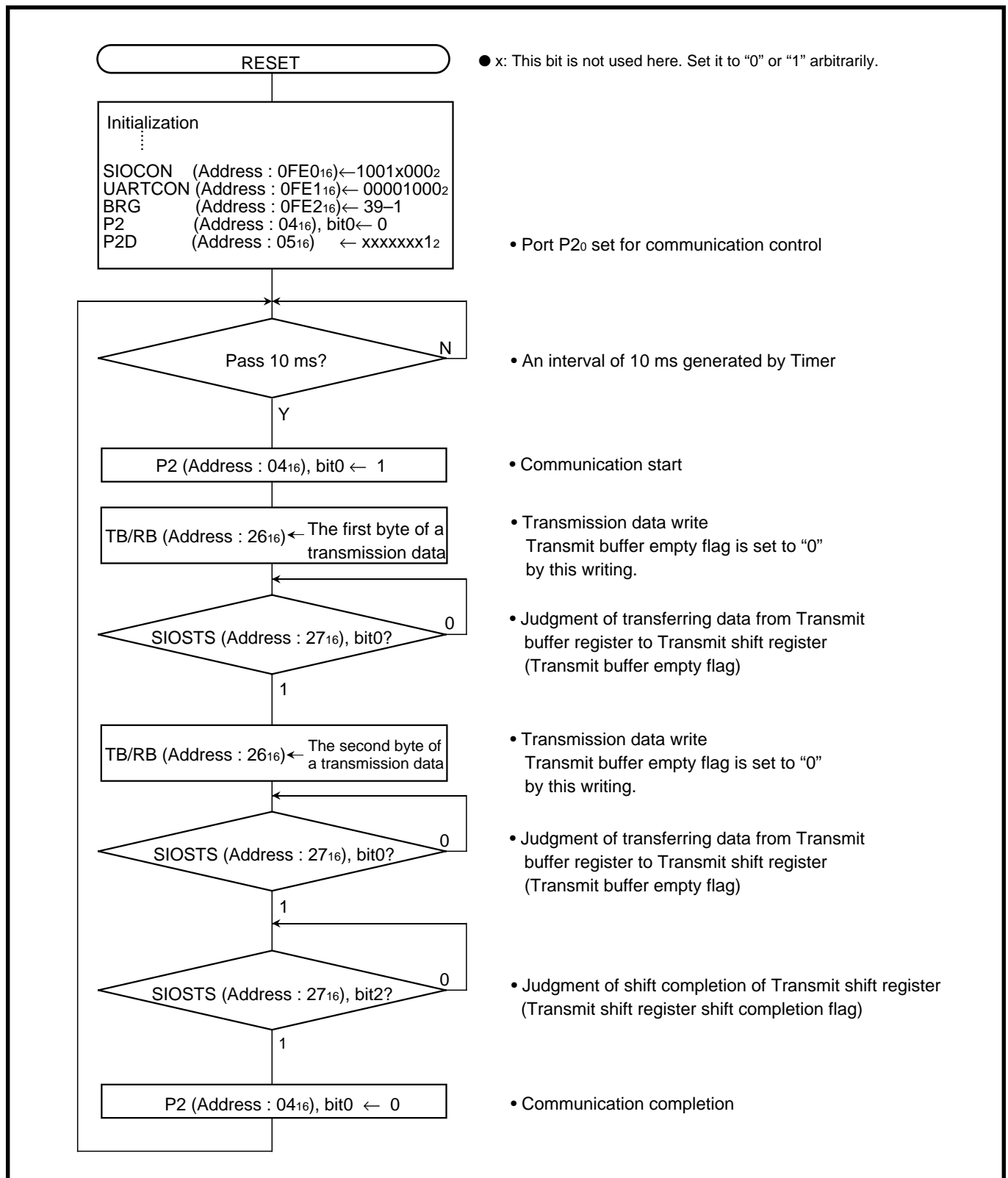


Fig. 2.4.33 Control procedure of transmitting side

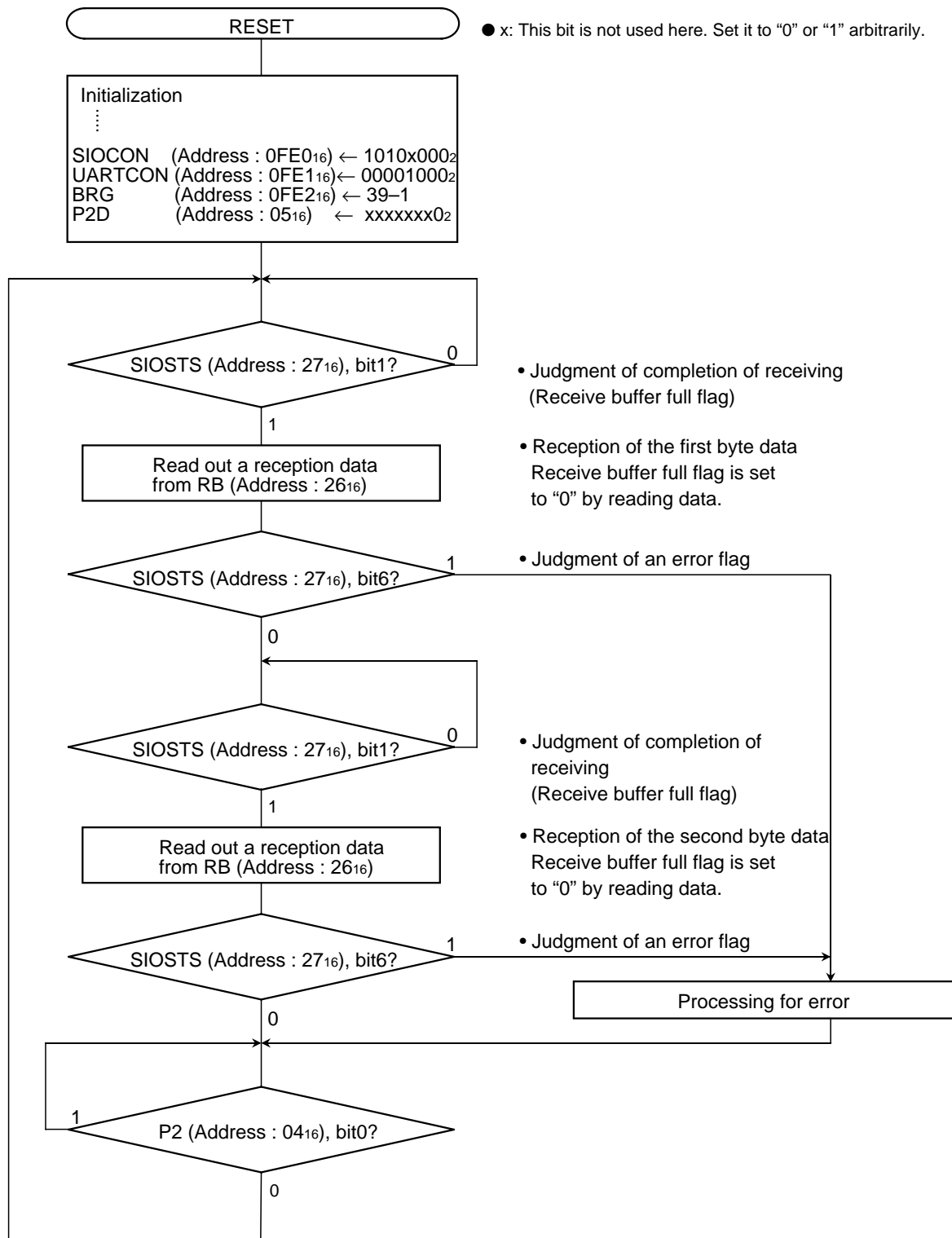


Fig. 2.4.34 Control procedure of receiving side

APPLICATION

2.4 Serial I/O

2.4.6 Notes on serial I/O

(1) Notes when selecting clock synchronous serial I/O (Serial I/O)

① Stop of transmission operation

Clear the serial I/O enable bit and the transmit enable bit to "0" (Serial I/O and transmit disabled).

● Reason

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O enable bit is cleared to "0" (Serial I/O disabled), the internal transmission is running (in this case, since pins TxD, RxD, SCLK, and SRDY function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register in this state, data starts to be shifted to the transmit shift register. When the serial I/O enable bit is set to "1" at this time, the data during internally shifting is output to the TxD pin and an operation failure occurs.

② Stop of receive operation

Clear the receive enable bit to "0" (receive disabled), or clear the serial I/O enable bit to "0" (Serial I/O disabled).

③ Stop of transmit/receive operation

Clear the transmit enable bit and receive enable bit to "0" simultaneously (transmit and receive disabled).

(when data is transmitted and received in the clock synchronous serial I/O mode, any one of data transmission and reception cannot be stopped.)

● Reason

In the clock synchronous serial I/O mode, the same clock is used for transmission and reception. If any one of transmission and reception is disabled, a bit error occurs because transmission and reception cannot be synchronized.

In this mode, the clock circuit of the transmission circuit also operates for data reception. Accordingly, the transmission circuit does not stop by clearing only the transmit enable bit to "0" (transmit disabled). Also, the transmission circuit is not initialized by clearing the serial I/O enable bit to "0" (Serial I/O disabled) (refer to (1) ①).

(2) Notes when selecting clock asynchronous serial I/O (Serial I/O)**① Stop of transmission operation**

Clear the transmit enable bit to "0" (transmit disabled).

● Reason

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O enable bit is cleared to "0" (Serial I/O disabled), the internal transmission is running (in this case, since pins TxD, RxD, SCLK, and SRDY function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register in this state, data starts to be shifted to the transmit shift register. When the serial I/O enable bit is set to "1" at this time, the data during internally shifting is output to the TxD pin and an operation failure occurs.

② Stop of receive operation

Clear the receive enable bit to "0" (receive disabled).

③ Stop of transmit/receive operation**Only transmission operation is stopped.**

Clear the transmit enable bit to "0" (transmit disabled).

● Reason

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O enable bit is cleared to "0" (Serial I/O disabled), the internal transmission is running (in this case, since pins TxD, RxD, SCLK, and SRDY function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register in this state, data starts to be shifted to the transmit shift register. When the serial I/O enable bit is set to "1" at this time, the data during internally shifting is output to the TxD pin and an operation failure occurs.

Only receive operation is stopped.

Clear the receive enable bit to "0" (receive disabled).

(3) $\overline{\text{SRDY}}$ output of reception side (Serial I/O)

When signals are output from the $\overline{\text{SRDY}}$ pin on the reception side by using an external clock in the clock synchronous serial I/O mode, set all of the receive enable bit, the $\overline{\text{SRDY}}$ output enable bit, and the transmit enable bit to "1" (transmit enabled).

(4) Setting serial I/O control register again (Serial I/O)

Set the serial I/O control register again after the transmission and the reception circuits are reset by clearing both the transmit enable bit and the receive enable bit to "0."

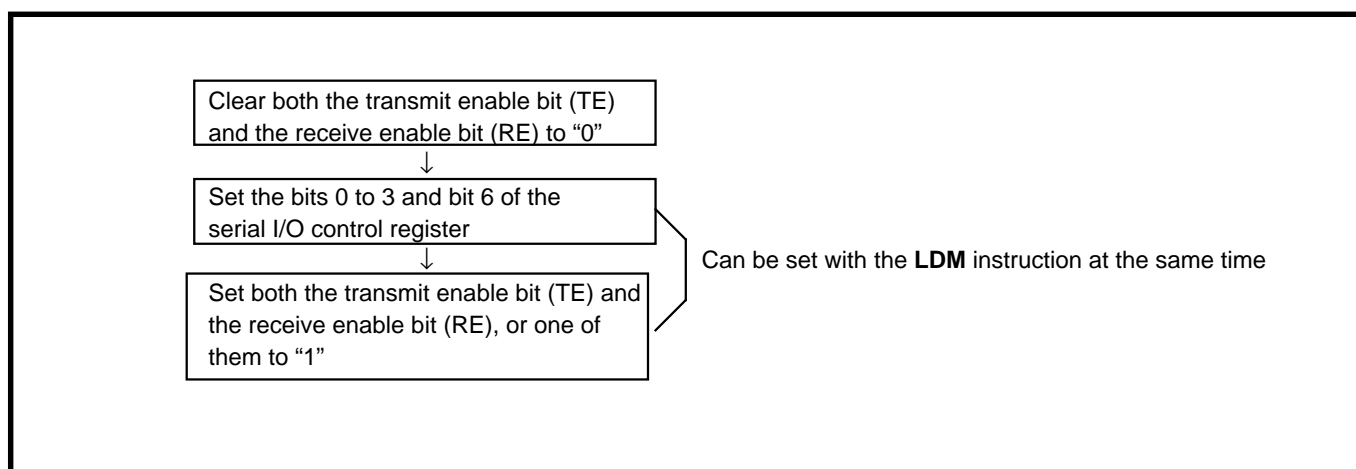


Fig. 2.4.35 Sequence of setting serial I/O control register again

APPLICATION

2.4 Serial I/O

(5) Data transmission control with referring to transmit shift register completion flag (Serial I/O)
The transmit shift register completion flag changes from “1” to “0” with a delay of 0.5 to 1.5 shift clocks. When data transmission is controlled with referring to the flag after writing the data to the transmit buffer register, note the delay.

(6) Transmission control when external clock is selected (Serial I/O)
When an external clock is used as the synchronous clock for data transmission, set the transmit enable bit to “1” at “H” of the SCLK input level. Also, write the transmit data to the transmit buffer register (serial I/O shift register) at “H” of the SCLK input level.

(7) Transmit interrupt request when transmit enable bit is set (Serial I/O)
When the transmit interrupt is used, set the transmit interrupt enable bit to transmit enabled as shown in the following sequence.

- ① Set the interrupt enable bit to “0” (disabled) with CLB instruction.
- ② Prepare serial I/O for transmission/reception.
- ③ Set the interrupt request bit to “0” with CLB instruction after 1 or more instruction has been executed.
- ④ Set the interrupt enable bit to “1” (enabled).

● Reason

When the transmission enable bit is set to “1”, the transmit buffer empty flag and transmit shift register completion flag are set to “1”. The interrupt request is generated and the transmission interrupt bit is set regardless of which of the two timings listed below is selected as the timing for the transmission interrupt to be generated.

- Transmit buffer empty flag is set to “1”
- Transmit shift register completion flag is set to “1”

2.5 USB function

Some application notes are available on the Web site: “ Mitsubishi MCU Technical Information ”
- USB MCU

(<http://www.infocom.maec.co.jp/indexe.htm>)

Please refer to them for explanation and application of USB function.

APPLICATION

2.6 External bus interface(EXB)

2.6 External bus interface(EXB)

Some application notes are available on the Web site: “ Mitsubishi MCU Technical Information ”
- USB MCU

(<http://www.infocom.maec.co.jp/indexe.htm>)

Please refer to them for explanation and application of external bus interface.

2.7 A-D converter

This paragraph explains the registers setting method and the notes related to the A-D converter.

2.7.1 Memory map

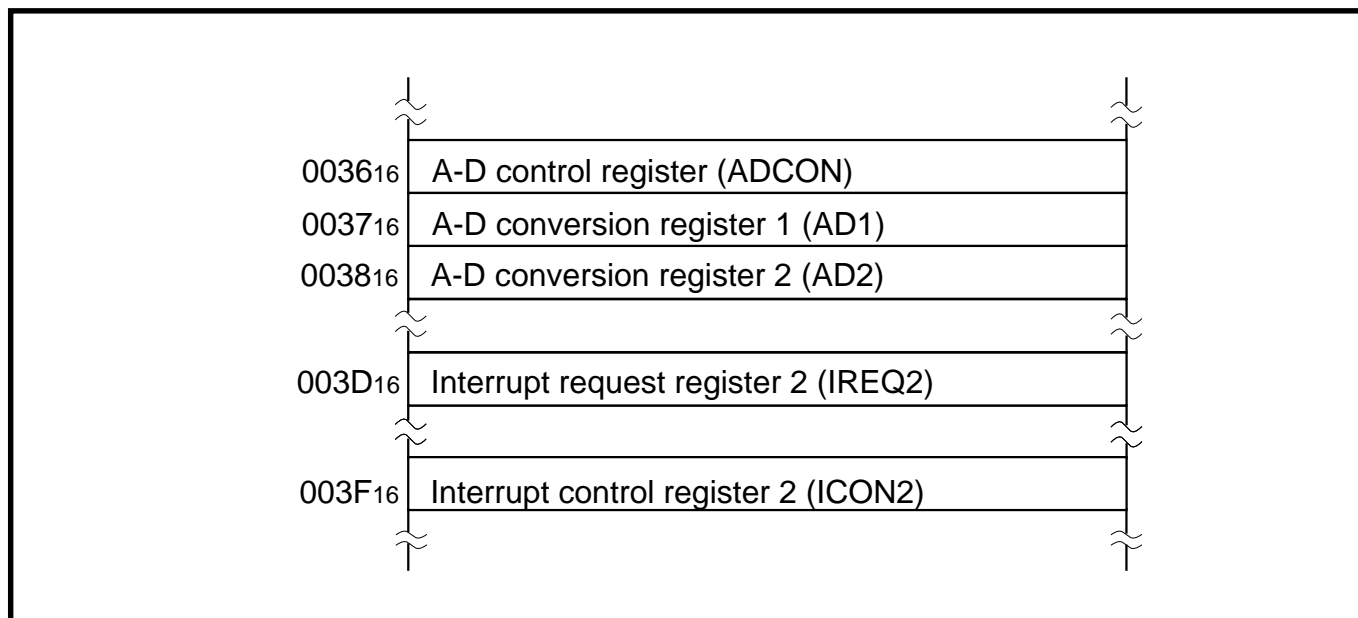


Fig. 2.7.1 Memory map of registers related to A-D converter

2.7.2 Related registers

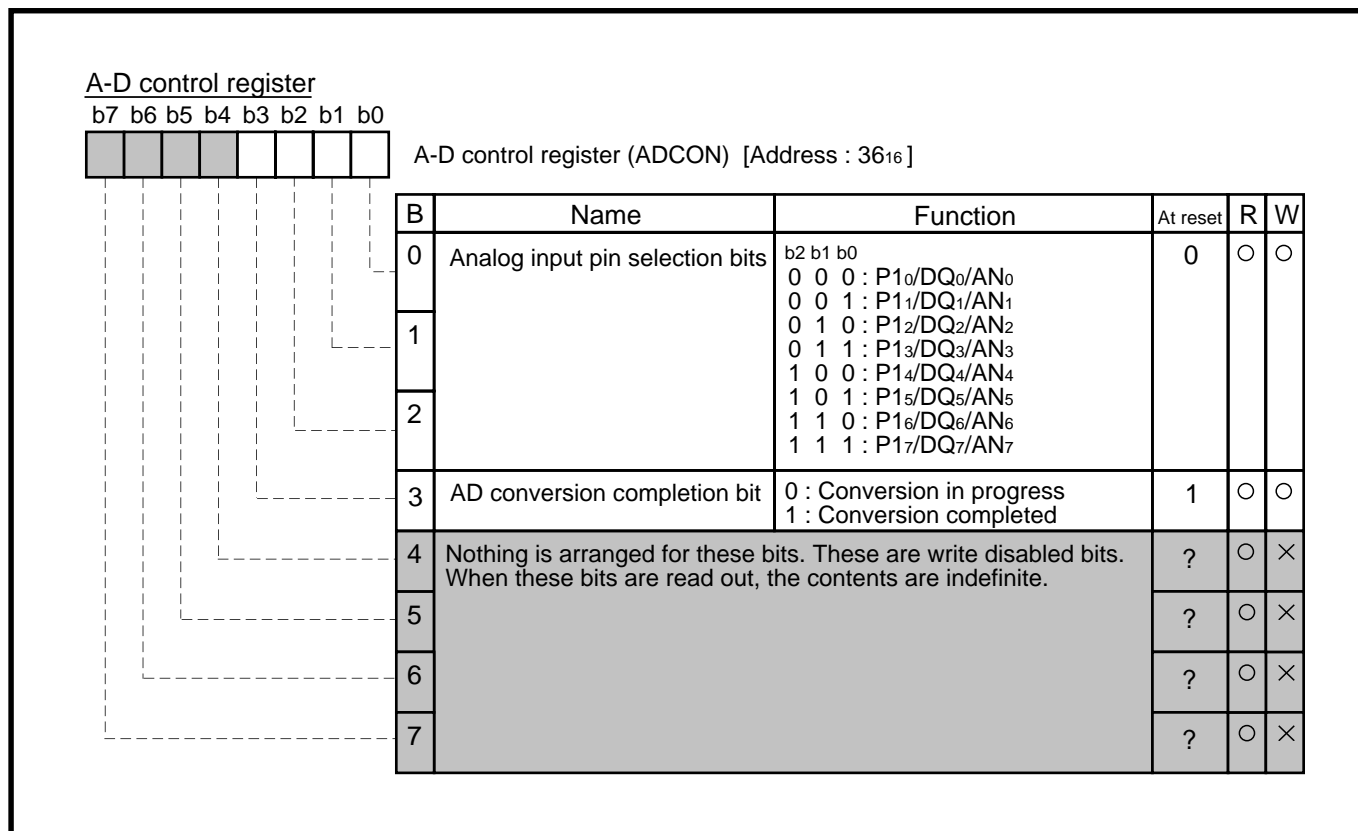


Fig. 2.7.2 Structure of A-D control register

APPLICATION

2.7 A-D converter

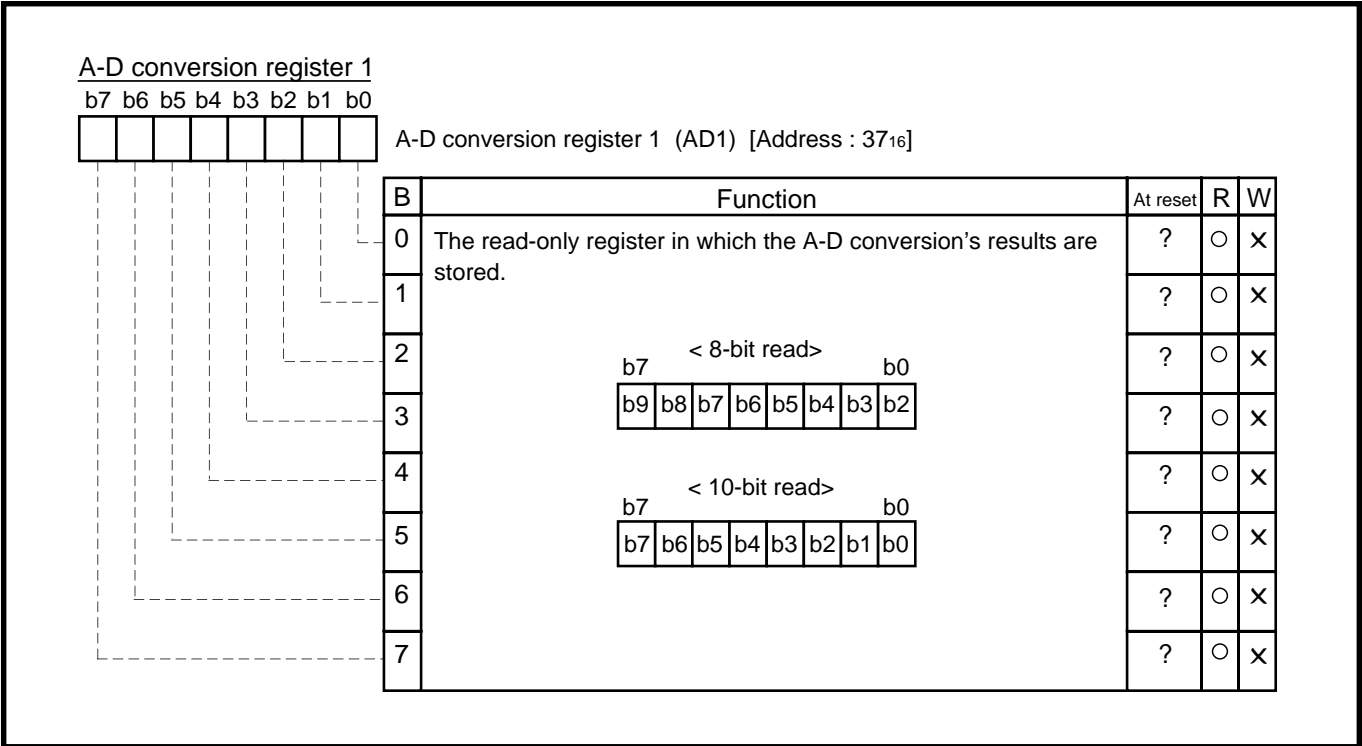


Fig. 2.7.3 Structure of A-D conversion register 1

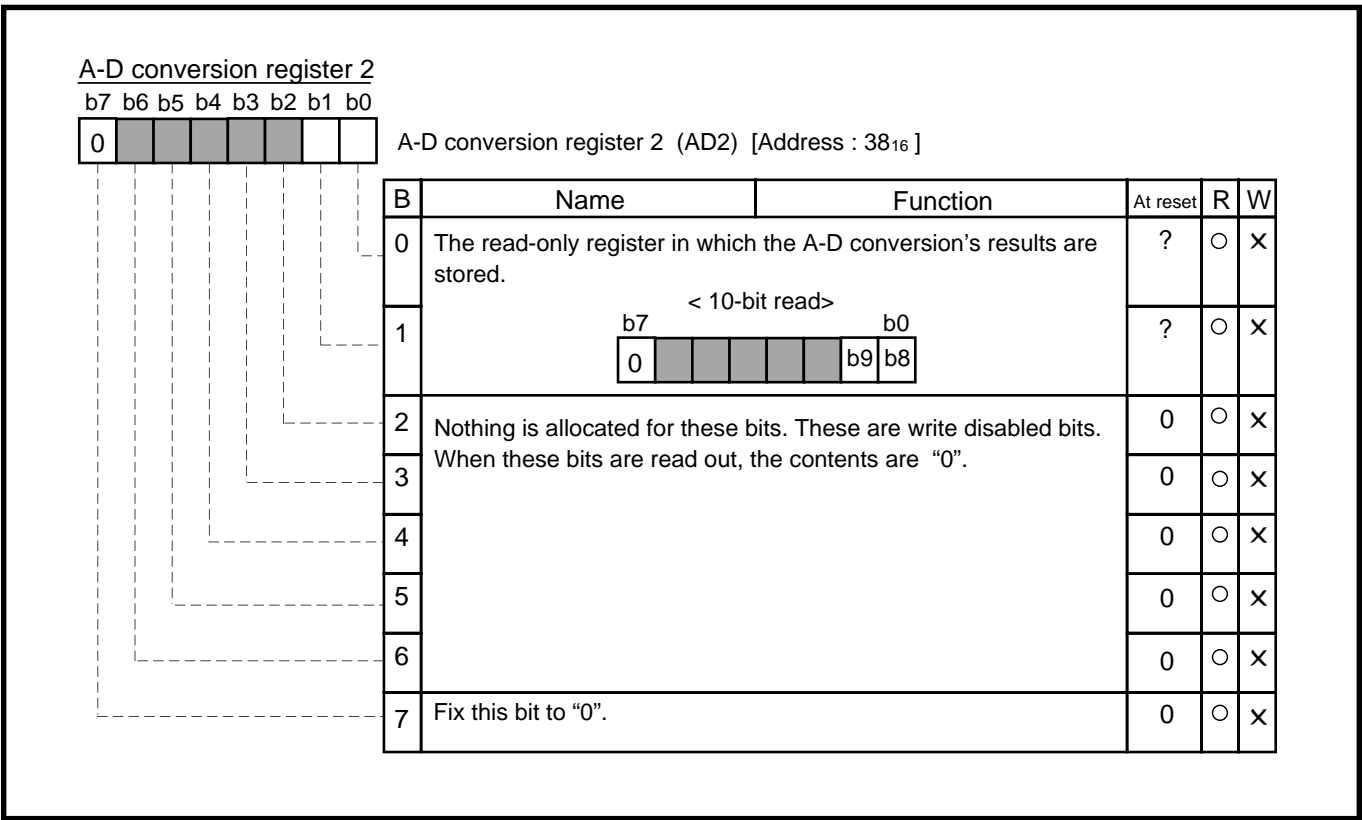


Fig. 2.7.4 Structure of A-D conversion register 2

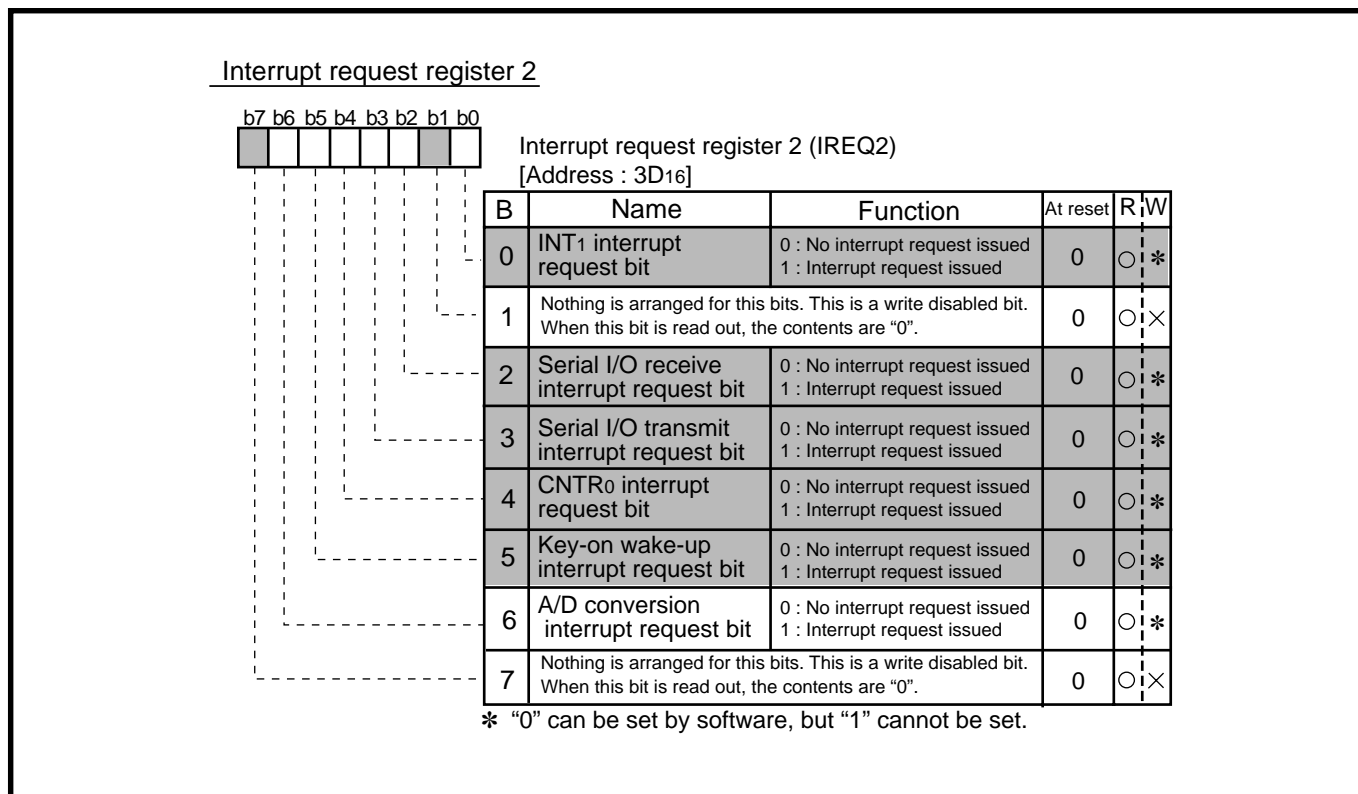


Fig. 2.7.5 Structure of Interrupt request register 2

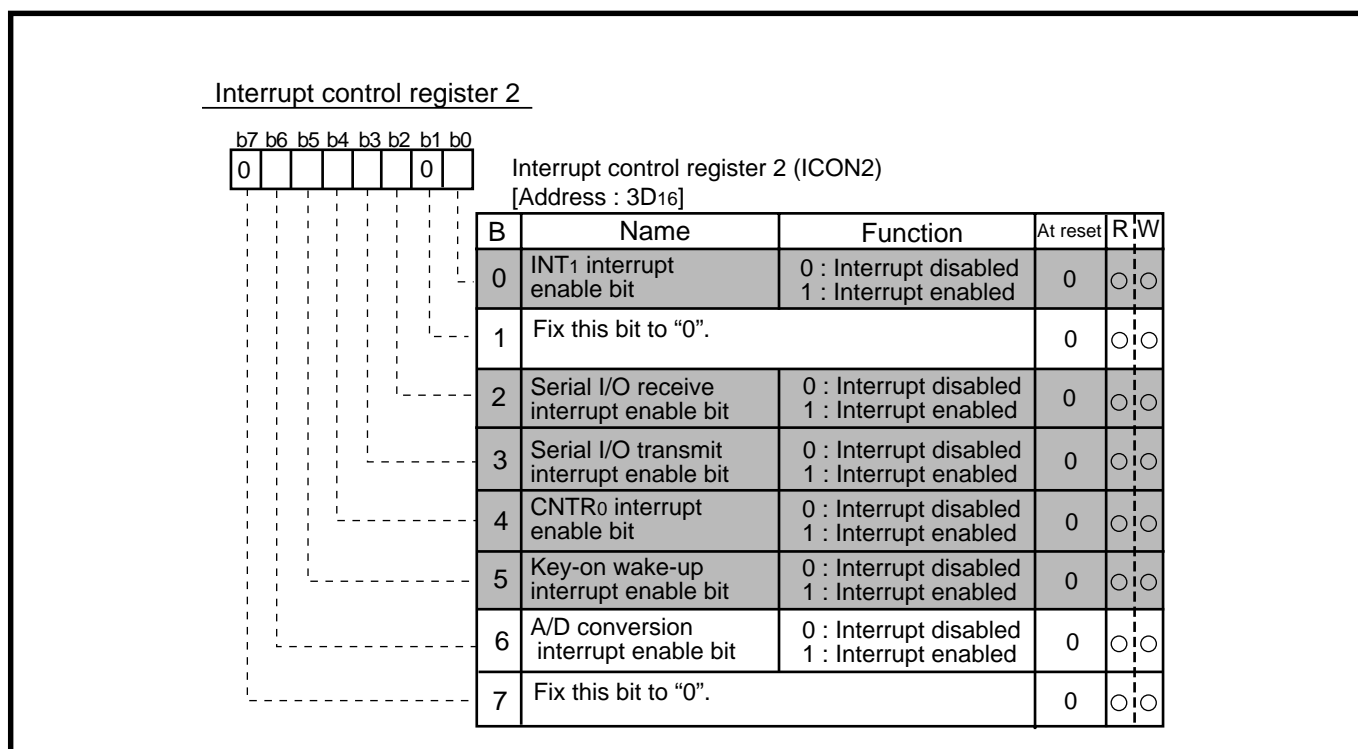


Fig. 2.7.6 Structure of Interrupt control register 2

APPLICATION

2.7 A-D converter

2.7.3 A-D converter application examples

(1) Conversion of analog input voltage

Outline : The analog input voltage input from a sensor is converted to digital values.

Figure 2.7.7 shows a connection diagram, and Figure 2.7.8 shows the related registers setting.

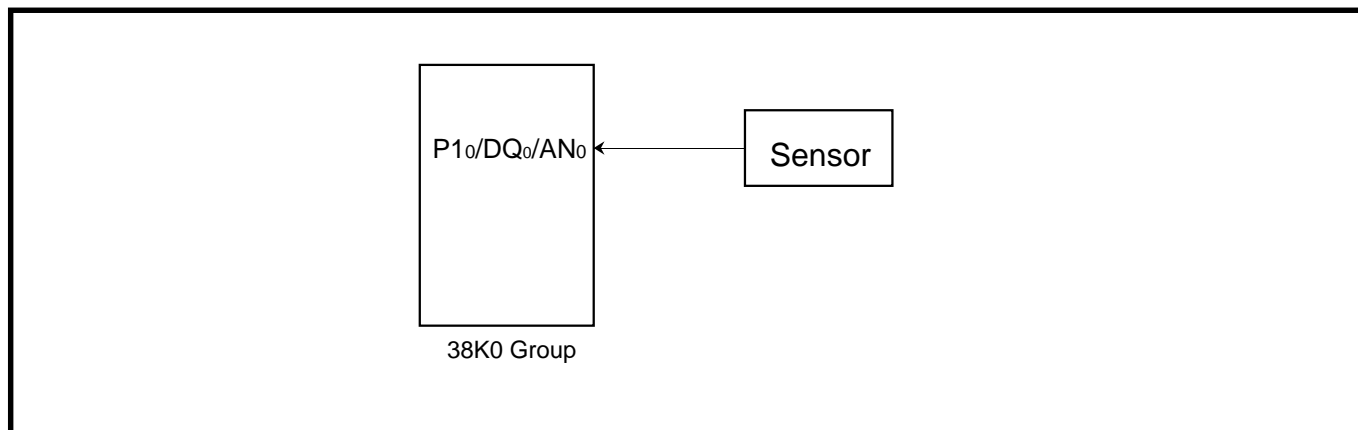


Fig. 2.7.7 Connection diagram

Specifications :

- The analog input voltage input from a sensor is converted to digital values.
- P10/DQ0/AN0 pin is used as an analog input pin.

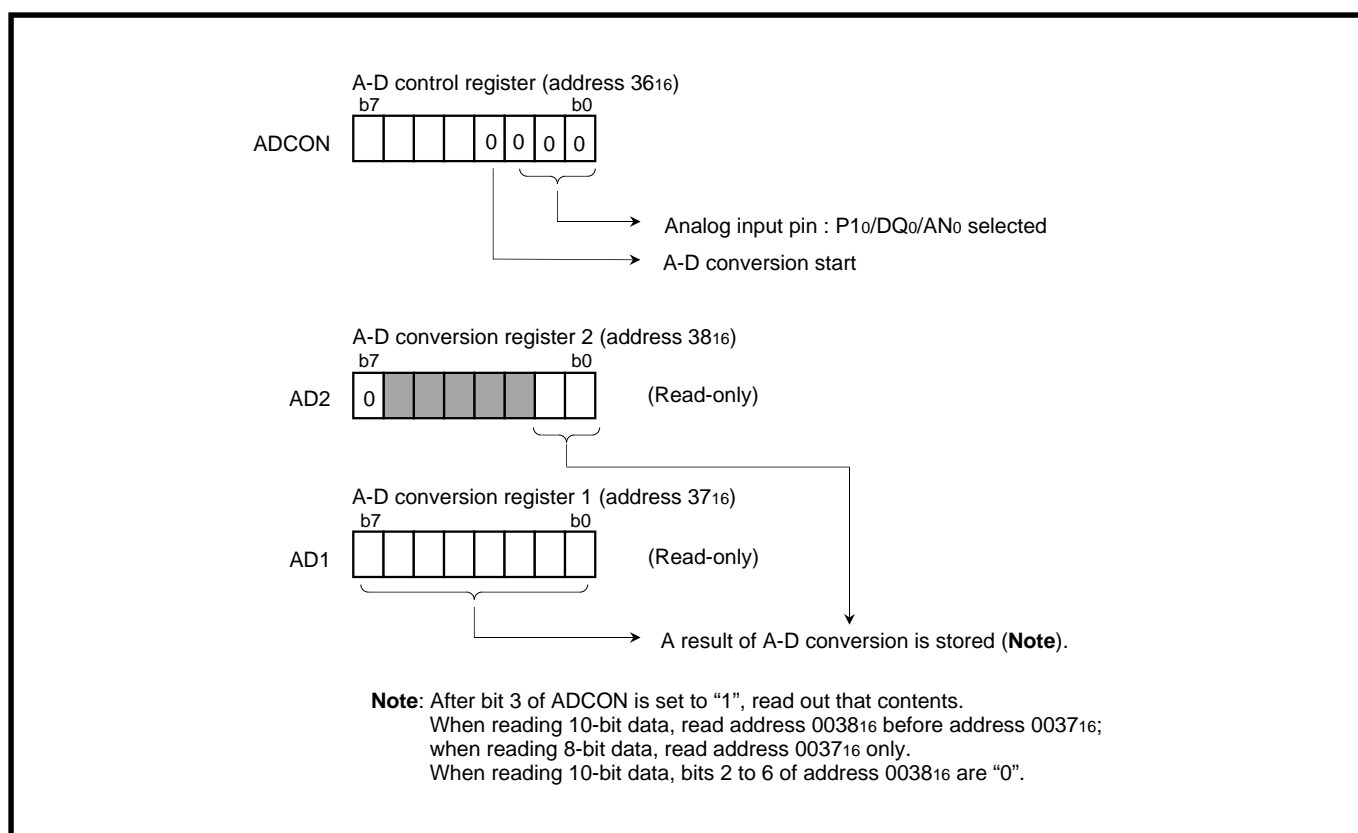


Fig. 2.7.8 Related registers setting

An analog input signal from a sensor is converted to the digital value according to the related registers setting shown by Figure 2.7.8. Figure 2.7.9 shows the control procedure for 8-bit read, and Figure 2.7.10 shows the control procedure for 10-bit read.

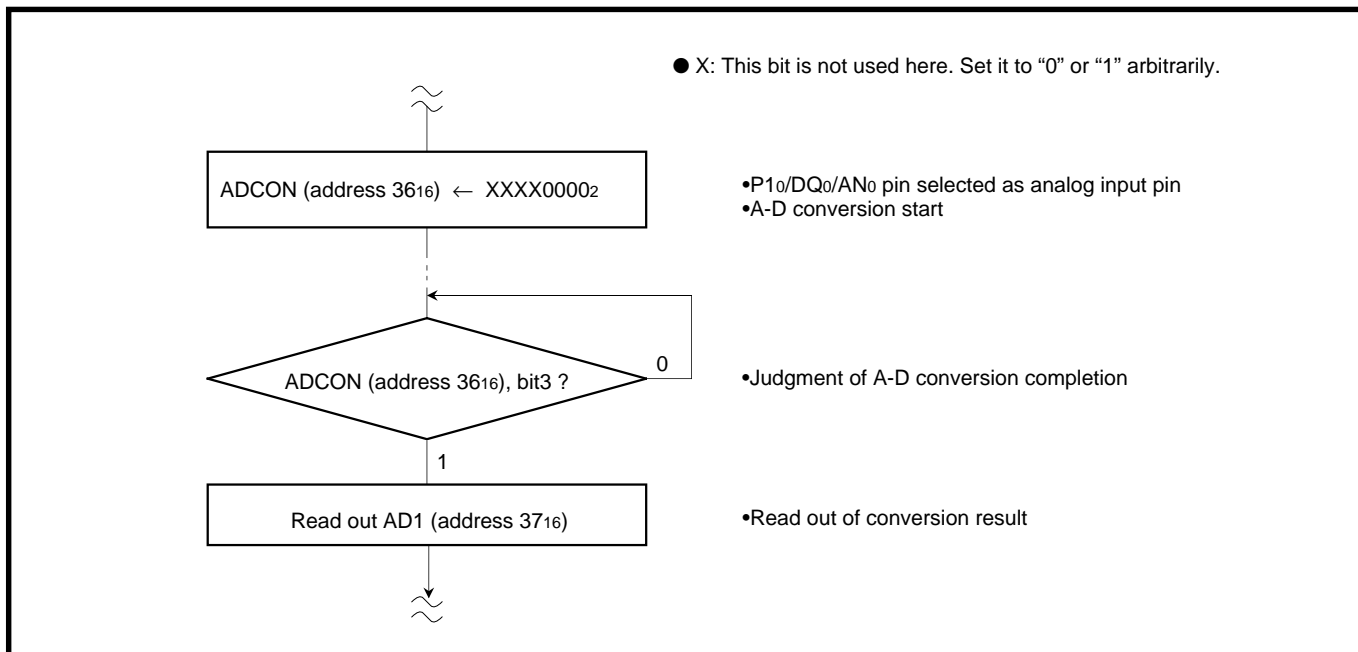


Fig. 2.7.9 Control procedure for 8-bit read

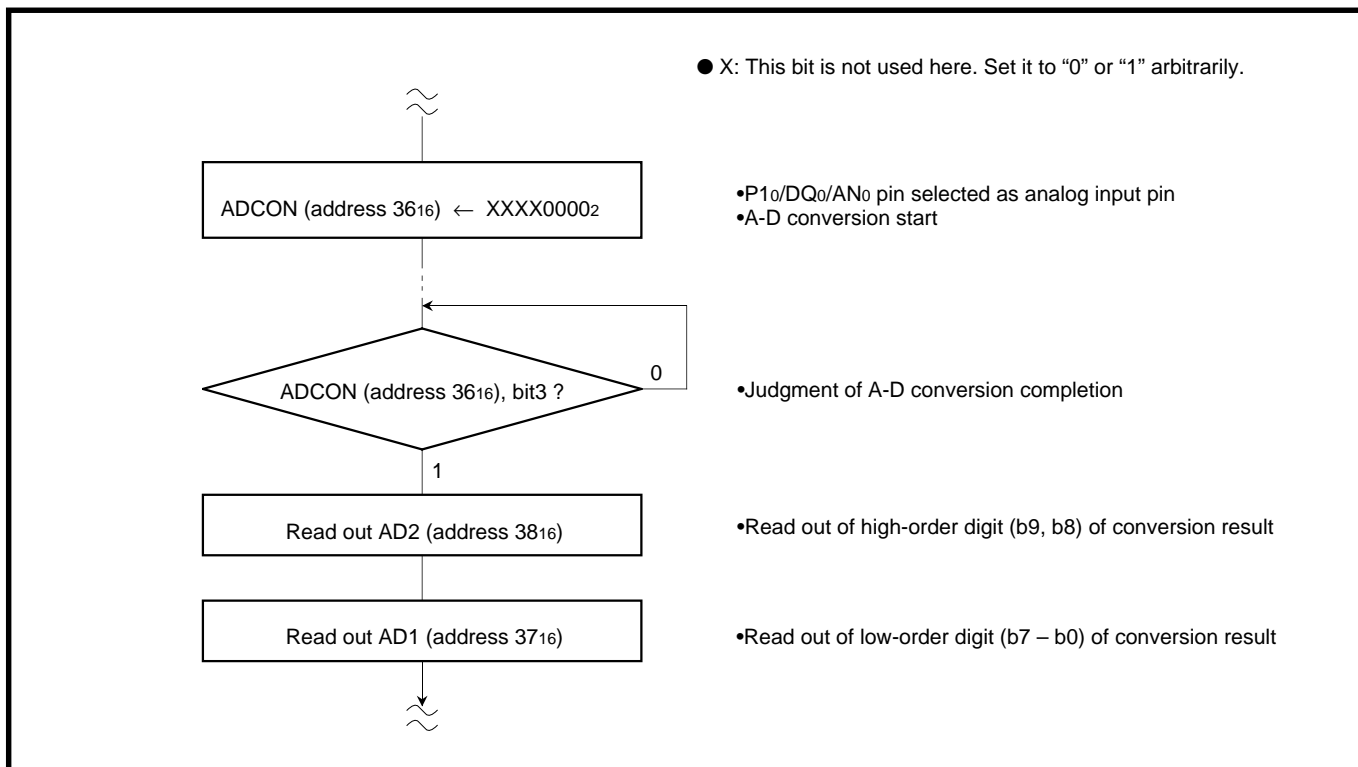


Fig. 2.7.10 Control procedure for 10-bit read

APPLICATION

2.7 A-D converter

2.7.4 Notes on A-D converter

(1) Analog input pin

Make the signal source impedance for analog input low, or equip an analog input pin with an external capacitor of 0.01 μ F to 1 μ F. Further, be sure to verify the operation of application products on the user side.

● Reason

An analog input pin includes the capacitor for analog voltage comparison. Accordingly, when signals from signal source with high impedance are input to an analog input pin, charge and discharge noise generates. This may cause the A-D conversion precision to be worse.

(2) Clock frequency during A-D conversion

The comparator consists of a capacity coupling, and a charge of the capacity will be lost if the clock frequency is too low. Thus, make sure the following during an A-D conversion.

- $f(X_{IN})$ is 500 kHz or more
- Do not execute the **STP** instruction

2.8 Watchdog timer

This paragraph explains the registers setting method and the notes related to the watchdog timer.

2.8.1 Memory map

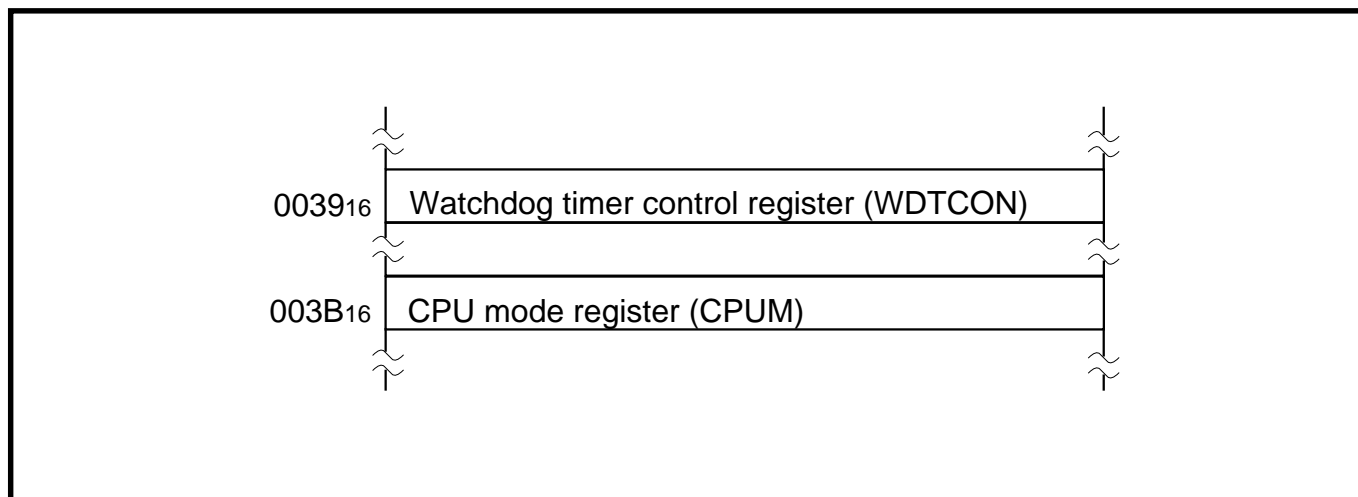


Fig. 2.8.1 Memory map of registers related to watchdog timer

2.8.2 Related registers

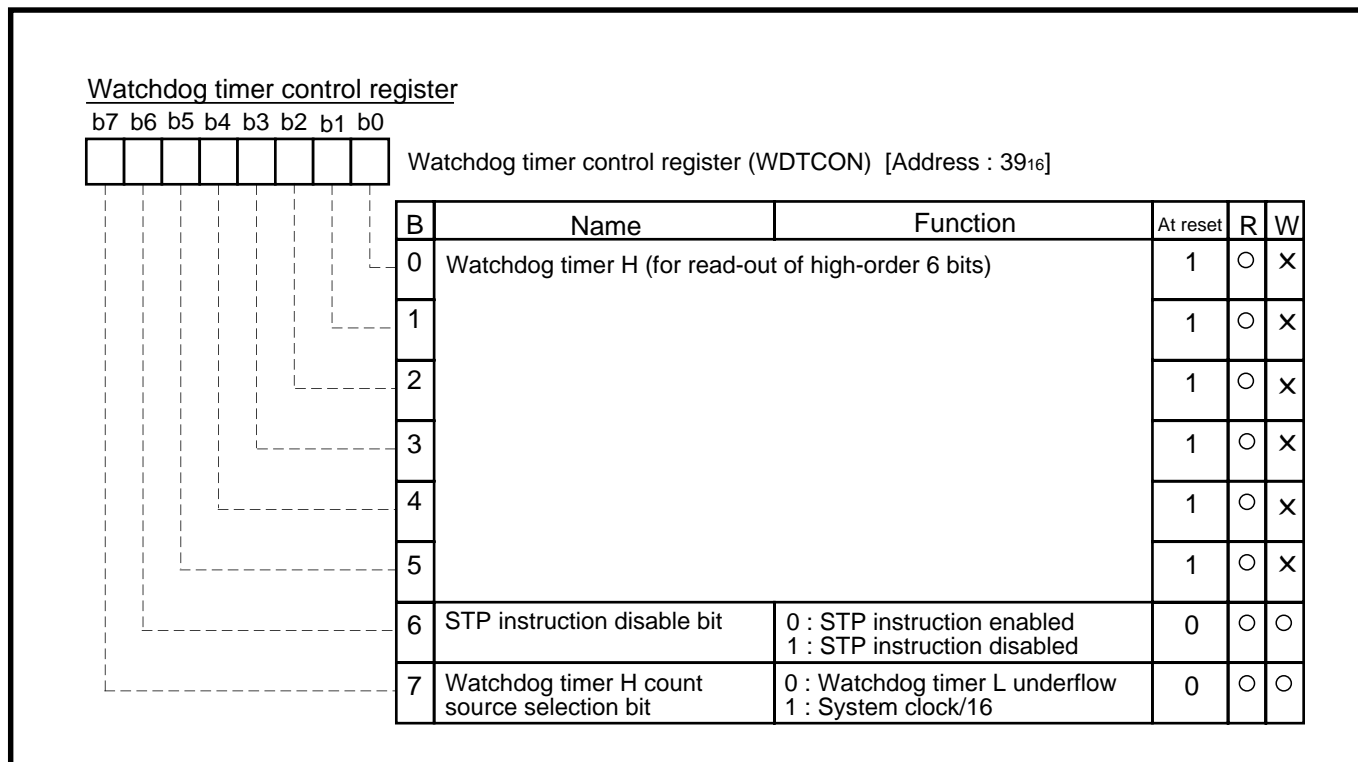
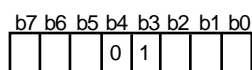


Fig. 2.8.2 Structure of Watchdog timer control register

APPLICATION

2.8 Watchdog timer

CPU mode register



CPU mode register
(CPUM: address 3B₁₆)

B	Name	Function	At reset	R ₁ W
0	Processor mode bits	b1 b0 0 0 : Single-chip mode	0	○ ○
		0 1 : Not available		
1		1 0 : Not available	*	○ ○
		1 1 : Not available		
2	Stack page selection bit	0 : 0 page 1 : 1 page	0	○ ○
3	Fix this bit to "1".		1	○ ○
4	Fix this bit to "0".		0	○ ○
5	System clock selection bit	0 : Main clock f(X _{IN}) 1 : f _{SYN}	0	○ ○
6	System clock division ratio selection bits	b7 b6 0 0 : $\phi = f(\text{system clock})/8$ (8-divide mode)	0	○ ○
7		0 1 : $\phi = f(\text{system clock})/4$ (4-divide mode) 1 0 : $\phi = f(\text{system clock})/2$ (2-divide mode) 1 1 : $\phi = f(\text{system clock})$ (Through mode)		

*: The initial value of bit 1 depends on the CNVss level.

Fig. 2.8.3 Structure of CPU mode register

2.8.3 Watchdog timer application examples

(1) Detection of program runaway

Outline: If program runaway occurs, let the microcomputer reset, using the internal timer for detection of program runaway.

- Specifications:**
- An underflow of watchdog timer H is judged to be program runaway, and the microcomputer is returned to the reset status.
 - Before the watchdog timer H underflows, "0" is set into bit 7 of the watchdog timer control register at every cycle in a main routine.
 - Through mode is used as a system clock division ratio.
 - An underflow signal of the watchdog timer L is supplied as the count source of watchdog timer H.

Figure 2.8.4 shows a watchdog timer connection and division ratio setting; Figure 2.8.5 shows the related registers setting; Figure 2.8.6 shows the control procedure.

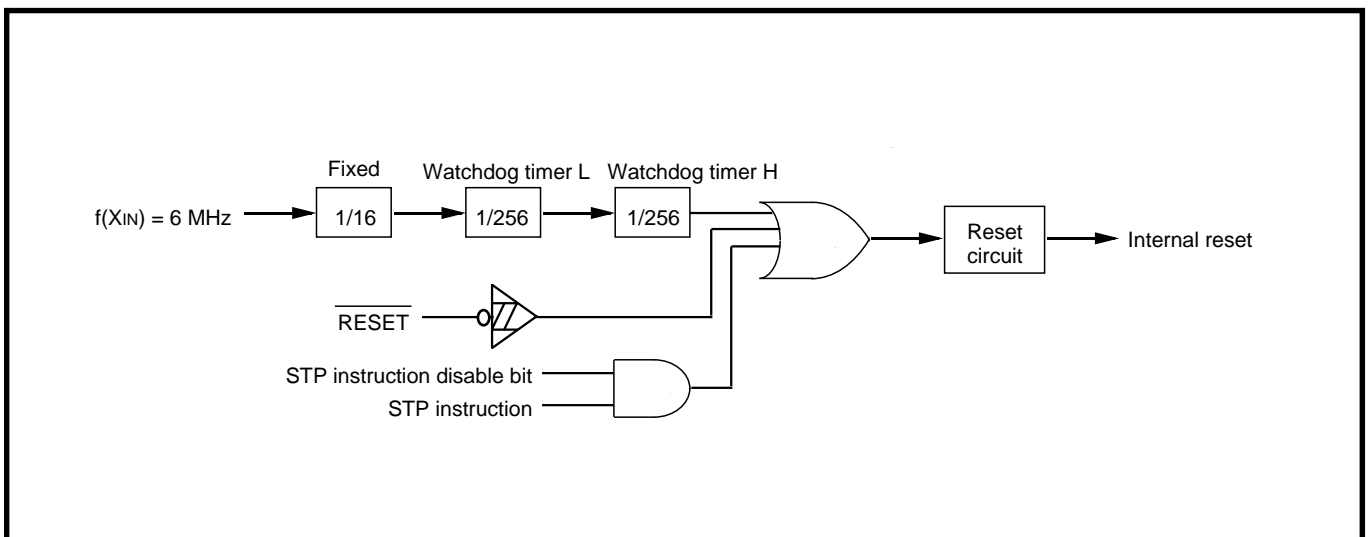


Fig. 2.8.4 Watchdog timer connection and division ratio setting

APPLICATION

2.8 Watchdog timer

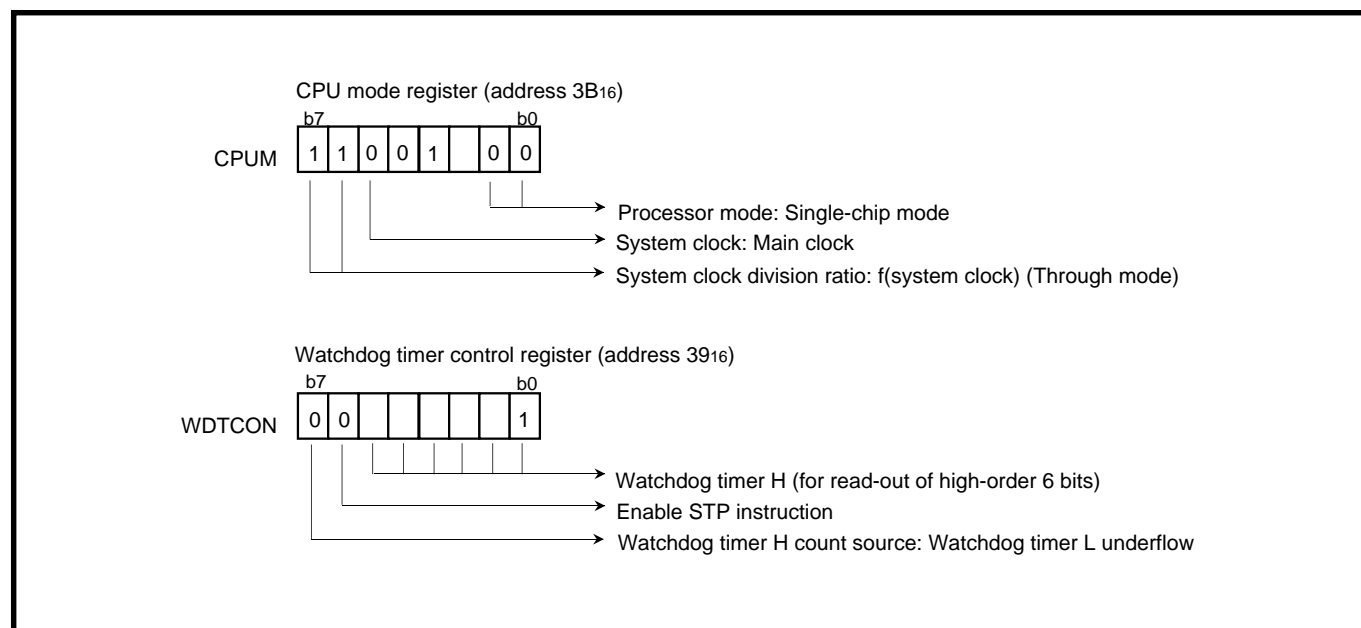


Fig. 2.8.5 Related registers setting

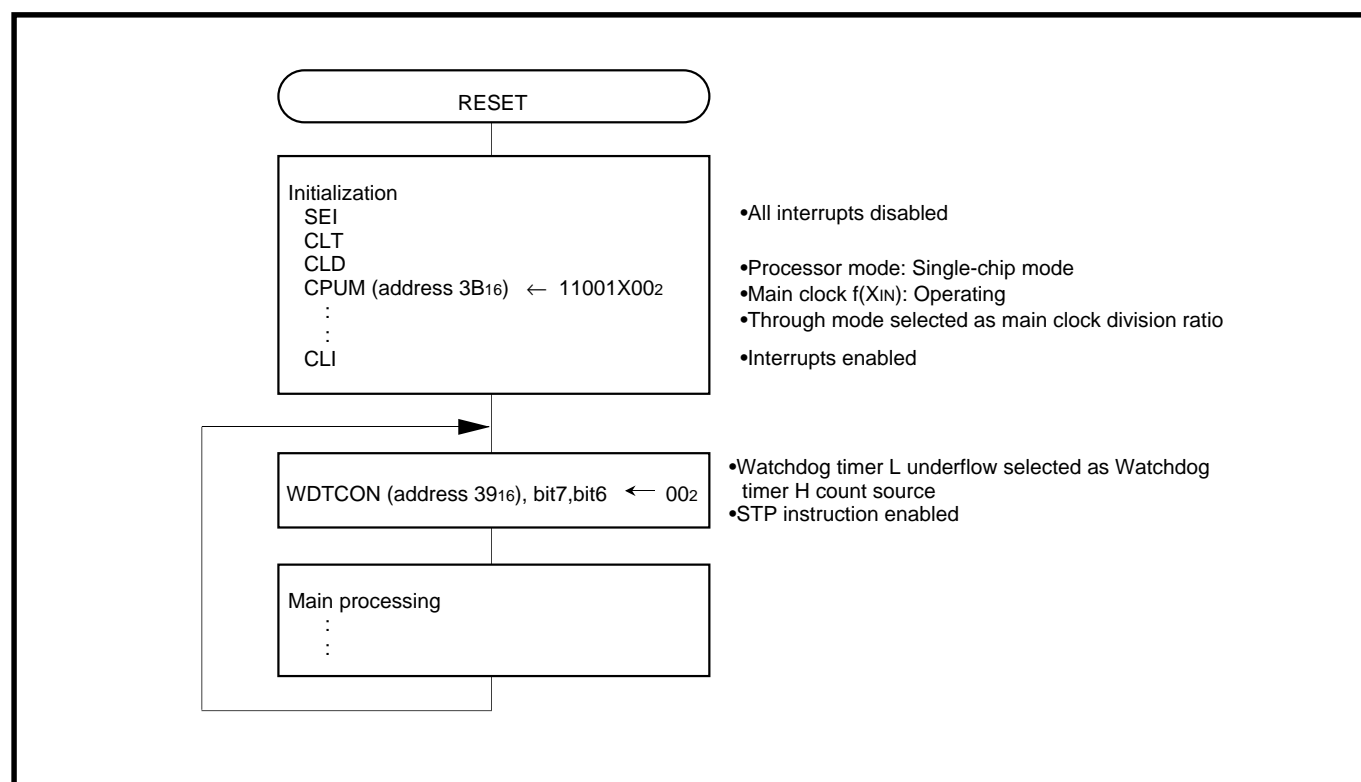


Fig. 2.8.6 Control procedure

2.8.4 Notes on watchdog timer

- Make sure that the watchdog timer does not underflow while waiting Stop release, because the watchdog timer keeps counting during that term.
- When the STP instruction disable bit has been set to “1”, it is impossible to switch it to “0” by a program.

2.9 Reset

2.9.1 Connection example of reset IC

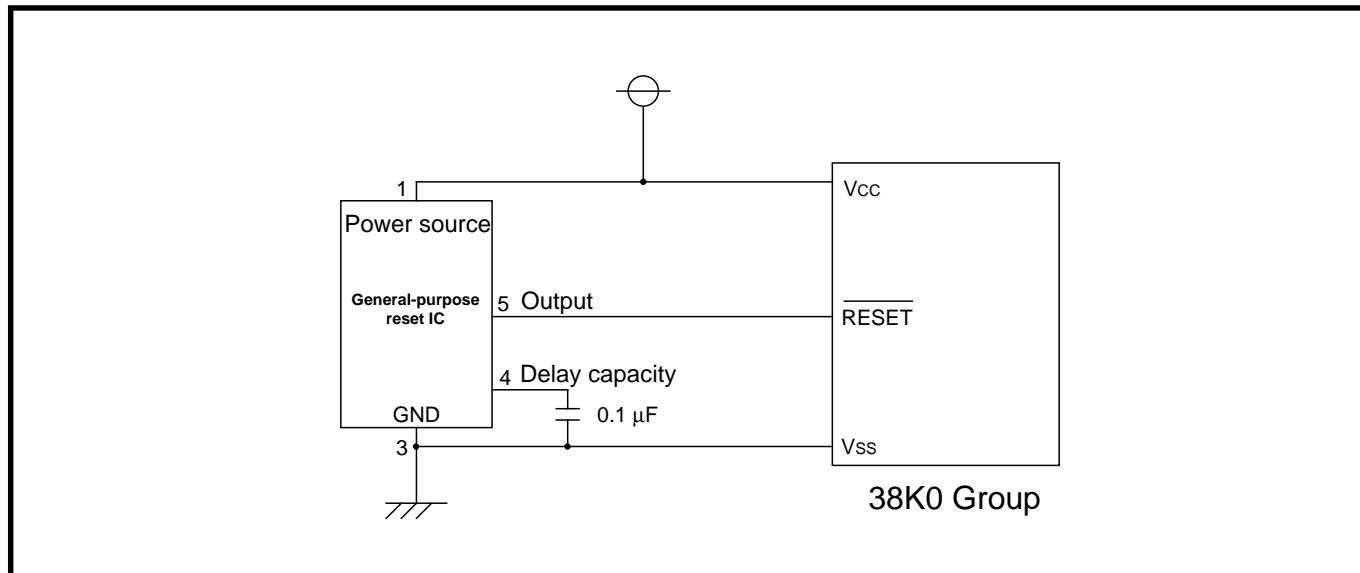


Fig. 2.9.1 Example of poweron reset circuit

Figure 2.9.2 shows the system example which switches to the RAM backup mode by detecting a drop of the system power source voltage with the INT interrupt.

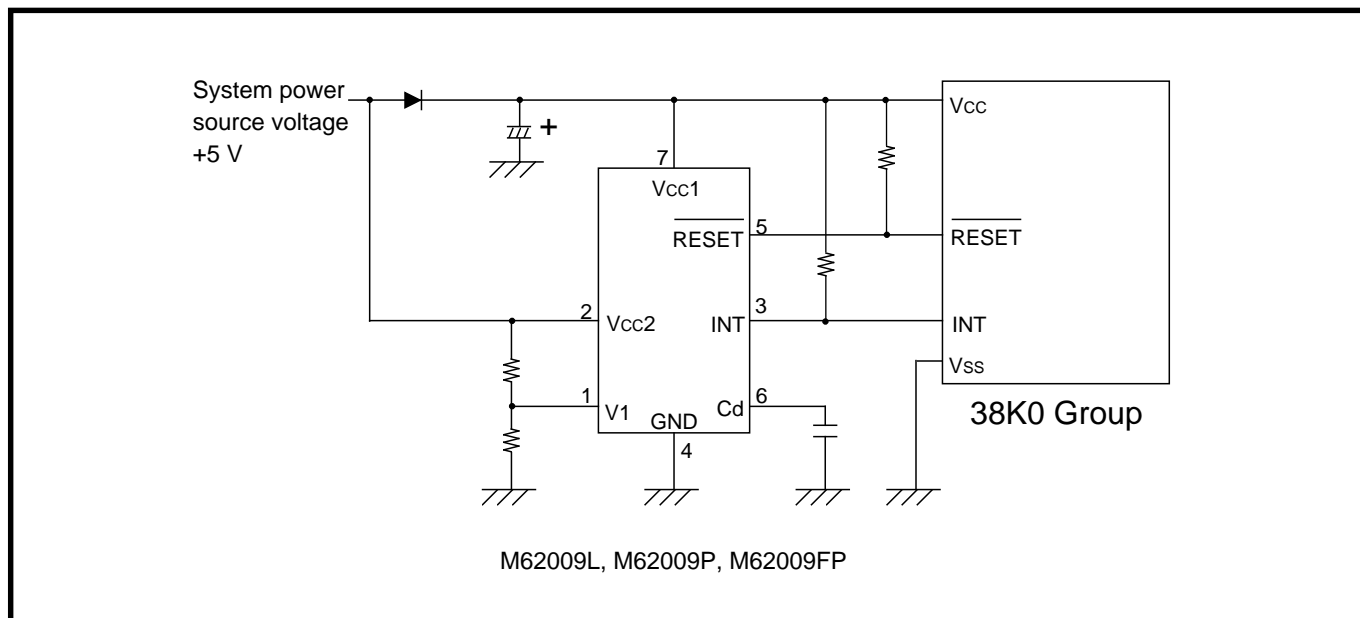


Fig. 2.9.2 RAM backup system

APPLICATION

2.9 Reset

2.9.2 Notes on $\overline{\text{RESET}}$ pin

Connecting capacitor

In case where the $\overline{\text{RESET}}$ signal rise time is long, connect a ceramic capacitor or others across the $\overline{\text{RESET}}$ pin and the VSS pin. Use a 1000 pF or more capacitor for high frequency use. When connecting the capacitor, note the following :

- Make the length of the wiring which is connected to a capacitor as short as possible.
- Be sure to verify the operation of application products on the user side.

● Reason

If the several nanosecond or several ten nanosecond impulse noise enters the $\overline{\text{RESET}}$ pin, it may cause a microcomputer failure.

2.10 Frequency synthesizer (PLL)

This paragraph explains the registers setting method and the notes related to the frequency synthesizer (PLL circuit).

2.10.1 Memory map

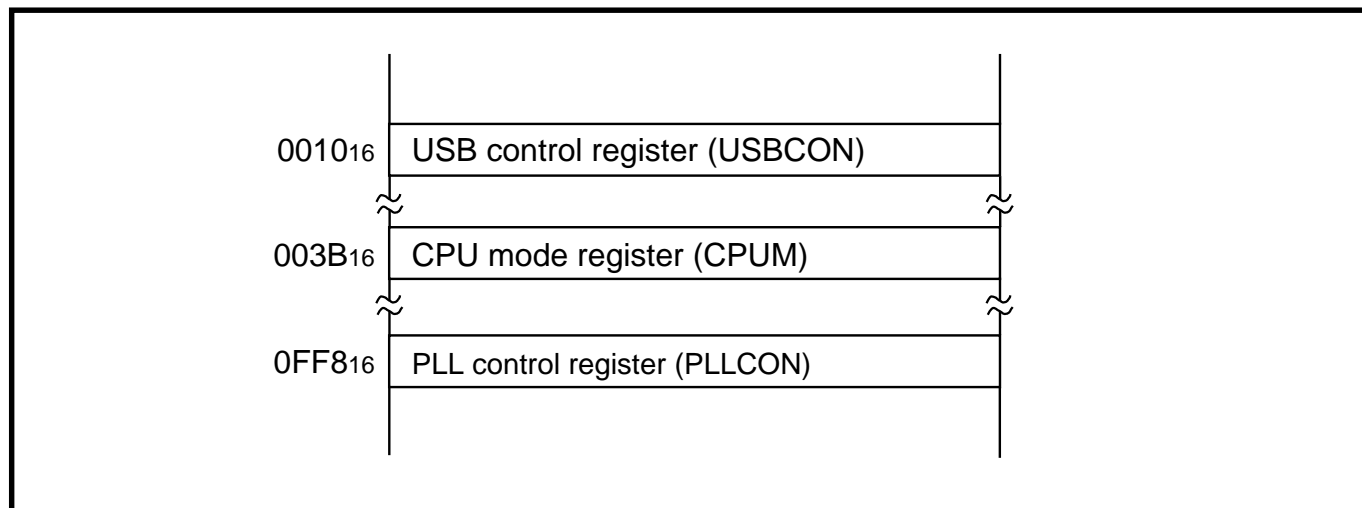


Fig. 2.10.1 Memory map of registers related to PLL

2.10.2 Related registers

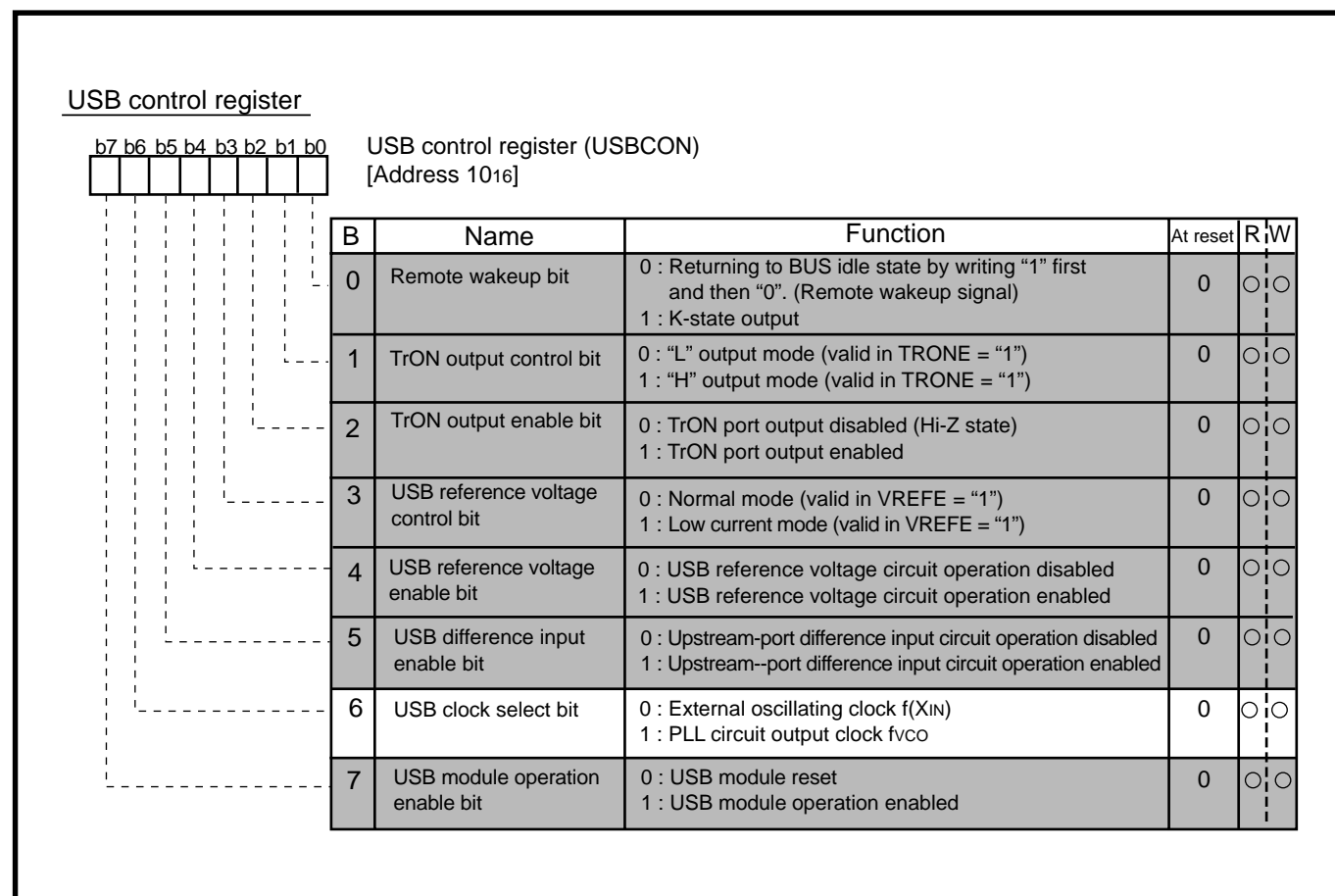


Fig. 2.10.2 Structure of USB control register

APPLICATION

2.10 Frequency synthesizer (PLL)

CPU mode register

b7	b6	b5	b4	b3	b2	b1	b0
			0	1			

CPU mode register
(CPUM: address 3B16)

B	Name	Function	At reset	R	W
0	Processor mode bits	b1 b0 0 0 : Single-chip mode 0 1 : Not available 1 0 : Not available 1 1 : Not available	0	○	○
1			*	○	○
2	Stack page selection bit	0 : 0 page 1 : 1 page	0	○	○
3	Fix this bit to "1".		1	○	○
4	Fix this bit to "0".		0	○	○
5	System clock selection bit	0 : Main clock f(XIN) 1 : fSYN	0	○	○
6	System clock division ratio selection bits	b7 b6 0 0 : $\phi = f(\text{system clock})/8$ (8-divide mode) 0 1 : $\phi = f(\text{system clock})/4$ (4-divide mode) 1 0 : $\phi = f(\text{system clock})/2$ (2-divide mode) 1 1 : $\phi = f(\text{system clock})$ (Through mode)	0	○	○
7					

*: The initial value of bit 1 depends on the CNVss level.

Fig. 2.10.3 Structure of CPU mode register

PLL control register

b7	b6	b5	b4	b3	b2	b1	b0
				</			

Fig. 2.10.4 Structure of PLL control register

2.10.3 Functional description

The frequency synthesizer generates the 48 MHz clock which is multiples of the external input reference $f(X_{IN})$ and is needed for operating USB function. When using the USB function, set PLL enable bit of PLL control register (PLLCON: address 0FF8₁₆) to “1” (enabled) to send the 48 MHz PLL output clock (f_{VCO}) into USB function control unit. Figure 2.10.5 shows the block diagram for the frequency synthesizer circuit.

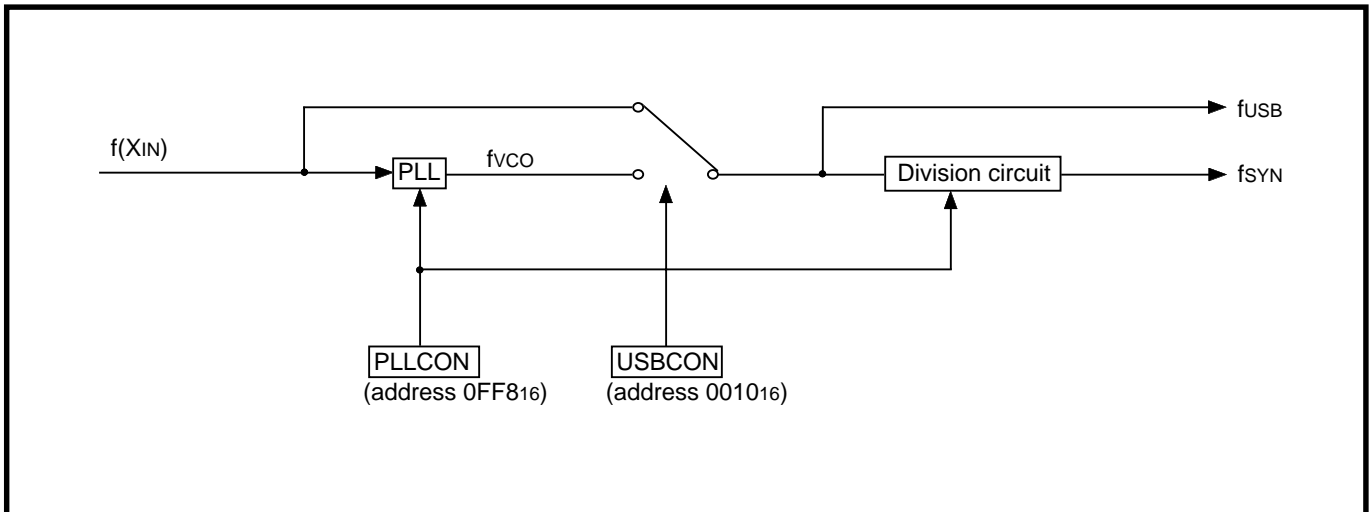


Fig. 2.10.5 Block diagram for frequency synthesizer circuit

● f_{VCO} (PLL output clock)

f_{VCO} is generated by multiplying PLL input clock according to the contents of PLL operation mode selection bits (bits 6, 5 of PLLCON), where

$$f_{VCO} = f(X_{IN}) \times n, n: \text{value selected by PLL operation mode selection bits}$$

Set PLL operation mode selection bits so that f_{VCO} may be set to 48 MHz.

While the PLL enable bit is “0” (disabled), f_{VCO} retains “L” level (except when PLL operation mode selection bits are set to “00₂”).

Table 2.10.1 shows the example of PLL operation mode selection bits setting.

Table 2.10.1 PLL operation mode selection bits setting example

$f(X_{IN})$	PLL operation mode selection bits *	f_{VCO}
6 MHz	11	48 MHz
12 MHz	10	48 MHz

*: PLL control register (bits 6,5)

Furthermore, when PLL operation mode selection bits are set to “00₂”, the clock input into PLL is used as f_{VCO} , which is not multiplied, regardless of PLL operation enabled or disabled.

● f_{USB} (USB clock)

Either $f(X_{IN})$ (main clock) or f_{VCO} (PLL output clock) can be selected for f_{USB} by USB clock select bit of USB control register (bit6 of USBCON: address 0010₁₆), and it is supplied to the USB function control circuit. When supplying f_{VCO} to the USB function control circuit, after setting PLL enable bit to “1” (enabled) and then set USB clock select bit to “1” (USB clock).

APPLICATION

2.10 Frequency synthesizer (PLL)

● f_{SYN} (f_{USB} division clock)

According to the setting of the USB clock division ratio selection bits (bits 4, 3 of PLLCON), the division clock of f_{USB} is supplied to f_{SYN} .

$f_{\text{SYN}} = f_{\text{USB}} / m$, m : value selected by USB clock division ratio selection bits

Set the USB clock division ratio selection bits so that f_{SYN} may be set to 6 MHz, 8 MHz or 12 MHz. When using f_{SYN} as internal system clock, set the system clock selection bit of CPU mode register (bit 5 of CPUM: address 003B₁₆) to "1" (f_{SYN}).

Table 2.10.2 shows the example of USB clock division ratio selection bits setting.

Table 2.10.2 USB clock division ratio selection bits setting example

f_{USB}	USB clock division ratio selection bits *	f_{SYN}
48 MHz	00	6 MHz
	01	8 MHz
	10	12 MHz

*: PLL control register (bit4,3)

● Setting for starting up PLL circuit when hardware reset

Figure 2.10.6 shows the example of related registers setting.

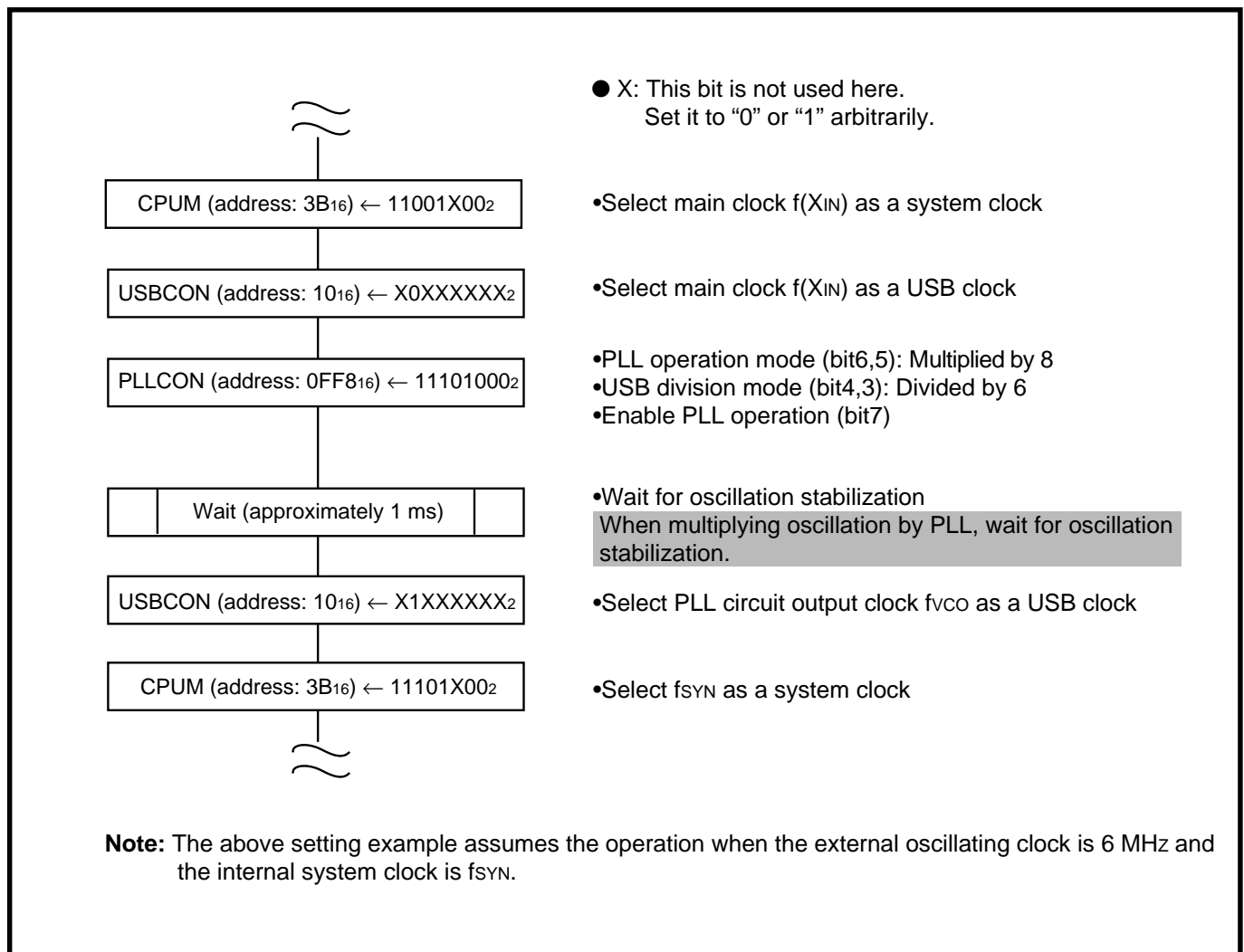


Fig. 2.10.6 Related registers setting when hardware reset

● Procedure for stop and return of PLL circuit when stop mode

Figure 2.10.7 shows the stop procedure of PLL circuit, and figure 2.10.8 shows the return procedure of PLL circuit.

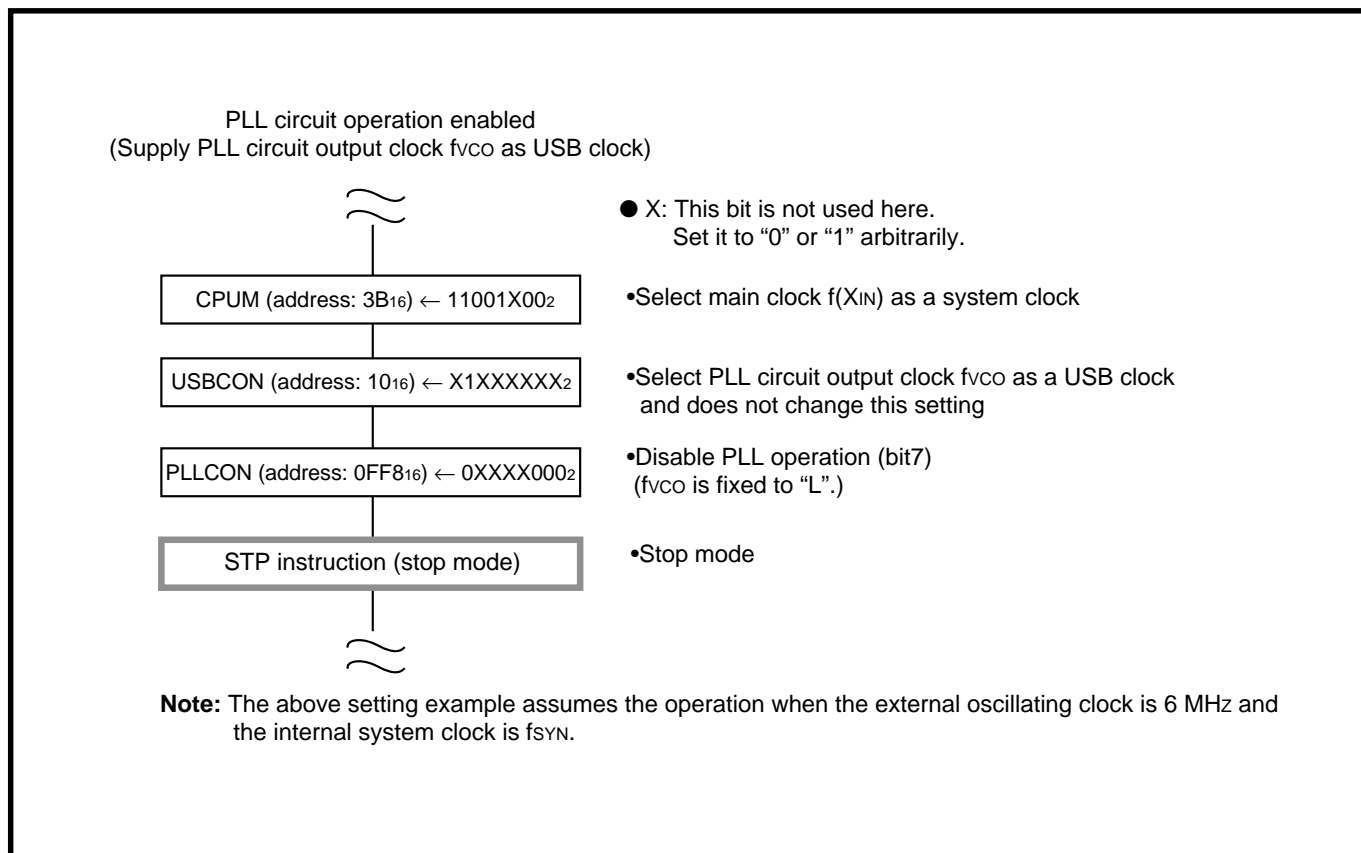


Fig. 2.10.7 Related registers setting when stop mode

APPLICATION

2.10 Frequency synthesizer (PLL)

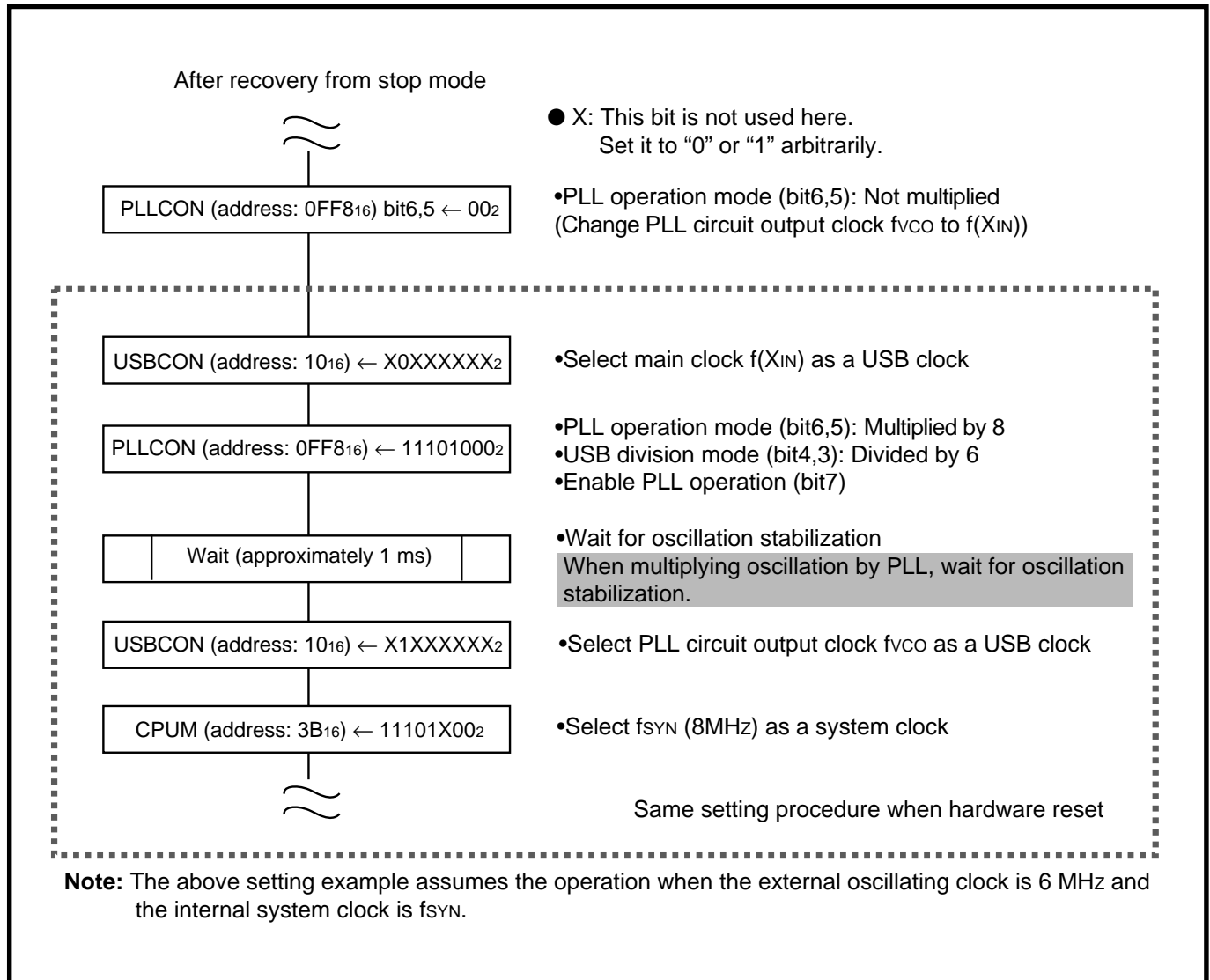


Fig. 2.10.8 Related registers setting when recovery from stop mode

2.10.4 Notes on PLL

- 6 MHz or 12 MHz external oscillator can be connected as an input reference clock ($f(X_{IN})$). When using the frequency synthesized clock function, we recommend using the fastest frequency possible of $f(X_{IN})$ as an input clock reference for the PLL.
- When enabling PLL operation from PLL disabled status (disabled when reset), set the USB clock select bit of USBCON to "0" ($f(X_{IN})$) to operate with the main clock ($f(X_{IN})$).
- When supplying f_{VCO} to the USB block after setting PLL operation enable bit to "1" (PLL enabled), wait for the oscillation stable time (1 ms or less) of PLL to avoid any instability caused by the clock, then set USB clock select bit to "1" (USB clock).
- When selecting f_{SYN} as an internal system clock, f_{USB} must be 48 MHz.
- When selecting f_{SYN} as an internal system clock, change the system clock selection bit to main clock ($f(X_{IN})$) before executing STP instruction. It is because the following are needed for the low-power consumption:
 - f_{USB} must be stopped by disabling PLL operation in Stop mode.
 - The timer 1 for waiting oscillation stabilization when returning from Stop mode will require the input count source.

2.11 Clock generating circuit

This paragraph explains the registers setting method and the notes related to the clock generating circuit.

2.11.1 Memory map

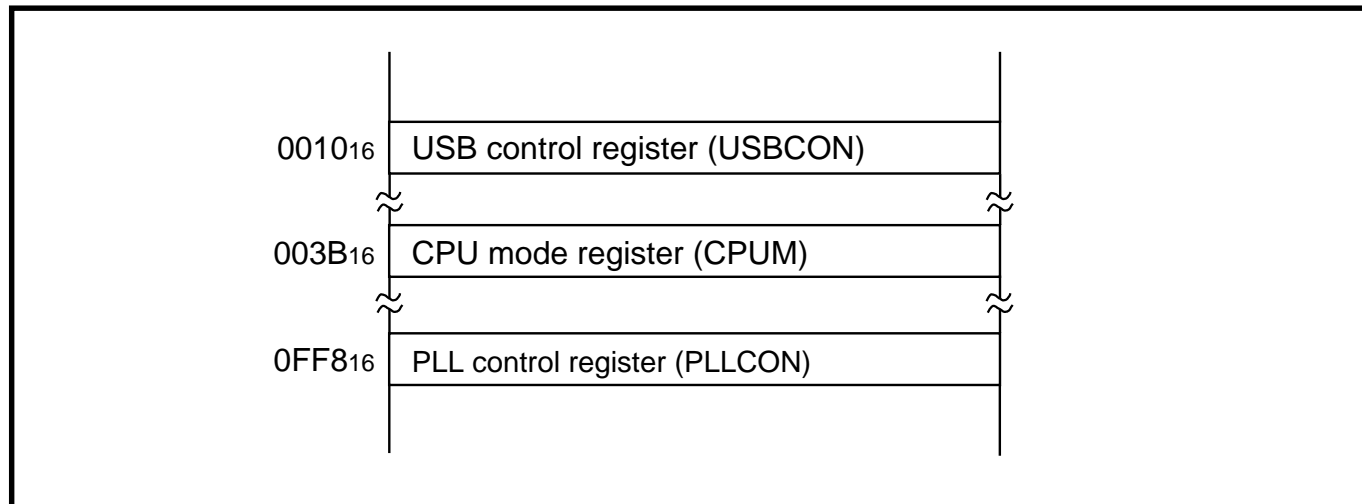


Fig. 2.11.1 Memory map of registers related to clock generating circuit

2.11.2 Related registers

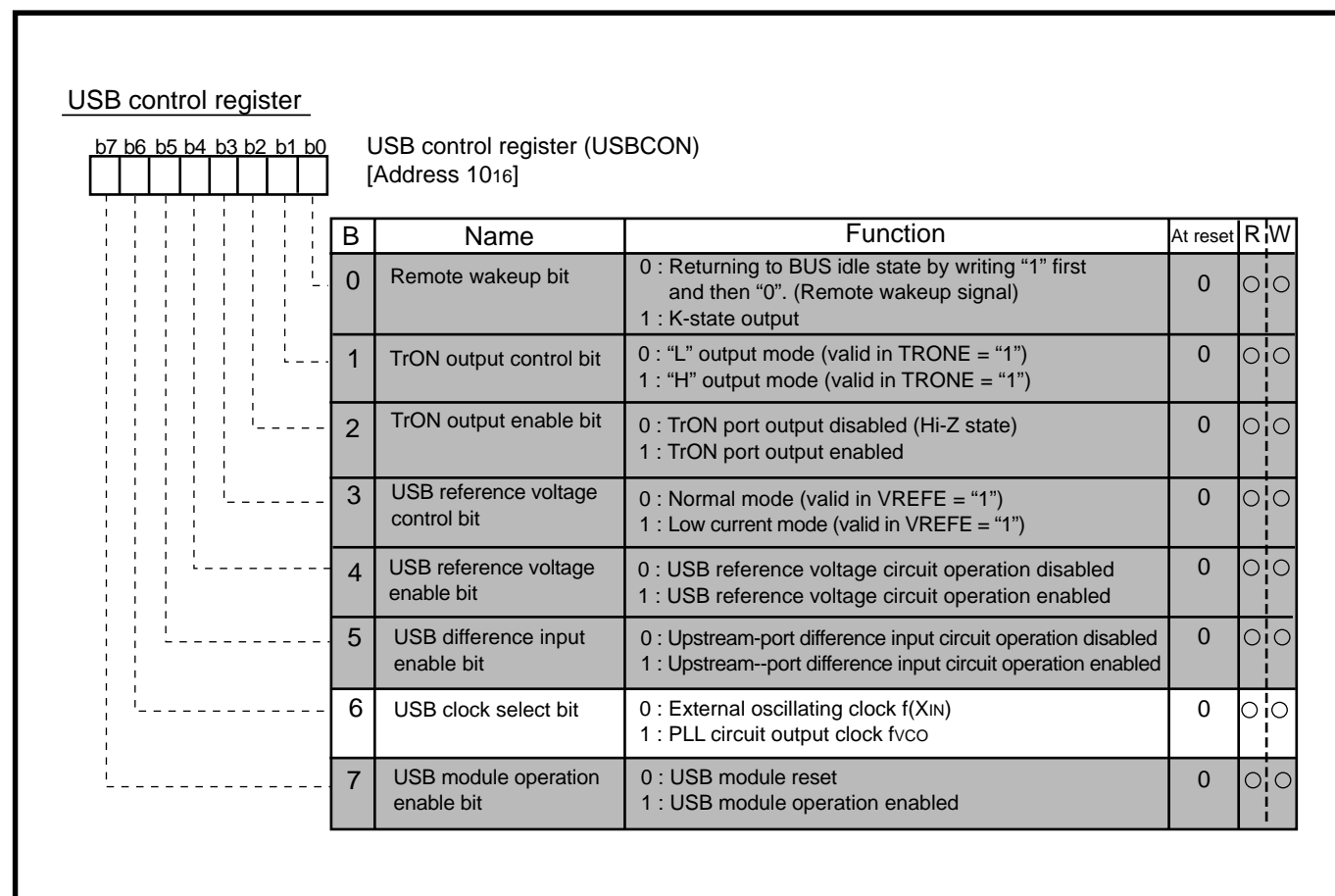
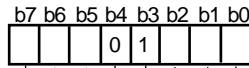


Fig. 2.11.2 Structure of USB control register

APPLICATION

2.11 Clock generating circuit

CPU mode register



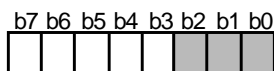
CPU mode register
(CPUM: address 3B16)

B	Name	Function	At reset	R	W		
0	Processor mode bits	b1 b0 0 0 : Single-chip mode 0 1 : Not available 1 0 : Not available 1 1 : Not available	0	○	○		
1			*	○	○		
2			Stack page selection bit	0 : 0 page 1 : 1 page	0	○	○
3			Fix this bit to "1".		1	○	○
4	Fix this bit to "0".		0	○	○		
5	System clock selection bit	0 : Main clock f(X _{IN}) 1 : f _{SYN}	0	○	○		
6	System clock division ratio selection bits	b7 b6 0 0 : φ = f(system clock)/8 (8-divide mode) 0 1 : φ = f(system clock)/4 (4-divide mode) 1 0 : φ = f(system clock)/2 (2-divide mode) 1 1 : φ = f(system clock) (Through mode)	0	○	○		
7							

*: The initial value of bit 1 depends on the CNVss level.

Fig. 2.11.3 Structure of CPU mode register

PLL control register



PLL control register (PLLCON)
[Address : 0FF816]

B	Name	Function	At reset	R	W
0	Nothing is arranged for these bit. These are write disabled bits. When these bits are read out, the contents are "0".		0	○	×
1					
2					
3	USB clock division ratio selection bits	b4 b3 0 0 : Divided by 8 ($f_{\text{SYN}} = f_{\text{USB}}/8$) 0 1 : Divided by 6 ($f_{\text{SYN}} = f_{\text{USB}}/6$) 1 0 : Divided by 4 ($f_{\text{SYN}} = f_{\text{USB}}/4$) 1 1 : Not selected	0	○	○
4					
5	PLL operation mode selection bits	b6 b5 0 0 : Not multiplied ($f_{\text{VCO}} = f_{\text{XIN}}$) 0 1 : Double ($f_{\text{VCO}} = f_{\text{XIN}} \times 2$) 1 0 : Quadruple ($f_{\text{VCO}} = f_{\text{XIN}} \times 4$) 1 1 : Multiplied by 8 ($f_{\text{VCO}} = f_{\text{XIN}} \times 8$)	0	○	○
6					
7	PLL enable bit	0 : Disabled 1 : Enabled	0	○	○

Fig. 2.11.4 Structure of PLL control register

2.11.3 Oscillation control

Either can be selected as an internal system clock between the following two by system clock selection bit.

- Main clock $f(X_{IN})$
- f_{SYN} (f_{USB} division clock)

Any one can be selected as an internal clock ϕ among the following four by system clock division ratio selection bits.

- $f(X_{IN})$ or $f_{SYN}/8$ (8-divide mode)
- $f(X_{IN})$ or $f_{SYN}/4$ (4-divide mode)
- $f(X_{IN})$ or $f_{SYN}/2$ (2-divide mode)
- $f(X_{IN})$ or f_{SYN} (Through mode)

(1) Generation of internal clock $f(\phi)$ using main clock $f(X_{IN})$

Table 2.11.1 shows the example of internal clock $f(\phi)$ generation using main clock $f(X_{IN})$; Figure 2.11.5 shows the related registers setting.

Table 2.11.1 Example of internal clock $f(\phi)$ generation using main clock $f(X_{IN})$

System clock	System clock division ratio selection bits *	$f(\phi)$	Power source voltage V_{CC} [V]
6 MHz	0 0	0.75 MHz	3.00 to 5.25
	0 1	1.5 MHz	
	1 0	3 MHz	
	1 1	6 MHz	
8 MHz	0 0	1 MHz	4.00 to 5.25
	0 1	2 MHz	
	1 0	4 MHz	
	1 1	8 MHz	
12 MHz	0 0	1.5 MHz	4.50 to 5.25 (Planning)
	0 1	3 MHz	
	1 0	6 MHz	
	Do not select (1 1)	12 MHz	

*: CPU mode register (bits 7,6)

- Select main clock $f(X_{IN})$ as system clock and set clock division mode

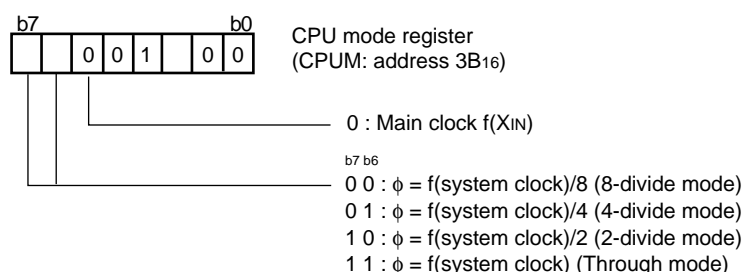


Fig. 2.11.5 Related registers setting

APPLICATION

2.11 Clock generating circuit

(2) Generation of internal clock $f(\phi)$ using f_{SYN} (f_{USB} division clock)

Table 2.11.2 shows the example of internal clock $f(\phi)$ generation using f_{SYN} ; Figure 2.11.6 shows the related registers setting.

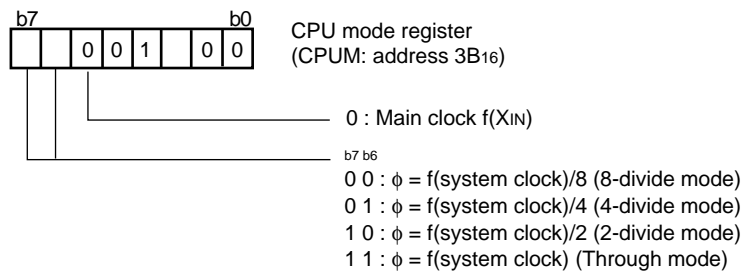
Table 2.11.2 Example of internal clock $f(\phi)$ generation using f_{SYN}

f_{USB}	USB clock division ratio selection bits *1	f_{SYN}	System clock division ratio selection bits *2	$f(\phi)$	Power source voltage V_{CC} [V]
48 MHz	0 0	6 MHz	0 0	0.75 MHz	3.00 to 5.25
			0 1	1.5 MHz	
			1 0	3 MHz	
			1 1	6 MHz	
	0 1	8 MHz	0 0	1 MHz	4.00 to 5.25
			0 1	2 MHz	
			1 0	4 MHz	
			1 1	8 MHz	
	1 1	12 MHz	0 0	1.5 MHz	
			0 1	3 MHz	
			1 0	6 MHz	
			Do not select (1 1)	12 MHz	4.50 to 5.25 (Planning)

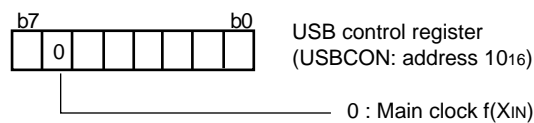
*1: PLL control register (bits 4,3)

*2: CPU mode register (bits 7,6)

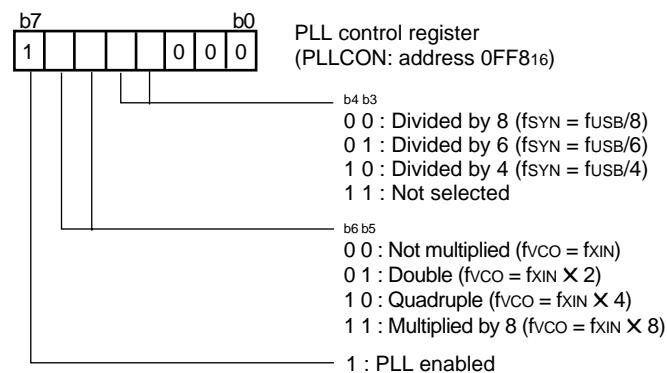
1. Select main clock $f(X_{IN})$ as system clock and set clock division mode.



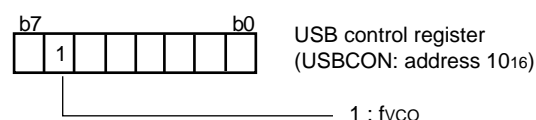
2. Select main clock $f(X_{IN})$ as USB clock.



3. Enable PLL circuit, and generating PLL output clock (f_{VCO}) 48 MHz and f_{SYN} .



4. Select PLL output clock (f_{VCO}) as USB clock.



5. Select f_{SYN} as system clock.

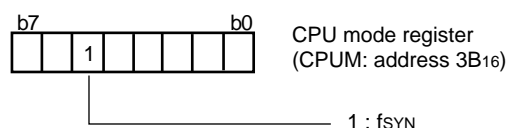


Fig. 2.11.6 Related registers setting

Note: When selecting f_{SYN} as an internal system clock, refer to “2.10 Frequency synthesizer (PLL)” for details concerning how to generate f_{USB} (USB clock) from $f(X_{IN})$ and the notes on PLL circuit.

APPLICATION

2.12 Standby function

2.12 Standby function

The 38K0 group is provided with standby functions to stop the CPU by software and put the CPU into the low-power operation.

The following two types of standby functions are available.

- Stop mode using STP instruction
- Wait mode using WIT instruction

2.12.1 Memory map

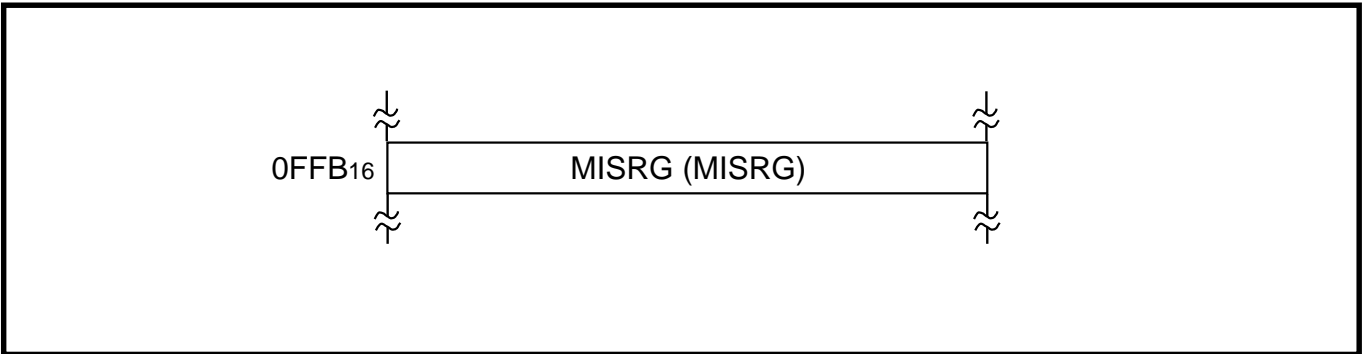


Fig. 2.12.1 Memory map of registers related to standby function

2.12.2 Related registers

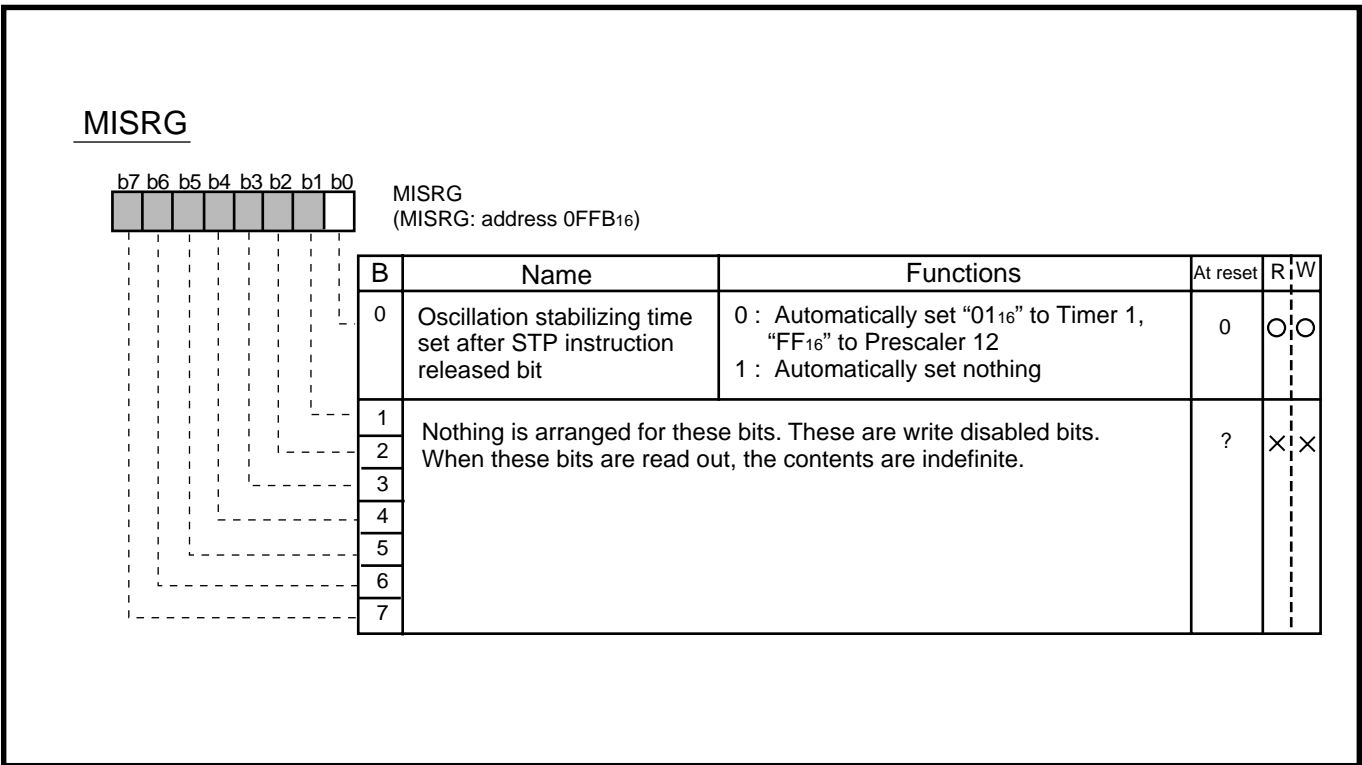


Fig. 2.12.2 Structure of MISRG

2.12.3 Stop mode

The stop mode is set by executing the STP instruction. In the stop mode, the oscillation of clock (X_{IN} – X_{OUT}) stops and the internal clock ϕ stops at the “H” level. The CPU stops and peripheral units stop operating. As a result, power dissipation is reduced.

(1) State in stop mode

Table 2.12.1 shows the state in the stop mode.

Table 2.12.1 State in stop mode

Item	State in stop mode
Oscillation	Stopped.
CPU	Stopped.
Internal clock ϕ	Stopped at “H” level.
I/O ports P0–P6	Retains the state at the STP instruction execution.
Timer	Stopped. (Timers 1, 2, X) However, Timers X can be operated in the event counter mode.
Watchdog timer	Stopped.
Serial I/O	Stopped. However, these can be operated only when an external clock is selected.
USB function	Stopped.
External BUS interface	Stopped.
A-D converter	Stopped.
Comparator	Stopped.

APPLICATION

2.12 Standby function

(2) Release of stop mode

The stop mode is released by a reset input or by the occurrence of an interrupt request. Note the differences in the restoration process according to reset input or interrupt request, as described below.

■Restoration by reset input

The stop mode is released by holding the $\overline{\text{RESET}}$ pin to the “L” input level during the stop mode. Oscillation is started when all ports are in the input state and the stop mode of the main clock (X_{IN} - X_{OUT}) is released.

Oscillation is unstable when restarted. For this reason, time for stabilizing of oscillation (oscillation stabilizing time) is required. The input of the $\overline{\text{RESET}}$ pin should be held at the “L” level until oscillation stabilizes.

When the $\overline{\text{RESET}}$ pin is held at the “L” level for 16 cycles or more of X_{IN} after the oscillation has stabilized, the microcomputer will go to the reset state. After the input level of the $\overline{\text{RESET}}$ pin is returned to “H”, the reset state is released in approximately 10.5 to 18.5 cycles of the X_{IN} input. Figure 2.12.3 shows the oscillation stabilizing time at restoration by reset input.

At release of the stop mode by reset input, the internal RAM retains its contents previous to the reset. However, the previous contents of the CPU register and SFR are not retained.

For more details concerning reset, refer to “2.9 Reset”.

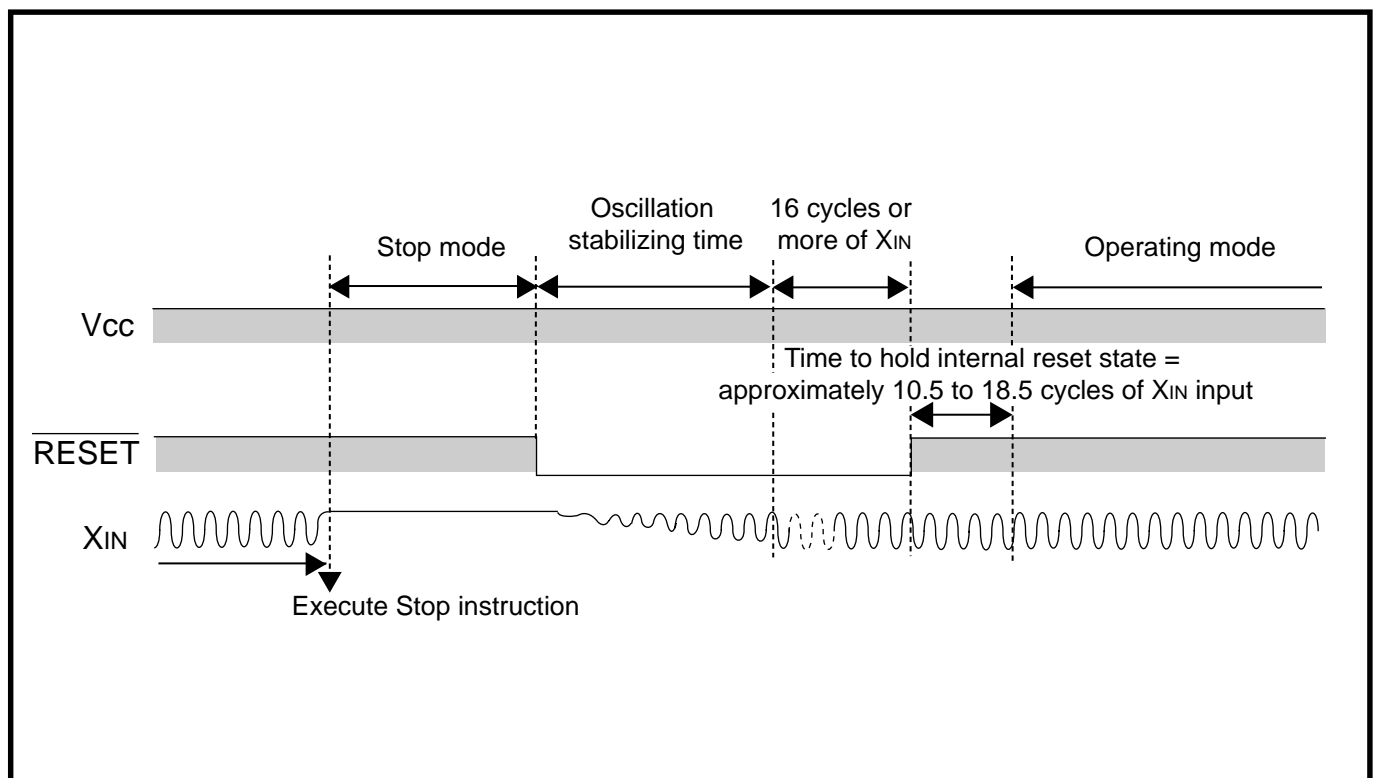


Fig. 2.12.3 Oscillation stabilizing time at restoration by reset input

■Restoration by interrupt request

The occurrence of an interrupt request in the stop mode releases the stop mode. As a result, oscillation is resumed. The interrupts available for restoration are:

- INT₀, INT₁
- CNTR₀
- Serial I/O using an external clock
- Timer X using an external event count
- Key input (key-on wake-up)
- USB function (resume)

However, when using any of these interrupt requests for restoration from the stop mode, in order to enable the selected interrupt, you must execute the STP instruction after setting the following conditions.

[Necessary register setting]

- ① Interrupt disable flag I = "0" (interrupt enabled)
- ② Timer 1 interrupt enable bit = "0" (interrupt disabled)
- ③ Interrupt request bit of interrupt source to be used for restoration = "0" (no interrupt request issued)
- ④ Interrupt enable bit of interrupt source to be used for restoration = "1" (interrupts enabled)

For more details concerning interrupts, refer to "2.2 Interrupts".

Oscillation is unstable when restarted. For this reason, time for stabilizing of oscillation (oscillation stabilizing time) is required. For restoration by an interrupt request, waiting time prior to supplying internal clock ϕ to the CPU is automatically generated*2 by Prescaler 12 and Timer 1*1. This waiting time is reserved as the oscillation stabilizing time on the system clock side. The supply of internal clock ϕ to the CPU is started at the Timer 1 underflow.

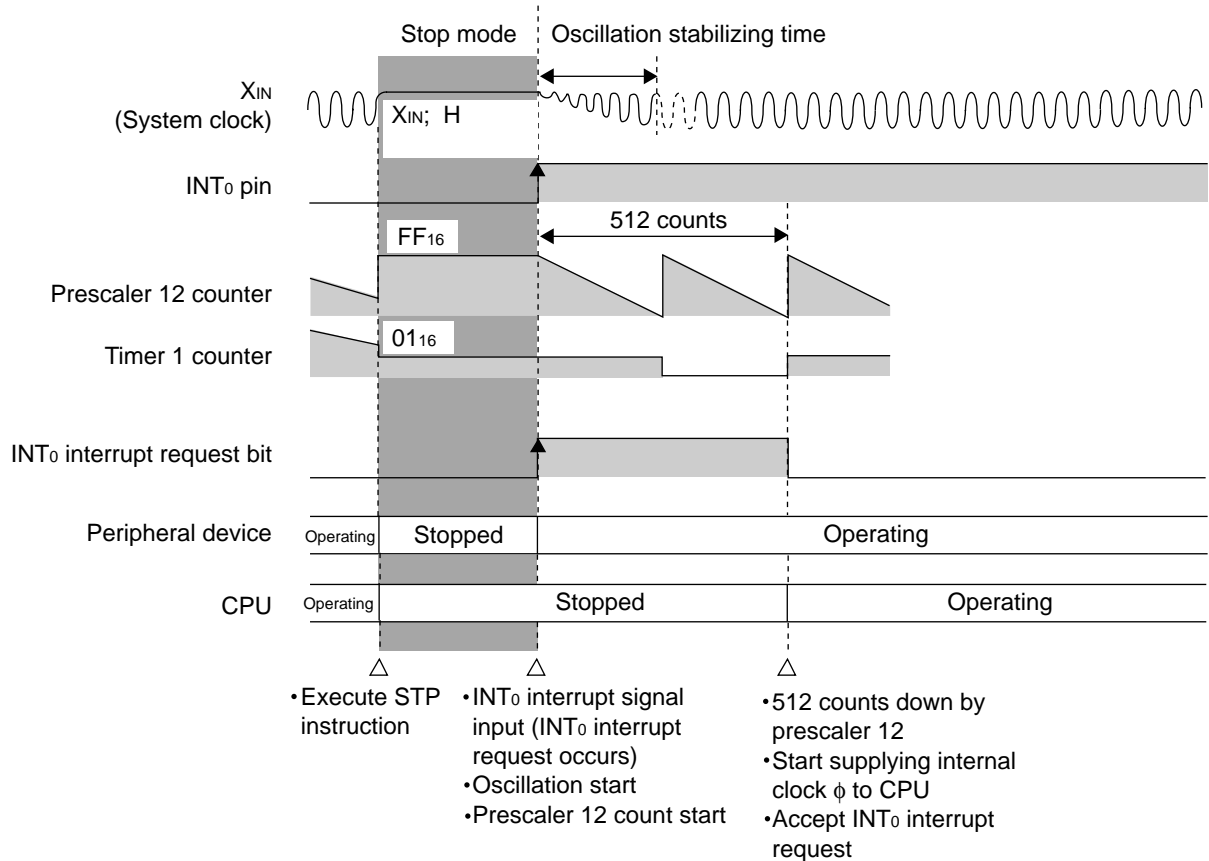
Figure 2.12.4 shows an execution sequence example at restoration by the occurrence of an INT₀ interrupt request.

- *1: If the STP instruction is executed when the oscillation stabilizing time set after STP instruction released bit is "0", "FF₁₆" and "01₁₆" are automatically set in the Prescaler 12 counter/latch and Timer 1 counter/latch, respectively. When the oscillation stabilizing time set after STP instruction released bit is "1", nothing is automatically set to either Prescaler 12 or Timer 1. For this reason, any suitable value can be set to Prescaler 12 and Timer 1 for the oscillation stabilizing time.
- *2: Immediately after the oscillation is started, the count source is supplied to the prescaler 12 so that a count operation is started.

APPLICATION

2.12 Standby function

- When restoring microcomputer from stop mode by INT₀ interrupt (rising edge selected)



Note: $f(X_{IN})/16$ is input as the prescaler 12 count source.

Fig. 2.12.4 Execution sequence example at restoration by occurrence of INT₀ interrupt request

(3) Notes on using stop mode

■Register setting

Since values of the prescaler 12 and Timer 1 are automatically reloaded when returning from the stop mode, set them again, respectively. (When the oscillation stabilizing time set after STP instruction released bit is "0")

■Clock restoration

When the main clock side is set as a system clock, the oscillation stabilizing time for approximately 8,000 cycles of the X_{IN} input is reserved at restoration from the stop mode.

2.12.4 Wait mode

The wait mode is set by execution of the WIT instruction. In the wait mode, oscillation continues, but the internal clock ϕ stops at the “H” level.

The CPU stops, but most of the peripheral units continue operating.

(1) State in wait mode

The continuation of oscillation permits clock supply to the peripheral units. Table 2.12.2 shows the state in the wait mode.

Table 2.12.2 State in wait mode

Item	State in wait mode
Oscillation	Operating.
CPU	Stopped.
Internal clock ϕ	Stopped at “H” level.
I/O ports P0–P6	Retains the state at the WIT instruction execution.
Timer	Operating.
Watchdog timer	Operating.
Serial I/O	Operating.
USB function	Operating.
External BUS interface	Stopped.
A-D converter	Operating.
Comparator	Operating.

APPLICATION

2.12 Standby function

(2) Release of wait mode

The wait mode is released by reset input or by the occurrence of an interrupt request. Note the differences in the restoration process according to reset input or interrupt request, as described below.

In the wait mode, oscillation is continued, so an instruction can be executed immediately after the wait mode is released.

■Restoration by reset input

The wait mode is released by holding the input level of the $\overline{\text{RESET}}$ pin at “L” in the wait mode. Upon release of the wait mode, all ports are in the input state, and supply of the internal clock ϕ to the CPU is started. To reset the microcomputer, the $\overline{\text{RESET}}$ pin should be held at an “L” level for 16 cycles or more of X_{IN} . The reset state is released in approximately 10.5 cycles to 18.5 cycles of the X_{IN} input after the input of the $\overline{\text{RESET}}$ pin is returned to the “H” level.

At release of wait mode, the internal RAM retains its contents previous to the reset. However, the previous contents of the CPU register and SFR are not retained.

Figure 2.12.5 shows the reset input time.

For more details concerning reset, refer to “2.9 Reset”.

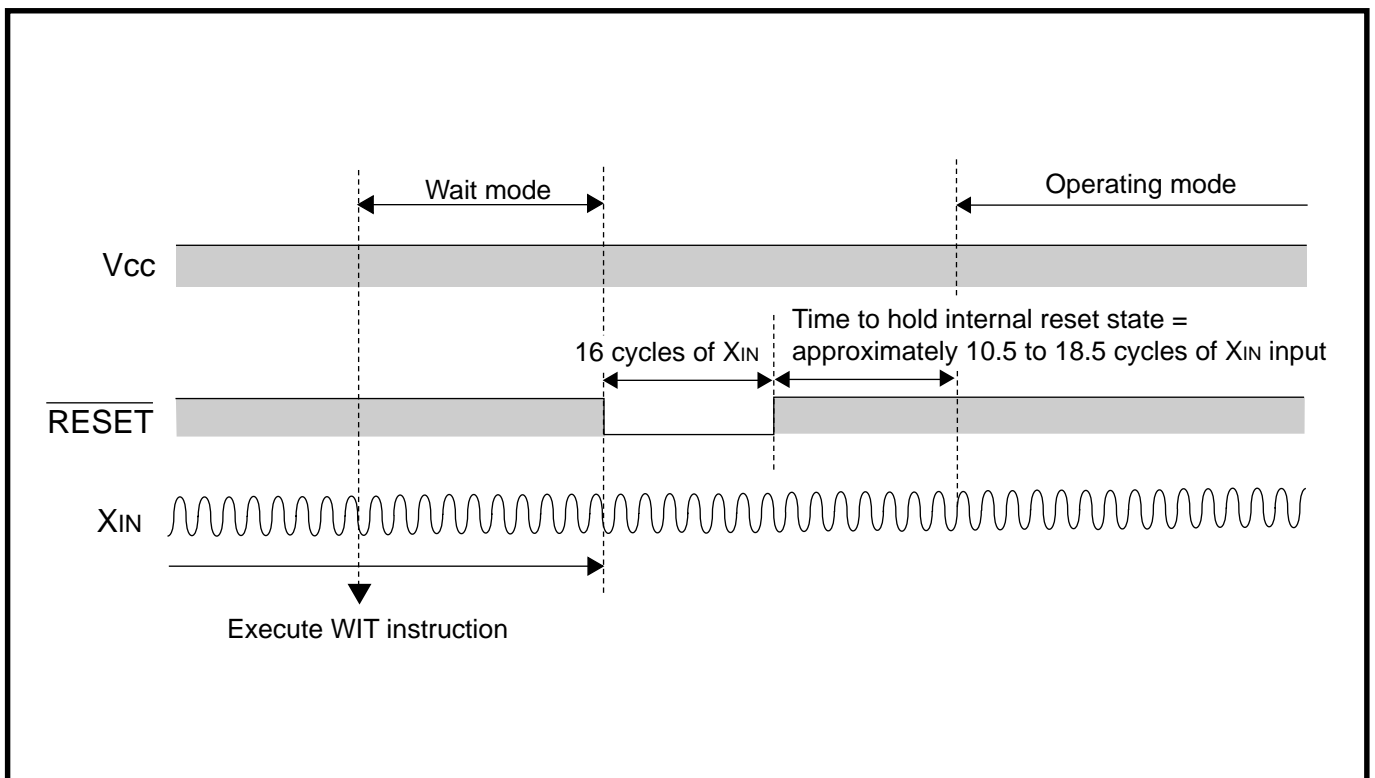


Fig. 2.12.5 Reset input time

■ Restoration by interrupt request

In the wait mode, the occurrence of an interrupt request releases the wait mode and supply of the internal clock ϕ to the CPU is started. At the same time, the interrupt request used for restoration is accepted, so the interrupt processing routine is executed.

However, when using an interrupt request for restoration from the wait mode, in order to enable the selected interrupt, you must execute the STP instruction after setting the following conditions.

[Necessary register setting]

- ① Interrupt disable flag I = "0" (interrupt enabled)
- ② Interrupt request bit of interrupt source to be used for restoration = "0" (no interrupt request issued)
- ③ Interrupt enable bit of interrupt source to be used for restoration = "1" (interrupts enabled)

For more details concerning interrupts, refer to "2.2 Interrupts".

2.12.5 Notes on stand-by function

In stand-by state*¹ for low-power dissipation, do not make input levels of an input port and an I/O port "undefined".

Pull-up (connect the port to V_{CC}) these ports through a resistor.

When determining a resistance value, note the following points:

- External circuit
- Variation of output levels during the ordinary operation

When using built-in pull-up resistor, note on varied current values.

- When setting as an input port: Fix its input level
- When setting as an output port: Prevent current from flowing out to external

● Reason

The potential which is input to the input buffer in a microcomputer is unstable in the state that input levels of an input port and an I/O port are "undefined". This may cause power source current.

*¹ stand-by state : the stop mode by executing the **STP** instruction
 the wait mode by executing the **WIT** instruction

APPLICATION

2.13 Flash memory

2.13 Flash memory

This paragraph explains the registers setting method and the notes related to the flash memory version.

2.13.1 Overview

The functions of the flash memory version are similar to those of the mask ROM version except that the flash memory is built-in and some of the SFR area differ from that of the mask ROM version (refer to “2.13.2 Memory map”).

In the flash memory version, the built-in flash memory can be programmed or erased by using the following three modes.

- CPU rewrite mode
- Parallel I/O mode
- Standard serial I/O mode

2.13.2 Memory map

38K0 group flash memory version has 32 Kbytes of built-in flash memory.

Figure 2.13.1 shows the memory map of the flash memory version.

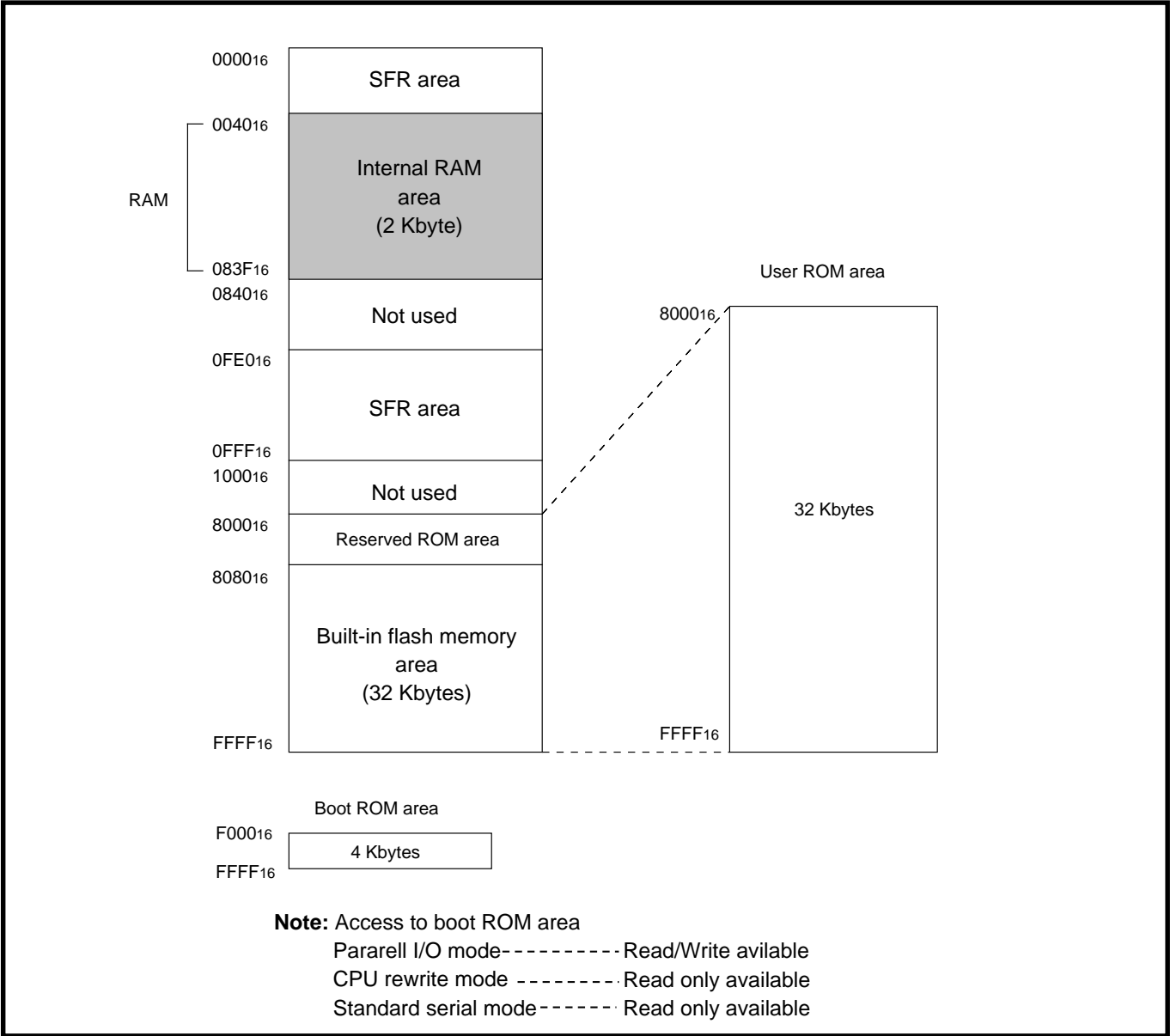


Fig. 2.13.1 Memory map of flash memory version for 38K0 Group

2.13.3 Related registers

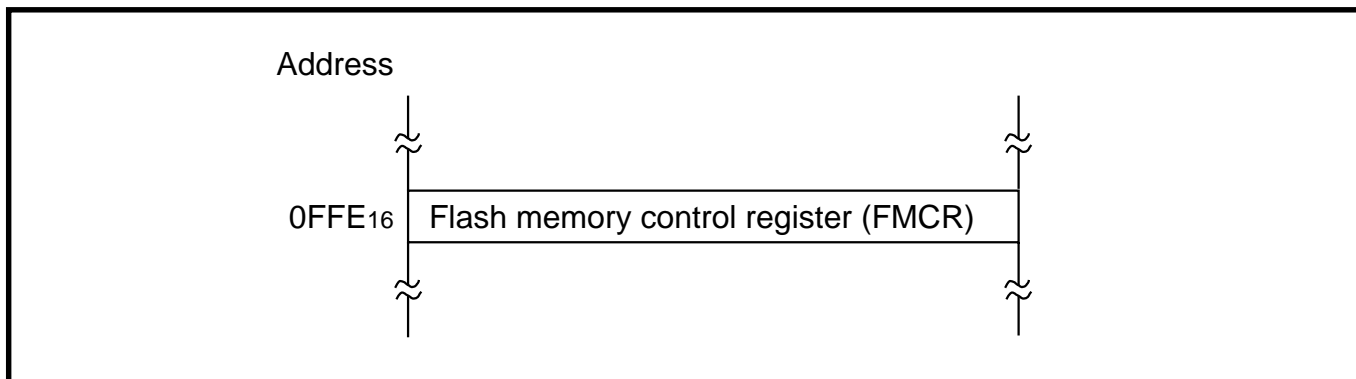
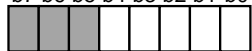


Fig. 2.13.2 Memory map of registers related to flash memory

Flash memory control register

b7 b6 b5 b4 b3 b2 b1 b0

Flash memory control register
(FMCR : address 0FFE₁₆) (**Note 1**)

b	Name	Functions	At reset	R	W
0	RY/ $\overline{\text{BY}}$ status flag	0 : Busy (being written or erased) 1 : Ready	1	○	×
1	CPU rewrite mode select bit (Note 2)	0 : Normal mode (Software commands invalid) 1 : CPU rewrite mode (Software commands acceptable)	0	○	○
2	CPU rewrite mode entry flag	0 : Normal mode 1 : CPU rewrite mode	0	○	×
3	Flash memory reset bit (Note 3)	0 : Normal operation 1 : Reset	0	○	○
4	User area/Boot area selection bit (Note 4)	0 : User ROM area 1 : Boot ROM area	0	○	○
5	Nothing is arranged for these bits. If writing, set "0". When these bits are read out, the contents are undefined.		Undefined	×	○
6			Undefined	×	○
7			Undefined	×	○

Notes 1: The contents of flash memory control register are "XXX00001" just after reset release.**2:** For this bit to be set to "1", the user needs to write "0" and then "1" to it in succession. If it is not this procedure, this bit will not be set to "1". Additionally, it is required to ensure that no interrupt will be generated during that interval.
Use the control program in the area except the built-in flash memory for write to this bit.**3:** This bit is valid when the CPU rewrite mode select bit is "1".
Set this bit 3 to "0" subsequently after setting bit 3 to "1".**4:** Use the control program in the area except the built-in flash memory for write to this bit.

Fig. 2.13.3 Structure of Flash memory control register

APPLICATION

2.13 Flash memory

2.13.4 Parallel I/O mode

In the parallel I/O mode, program/erase to the built-in flash memory can be performed by a flash programmer (MFW-I).

The memory area of program/erase is from 0F000₁₆ to 0FFFF₁₆ (boot ROM area) or from 08000₁₆ to 0FFFF₁₆ (user ROM area). Be especially careful when erasing; if the memory area is not set correctly, the products will be damaged eternally.

Table 2.13.1 shows the setting of programmers when programming in the parallel I/O mode.

•MFW-I provided by Sunny Giken Inc. (<http://www.sunnygiken.co.jp/english/index.html>)

Table 2.13.1 Setting of programmers when parallel programming

Products	Parallel adapter	Boot ROM area	User ROM area
M38K09F8HP/LHP	MFW-S18	0F000 ₁₆ to 0FFFF ₁₆	08000 ₁₆ to 0FFFF ₁₆
M38K09F8FP/LFP	MFW-S19		

2.13.5 Standard serial I/O mode

Table 2.13.2 shows a pin connection example (4 wires) between the programmer (MFW-I) and the microcomputer when programming in the standard serial I/O mode.

•MFW-I provided by Sunny Giken Inc. (<http://www.sunnygiken.co.jp/english/index.html>)

Table 2.13.2 Connection example to flash programmer when serial programming (4 wires)

Function	MFW-1		38K0 Group flash memory version	
	Signal name	MFW-1 side connector Line number	Pin name	Pin number
Transfer clock input	CLK	3	P4 ₂ /E _x TC/S _{CLK}	53
Serial data input	RxD	10	P4 ₀ /E _x DREQ/RxD	51
Serial data output	TxD	4	P4 ₁ /E _x DACK/TxD	52
Transmit/Receive enable output	BUSY	2	P4 ₃ /E _x A1/S _{RDY}	54
V _{PP} input	CNV _{SS}	1	CNV _{SS}	7
Reset input	RESET	8	RESET	8
Target board power source monitor input	V _{CC} (Note 2)	1	V _{CC} , PV _{CC} , DV _{CC} (Note 2)	14, 21, 22
GND	GND (Note 1)	7	V _{SS} , PV _{SS} (Note 1)	11, 20

Notes 1: When connecting a serial programmer, first connect both GNDs to the same GND level.

2: V_{CC} power of MFW-1 is supplied from a target board. Power consumption of MFW-1 is Max. 200 mA when serial programming. Therefore, when the current capacity of target board is short, connect AC adapter and supply power source to MFW-1.

2.13.6 CPU rewrite mode

In the CPU rewrite mode, issuing software commands through the Central Processing Unit (CPU) can rewrite the built-in flash memory. Accordingly, the contents of the built-in flash memory can be rewritten with the microcomputer itself mounted on board, without using the programmer.

Store the rewrite control program to the built-in flash memory in advance. The built-in flash memory cannot be read in the CPU rewrite mode. Accordingly, after transferring the rewrite control program to the internal RAM, execute it on the RAM.

The following commands can be used in the CPU rewrite mode: read array, read status register, clear status register, program, erase all block, and block erase. For details concerning each command, refer to "CHAPTER 1 Flash memory mode (CPU rewrite mode)".

(1) CPU rewrite mode beginning/release procedures

Operation procedure in the CPU rewrite mode for the built-in flash memory is described below. As for the control example, refer to "2.13.7 (2) Control example in the CPU rewrite mode."

[Beginning procedure]

- ① Apply 4.50 to 5.25 V to the CNV_{SS}/V_{PP} pin (at selecting boot ROM area).
- ② Release reset.
- ③ Set bits 6 and 7 (main clock division ratio selection bits) of the CPU mode register.
- ④ After CPU rewrite mode control program is transferred to internal RAM, jump to this control program on RAM. (The following operations are controlled by this control program).
- ⑤ Apply 4.50 to 5.25 to the CNV_{SS}/V_{PP} pin (in single-chip mode).
- ⑥ Set "1" to the CPU rewrite mode select bit (bit 1 of address 0FFE₁₆).
- ⑦ Read the CPU rewrite mode entry flag (bit 2 of address 0FFE₁₆) to confirm that the CPU rewrite mode is set to "1".
- ⑧ Flash memory operations are executed by using software commands.

Note: The following procedures are also necessary.

- Control for data which is input from the external (serial I/O etc.) and to be programmed to the flash memory.
- Initial setting for ports, etc.
- Writing to the watchdog timer

[Release procedure]

- ① Execute the read command or set the flash memory reset bit (bit 3 of address 0FFE₁₆).
- ② Set the CPU rewrite mode select bit (bit 0 of address 0FFE₁₆) to "0".

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2.13 Flash memory

2.13.7 Flash memory mode application examples

The control pin processing example on the system board in the standard serial I/O mode and the control example in the CPU rewrite mode are described below.

(1) Control pin connection example on the system board in standard serial I/O mode

As shown in Figure 2.13.4, in the standard serial I/O mode, the built-in flash memory can be rewritten with the microcomputer mounted on board. Connection examples of control pins ($P4_0/\overline{E_xDREQ}/R_xD$, $P4_1/\overline{E_xDACK}/T_xD$, $P4_2/\overline{E_xTC}/S_{CLK}$, $P4_3/\overline{E_xA1}/\overline{S_{RDY}}$, $P1_6$, CNV_{SS} , and $RESET$ pin) in the standard serial I/O mode are described below.

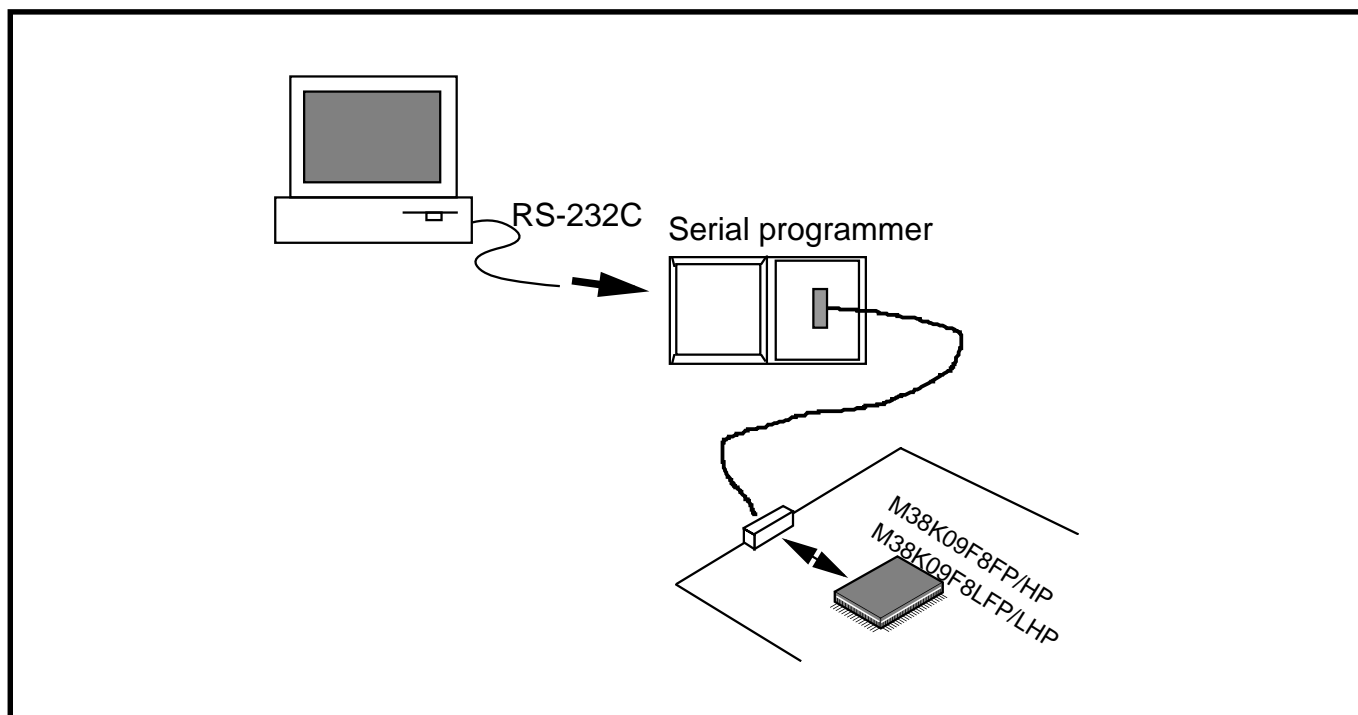


Fig. 2.13.4 Rewrite example of built-in flash memory in standard serial I/O mode

Table 2.13.3 shows the setting condition in the standard serial I/O mode.

Table 2.13.3 Setting condition in serial I/O mode

38K0 Group flash memory version		Value
Pin name	Pin number	
CNV_{SS}/V_{PP} (Note)	7	4.50 to 5.25 V
$P1_6$	5	V_{CC}
$P4_2/\overline{E_xTC}/S_{CLK}$	53	V_{CC}
$RESET$	8	Edge from V_{SS} to V_{CC}

Note: CNV_{SS}/V_{PP} is not V_{CC} but a voltage when programming.

① When control signals are not affected to user system circuit

When the control signals in the standard serial I/O mode are not used or not affected to the user system circuit, they can be connected as shown in Figure 2.13.5.

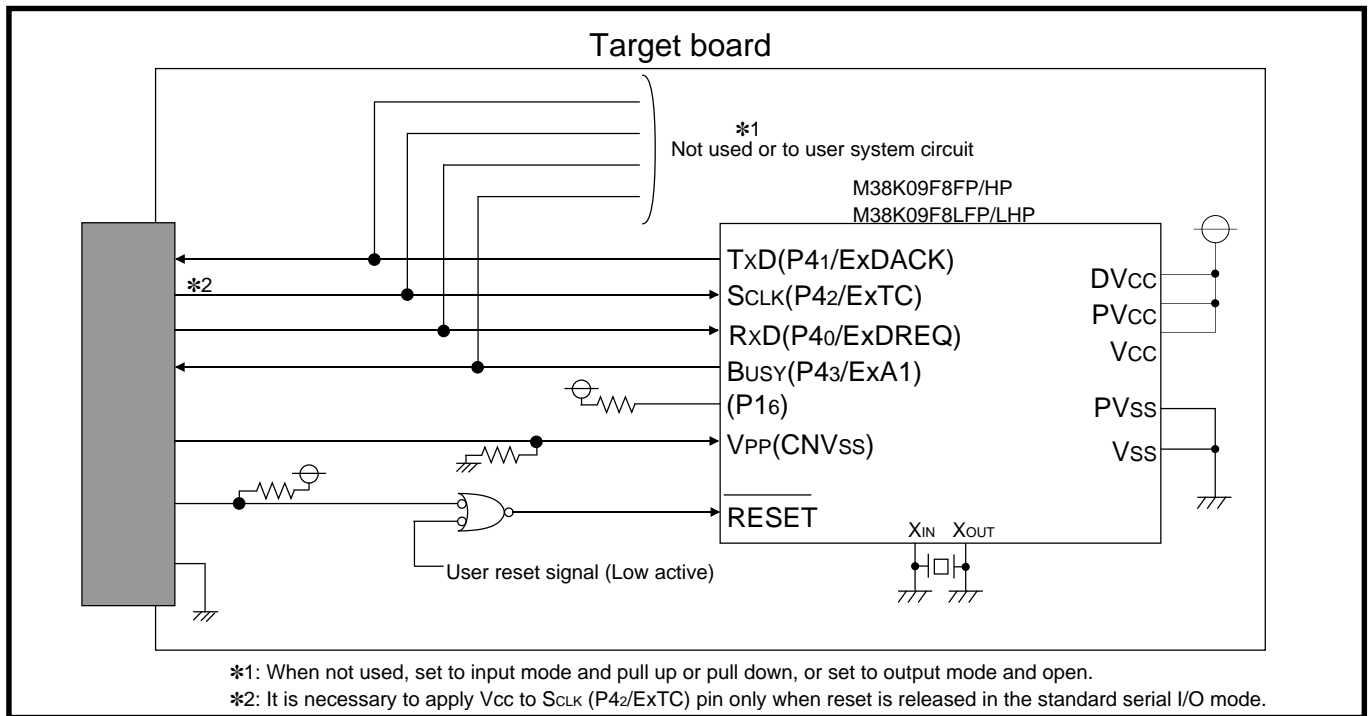


Fig. 2.13.5 Connection example in standard serial I/O mode (1)

② When control signals are affected to user system circuit-1

Figure 2.13.6 shows an example that the jumper switch cut-off the control signals not to supply to the user system circuit in the standard serial I/O mode.

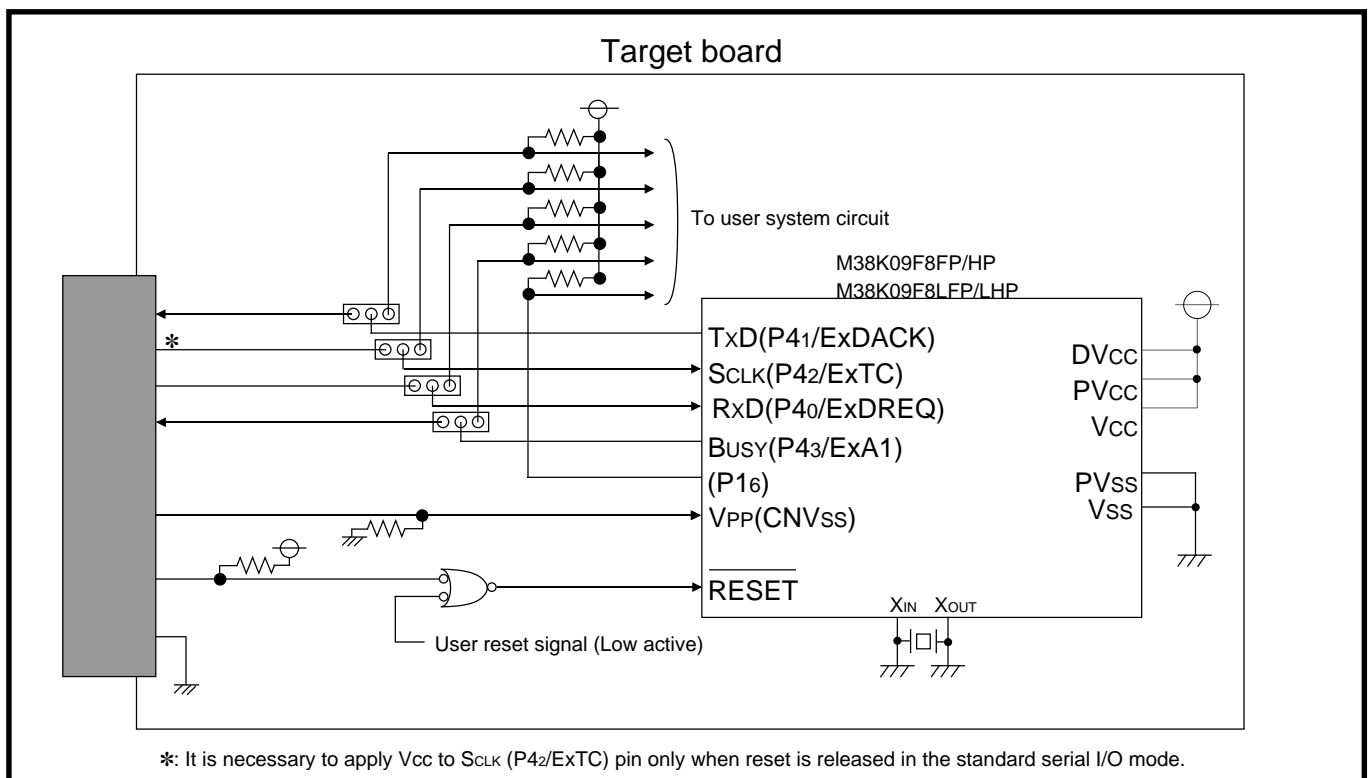


Fig. 2.13.6 Connection example in standard serial I/O mode (2)

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2.13 Flash memory

③ When control signals are affected to user system circuit-2

Figure 2.13.7 shows an example that the analog switch (74HC4066) cut-off the control signals not to supply to the user system circuit in the standard serial I/O mode.

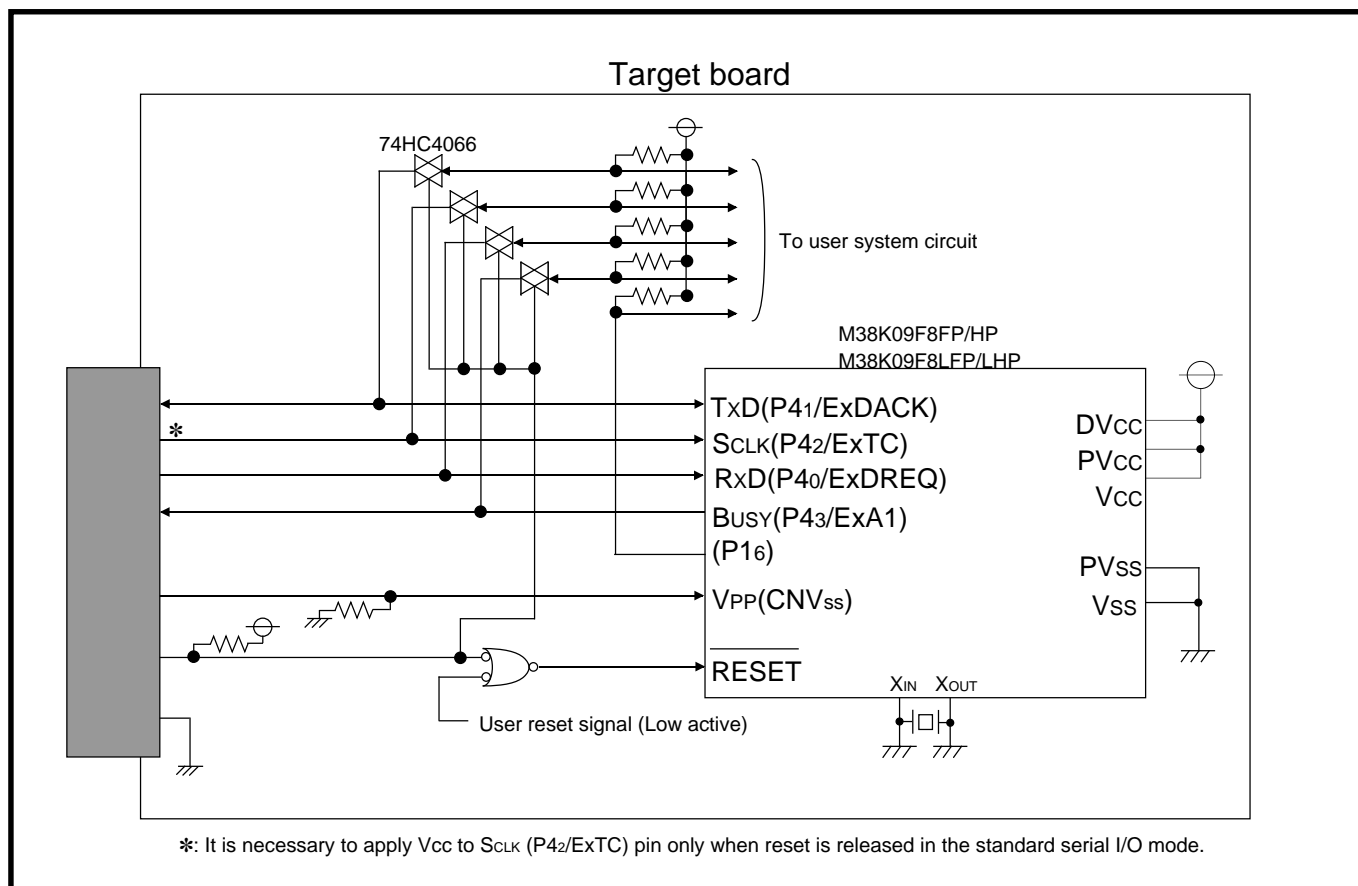


Fig. 2.13.7 Connection example in standard serial I/O mode (3)

(2) Control example in CPU rewrite mode

In this example, data is received by using serial I/O, and the data is programmed to the built-in flash memory in the CPU rewrite mode.

Figure 2.13.8 shows an example of the reprogramming system for the built-in flash memory in the CPU rewrite mode. Figure 2.13.9 shows the CPU rewrite mode beginning/release flowchart.

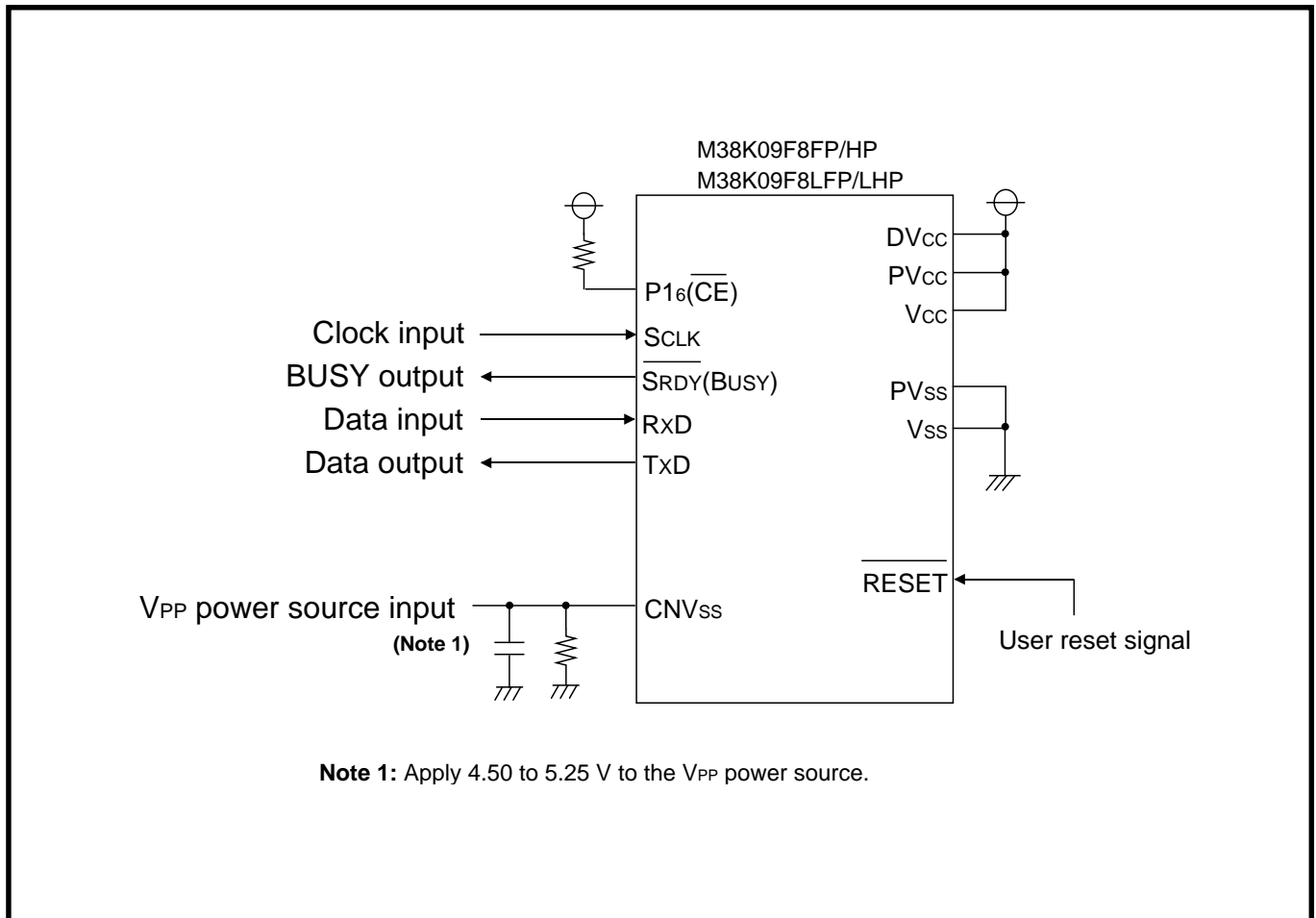
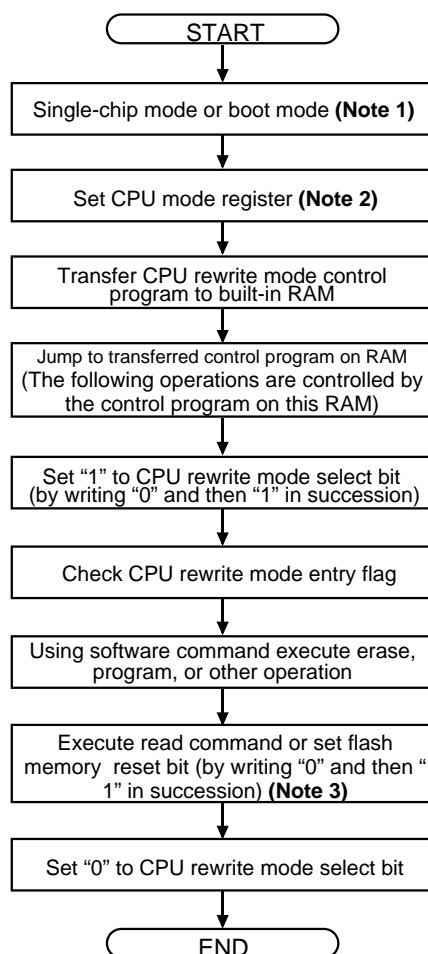


Fig. 2.13.8 Example of rewrite system for built-in flash memory in CPU rewrite mode

APPLICATION

2.13 Flash memory



Notes 1: When MCU starts in the single-chip mode, it is necessary to apply 4.50 to 5.25 V to the CNVss pin until confirming of the CPU rewrite mode entry flag.

2: Set bits 6 and 7 (system clock division ratio selection bits) of the CPU mode register (address 003B₁₆).

3: Before releasing the CPU rewrite mode after completing erase or program operation, always be sure to execute the read array command or reset the flash memory.

Fig. 2.13.9 CPU rewrite mode beginning/release flowchart

2.13.8 Notes on CPU rewrite mode

(1) Operation speed

During CPU rewrite mode, set the internal clock ϕ 1.5 MHz or less using the system clock division ratio selection bits (bits 6 and 7 of address 003B₁₆).

(2) Instructions inhibited against use

The instructions which refer to the internal data of the flash memory cannot be used during the CPU rewrite mode .

(3) Interrupts inhibited against use

The interrupts cannot be used during the CPU rewrite mode because they refer to the internal data of the flash memory.

(4) Watchdog timer

In case of the watchdog timer has been running already, the internal reset generated by watchdog timer underflow does not happen, because of watchdog timer is always clearing during program or erase operation.

(5) Reset

Reset is always valid. In case of CNV_{SS} = "H" when reset is released, boot mode is active. So the program starts from the address contained in address FFFC₁₆ and FFFD₁₆ in boot ROM area.



CHAPTER 3

APPENDIX

- 3.1 Electrical characteristics
- 3.2 Standard characteristics
- 3.3 Notes on use
- 3.4 Countermeasures against noise
- 3.5 List of registers
- 3.6 Package outline
- 3.7 List of instruction code
- 3.8 Machine instructions
- 3.9 SFR memory map
- 3.10 Pin configurations

APPENDIX

3.1 Electrical characteristics

3.1 Electrical characteristics

3.1.1 Absolute maximum ratings

Table 3.1.1 Absolute maximum ratings

Symbol	Parameter			Conditions	Ratings	Unit
VCC	Power source voltage			All voltages are based on VSS. Output transistors are cut off.	−0.3 to 6.5	V
AVCC	Analog power source voltage VCC _E , VREF, PVCC, DVCC, USBVREF				−0.3 to VCC + 0.3	V
VI	Input voltage	P00–P07, P10–P17, P20–P27, P30–P37, P40–P43, P50–P57, P60–P63			−0.3 to VCC + 0.3	V
VI	Input voltage	RESET, XIN, CNVss2			−0.3 to VCC + 0.3	V
VI	Input voltage	CNVss	Mask ROM version		−0.3 to VCC + 0.3	V
			Flash memory version		−0.3 to 6.5	V
VI	Input voltage	D0+, D0-			−0.5 to 3.8	V
VO	Output voltage	P00–P07, P10–P17, P20–P27, P30–P37, P40–P43, P50–P57, P60–P63, XOUT			−0.3 to VCC + 0.3	V
VO	Output voltage	D0+, D0-, TrON		−0.5 to 3.8	V	
Pd	Power dissipation	(Note)		Ta = 25°C	500	mW
Topr	Operating temperature			MCU operating	−20 to 85	°C
				In flash memory mode (For flash memory version)	25±5	°C
Tstg	Storage temperature				−40 to 125	°C

Note: The maximum rating value depends on not only the MCU's power dissipation but the heat consumption characteristics of the package.

3.1 Electrical characteristics (STANDARD)

3.1.2 Recommended operating conditions

Table 3.1.2 Recommended operating conditions ($V_{CC} = 4.00$ to 5.25 V, $V_{SS} = 0$ V, $T_a = -20$ to 85°C , unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V _{CC}	Power source voltage	V _{CC}	4.00	5.00	5.25	V
		System clock 12 MHz (8-divide mode)				V
		System clock ≤ 8 MHz	4.00	5.00	5.25	V
AV _{CC}	Analog power source voltage	PV _{CC} , DV _{CC}		V _{CC}		V
AV _{CC}	Analog power source voltage	V _{CC} E		V _{CC}		V
V _{REF}	Analog reference voltage	V _{REF}	2.0		V _{CC}	V
V _{SS}	Power source voltage	V _{SS}		0		V
AV _{SS}	Analog power source voltage	PV _{SS}		0		V
V _{IH}	"H" input voltage	P00–P07, P20–P27, P50–P57, P60–P63	0.8V _{CC}		V _{CC}	V
V _{IH}	"H" input voltage	P10–P17, P30–P37, P40–P43	0.8V _{CC} E		V _{CC} E	V
V _{IH}	"H" input voltage	RESET, X _{IN} , CNV _{SS} , CNV _{SS} 2	0.8V _{CC}		V _{CC}	V
V _{IH}	"H" input voltage	D0+, D0-	2.0		3.6	V
V _{IL}	"L" input voltage	P00–P07, P20–P27, P50–P57, P60–P63	0		0.2V _{CC}	V
V _{IL}	"L" input voltage	P10–P17, P30–P37, P40–P43	0		0.2V _{CC} E	V
V _{IL}	"L" input voltage	RESET, X _{IN} , CNV _{SS} , CNV _{SS} 2	0		0.2V _{CC}	V
V _{IL}	"L" input voltage	D0+, D0-	0		0.8	V

APPENDIX

3.1 Electrical characteristics (STANDARD)

Table 3.1.3 Recommended operating conditions ($V_{CC} = 4.00$ to 5.25 V, $V_{SS} = 0$ V, $T_a = -20$ to 85°C , unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$\Sigma I_{OH}(\text{peak})$	"H" total peak output current (Note 1) P00–P07, P20–P27, P50–P57, P60–P63			–80	mA
$\Sigma I_{OH}(\text{peak})$	"H" total peak output current (Note 1) P10–P17, P30–P37, P40–P43			–80	mA
$\Sigma I_{OL}(\text{peak})$	"L" total peak output current (Note 1) P00–P07, P20–P27, P50–P57			80	mA
$\Sigma I_{OL}(\text{peak})$	"L" total peak output current (Note 1) P60–P63			80	mA
$\Sigma I_{OL}(\text{peak})$	"L" total peak output current (Note 1) P10–P17, P30–P37, P40–P43			80	mA
$\Sigma I_{OH}(\text{avg})$	"H" total average output current (Note 1) P00–P07, P20–P27, P50–P57, P60–P63			–40	mA
$\Sigma I_{OH}(\text{avg})$	"H" total average output current (Note 1) P10–P17, P30–P37, P40–P43			–40	mA
$\Sigma I_{OL}(\text{avg})$	"L" total average output current (Note 1) P00–P07, P20–P27, P50–P57			40	mA
$\Sigma I_{OL}(\text{avg})$	"L" total average output current (Note 1) P60–P63			40	mA
$\Sigma I_{OL}(\text{avg})$	"L" total average output current (Note 1) P10–P17, P30–P37, P40–P43			40	mA
$I_{OH}(\text{peak})$	"H" peak output current (Note 2) P00–P07, P20–P27, P50–P57, P60–P63			–10	mA
$I_{OH}(\text{peak})$	"H" peak output current (Note 2) P10–P17, P30–P37, P40–P43			–10	mA
$I_{OL}(\text{peak})$	"L" peak output current (Note 2) P00–P07, P20–P27, P50–P57			10	mA
$I_{OL}(\text{peak})$	"L" peak output current (Note 2) P60–P63			20	mA
$I_{OL}(\text{peak})$	"L" peak output current (Note 2) P10–P17, P30–P37, P40–P43			10	mA
$I_{OH}(\text{avg})$	"H" average output current (Note 3) P00–P07, P20–P27, P50–P57, P60–P63			–5	mA
$I_{OH}(\text{avg})$	"H" average output current (Note 3) P10–P17, P30–P37, P40–P43			–5	mA
$I_{OL}(\text{avg})$	"L" average output current (Note 3) P00–P07, P20–P27, P50–P57			5	mA
$I_{OL}(\text{avg})$	"L" average output current (Note 3) P60–P63			10	mA
$I_{OL}(\text{avg})$	"L" average output current (Note 3) P10–P17, P30–P37, P40–P43			5	mA
$f(XIN)$	Main clock input oscillation frequency (Note 4)	6		12	MHz
$f(XIN)$ or $f(SYN)$	System clock frequency	6		12	MHz
$f(\phi)$	ϕ frequency			8	MHz

Notes 1: The total peak output current is the absolute value of the peak currents flowing through all the applicable ports. The total average output current is the average value of the absolute value of the currents measured over 100 ms flowing through all the applicable ports.

2: The peak output current is the absolute value of the peak current flowing in each port.

3: The average output current is the average value of the absolute value of the currents measured over 100 ms.

4: The duty of oscillation frequency is 50 %. 6 MHz or 12 MHz is usable.

3.1 Electrical characteristics (STANDARD)

3.1.3 Electrical characteristics

Table 3.1.4 Electrical characteristics (1) (V_{CC} = 4.00 to 5.25 V, V_{SS} = 0 V, T_a = -20 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
VOH	“H” output voltage P00–P07, P20–P27, P50–P57, P60–P63	IOH = -10 mA	V _{CC} -2.0			V
		IOH = -1 mA	V _{CC} -1.0			V
VOH	“H” output voltage P10–P17, P30–P37, P40–P43	IOH = -10 mA	V _{CC} E-2.0			V
		IOH = -1 mA	V _{CC} E-1.0			V
VOH	“H” output voltage D0+, D0-	D+ and D- pins pull-down with 0 V via a resistor of 15 kΩ ± 5 %	2.8		3.6	V
VOL	“L” output voltage P00–P07, P20–P27, P50–P57	IOL = 10 mA			2.0	V
		IOL = 1 mA			1.0	V
VOL	“L” output voltage P60–P63	IOL = 20 mA			2.0	V
		IOL = 1 mA			1.0	V
VOL	“L” output voltage P10–P17, P30–P37, P40–P43	IOL = 10 mA			2.0	V
		IOL = 1 mA			1.0	V
VOL	“L” output voltage D0+, D0-	D+ and D- pins pull-up with 3.6 V via a resistor of 1.5 kΩ ± 5 %	0		0.3	V
VT+–VT-	Hysteresis CNTR0, INT0, INT1			0.6		V
VT+–VT-	Hysteresis P10/DQ0–P17/DQ7, P30–P32, P33/ExINT, P34/ExCS, P35/ExWR, P36/ExRD, P37/ ExA0, P40/ExDREQ/RxD, P41/ExDACK/ TxD, P42/ExTC/SCLK, P43/ExA1/SRDY			0.6		V
VT+–VT	Hysteresis D0+, D0-			0.25		V
VT+–VT-	Hysteresis RESET			0.5		V
I _{IH}	“H” input current P00–P07, P20–P27, P50–P57, P60–P63	V _I = V _{CC} (Pull-ups “off”)			5.0	μA
I _{IH}	“H” input current P10–P17, P30–P37, P40–P43	V _I = V _{CC} E			5.0	μA
I _{IH}	“H” input current RESET, CNVss	V _I = V _{CC}			5.0	μA
I _{IH}	“H” input current X _{IN}	V _I = V _{CC}		4.0		μA
I _{IL}	“L” input current P00–P07, P20–P27, P50–P57, P60–P63	V _I = V _{SS} (Pull-ups “off”)			-5.0	μA
I _{IL}	“L” input current P10–P17, P30–P37, P40–P43	V _I = V _{SS}			-5.0	μA
I _{IL}	“L” input current RESET, CNVss, CNVss2	V _I = V _{SS}			-5.0	μA
I _{IL}	“L” input current X _{IN}	V _I = V _{SS}		-4.0		μA
I _{IL}	“L” input current P00–P07, P50, P52 (Pull-ups “on”)	V _I = V _{SS}	-20.0	-60.0	-120.0	μA
VRAM	RAM hold voltage	When clock is stopped	2.00		5.25	V

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3.1 Electrical characteristics (STANDARD)

Table 3.1.5 Electrical characteristics (2) ($V_{CC} = 4.00$ to 5.25 V, $V_{SS} = 0$ V, $T_a = -20$ to 85°C , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min.	Typ.	Max.		
ICC	Power source current (Output transistor is isolated.)	Normal mode (Note 1)	f(XIN) = system clock = 12 MHz, ϕ = 6 MHz, USB reference voltage circuit enabled		21.0	60	mA
			f(XIN) = 12 MHz, System clock = ϕ = 8 MHz, USB reference voltage circuit enabled		22.5	60	mA
			f(XIN) = 6 MHz, System clock = ϕ = 8 MHz, USB reference voltage circuit enabled		22.0	60	mA
			f(XIN) = system clock = ϕ = 6 MHz, USB reference voltage circuit enabled		21.0	60	mA
		Wait mode (Note 2)	f(XIN) = 12 MHz, System clock = ϕ = 8 MHz, USB reference voltage circuit enabled		6.0		mA
		Stop mode (Note 3)	USB reference voltage circuit enabled Low current mode		125.0	250	μ A
			USB reference voltage circuit disabled Ta = 25 °C		0.1		μ A
			USB reference voltage circuit disabled Ta = 85 °C			10	μ A

<Test conditions>

Notes 1: Operating in single-chip mode

Clock input from X_{IN} pin (X_{OUT} oscillator stopped)

f_{USB} = 48 MHz

All USB difference-input circuits enabled

Leaving I/O pins open

Operating functions: PLL circuit, CPU, Timers

2: Operating in single-chip mode with Wait mode

Clock input from X_{IN} pin (X_{OUT} oscillator stopped)

f_{USB} = 48 MHz

All USB difference-input circuits enabled

Leaving I/O pins open

Operating functions: PLL circuit, Timers, USB receiving

Disabled functions: CPU

3: Operating in single-chip mode with Stop mode

Oscillation stopped

All USB difference-input circuits disabled

Leaving I/O pins open

3.1 Electrical characteristics (STANDARD)

3.1.4 A-D converter characteristics

Table 3.1.6 A-D Converter characteristics ($V_{CC} = 4.00$ to 5.25 V, $V_{SS} = 0$ V, $T_a = -20$ to 85°C , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				10	Bits
—	Linearity error	$T_a = 25^{\circ}\text{C}$			± 3	LSB
—	Differential nonlinear error	$T_a = 25^{\circ}\text{C}$			± 1.5	LSB
VOT	Zero transition voltage	$V_{CC} = V_{REF} = 5.12$ V	0	15	35	mV
VFST	Full scale transition voltage	$V_{CC} = V_{REF} = 5.12$ V	5105	5125	5150	mV
tCONV	Conversion time				122	tc(XIN) or tc(fSYN)
RLADDER	Ladder resistor			35		k Ω
IVREF	Reference power source input current	A-D converter operating; $V_{REF} = 5.0$ V	50	150	200	μA
		A-D converter not operating; $V_{REF} = 5.0$ V			5	
II(AD)	A-D port input current				5.0	μA

APPENDIX

3.1 Electrical characteristics (STANDARD)

3.1.5 Timing requirements

Table 3.1.7 Timing requirements ($V_{CC} = 4.00$ to 5.25 V, $V_{SS} = 0$ V, $T_a = -20$ to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_w(\text{RESET})$	Reset input "L" pulse width	2			μs
$t_c(\text{XIN})$	Main clock input cycle time	83			ns
$t_{WH}(\text{XIN})$	Main clock input "H" pulse width	35			ns
$t_{WL}(\text{XIN})$	Main clock input "L" pulse width	35			ns
$t_c(\text{CNTR})$	CNTR ₀ input cycle time	200			ns
$t_{WH}(\text{CNTR})$	CNTR ₀ input "H" pulse width	80			ns
$t_{WL}(\text{CNTR})$	CNTR ₀ input "L" pulse width	80			ns
$t_{WH}(\text{INT})$	INT ₀ , INT ₁ input "H" pulse width	80			ns
$t_{WL}(\text{INT})$	INT ₀ , INT ₁ input "L" pulse width	80			ns
$t_c(\text{SCLK})$	Serial I/O clock input cycle time (Note)	800			ns
$t_{WH}(\text{SCLK})$	Serial I/O clock input "H" pulse width (Note)	370			ns
$t_{WL}(\text{SCLK})$	Serial I/O clock input "L" pulse width (Note)	370			ns
$t_{su}(\text{RXD-SCLK})$	Serial I/O input set up time	220			ns
$t_h(\text{SCLK-RXD})$	Serial I/O input hold time	100			ns

Note: These limits are the rating values in the clock synchronous mode, bit 6 of address 0FE0₁₆ = "1". In the UART mode, bit 6 of address 0FE0₁₆ = "0"; the rating values are set to one fourth.

Table 3.1.8 Timing requirements of external bus interface (EXB)

($V_{CC} = 4.00$ to 5.25 V, $V_{SS} = 0$ V, $T_a = -20$ to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su}(\text{S-R})$	ExCS setup time for read	0			ns
$t_{su}(\text{S-W})$	ExCS setup time for write	0			ns
$t_h(\text{R-S})$	ExCS hold time for read	0			ns
$t_h(\text{W-S})$	ExCS hold time for write	0			ns
$t_{su}(\text{A-R})$	ExA ₀ , ExA ₁ setup time for read	10			ns
$t_{su}(\text{A-W})$	ExA ₀ , ExA ₁ setup time for write	10			ns
$t_h(\text{R-A})$	ExA ₀ , ExA ₁ hold time for read	0			ns
$t_h(\text{W-A})$	ExA ₀ , ExA ₁ hold time for write	0			ns
$t_{su}(\text{ACK-R})$	ExDACK setup time for read	10			ns
$t_{su}(\text{ACK-W})$	ExDACK setup time for write	10			ns
$t_h(\text{R-ACK})$	ExDACK hold time for read	0			ns
$t_h(\text{W-ACK})$	ExDACK hold time for write	0			ns
$t_{WH}(\text{R})$	Read "H" pulse width	80			ns
$t_{WL}(\text{R})$	Read "L" pulse width	80			ns
$t_{WH}(\text{W})$	Write "H" pulse width	80			ns
$t_{WL}(\text{W})$	Write "L" pulse width	80			ns
$t_{WH}(\text{ACK})$	ExDACK "H" pulse width	120			ns
$t_{WL}(\text{ACK})$	ExDACK "L" pulse width	120			ns
$t_{su}(\text{D-W})$	Data input setup time before write	40			ns
$t_h(\text{W-D})$	Data input hold time after write	0			ns
$t_{su}(\text{D-ACK})$	Data input setup time before ExDACK	60			ns
$t_h(\text{ACK-W})$	Data input hold time after ExDACK	5			ns
$t_c(\phi)$	CPU clock cycle time	125			ns
$t_w(\text{cycle})$	Burst mode access cycle time	USB function not operating	$t_c(\phi) \cdot 3 + 10$		ns
		USB function operating	$t_c(\phi) \cdot 5 + 10$		ns

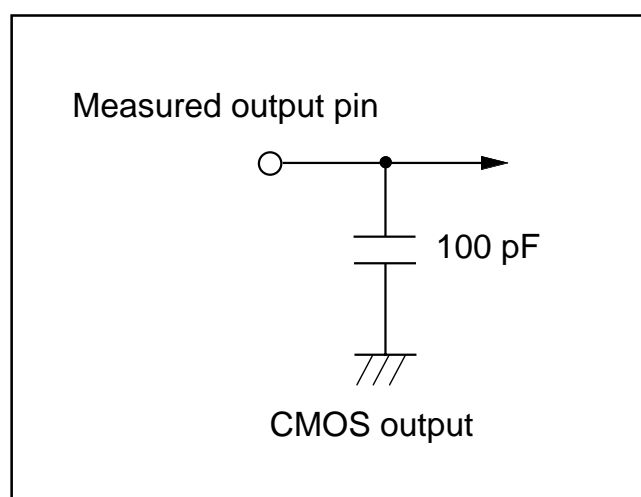
3.1 Electrical characteristics (STANDARD)

3.1.6 Switching characteristics

Table 3.1.9 Switching characteristics ($V_{CC} = 4.00$ to 5.25 V, $V_{SS} = 0$ V, $T_a = -20$ to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH}(SCLK)$	Serial I/O clock output "H" pulse width	$t_c(SCLK)/2-30$			ns
$t_{WL}(SCLK)$	Serial I/O clock output "L" pulse width	$t_c(SCLK)/2-30$			ns
$t_d(SCLK-TxD)$	Serial I/O output delay time			140	ns
$t_v(SCLK-TxD)$	Serial I/O output valid time	-30			ns
$t_r(SCLK)$	Serial I/O clock output rising time			30	ns
$t_f(SCLK)$	Serial I/O clock output falling time			30	ns
$t_r(CMOS)$	CMOS output rising time (Note)			30	ns
$t_f(CMOS)$	CMOS output falling time (Note)			30	ns

Notes: Pins XOUT, D0+, D0- are excluded.

**Fig. 3.1.1 Output switching characteristics measurement circuit****Table 3.1.10 Switching characteristics of external bus interface (EXB)**

($V_{CC} = 4.00$ to 5.25 V, $V_{SS} = 0$ V, $T_a = -20$ to 85 °C, unless otherwise noted)

VCC = 4.00 to 5.25 V, VSS = 0 V, Ta = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
ta(R-D)	Data output enable time after read				60	ns
tv(R-D)	Data output disable time after read		0			ns
ta(ACK-D)	Data output enable time after ExDACK				80	ns
tv(ACK-D)	Data output disable time after ExDACK		0			ns
td(R-Mdis)	In cycle mode Mch_req disable output delay time after read				tc(φ)+10	ns
td(W-Mdis)	In cycle mode Mch_req disable output delay time after write				tc(φ)+10	ns
td(R-Men)	In cycle mode Mch_req enable output delay time after read	USB function not operating			tc(φ)•3+10	ns
		USB function operating			tc(φ)•5+10	ns
td(W-Men)	In cycle mode Mch_req enable output delay time after write	USB function not operating			tc(φ)•3+10	ns
		USB function operating			tc(φ)•5+10	ns

APPENDIX

3.1 Electrical characteristics (STANDARD)

Table 3.1.11 Switching characteristics (USB ports) ($V_{CC} = 4.00$ to 5.25 V, $V_{SS} = 0$ V, $T_a = -20$ to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$t_{fr}(D+/D-)$	USB full-speed output rising time	$CL = 50$ pF	4		20	ns
$t_{ff}(D+/D-)$	USB full-speed output falling time	$CL = 50$ pF	4		20	ns
$t_{frfm}(D+/D-)$	USB full-speed ports rising/falling ratio	$t_{fr}(D+/D-)/t_{ff}(D+/D-)$	90		111.11	%
$V_{crs}(D+/D-)$	USB output signal cross-over voltage		1.3		2.0	V

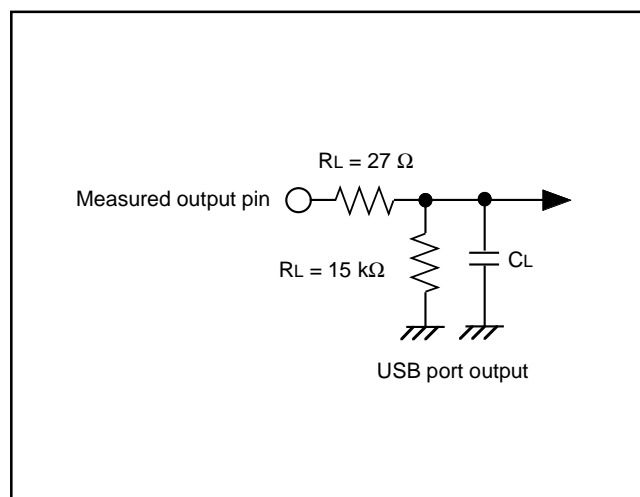


Fig. 3.1.2 USB output switching characteristics measurement circuit (1) for D0-

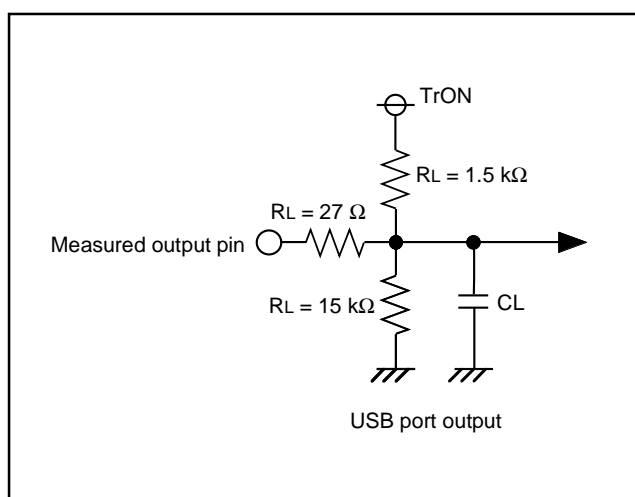


Fig. 3.1.3 USB output switching characteristics measurement circuit (2) for D0+

3.1 Electrical characteristics (L.Ver)

3.1.7 Recommended operating conditions

Table 3.1.12 Recommended operating conditions (V_{CC} = 3.00 to 5.25 V, V_{SS} = 0 V, T_a = -20 to 85°C, unless otherwise noted)

Symbol	Parameter			Limits			Unit
				Min.	Typ.	Max.	
V _{CC}	Power source voltage	V _{CC}	System clock 12 MHz (2-/4-/8-divide mode)	4.00	5.00	5.25	V
			System clock 8 MHz	4.00	5.00	5.25	V
			System clock 6 MHz	3.00	5.00	5.25	V
AV _{CC}	Analog power source voltage	PV _{CC} , DV _{CC}			V _{CC}		V
AV _{CC}	Analog power source voltage	V _{CC} E			V _{CC}		V
V _{REF}	Analog reference voltage	V _{REF}		2.0		V _{CC}	V
V _{REF}	Analog reference voltage	USBV _{REF}	V _{CC} = 3.6 to 4.0 V	3.0		3.6	V
			V _{CC} = 3.0 to 3.6 V	3.0		V _{CC}	V
V _{SS}	Power source voltage	V _{SS}			0		V
AV _{SS}	Analog power source voltage	PV _{SS}			0		V
V _{IH}	"H" input voltage	P00–P07, P20–P27, P50–P57, P60–P63		0.8V _{CC}		V _{CC}	V
V _{IH}	"H" input voltage	P10–P17, P30–P37, P40–P43		0.8V _{CC} E		V _{CC} E	V
V _{IH}	"H" input voltage	RESET, X _{IN} , CNV _{SS} , CNV _{SS} 2		0.8V _{CC}		V _{CC}	V
V _{IH}	"H" input voltage	D0+, D0-		2.0		3.6	V
V _{IL}	"L" input voltage	P00–P07, P20–P27, P50–P57, P60–P63		0		0.2V _{CC}	V
V _{IL}	"L" input voltage	P10–P17, P30–P37, P40–P43		0		0.2V _{CC} E	V
V _{IL}	"L" input voltage	RESET, X _{IN} , CNV _{SS} , CNV _{SS} 2		0		0.2V _{CC}	V
V _{IL}	"L" input voltage	D0+, D0-		0		0.8	V

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3.1 Electrical characteristics (L.Ver)

Table 3.1.13 Recommended operating conditions (Vcc = 3.00 to 5.25 V, Vss = 0 V, Ta = -20 to 85°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$\Sigma I_{OH(peak)}$	"H" total peak output current (Note 1)	P00-P07, P20-P27, P50-P57, P60-P63			-80	mA
$\Sigma I_{OH(peak)}$	"H" total peak output current (Note 1)	P10-P17, P30-P37, P40-P43			-80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current (Note 1)	P00-P07, P20-P27, P50-P57			80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current (Note 1)	P60-P63			80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current (Note 1)	P10-P17, P30-P37, P40-P43			80	mA
$\Sigma I_{OH(avg)}$	"H" total average output current (Note 1)	P00-P07, P20-P27, P50-P57, P60-P63			-40	mA
$\Sigma I_{OH(avg)}$	"H" total average output current (Note 1)	P10-P17, P30-P37, P40-P43			-40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current (Note 1)	P00-P07, P20-P27, P50-P57			40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current (Note 1)	P60-P63			40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current (Note 1)	P10-P17, P30-P37, P40-P43			40	mA
$I_{OH(peak)}$	"H" peak output current (Note 2)	P00-P07, P20-P27, P50-P57, P60-P63			-10	mA
$I_{OH(peak)}$	"H" peak output current (Note 2)	P10-P17, P30-P37, P40-P43			-10	mA
$I_{OL(peak)}$	"L" peak output current (Note 2)	P00-P07, P20-P27, P50-P57			10	mA
$I_{OL(peak)}$	"L" peak output current (Note 2)	P60-P63			20	mA
$I_{OL(peak)}$	"L" peak output current (Note 2)	P10-P17, P30-P37, P40-P43			10	mA
$I_{OH(avg)}$	"H" average output current (Note 3)	P00-P07, P20-P27, P50-P57, P60-P63			-5	mA
$I_{OH(avg)}$	"H" average output current (Note 3)	P10-P17, P30-P37, P40-P43			-5	mA
$I_{OL(avg)}$	"L" average output current (Note 3)	P00-P07, P20-P27, P50-P57			5	mA
$I_{OL(avg)}$	"L" average output current (Note 3)	P60-P63			10	mA
$I_{OL(avg)}$	"L" average output current (Note 3)	P10-P17, P30-P37, P40-P43			5	mA
$f(XIN)$	Main clock input oscillation frequency (Note 4)	Vcc = 4.00 to 5.25 V	6		12	MHz
		Vcc = 3.00 to 4.00 V	6		6	MHz
$f(XIN)$ or $f(SYN)$	System clock frequency	Vcc = 4.00 to 5.25 V	6		12	MHz
		Vcc = 3.00 to 4.00 V	6		6	MHz
$f(\phi)$	ϕ frequency	Vcc = 4.00 to 5.25 V			8	MHz
		Vcc = 3.00 to 4.00 V			6	MHz

Notes 1: The total peak output current is the absolute value of the peak currents flowing through all the applicable ports. The total average output current is the average value of the absolute value of the currents measured over 100 ms flowing through all the applicable ports.

2: The peak output current is the absolute value of the peak current flowing in each port.

3: The average output current is the average value of the absolute value of the currents measured over 100 ms.

4: The duty of oscillation frequency is 50 %. 6 MHz or 12 MHz is usable.

3.1 Electrical characteristics (L.Ver)

3.1.8 Electrical characteristics

Table 3.1.14 Electrical characteristics (1) ($V_{CC} = 3.00$ to 5.25 V, $V_{SS} = 0$ V, $T_a = -20$ to 85°C , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
VOH	“H” output voltage P00–P07, P20–P27, P50–P57, P60–P63	IOH = –10 mA (VCC = 4.00 to 5.25 V)	VCC–2.0			V
		IOH = –1 mA	VCC–1.0			V
VOH	“H” output voltage P10–P17, P30–P37, P40–P43	IOH = –10 mA (VCC = 4.00 to 5.25 V)	VCC–2.0			V
		IOH = –1 mA	VCC–1.0			V
VOH	“H” output voltage D0+, D0–	D+ and D– pins pull-down with 0 V via a resistor of $15\text{ k}\Omega \pm 5\%$	2.8		3.6	V
VOL	“L” output voltage P00–P07, P20–P27, P50–P57	IOL = 10 mA (VCC = 4.00 to 5.25 V)			2.0	V
		IOL = 1 mA			1.0	V
VOL	“L” output voltage P60–P63	IOL = 20 mA (VCC = 4.00 to 5.25 V)			2.0	V
		IOL = 1 mA			1.0	V
VOL	“L” output voltage P10–P17, P30–P37, P40–P43	IOL = 10 mA (VCC = 4.00 to 5.25 V)			2.0	V
		IOL = 1 mA (VCC = 3.00 to 5.25 V)			1.0	V
VOL	“L” output voltage D0+, D0–	D+ and D– pins pull-up with 3.6 V via a resistor of $1.5\text{ k}\Omega \pm 5\%$	0		0.3	V
VT+–VT–	Hysteresis CNTR0, INT0, INT1			0.6		V
VT+–VT–	Hysteresis P10/DQ0–P17/DQ7, P30–P32, P33/ExINT, P34/ExCS, P35/ExWR, P36/ExRD, P37/ ExA0, P40/ExDREQ/RxD, P41/ExDACK/ TxD, P42/ExTC/SCLK, P43/ExA1/SRDY			0.6		V
VT+–VT	Hysteresis D0+, D0–			0.25		V
VT+–VT–	Hysteresis $\overline{\text{RESET}}$			0.5		V
IiH	“H” input current P00–P07, P20–P27, P50–P57, P60–P63	VI = VCC (Pull-ups “off”)			5.0	μA
IiH	“H” input current P10–P17, P30–P37, P40–P43	VI = VCC			5.0	μA
IiH	“H” input current $\overline{\text{RESET}}$, CNVSS	VI = VCC			5.0	μA
IiH	“H” input current XIN	VI = VCC		4.0		μA
IiL	“L” input current P00–P07, P20–P27, P50–P57, P60–P63	VI = VSS (Pull-ups “off”)			–5.0	μA
IiL	“L” input current P10–P17, P30–P37, P40–P43	VI = VSS			–5.0	μA
IiL	“L” input current $\overline{\text{RESET}}$, CNVSS, CNVSS2	VI = VSS			–5.0	μA
IiL	“L” input current XIN	VI = VSS		–4.0		μA
IiL	“L” input current P00–P07, P50, P52 (Pull-ups “on”)	VI = VSS (VCC = 4.00 to 5.25 V)	–20.0	–60.0	–120.0	μA
		VI = VSS	–10.0			μA
VRAM	RAM hold voltage	When clock is stopped	2.00		5.25	V

APPENDIX

3.1 Electrical characteristics (L.Ver)

Table 3.1.15 Electrical characteristics (2) (V_{CC} = 3.00 to 5.25 V, V_{SS} = 0 V, T_a = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions			Limits			Unit
					Min.	Typ.	Max.	
ICC	Power source current (Output transistor is isolated.)	Normal mode (Note 1)	Vcc = 4.00 to 5.25 V	f(XIN) = system clock = 12 MHz, ϕ = 6 MHz, USB reference voltage circuit enabled		21.0	60	mA
				f(XIN) = 12 MHz, System clock = ϕ = 8 MHz, USB reference voltage circuit enabled		22.5	60	mA
				f(XIN) = 6 MHz, System clock = ϕ = 8 MHz, USB reference voltage circuit enabled		22.0	60	mA
				f(XIN) = system clock = ϕ = 6 MHz, USB reference voltage circuit enabled		21.0	60	mA
			Vcc = 3.00 to 4.00 V	f(XIN) = system clock = ϕ = 6 MHz, USB reference voltage circuit disabled			35	mA
			Vcc = 3.00 to 3.60 V	f(XIN) = system clock = ϕ = 6 MHz, USB reference voltage circuit disabled		9.0	30	mA
		Wait mode (Note 2)	Vcc = 4.00 to 5.25 V	f(XIN) = 12 MHz, System clock = ϕ = 8 MHz, USB reference voltage circuit enabled		6.0		mA
			Vcc = 3.00 to 4.00 V	f(XIN) = system clock = ϕ = 6 MHz, USB reference voltage circuit disabled		2.0		mA
		Stop mode (Note 3)	Vcc = 4.00 to 5.25 V	USB reference voltage circuit enabled Low current mode		125.0	250	μA
			Vcc = 3.00 to 5.25 V	USB reference voltage circuit disabled Ta = 25 °C		0.1		μA
				USB reference voltage circuit disabled Ta = 85 °C			10	μA

<Test conditions>

Notes 1: Operating in single-chip mode

Clock input from X_{IN} pin (X_{OUT} oscillator stopped)

f_{USB} = 48 MHz

All USB difference-input circuits enabled

Leaving I/O pins open

Operating functions: PLL circuit, CPU, Timers

2: Operating in single-chip mode with Wait mode

Clock input from X_{IN} pin (X_{OUT} oscillator stopped)

f_{USB} = 48 MHz

All USB difference-input circuits enabled

Leaving I/O pins open

Operating functions: PLL circuit, Timers, USB receiving

Disabled functions: CPU

3: Operating in single-chip mode with Stop mode

Oscillation stopped

All USB difference-input circuits disabled

Leaving I/O pins open

3.1 Electrical characteristics (L.Ver)

3.1.9 A-D converter characteristics

Table 3.1.16 A-D Converter characteristics ($V_{CC} = 3.00$ to 5.25 V, $V_{SS} = 0$ V, $T_a = -20$ to 85°C , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				10	Bits
—	Linearity error	$T_a = 25^{\circ}\text{C}$			± 3	LSB
—	Differential nonlinear error	$T_a = 25^{\circ}\text{C}$			± 1.5	LSB
VOT	Zero transition voltage	$V_{CC} = V_{REF} = 5.12$ V	0	15	35	mV
VFST	Full scale transition voltage	$V_{CC} = V_{REF} = 5.12$ V	5105	5125	5150	mV
tCONV	Conversion time				122	tc(XIN) or tc(fSYN)
RLADDER	Ladder resistor			35		k Ω
IVREF	Reference power source input current	A-D converter operating; $V_{REF} = 5.0$ V	50	150	200	μA
		A-D converter not operating; $V_{REF} = 5.0$ V			5	
II(AD)	A-D port input current				5.0	μA

APPENDIX

3.1 Electrical characteristics (L.Ver)

3.1.10 Timing requirements

Table 3.1.17 Timing requirements (1) (VCC = 4.00 to 5.25 V, VSS = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tw(RESET)	Reset input “L” pulse width	2			μs
tc(XIN)	Main clock input cycle time	83			ns
tWH(XIN)	Main clock input “H” pulse width	35			ns
tWL(XIN)	Main clock input “L” pulse width	35			ns
tc(CNTR)	CNTR0 input cycle time	200			ns
tWH(CNTR)	CNTR0 input “H” pulse width	80			ns
tWL(CNTR)	CNTR0 input “L” pulse width	80			ns
tWH(INT)	INT0, INT1 input “H” pulse width	80			ns
tWL(INT)	INT0, INT1 input “L” pulse width	80			ns
tc(SCLK)	Serial I/O clock input cycle time (Note)	800			ns
tWH(SCLK)	Serial I/O clock input “H” pulse width (Note)	370			ns
tWL(SCLK)	Serial I/O clock input “L” pulse width (Note)	370			ns
tsu(RxD–SCLK)	Serial I/O input set up time	220			ns
th(SCLK–RxD)	Serial I/O input hold time	100			ns

Note: These limits are the rating values in the clock synchronous mode, bit 6 of address 0FE016 = “1”. In the UART mode, bit 6 of address 0FE016 = “0”; the rating values are set to one fourth.

Table 3.1.18 Timing requirements (2) (VCC = 3.00 to 4.00 V, VSS = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tw(RESET)	Reset input “L” pulse width	2			μs
tc(XIN)	Main clock input cycle time	166			ns
tWH(XIN)	Main clock input “H” pulse width	70			ns
tWL(XIN)	Main clock input “L” pulse width	70			ns
tc(CNTR)	CNTR0 input cycle time	500			ns
tWH(CNTR)	CNTR0 input “H” pulse width	230			ns
tWL(CNTR)	CNTR0 input “L” pulse width	230			ns
tWH(INT)	INT0, INT1 input “H” pulse width	230			ns
tWL(INT)	INT0, INT1 input “L” pulse width	230			ns
tc(SCLK)	Serial I/O clock input cycle time (Note)	2000			ns
tWH(SCLK)	Serial I/O clock input “H” pulse width (Note)	950			ns
tWL(SCLK)	Serial I/O clock input “L” pulse width (Note)	950			ns
tsu(RxD–SCLK)	Serial I/O input set up time	400			ns
th(SCLK–RxD)	Serial I/O input hold time	200			ns

Note: These limits are the rating values in the clock synchronous mode, bit 6 of address 0FE016 = “1”. In the UART mode, bit 6 of address 0FE016 = “0”; the rating values are set to one fourth.

3.1 Electrical characteristics (L.Ver)

Table 3.1.19 Timing requirements of external bus interface (EXB) (1)(V_{CC} = 4.00 to 5.25 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
t _{su} (S-R)	ExCS setup time for read		0			ns
t _{su} (S-W)	ExCS setup time for write		0			ns
t _h (R-S)	ExCS hold time for read		0			ns
t _h (W-S)	ExCS hold time for write		0			ns
t _{su} (A-R)	ExA0, ExA1 setup time for read		10			ns
t _{su} (A-W)	ExA0, ExA1 setup time for write		10			ns
t _h (R-A)	ExA0, ExA1 hold time for read		0			ns
t _h (W-A)	ExA0, ExA1 hold time for write		0			ns
t _{su} (ACK-R)	ExDACK setup time for read		10			ns
t _{su} (ACK-W)	ExDACK setup time for write		10			ns
t _h (R-ACK)	ExDACK hold time for read		0			ns
t _h (W-ACK)	ExDACK hold time for write		0			ns
t _{WH} (R)	Read “H” pulse width		80			ns
t _{WL} (R)	Read “L” pulse width		80			ns
t _{WH} (W)	Write “H” pulse width		80			ns
t _{WL} (W)	Write “L” pulse width		80			ns
t _{WH} (ACK)	ExDACK “H” pulse width		120			ns
t _{WL} (ACK)	ExDACK “L” pulse width		120			ns
t _{su} (D-W)	Data input setup time before write		40			ns
t _h (W-D)	Data input hold time after write		0			ns
t _{su} (D-ACK)	Data input setup time before ExDACK		60			ns
t _h (ACK-W)	Data input hold time after ExDACK		5			ns
t _C (ϕ)	CPU clock cycle time		125			ns
t _w (cycle)	Burst mode access cycle time	USB function not operating	t _C (ϕ)*3+10			ns
		USB function operating	t _C (ϕ)*5+10			ns

APPENDIX

3.1 Electrical characteristics (L.Ver)

Table 3.1.20 Timing requirements of external bus interface (EXB) (2)

(VCC = 3.00 to 4.00 V, VSS = 0 V, Ta = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
tsu(S-R)	ExCS setup time for read		0			ns
tsu(S-W)	ExCS setup time for write		0			ns
th(R-S)	ExCS hold time for read		0			ns
th(W-S)	ExCS hold time for write		0			ns
tsu(A-R)	ExA0, ExA1 setup time for read		30			ns
tsu(A-W)	ExA0, ExA1 setup time for write		30			ns
th(R-A)	ExA0, ExA1 hold time for read		0			ns
th(W-A)	ExA0, ExA1 hold time for write		0			ns
tsu(ACK-R)	ExDACK setup time for read		30			ns
tsu(ACK-W)	ExDACK setup time for write		30			ns
th(R-ACK)	ExDACK hold time for read		0			ns
th(W-ACK)	ExDACK hold time for write		0			ns
tWH(R)	Read "H" pulse width		120			ns
tWL(R)	Read "L" pulse width		120			ns
tWH(W)	Write "H" pulse width		120			ns
tWL(W)	Write "L" pulse width		120			ns
tWH(ACK)	ExDACK "H" pulse width		160			ns
tWL(ACK)	ExDACK "L" pulse width		160			ns
tsu(D-W)	Data input setup time before write		60			ns
th(W-D)	Data input hold time after write		0			ns
tsu(D-ACK)	Data input setup time before ExDACK		80			ns
th(ACK-W)	Data input hold time after ExDACK		10			ns
tC(ϕ)	CPU clock cycle time		166			ns
tw(cycle)	Burst mode access cycle time	USB function not operating	tC(ϕ)*3+30			ns
		USB function operating	tC(ϕ)*5+30			ns

3.1 Electrical characteristics (L.Ver)

3.1.11 Switching characteristics

Table 3.1.21 Switching characteristics (1) ($V_{CC} = 4.00$ to 5.25 V, $V_{SS} = 0$ V, $T_a = -20$ to 85 °C, unless otherwise noted)

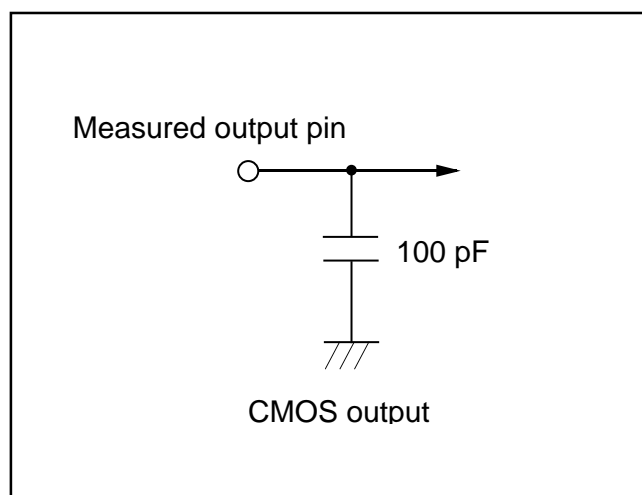
Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH}(SCLK)$	Serial I/O clock output "H" pulse width	$t_c(SCLK)/2-30$			ns
$t_{WL}(SCLK)$	Serial I/O clock output "L" pulse width	$t_c(SCLK)/2-30$			ns
$t_d(SCLK-TxD)$	Serial I/O output delay time			140	ns
$t_v(SCLK-TxD)$	Serial I/O output valid time	-30			ns
$t_r(SCLK)$	Serial I/O clock output rising time			30	ns
$t_f(SCLK)$	Serial I/O clock output falling time			30	ns
$t_r(CMOS)$	CMOS output rising time (Note)			30	ns
$t_f(CMOS)$	CMOS output falling time (Note)			30	ns

Notes: Pins XOUT, D0+, D0- are excluded.

Table 3.1.22 Switching characteristics (2) ($V_{CC} = 3.00$ to 4.00 V, $V_{SS} = 0$ V, $T_a = -20$ to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH}(SCLK)$	Serial I/O clock output "H" pulse width	$t_c(SCLK)/2-50$			ns
$t_{WL}(SCLK)$	Serial I/O clock output "L" pulse width	$t_c(SCLK)/2-50$			ns
$t_d(SCLK-TxD)$	Serial I/O output delay time			350	ns
$t_v(SCLK-TxD)$	Serial I/O output valid time	-30			ns
$t_r(SCLK)$	Serial I/O clock output rising time			50	ns
$t_f(SCLK)$	Serial I/O clock output falling time			50	ns
$t_r(CMOS)$	CMOS output rising time (Note)			50	ns
$t_f(CMOS)$	CMOS output falling time (Note)			50	ns

Notes: Pins XOUT, D0+, D0- are excluded.

**Fig. 3.1.4 Output switching characteristics measurement circuit**

APPENDIX

3.1 Electrical characteristics (L.Ver)

Table 3.1.23 Switching characteristics of external bus interface (EXB) (1)

(VCC = 4.00 to 5.25 V, VSS = 0 V, Ta = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
ta(R-D)	Data output enable time after read			60	ns
tv(R-D)	Data output disable time after read	0			ns
ta(ACK-D)	Data output enable time after ExDACK			80	ns
tv(ACK-D)	Data output disable time after ExDACK	0			ns
td(R-Mdis)	In cycle mode Mch_req disable output delay time after read			tc(φ)+10	ns
td(W-Mdis)	In cycle mode Mch_req disable output delay time after write			tc(φ)+10	ns
td(R-Men)	In cycle mode Mch_req enable output delay time after read	USB function not operating		tc(φ)•3+10	ns
		USB function operating		tc(φ)•5+10	ns
td(W-Men)	In cycle mode Mch_req enable output delay time after write	USB function not operating		tc(φ)•3+10	ns
		USB function operating		tc(φ)•5+10	ns

Table 3.1.24 Switching characteristics of external bus interface (EXB) (2)

(VCC = 3.00 to 4.00 V, VSS = 0 V, Ta = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
ta(R-D)	Data output enable time after read			80	ns
tv(R-D)	Data output disable time after read	0			ns
ta(ACK-D)	Data output enable time after ExDACK			120	ns
tv(ACK-D)	Data output disable time after ExDACK	0			ns
td(R-Mdis)	In cycle mode Mch_req disable output delay time after read			tc(φ)+30	ns
td(W-Mdis)	In cycle mode Mch_req disable output delay time after write			tc(φ)+30	ns
td(R-Men)	In cycle mode Mch_req enable output delay time after read	USB function not operating		tc(φ)•3+30	ns
		USB function operating		tc(φ)•5+30	ns
td(W-Men)	In cycle mode Mch_req enable output delay time after write	USB function not operating		tc(φ)•3+30	ns
		USB function operating		tc(φ)•5+30	ns

3.1 Electrical characteristics (L.Ver)

Table 3.1.25 Switching characteristics (USB ports) ($V_{CC} = 3.00$ to 5.25 V, $V_{SS} = 0$ V, $T_a = -20$ to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$t_{fr}(D+/D-)$	USB full-speed output rising time	$CL = 50$ pF	4		20	ns
$t_{ff}(D+/D-)$	USB full-speed output falling time	$CL = 50$ pF	4		20	ns
$t_{frfm}(D+/D-)$	USB full-speed ports rising/falling ratio	$t_{fr}(D+/D-)/t_{ff}(D+/D-)$	90		111.11	%
$V_{crs}(D+/D-)$	USB output signal cross-over voltage		1.3		2.0	V

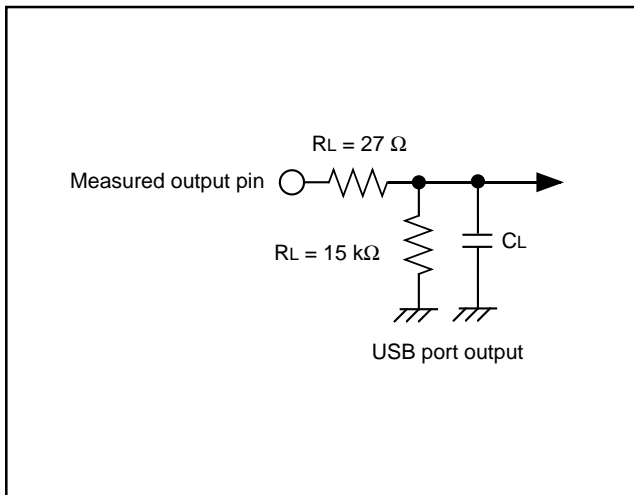


Fig. 3.1.5 USB output switching characteristics measurement circuit (1) for D0-

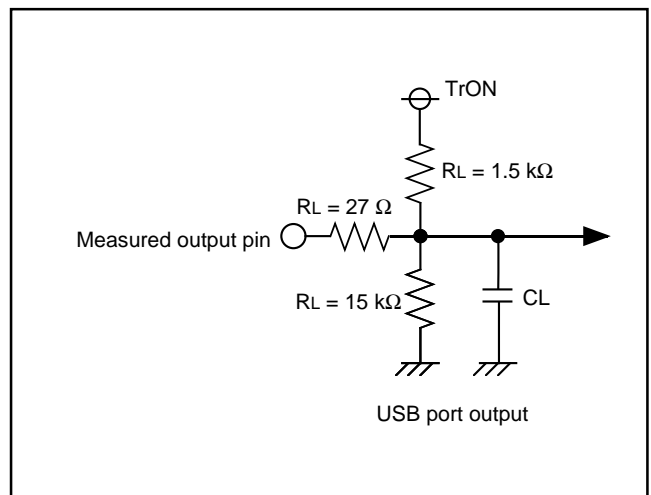


Fig. 3.1.6 USB output switching characteristics measurement circuit (2) for D0+

APPENDIX

3.1 Electrical characteristics

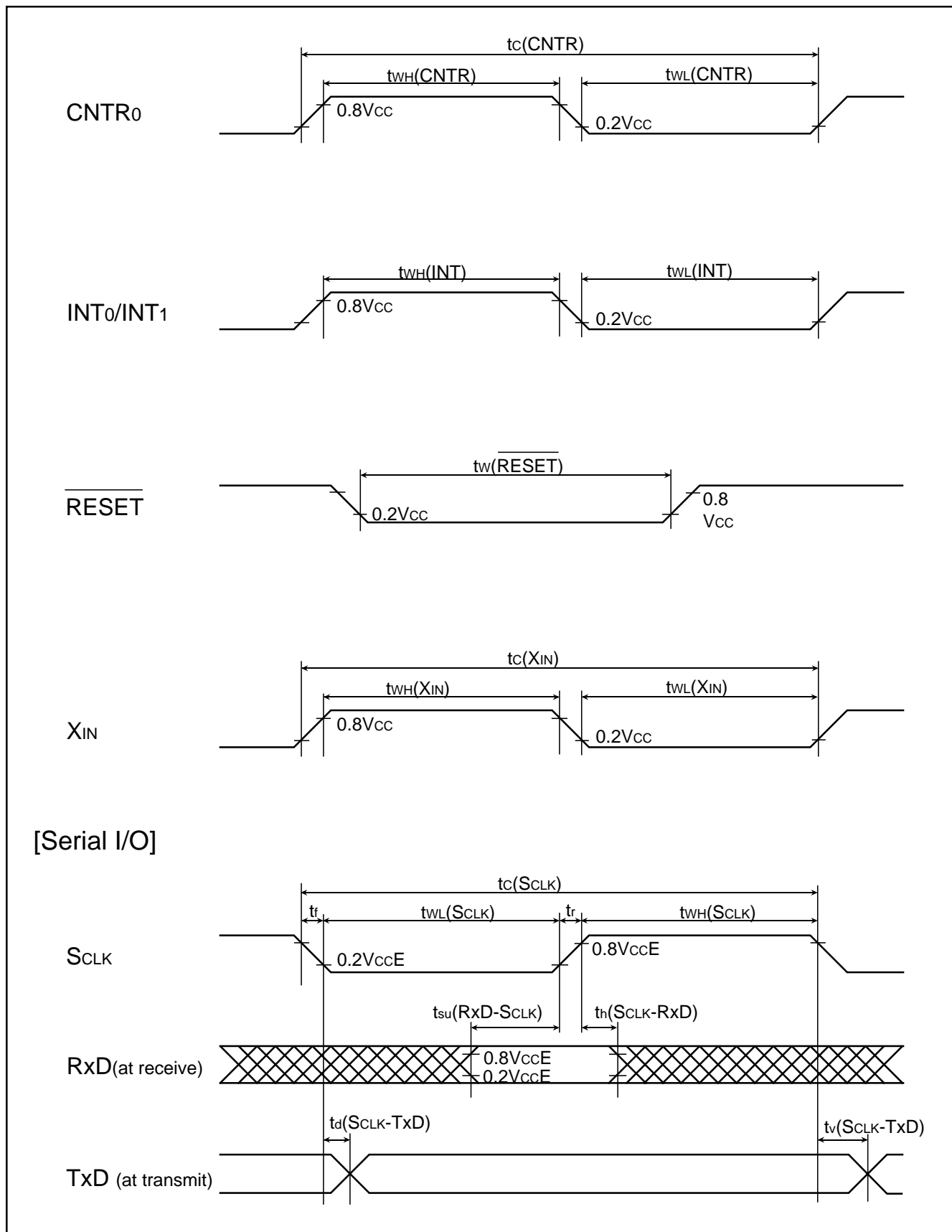
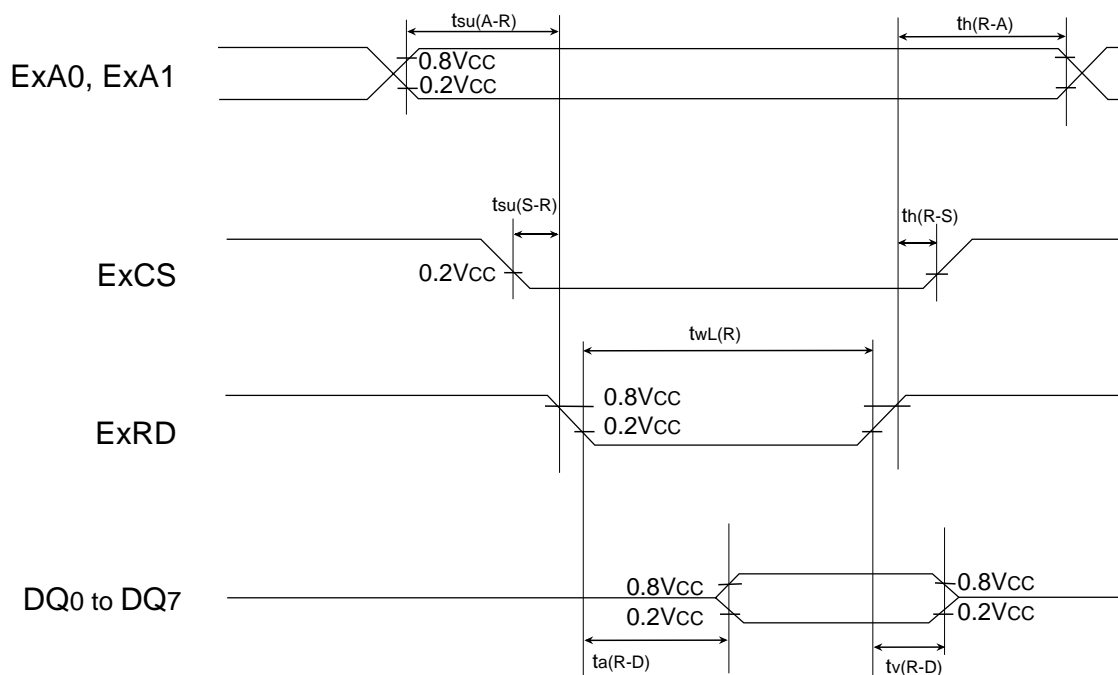


Fig. 3.1.7 Timing chart (1)

● Timing chart

[EXB <CPU channel mode>]

< Read >



< Write >

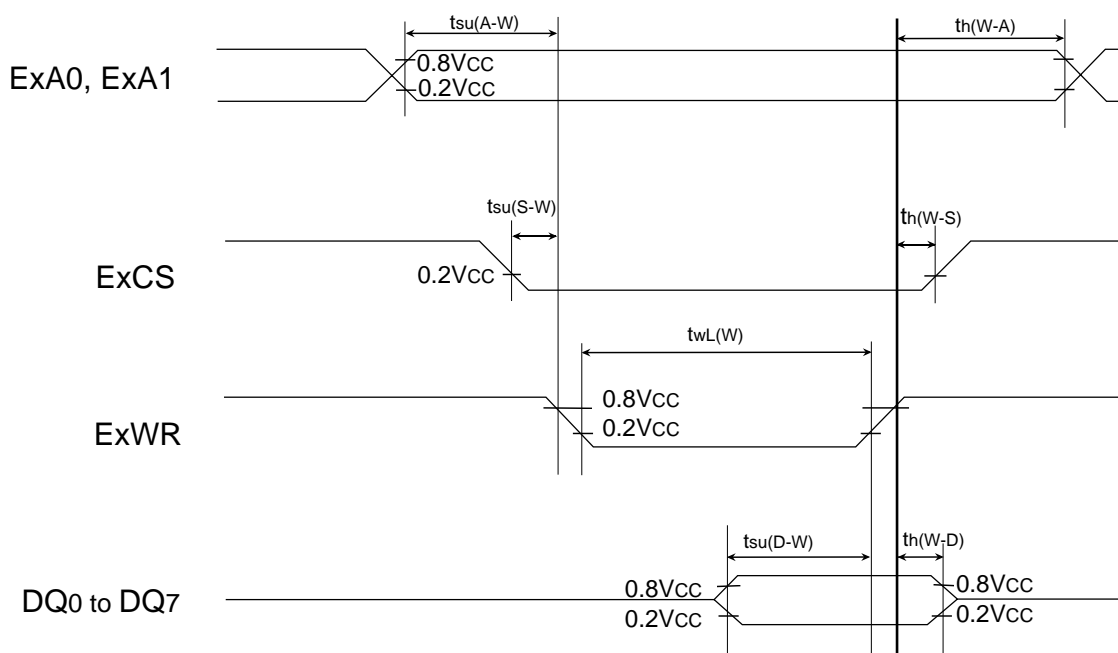


Fig. 3.1.8 Timing chart (2)

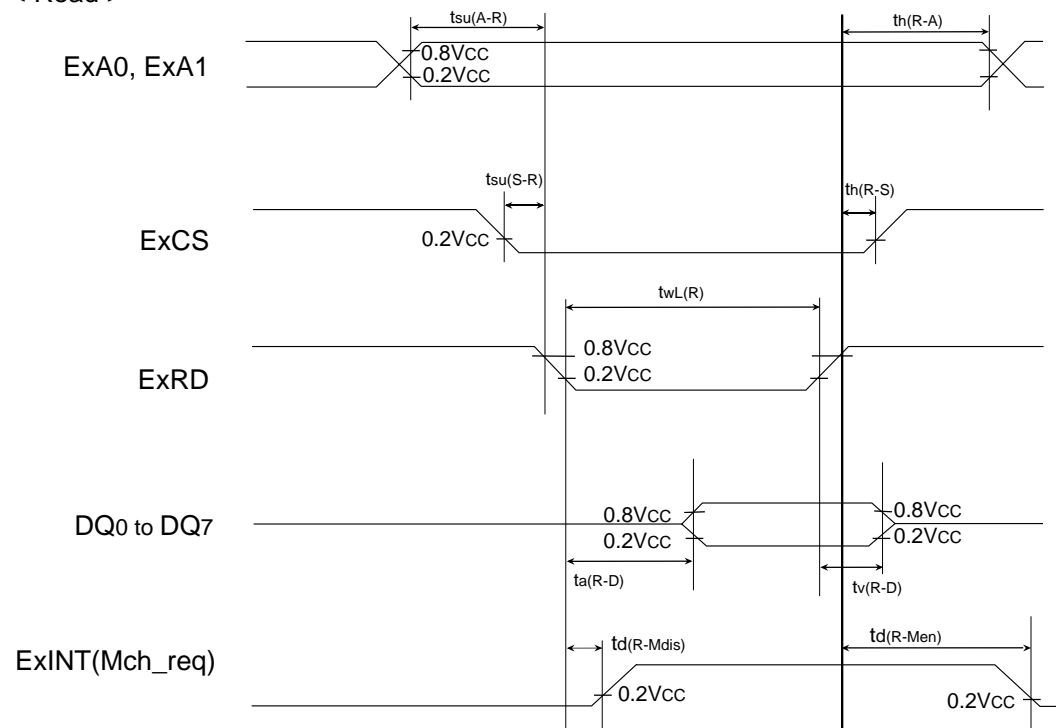
APPENDIX

3.1 Electrical characteristics

● Timing chart

[EXB <Memory channel mode, Normal port function>]

< Read >



< Write >

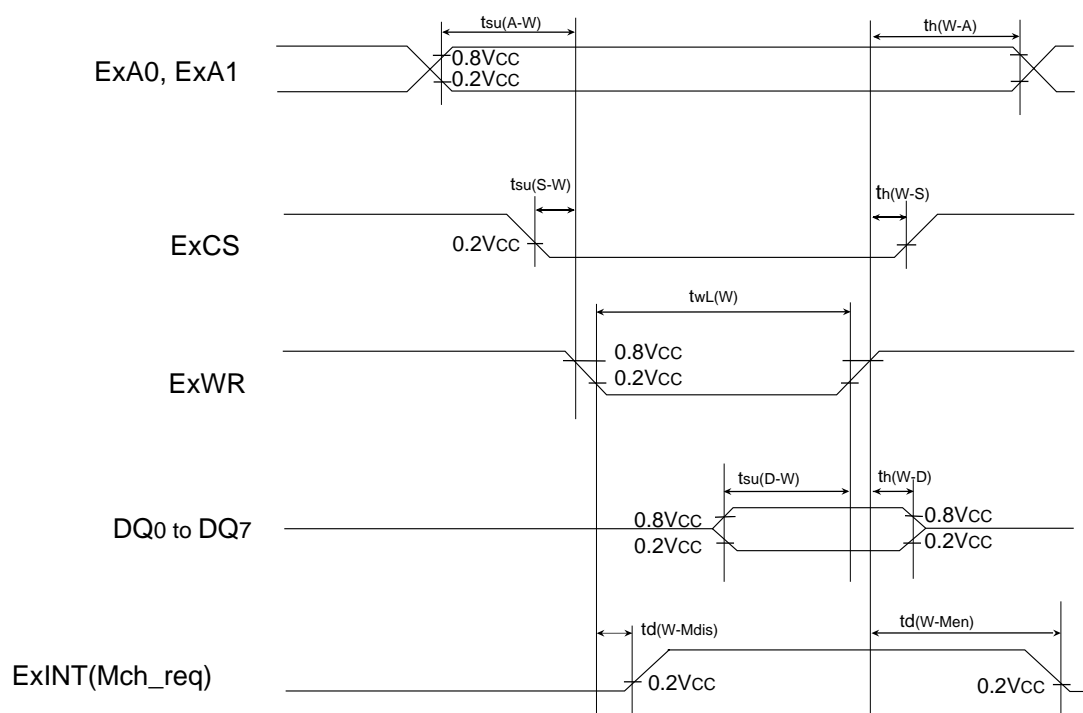
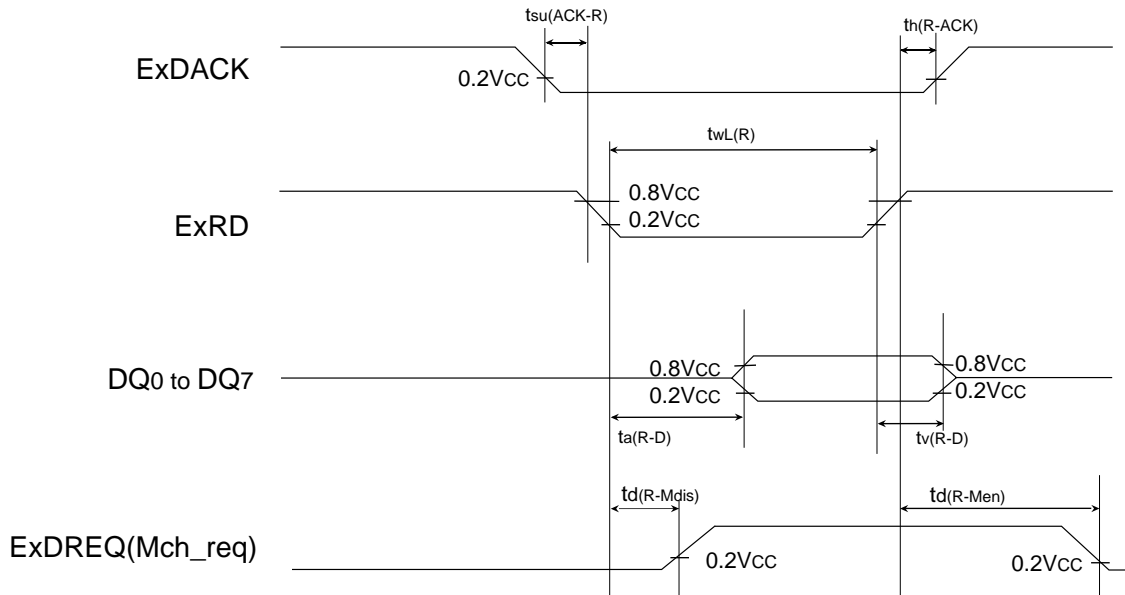


Fig. 3.1.9 Timing chart (3)

● Timing chart

[EXB <Memory channel mode, DMA interface pin function,
Read and write signals used together mode>]

< Read >



< Write >

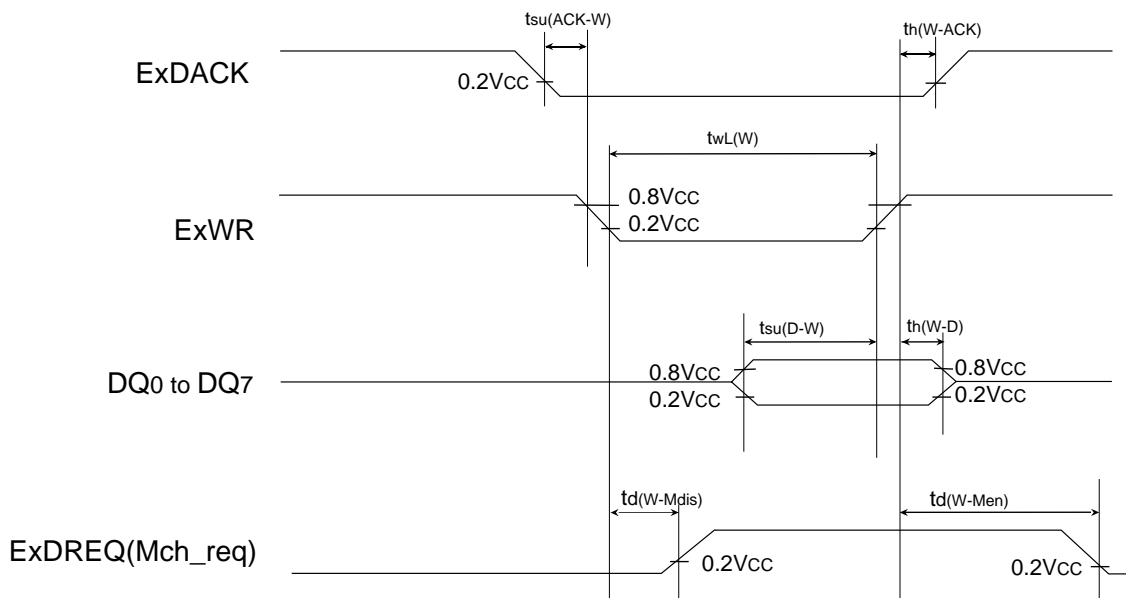


Fig. 3.1.10 Timing chart (4)

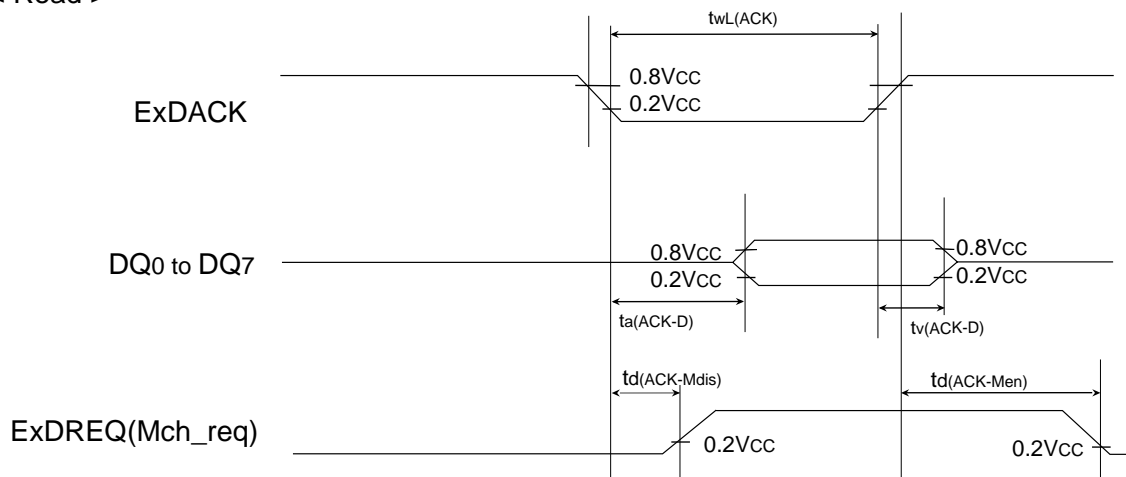
APPENDIX

3.1 Electrical characteristics

● Timing chart

[EXB <Memory channel mode, DMA interface pin function,
Read and write signals not required mode>]

< Read >



< Write >

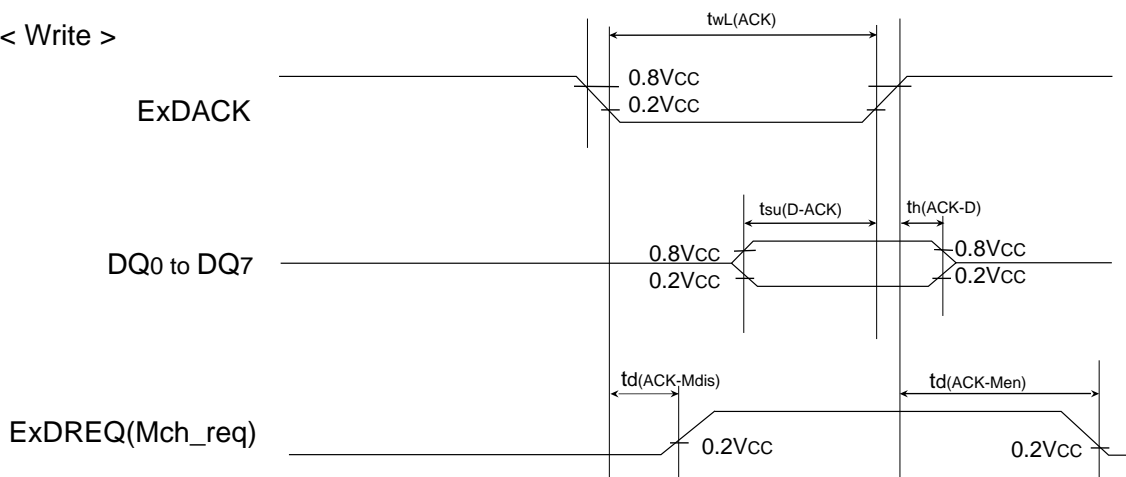
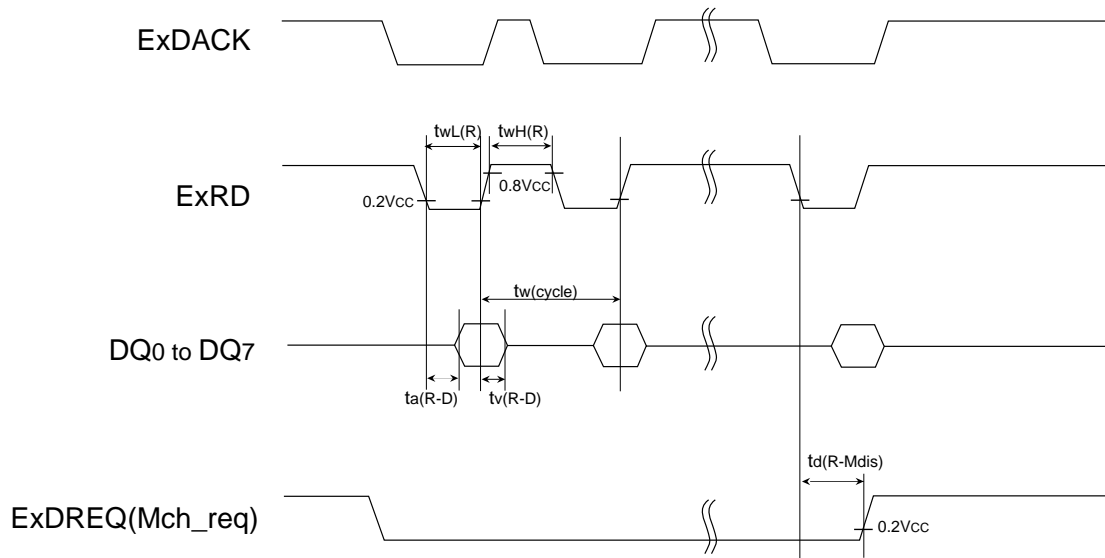


Fig. 3.1.11 Timing chart (5)

● Timing chart

[EXB <Memory channel mode, Burst transfer>]

< Read >



< Write >

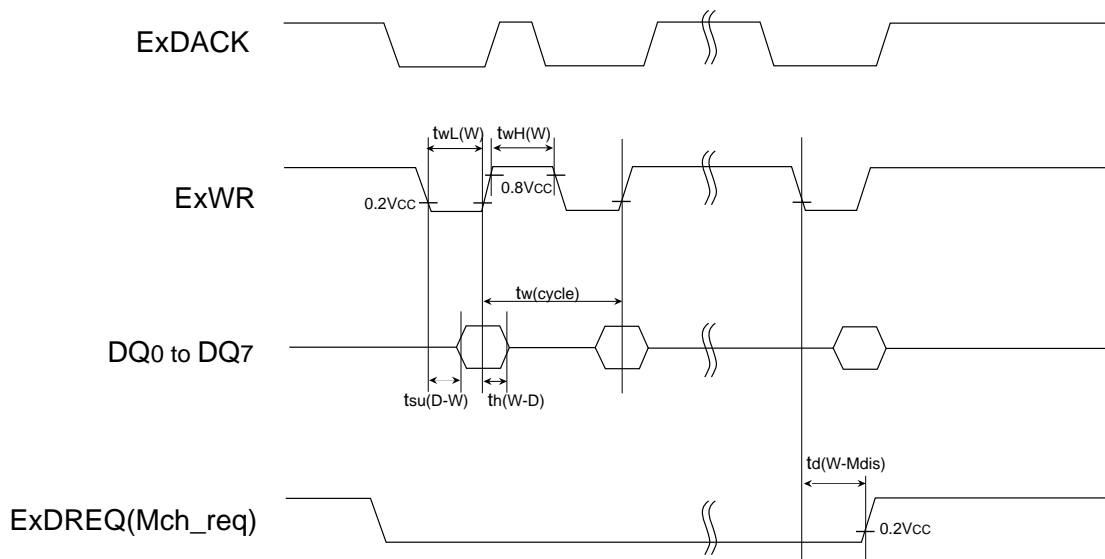


Fig. 3.1.12 Timing chart (6)

APPENDIX

3.2 Standard characteristics

3.2 Standard characteristics

There are no information in this issue.

3.3 Notes on use

3.3.1 Notes on input and output ports

(1) Modifying output data with bit managing instruction

When the port latch of an I/O port is modified with the bit managing instruction*¹, the value of the unspecified bit may be changed.

● Reason

The bit managing instructions are read-modify-write form instructions for reading and writing data by a byte unit. Accordingly, when these instructions are executed on a bit of the port latch of an I/O port, the following is executed to all bits of the port latch.

- As for bit which is set for input port:

The pin state is read in the CPU, and is written to this bit after bit managing.

- As for bit which is set for output port:

The bit value is read in the CPU, and is written to this bit after bit managing.

Note the following:

- Even when a port which is set as an output port is changed for an input port, its port latch holds the output data.
- As for a bit of which is set for an input port, its value may be changed even when not specified with a bit managing instruction in case where the pin state differs from its port latch contents.

*¹ Bit managing instructions: **SEB** and **CLB** instructions

APPENDIX

3.3 Notes on use

3.3.2 Termination of unused pins

(1) Terminate unused pins

① I/O ports :

- Set the I/O ports for the input mode and connect them to VCC or VSS through each resistor of 1 k Ω to 10 k Ω .
Set the I/O ports for the output mode and open them at "L" or "H".
- When opening them in the output mode, the input mode of the initial status remains until the mode of the ports is switched over to the output mode by the program after reset. Thus, the potential at these pins is undefined and the power source current may increase in the input mode. With regard to an effects on the system, thoroughly perform system evaluation on the user side.
- Since the direction register setup may be changed because of a program runaway or noise, set direction registers by program periodically to increase the reliability of program.

(2) Termination remarks

① I/O ports :

Do not open in the input mode.

● Reason

- The power source current may increase depending on the first-stage circuit.
- An effect due to noise may be easily produced as compared with proper termination shown on the above.

② I/O ports :

When setting for the input mode, do not connect to VCC or VSS directly.

● Reason

If the direction register setup changes for the output mode because of a program runaway or noise, a short circuit may occur between a port and VCC (or VSS).

③ I/O ports :

When setting for the input mode, do not connect multiple ports in a lump to VCC or VSS through a resistor.

● Reason

If the direction register setup changes for the output mode because of a program runaway or noise, a short circuit may occur between ports.

- At the termination of unused pins, perform wiring at the shortest possible distance (20 mm or less) from microcomputer pins.

3.3.3 Notes on interrupts

(1) Change of relevant register settings

When the setting of the following registers or bits is changed, the interrupt request bit may be set to "1". When not requiring the interrupt occurrence synchronized with these setting, take the following sequence.

- Interrupt edge selection register (address $0FF3_{16}$)
- Timer X mode register (address 23_{16})

Set the above listed registers or bits as the following sequence.

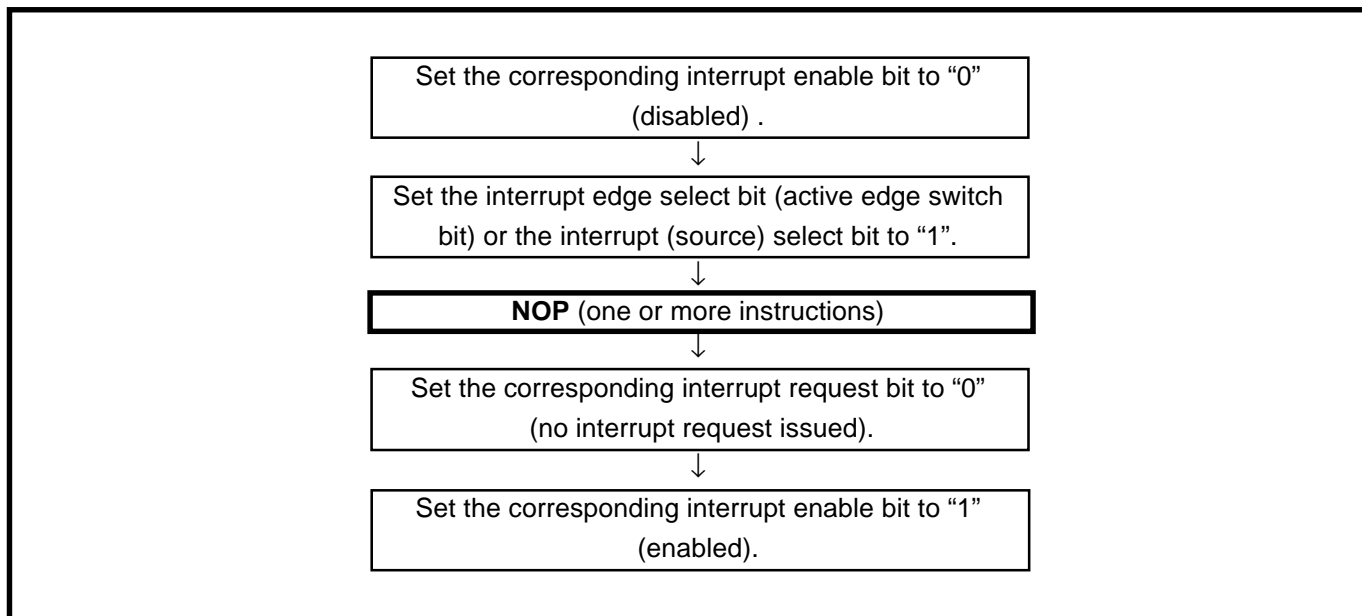


Fig. 3.3.1 Sequence of changing relevant register

■ Reason

When setting the following, the interrupt request bit may be set to "1".

- When setting external interrupt active edge
Concerned register: Interrupt edge selection register (address $0FF3_{16}$)
Timer X mode register (address 23_{16})

APPENDIX

3.3 Notes on use

(2) Check of interrupt request bit

- When executing the **BBC** or **BBS** instruction to an interrupt request bit of an interrupt request register immediately after this bit is set to “0” by using a data transfer instruction, execute one or more instructions before executing the **BBC** or **BBS** instruction.

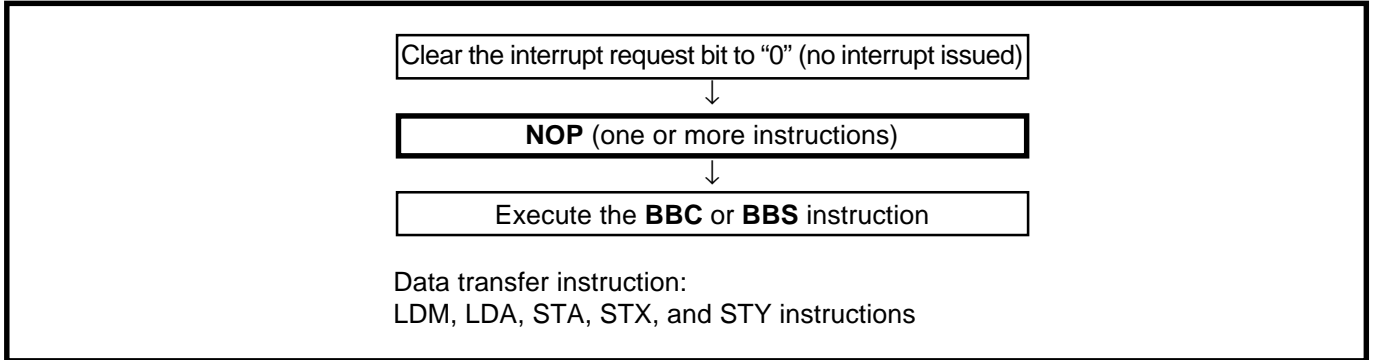


Fig. 3.3.2 Sequence of check of interrupt request bit

■ Reason

If the BBC or BBS instruction is executed immediately after an interrupt request bit of an interrupt request register is cleared to “0”, the value of the interrupt request bit before being cleared to “0” is read.

3.3.4 Notes on timer

- If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is $1/(n+1)$.
- When switching the count source by the timer 12 and X count source selection bits, the value of timer count is altered in unconsiderable amount owing to generating of thin pulses in the count input signals.
Therefore, select the timer count source before set the value to the prescaler and the timer.

3.3.5 Notes on serial I/O

(1) Notes when selecting clock synchronous serial I/O (Serial I/O)

① Stop of transmission operation

Clear the serial I/O enable bit and the transmit enable bit to "0" (Serial I/O and transmit disabled).

● Reason

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O enable bit is cleared to "0" (Serial I/O disabled), the internal transmission is running (in this case, since pins TxD, RxD, SCLK, and SRDY function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register in this state, data starts to be shifted to the transmit shift register. When the serial I/O enable bit is set to "1" at this time, the data during internally shifting is output to the TxD pin and an operation failure occurs.

② Stop of receive operation

Clear the receive enable bit to "0" (receive disabled), or clear the serial I/O enable bit to "0" (Serial I/O disabled).

③ Stop of transmit/receive operation

Clear the transmit enable bit and receive enable bit to "0" simultaneously (transmit and receive disabled).

(when data is transmitted and received in the clock synchronous serial I/O mode, any one of data transmission and reception cannot be stopped.)

● Reason

In the clock synchronous serial I/O mode, the same clock is used for transmission and reception. If any one of transmission and reception is disabled, a bit error occurs because transmission and reception cannot be synchronized.

In this mode, the clock circuit of the transmission circuit also operates for data reception. Accordingly, the transmission circuit does not stop by clearing only the transmit enable bit to "0" (transmit disabled). Also, the transmission circuit is not initialized by clearing the serial I/O enable bit to "0" (Serial I/O disabled) (refer to (1) ①).

APPENDIX

3.3 Notes on use

(2) Notes when selecting clock asynchronous serial I/O (Serial I/O)

① Stop of transmission operation

Clear the transmit enable bit to “0” (transmit disabled).

● Reason

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O enable bit is cleared to “0” (Serial I/O disabled), the internal transmission is running (in this case, since pins TxD, RxD, SCLK, and SRDY function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register in this state, data starts to be shifted to the transmit shift register. When the serial I/O enable bit is set to “1” at this time, the data during internally shifting is output to the TxD pin and an operation failure occurs.

② Stop of receive operation

Clear the receive enable bit to “0” (receive disabled).

③ Stop of transmit/receive operation

Only transmission operation is stopped.

Clear the transmit enable bit to “0” (transmit disabled).

● Reason

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O enable bit is cleared to “0” (Serial I/O disabled), the internal transmission is running (in this case, since pins TxD, RxD, SCLK, and SRDY function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register in this state, data starts to be shifted to the transmit shift register. When the serial I/O enable bit is set to “1” at this time, the data during internally shifting is output to the TxD pin and an operation failure occurs.

Only receive operation is stopped.

Clear the receive enable bit to “0” (receive disabled).

(3) $\overline{\text{SRDY}}$ output of reception side (Serial I/O)

When signals are output from the $\overline{\text{SRDY}}$ pin on the reception side by using an external clock in the clock synchronous serial I/O mode, set all of the receive enable bit, the $\overline{\text{SRDY}}$ output enable bit, and the transmit enable bit to “1” (transmit enabled).

(4) Setting serial I/O control register again (Serial I/O)

Set the serial I/O control register again after the transmission and the reception circuits are reset by clearing both the transmit enable bit and the receive enable bit to “0.”

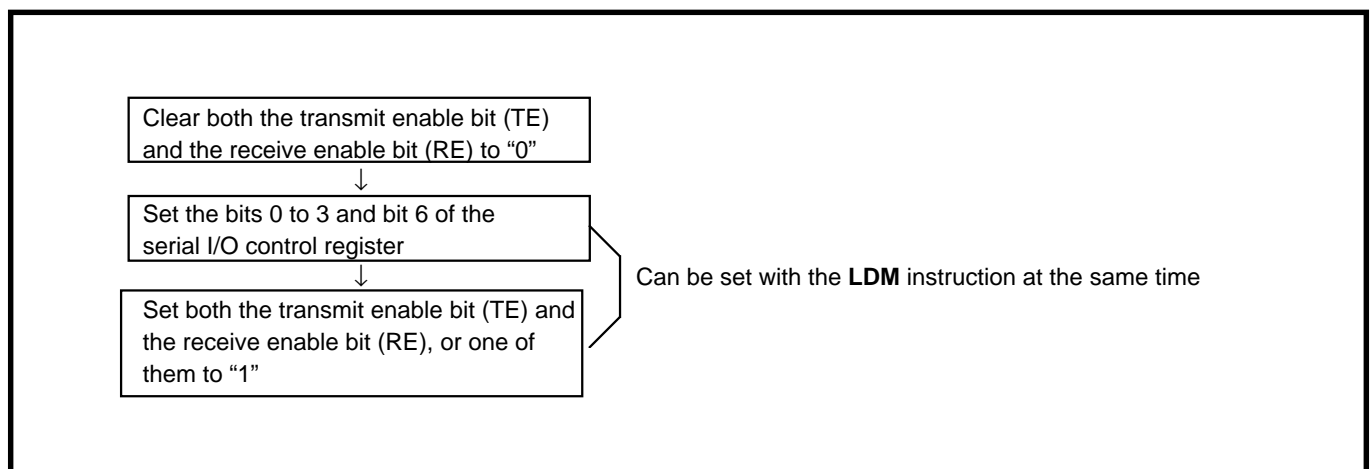


Fig. 3.3.3 Sequence of setting serial I/O control register again

(5) Data transmission control with referring to transmit shift register completion flag (Serial I/O)

The transmit shift register completion flag changes from “1” to “0” with a delay of 0.5 to 1.5 shift clocks. When data transmission is controlled with referring to the flag after writing the data to the transmit buffer register, note the delay.

(6) Transmission control when external clock is selected (Serial I/O)

When an external clock is used as the synchronous clock for data transmission, set the transmit enable bit to “1” at “H” of the SCLK input level. Also, write the transmit data to the transmit buffer register (serial I/O shift register) at “H” of the SCLK input level.

(7) Transmit interrupt request when transmit enable bit is set (Serial I/O)

When the transmit interrupt is used, set the transmit interrupt enable bit to transmit enabled as shown in the following sequence.

- ① Set the interrupt enable bit to “0” (disabled) with CLB instruction.
- ② Prepare serial I/O for transmission/reception.
- ③ Set the interrupt request bit to “0” with CLB instruction after 1 or more instruction has been executed.
- ④ Set the interrupt enable bit to “1” (enabled).

● Reason

When the transmission enable bit is set to “1”, the transmit buffer empty flag and transmit shift register completion flag are set to “1”. The interrupt request is generated and the transmission interrupt bit is set regardless of which of the two timings listed below is selected as the timing for the transmission interrupt to be generated.

- Transmit buffer empty flag is set to “1”
- Transmit shift register completion flag is set to “1”

3.3.6 Notes on USB function

(1) Port pins (D0+, D0-) treatment

- The USB specification requires a driver-impedance 28 to 44 Ω . In order to meet the USB specification impedance requirements, connect a resistor (27 Ω recommended) in series to the USB port pins. In addition, in order to reduce the ringing and control the falling/rising timing and a crossover point, connect a capacitor between the USB port pins and the Vss pin if necessary. The values and structure of those peripheral elements depend on the impedance characteristics and the layout of the printed circuit board. Accordingly, evaluate your system and observe waveforms before actual use and decide use of elements and the values of resistors and capacitors.
- Make sure the USB D+/D- lines do not cross any other wires. Keep a large GND area to protect the USB lines. Also, make sure you use a USB specification compliant connector for the connection.

(2) USBV_{REF} pin treatment (Noise Elimination)

- Connect a capacitor between the USBV_{REF} pin and the Vss pin. The capacitor should have a 2.2 μ F capacitor (electrolytic capacitor) and a 0.1 μ F capacitor (ceramic type capacitor) connected in parallel.
- In Vcc = 3.0 to 3.6 V operation, connect the USBV_{REF} pin directly to the Vcc pin in order to supply power to the USB port circuit. In addition, you will need to disable the built-in USB reference voltage circuit in this operation (set bit 4 of the USB control register to “0”). If you are using the bus powered supply in this condition, the DC-DC converter must be placed outside the MCU.
- In Vcc = 4.00 to 5.25 V operation, do not connect the external DC-DC converter to the USBV_{REF} pin. Use the built-in USB reference voltage circuit.

APPENDIX

3.3 Notes on use

3.3.7 Notes on A-D converter

(1) Analog input pin

Make the signal source impedance for analog input low, or equip an analog input pin with an external capacitor of 0.01 μF to 1 μF . Further, be sure to verify the operation of application products on the user side.

● Reason

An analog input pin includes the capacitor for analog voltage comparison. Accordingly, when signals from signal source with high impedance are input to an analog input pin, charge and discharge noise generates. This may cause the A-D conversion precision to be worse.

(2) Clock frequency during A-D conversion

The comparator consists of a capacity coupling, and a charge of the capacity will be lost if the clock frequency is too low. Thus, make sure the following during an A-D conversion.

- $f(X_{IN})$ is 500 kHz or more
- Do not execute the **STP** instruction

3.3.8 Notes on watchdog timer

- Make sure that the watchdog timer does not underflow while waiting Stop release, because the watchdog timer keeps counting during that term.

- When the STP instruction disable bit has been set to “1”, it is impossible to switch it to “0” by a program

3.3.9 Notes on RESET pin

Connecting capacitor

In case where the RESET signal rise time is long, connect a ceramic capacitor or others across the RESET pin and the VSS pin. Use a 1000 pF or more capacitor for high frequency use. When connecting the capacitor, note the following :

- Make the length of the wiring which is connected to a capacitor as short as possible.
- Be sure to verify the operation of application products on the user side.

● Reason

If the several nanosecond or several ten nanosecond impulse noise enters the RESET pin, it may cause a microcomputer failure.

3.3.10 Notes on PLL

- 6 MHz or 12 MHz external oscillator can be connected as an input reference clock ($f(X_{IN})$). When using the frequency synthesized clock function, we recommend using the fastest frequency possible of $f(X_{IN})$ as an input clock reference for the PLL.
- When enabling PLL operation from PLL disabled status (disabled when reset), set the USB clock select bit of USBCON to “0” ($f(X_{IN})$) to operate with the main clock ($f(X_{IN})$).
- When supplying f_{VCO} to the USB block after setting PLL operation enable bit to “1” (PLL enabled), wait for the oscillation stable time (1 ms or less) of PLL to avoid any instability caused by the clock, then set USB clock select bit to “1” (USB clock).
- When selecting f_{SYN} as an internal system clock, f_{USB} must be 48 MHz.
- When selecting f_{SYN} as an internal system clock, change the system clock selection bit to main clock ($f(X_{IN})$) before executing STP instruction. It is because the following are needed for the low-power consumption:
 - f_{USB} must be stopped by disabling PLL operation in Stop mode.
 - The timer 1 for waiting oscillation stabilization when returning from Stop mode will require the input count source.

3.3.11 Notes on stand-by function**(1) Notes on using stop mode****■Register setting**

Since values of the prescaler 12 and Timer 1 are automatically reloaded when returning from the stop mode, set them again, respectively. (When the oscillation stabilizing time set after STP instruction released bit is "0")

■Clock restoration

When the main clock side is set as a system clock, the oscillation stabilizing time for approximately 8,000 cycles of the X_{IN} input is reserved at restoration from the stop mode.

(2) Notes on stand-by function

In stand-by state*¹ for low-power dissipation, do not make input levels of an input port and an I/O port "undefined".

Pull-up (connect the port to V_{CC}) these ports through a resistor.

When determining a resistance value, note the following points:

- External circuit
- Variation of output levels during the ordinary operation

When using built-in pull-up resistor, note on varied current values.

- When setting as an input port: Fix its input level
- When setting as an output port: Prevent current from flowing out to external

● Reason

The potential which is input to the input buffer in a microcomputer is unstable in the state that input levels of an input port and an I/O port are "undefined". This may cause power source current.

*¹ stand-by state : the stop mode by executing the **STP** instruction
the wait mode by executing the **WIT** instruction

3.3.12 Notes on CPU rewrite mode**(1) Operation speed**

During CPU rewrite mode, set the internal clock ϕ 1.5 MHz or less using the system clock division ratio selection bits (bits 6 and 7 of address 003B₁₆).

(2) Instructions inhibited against use

The instructions which refer to the internal data of the flash memory cannot be used during the CPU rewrite mode .

(3) Interrupts inhibited against use

The interrupts cannot be used during the CPU rewrite mode because they refer to the internal data of the flash memory.

(4) Watchdog timer

In case of the watchdog timer has been running already, the internal reset generated by watchdog timer underflow does not happen, because of watchdog timer is always clearing during program or erase operation.

(5) Reset

Reset is always valid. In case of $CNV_{SS} = "H"$ when reset is released, boot mode is active. So the program starts from the address contained in address FFFC₁₆ and FFFD₁₆ in boot ROM area.

APPENDIX

3.3 Notes on use

3.3.13 Notes on programming

(1) Processor status register

① Initializing of processor status register

Flags which affect program execution must be initialized after a reset.

In particular, it is essential to initialize the T and D flags because they have an important effect on calculations.

● Reason

After a reset, the contents of the processor status register (PS) are undefined except for the I flag which is "1".

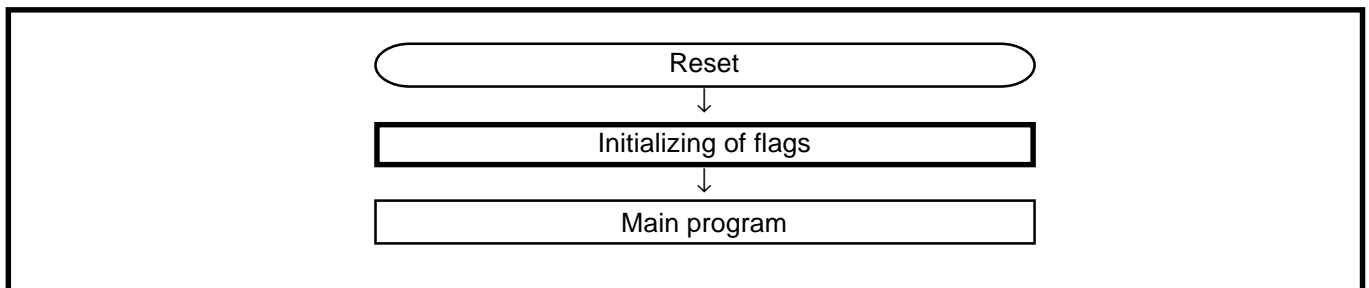


Fig. 3.3.4 Initialization of processor status register

② How to reference the processor status register

To reference the contents of the processor status register (PS), execute the **PHP** instruction once then read the contents of (S+1). If necessary, execute the **PLP** instruction to return the PS to its original status.

A **NOP** instruction should be executed after every **PLP** instruction.

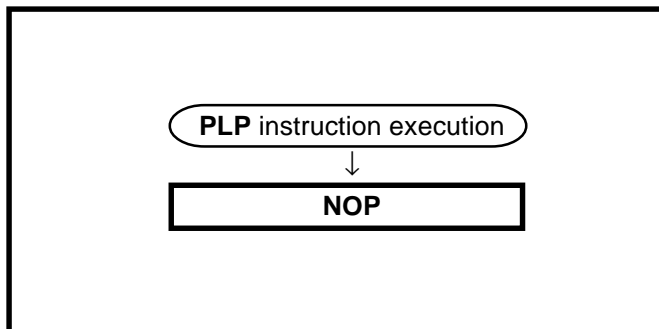


Fig. 3.3.5 Sequence of PLP instruction execution

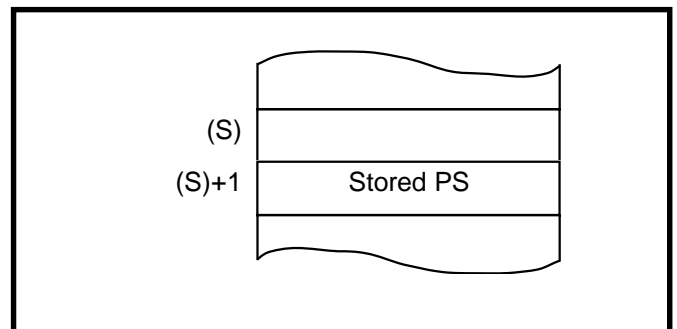


Fig. 3.3.6 Stack memory contents after PHP instruction execution

(2) BRK instruction

① Interrupt priority level

When the BRK instruction is executed with the following conditions satisfied, the interrupt execution is started from the address of interrupt vector which has the highest priority.

- Interrupt request bit and interrupt enable bit are set to "1".
- Interrupt disable flag (I) is set to "1" to disable interrupt.

(3) Decimal calculations**① Execution of decimal calculations**

The **ADC** and **SBC** are the only instructions which will yield proper decimal notation, set the decimal mode flag (D) to “1” with the **SED** instruction. After executing the **ADC** or **SBC** instruction, execute another instruction before executing the **SEC**, **CLC**, or **CLD** instruction.

② Notes on status flag in decimal mode

When decimal mode is selected, the values of three of the flags in the status register (the N, V, and Z flags) are invalid after a **ADC** or **SBC** instruction is executed.

The carry flag (C) is set to “1” if a carry is generated as a result of the calculation, or is cleared to “0” if a borrow is generated. To determine whether a calculation has generated a carry, the C flag must be initialized to “0” before each calculation. To check for a borrow, the C flag must be initialized to “1” before each calculation.

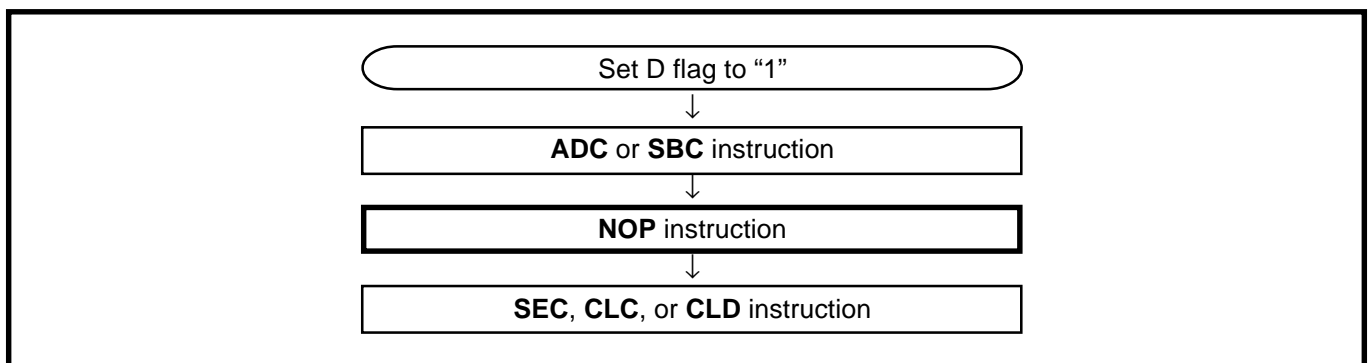


Fig. 3.3.7 Status flag at decimal calculations

(4) JMP instruction

When using the **JMP** instruction in indirect addressing mode, do not specify the last address on a page as an indirect address.

(5) Multiplication and Division Instructions

- The index X mode (T) and the decimal mode (D) flags do not affect the **MUL** and **DIV** instruction.
- The execution of these instructions does not change the contents of the processor status register.

(6) Ports

The contents of the port direction registers cannot be read. The following cannot be used:

- The data transfer instruction (**LDA**, etc.)
- The operation instruction when the index X mode flag (T) is “1”
- The addressing mode which uses the value of a direction register as an index
- The bit-test instruction (**BBC** or **BBS**, etc.) to a direction register
- The read-modify-write instructions (**ROR**, **CLB**, or **SEB**, etc.) to a direction register.

Use instructions such as **LDM** and **STA**, etc., to set the port direction registers.

(7) Instruction Execution Time

The instruction execution time is obtained by multiplying the frequency of the internal clock f by the number of cycles needed to execute an instruction.

The number of cycles required to execute an instruction is shown in the list of machine instructions.

The frequency of the internal clock f is half of the X_{IN} frequency in high-speed mode.

APPENDIX

3.3 Notes on use

3.3.14 Notes on flash memory version

The CNVss pin is connected to the internal memory circuit block by a low-ohmic resistance, since it has the multiplexed function to be a programmable power source pin (V_{PP} pin) as well.

To improve the noise reduction, connect a track between CNVss pin and Vss pin or Vcc pin with 1 to 10 k Ω resistance.

The mask ROM version track of CNVss pin has no operational interference even if it is connected to Vss pin or Vcc pin via a resistor.

3.3.15 Electric Characteristic Differences Between Mask ROM and Flash Memory Version MCUs

There are differences in electric characteristics, operation margin, noise immunity, and noise radiation between Mask ROM and Flash Memory version MCUs due to the difference in the manufacturing processes. When manufacturing an application system with the Flash Memory version and then switching to use of the Mask ROM version, please perform sufficient evaluations for the commercial samples of the Mask ROM version.

3.4 Countermeasures against noise

Countermeasures against noise are described below. The following countermeasures are effective against noise in theory, however, it is necessary not only to take measures as follows but to evaluate before actual use.

3.4.1 Shortest wiring length

The wiring on a printed circuit board can function as an antenna which feeds noise into the microcomputer. The shorter the total wiring length (by mm unit), the less the possibility of noise insertion into a microcomputer.

(1) Package

Select the smallest possible package to make the total wiring length short.

● Reason

The wiring length depends on a microcomputer package. Use of a small package, for example QFP and not DIP, makes the total wiring length short to reduce influence of noise.

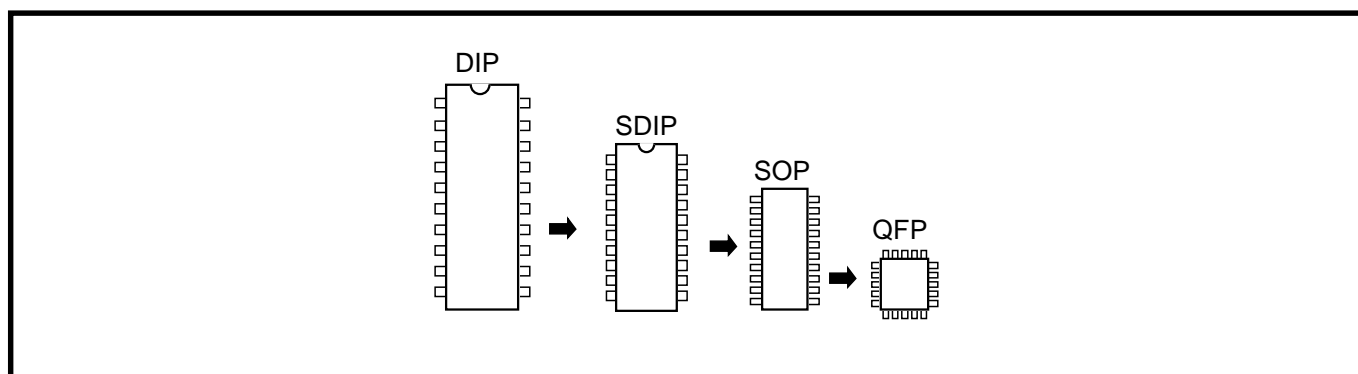


Fig. 3.4.1 Selection of packages

(2) Wiring for $\overline{\text{RESET}}$ pin

Make the length of wiring which is connected to the $\overline{\text{RESET}}$ pin as short as possible. Especially, connect a capacitor across the $\overline{\text{RESET}}$ pin and the Vss pin with the shortest possible wiring (within 20mm).

● Reason

The width of a pulse input into the $\overline{\text{RESET}}$ pin is determined by the timing necessary conditions. If noise having a shorter pulse width than the standard is input to the $\overline{\text{RESET}}$ pin, the reset is released before the internal state of the microcomputer is completely initialized. This may cause a program runaway.

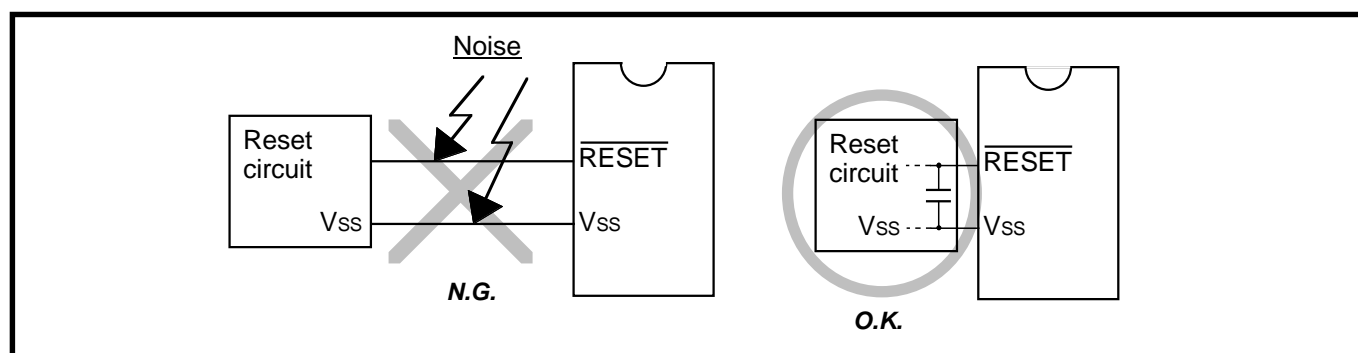


Fig. 3.4.2 Wiring for the $\overline{\text{RESET}}$ pin

APPENDIX

3.4 Countermeasures against noise

(3) Wiring for clock input/output pins

- Make the length of wiring which is connected to clock I/O pins as short as possible.
- Make the length of wiring (within 20 mm) across the grounding lead of a capacitor which is connected to an oscillator and the VSS pin of a microcomputer as short as possible.
- Separate the VSS pattern only for oscillation from other VSS patterns.

● Reason

If noise enters clock I/O pins, clock waveforms may be deformed. This may cause a program failure or program runaway. Also, if a potential difference is caused by the noise between the VSS level of a microcomputer and the VSS level of an oscillator, the correct clock will not be input in the microcomputer.

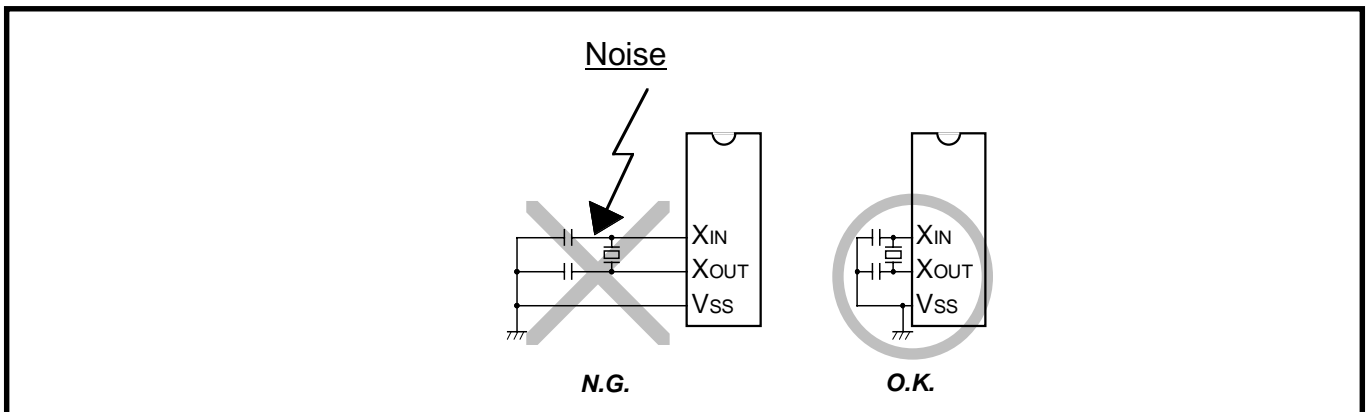


Fig. 3.4.3 Wiring for clock I/O pins

(4) Wiring to CNVss pin

Connect the CNVss pin to the VSS pin with the shortest possible wiring.

● Reason

The processor mode of a microcomputer is influenced by a potential at the CNVss pin. If a potential difference is caused by the noise between pins CNVss and VSS, the processor mode may become unstable. This may cause a microcomputer malfunction or a program runaway.

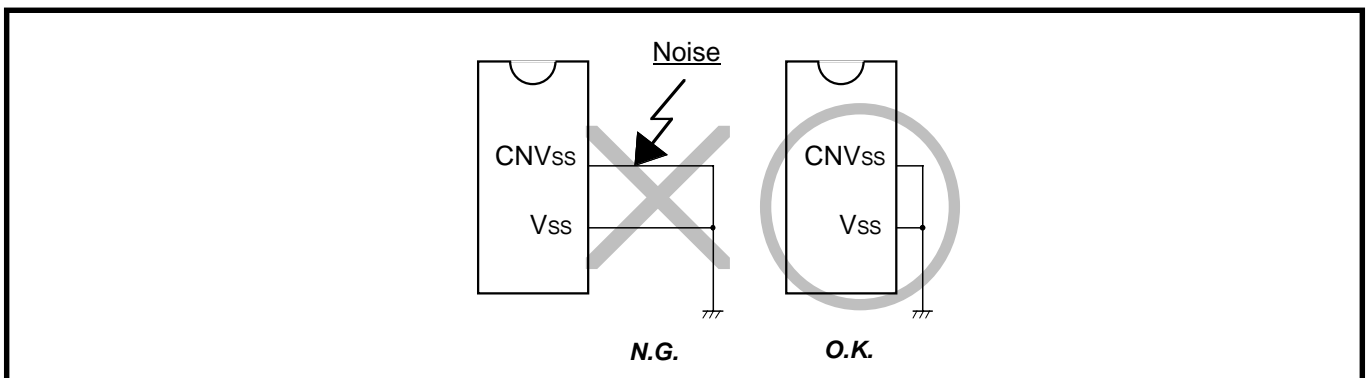


Fig. 3.4.4 Wiring for CNVss pin

(5) Wiring to VPP pin of Flash memory version

Connect an approximately 5 kΩ resistor to the VPP pin the shortest possible in series and also to the VSS pin. When not connecting the resistor, make the length of wiring between the VPP pin and the VSS pin the shortest possible.

Note: Even when a circuit which included an approximately 5 kΩ resistor is used in the Mask ROM version, the microcomputer operates correctly.

● Reason

The VPP pin of the flash memory version is the power source input pin for the built-in flash memory. When programming in the built-in flash memory, the impedance of the VPP pin is low to allow the electric current for writing flow into the flash memory. Because of this, noise can enter easily. If noise enters the VPP pin, abnormal instruction codes or data are read from the built-in flash memory, which may cause a program runaway.

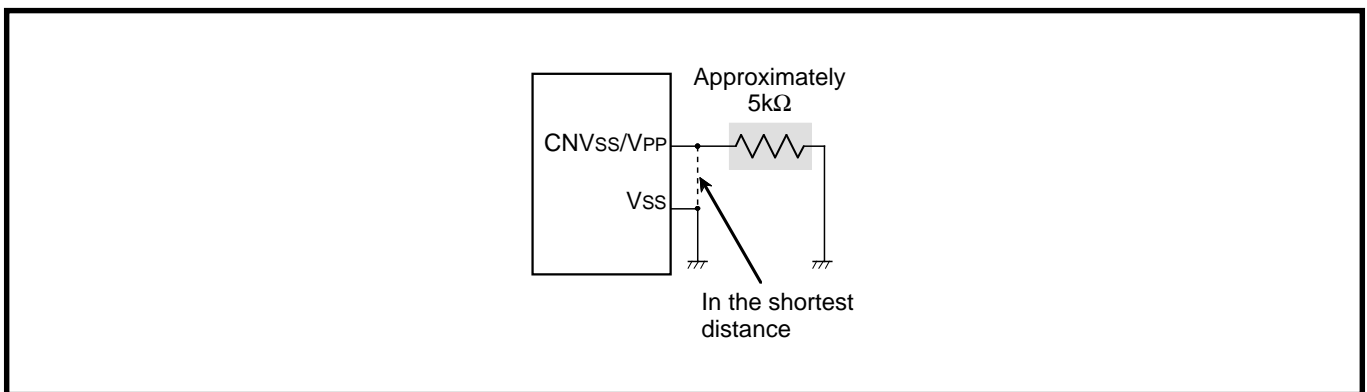


Fig. 3.4.5 Wiring for the VPP pin of the flash memory version

3.4.2 Connection of bypass capacitor across Vss line and Vcc line

Connect an approximately 0.1 μF bypass capacitor across the VSS line and the VCC line as follows:

- Connect a bypass capacitor across the VSS pin and the VCC pin at equal length.
- Connect a bypass capacitor across the VSS pin and the VCC pin with the shortest possible wiring.
- Use lines with a larger diameter than other signal lines for VSS line and VCC line.
- Connect the power source wiring via a bypass capacitor to the VSS pin and the VCC pin.

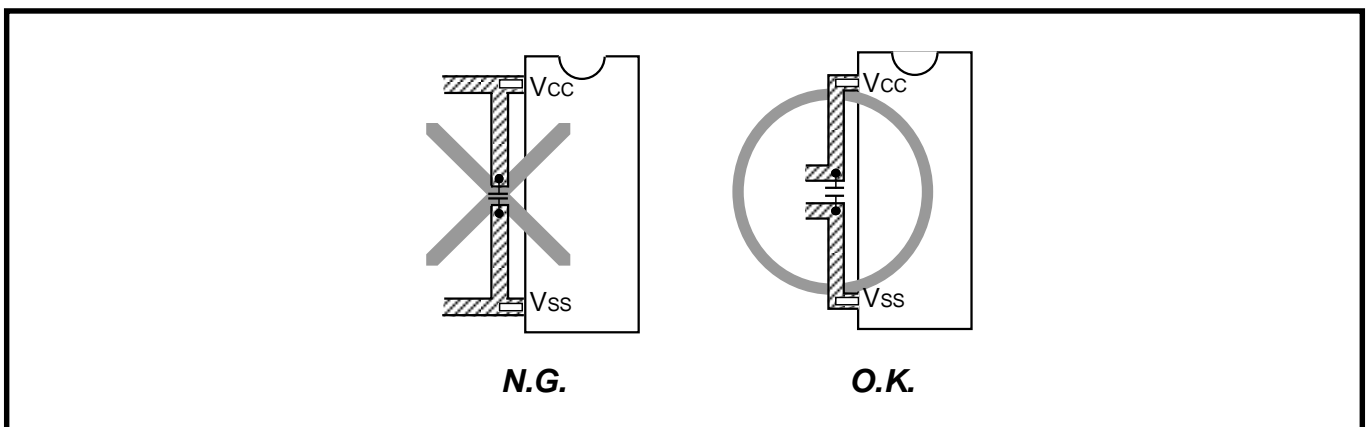


Fig. 3.4.6 Bypass capacitor across the Vss line and the Vcc line

APPENDIX

3.4 Countermeasures against noise

3.4.3 Wiring to analog input pins

- Connect an approximately $100\ \Omega$ to $1\ \text{k}\Omega$ resistor to an analog signal line which is connected to an analog input pin in series. Besides, connect the resistor to the microcomputer as close as possible.
- Connect an approximately $1000\ \text{pF}$ capacitor across the Vss pin and the analog input pin. Besides, connect the capacitor to the Vss pin as close as possible. Also, connect the capacitor across the analog input pin and the Vss pin at equal length.

● Reason

Signals which is input in an analog input pin (such as an A-D converter/comparator input pin) are usually output signals from sensor. The sensor which detects a change of event is installed far from the printed circuit board with a microcomputer, the wiring to an analog input pin is longer necessarily. This long wiring functions as an antenna which feeds noise into the microcomputer, which causes noise to an analog input pin.

If a capacitor between an analog input pin and the Vss pin is grounded at a position far away from the Vss pin, noise on the GND line may enter a microcomputer through the capacitor.

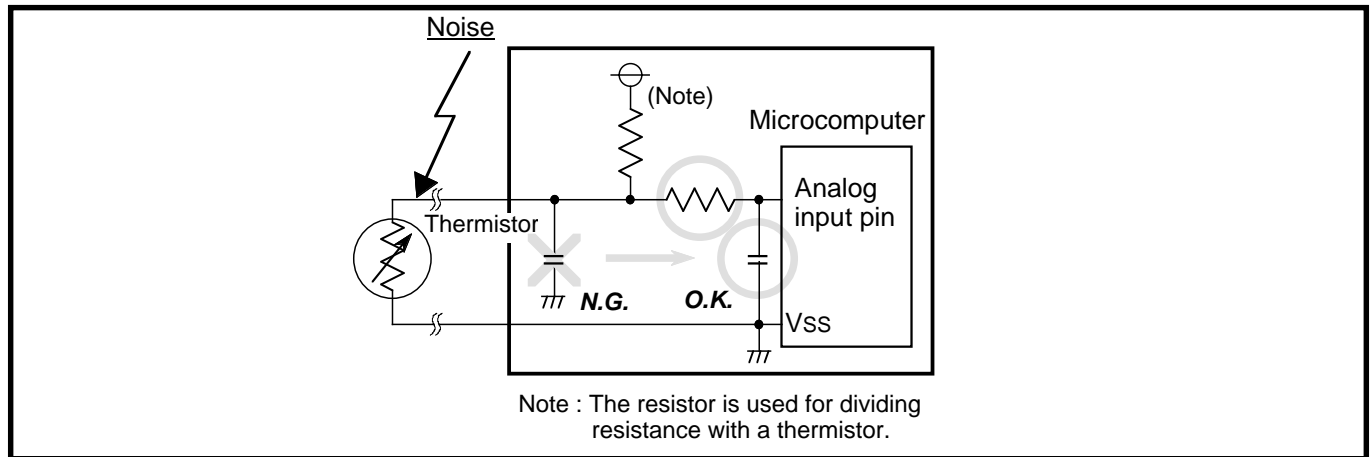


Fig. 3.4.7 Analog signal line and a resistor and a capacitor

3.4.4 Oscillator concerns

Take care to prevent an oscillator that generates clocks for a microcomputer operation from being affected by other signals.

(1) Keeping oscillator away from large current signal lines

Install a microcomputer (and especially an oscillator) as far as possible from signal lines where a current larger than the tolerance of current value flows.

● Reason

In the system using a microcomputer, there are signal lines for controlling motors, LEDs, and thermal heads or others. When a large current flows through those signal lines, strong noise occurs because of mutual inductance.

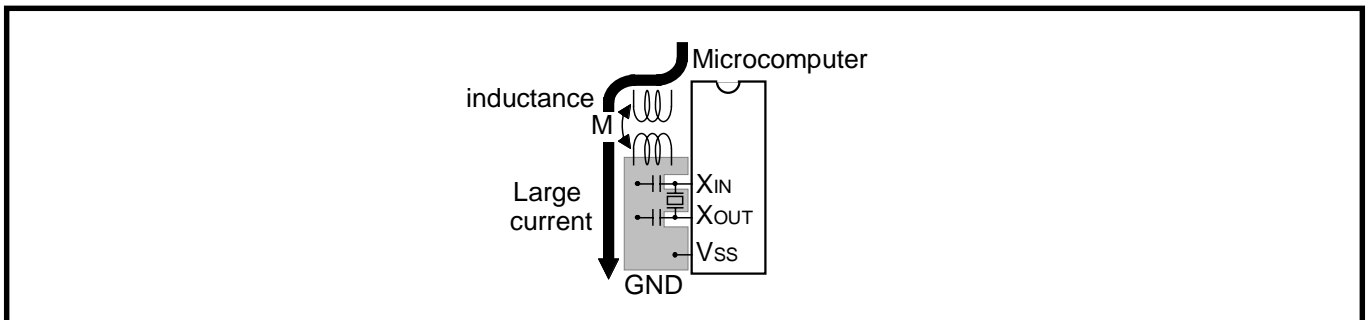


Fig. 3.4.8 Wiring for a large current signal line

(2) Installing oscillator away from signal lines where potential levels change frequently

Install an oscillator and a connecting pattern of an oscillator away from signal lines where potential levels change frequently. Also, do not cross such signal lines over the clock lines or the signal lines which are sensitive to noise.

● Reason

Signal lines where potential levels change frequently (such as the CNTR pin signal line) may affect other lines at signal rising edge or falling edge. If such lines cross over a clock line, clock waveforms may be deformed, which causes a microcomputer failure or a program runaway.

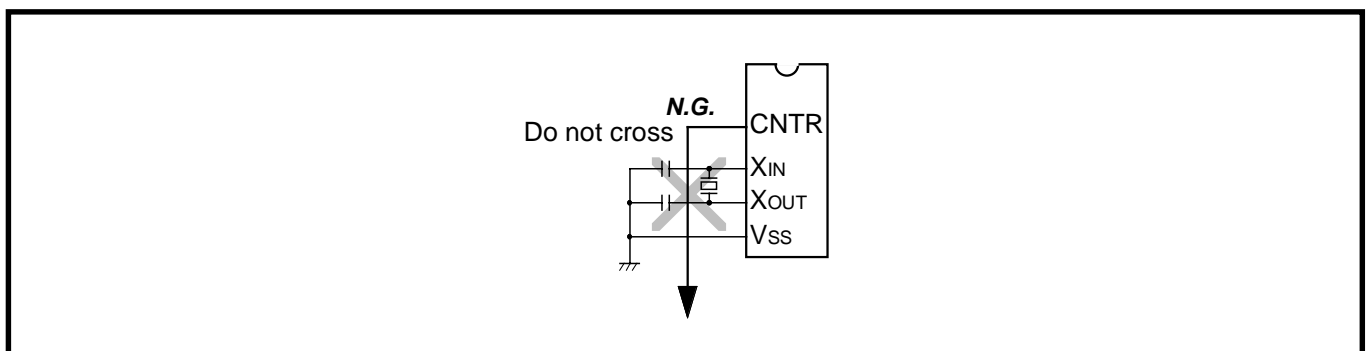


Fig. 3.4.9 Wiring of RESET pin

APPENDIX

3.4 Countermeasures against noise

(3) Oscillator protection using Vss pattern

As for a two-sided printed circuit board, print a Vss pattern on the underside (soldering side) of the position (on the component side) where an oscillator is mounted.

Connect the Vss pattern to the microcomputer Vss pin with the shortest possible wiring. Besides, separate this Vss pattern from other Vss patterns.

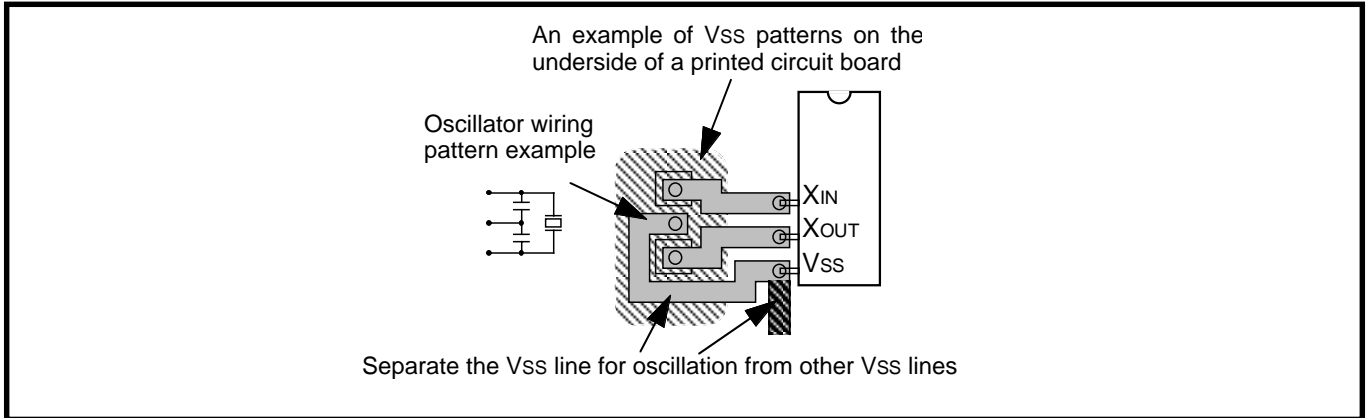


Fig. 3.4.10 Vss pattern on the underside of an oscillator

3.4.5 Setup for I/O ports

Setup I/O ports using hardware and software as follows:

<Hardware>

- Connect a resistor of 100 Ω or more to an I/O port in series.

<Software>

- As for an input port, read data several times by a program for checking whether input levels are equal or not.
- As for an output port, since the output data may reverse because of noise, rewrite data to its port latch at fixed periods.
- Rewrite data to direction registers at fixed periods.

Note: When a direction register is set for input port again at fixed periods, a several-nanosecond short pulse may be output from this port. If this is undesirable, connect a capacitor to this port to remove the noise pulse.

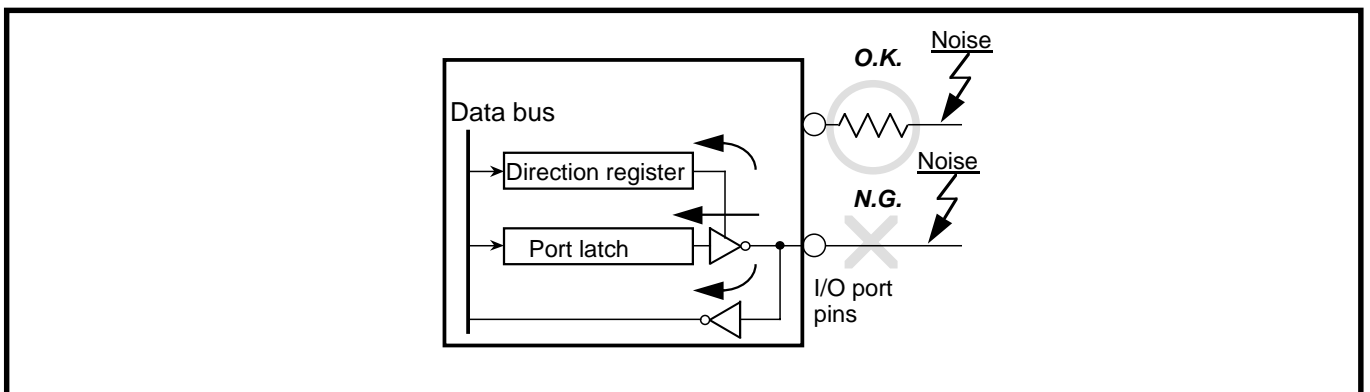


Fig. 3.4.11 Setup for I/O ports

3.4.6 Providing of watchdog timer function by software

If a microcomputer runs away because of noise or others, it can be detected by a software watchdog timer and the microcomputer can be reset to normal operation. This is equal to or more effective than program runaway detection by a hardware watchdog timer. The following shows an example of a watchdog timer provided by software.

In the following example, to reset a microcomputer to normal operation, the main routine detects errors of the interrupt processing routine and the interrupt processing routine detects errors of the main routine. This example assumes that interrupt processing is repeated multiple times in a single main routine processing.

<The main routine>

- Assigns a single byte of RAM to a software watchdog timer (SWDT) and writes the initial value N in the SWDT once at each execution of the main routine. The initial value N should satisfy the following condition:

$$N+1 \geq (\text{Counts of interrupt processing executed in each main routine})$$
 As the main routine execution cycle may change because of an interrupt processing or others, the initial value N should have a margin.
- Watches the operation of the interrupt processing routine by comparing the SWDT contents with counts of interrupt processing after the initial value N has been set.
- Detects that the interrupt processing routine has failed and determines to branch to the program initialization routine for recovery processing in the following case:
 If the SWDT contents do not change after interrupt processing.

<The interrupt processing routine>

- Decrements the SWDT contents by 1 at each interrupt processing.
- Determines that the main routine operates normally when the SWDT contents are reset to the initial value N at almost fixed cycles (at the fixed interrupt processing count).
- Detects that the main routine has failed and determines to branch to the program initialization routine for recovery processing in the following case:
 If the SWDT contents are not initialized to the initial value N but continued to decrement and if they reach 0 or less.

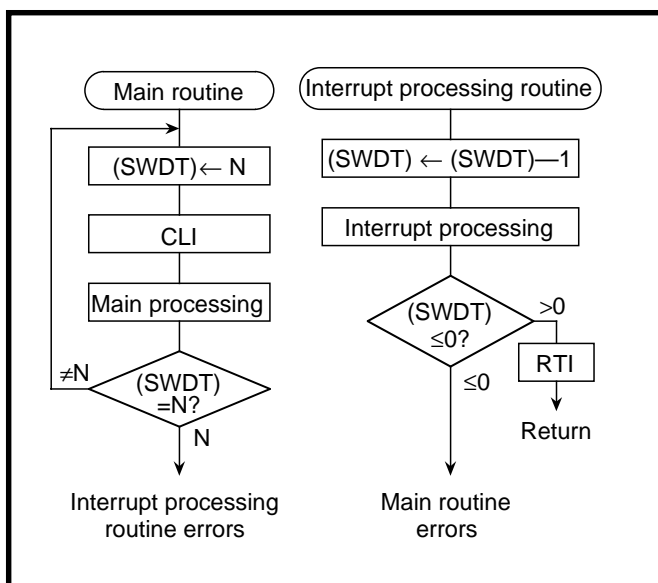


Fig. 3.4.12 Watchdog timer by software

APPENDIX

3.5 List of registers

3.5 List of registers

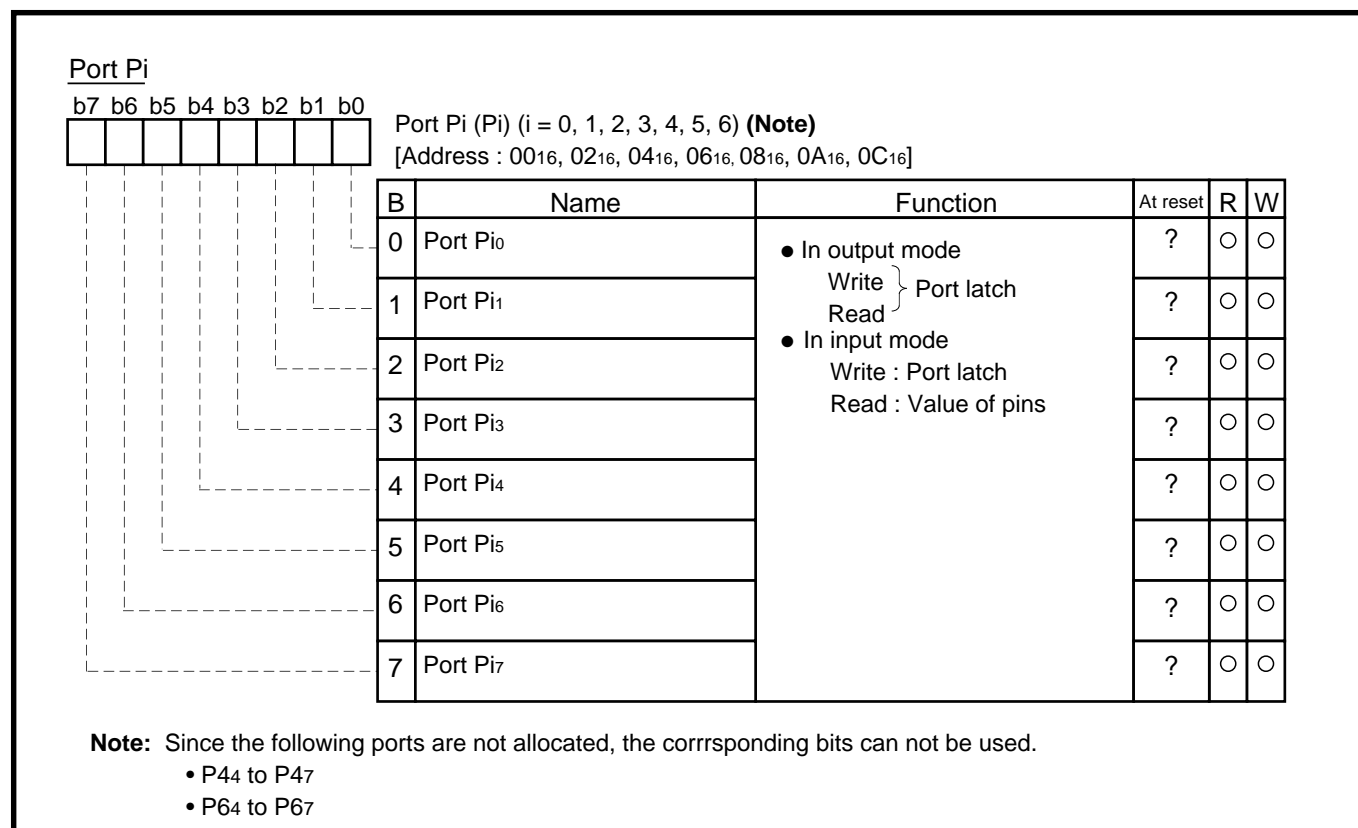


Fig. 3.5.1 Structure of Port Pi

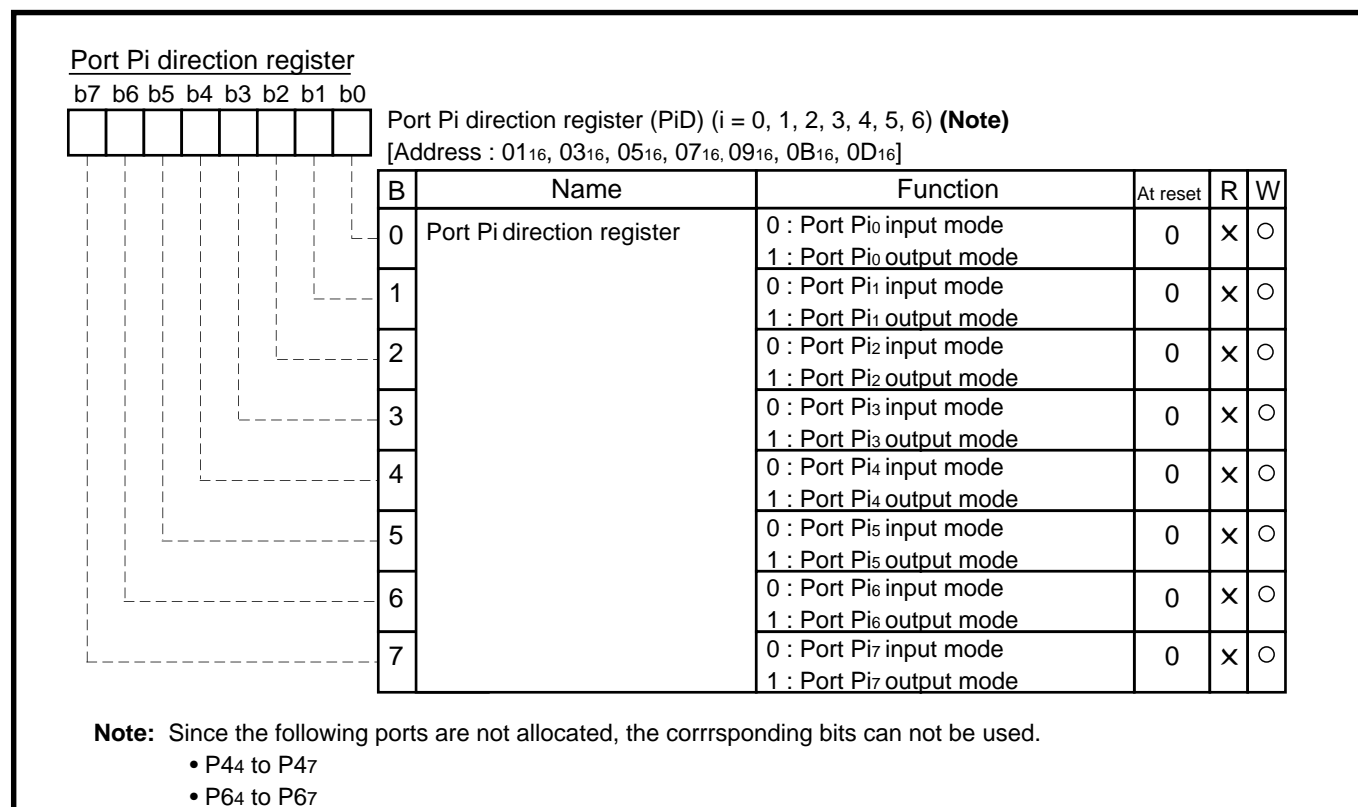


Fig. 3.5.2 Structure of Port Pi direction register

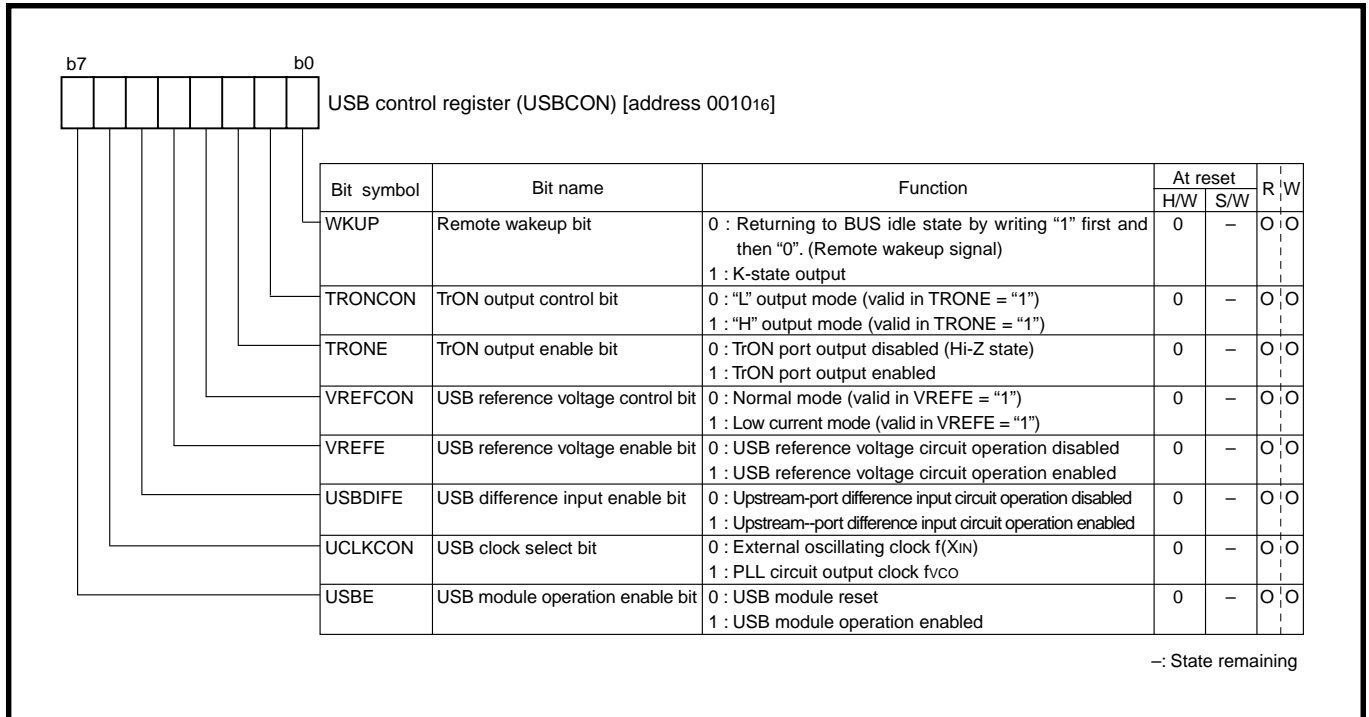


Fig. 3.5.3 Structure of USB control register

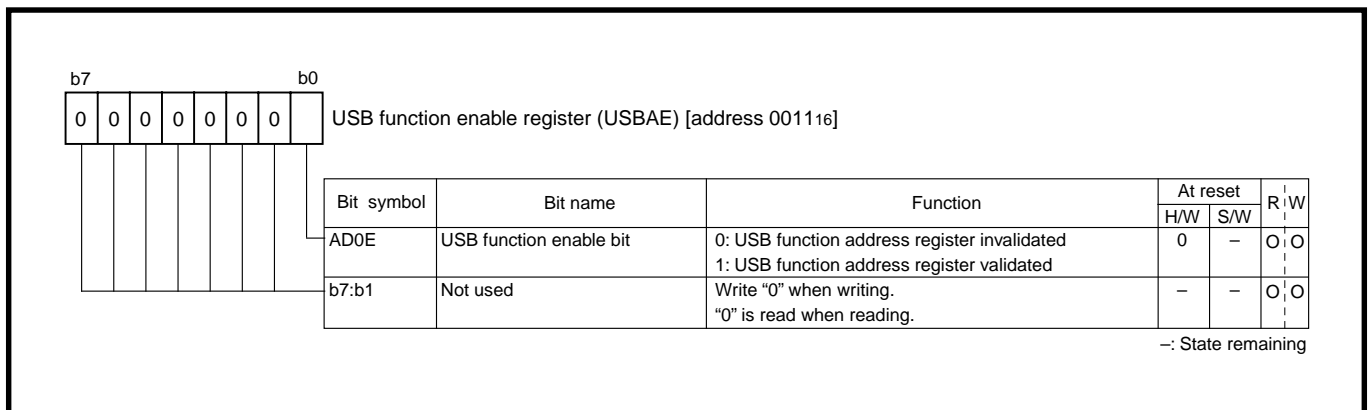


Fig. 3.5.4 Structure of USB function enable register

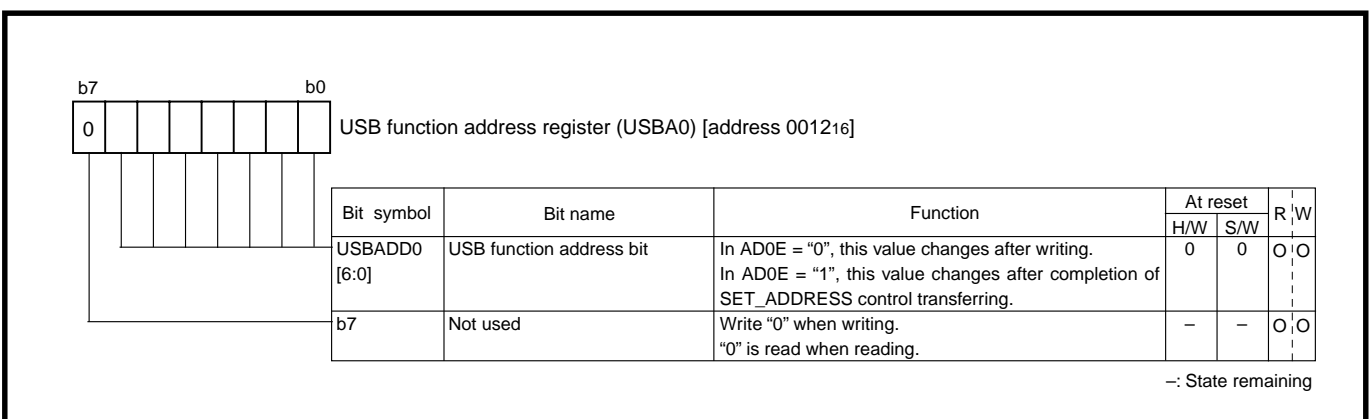


Fig. 3.5.5 Structure of USB function address register

APPENDIX

3.5 List of registers

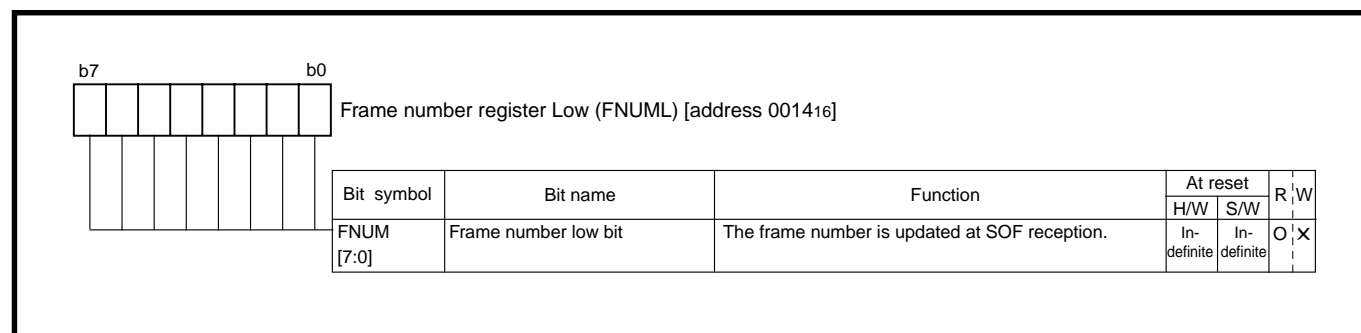


Fig. 3.5.6 Structure of Frame number register Low

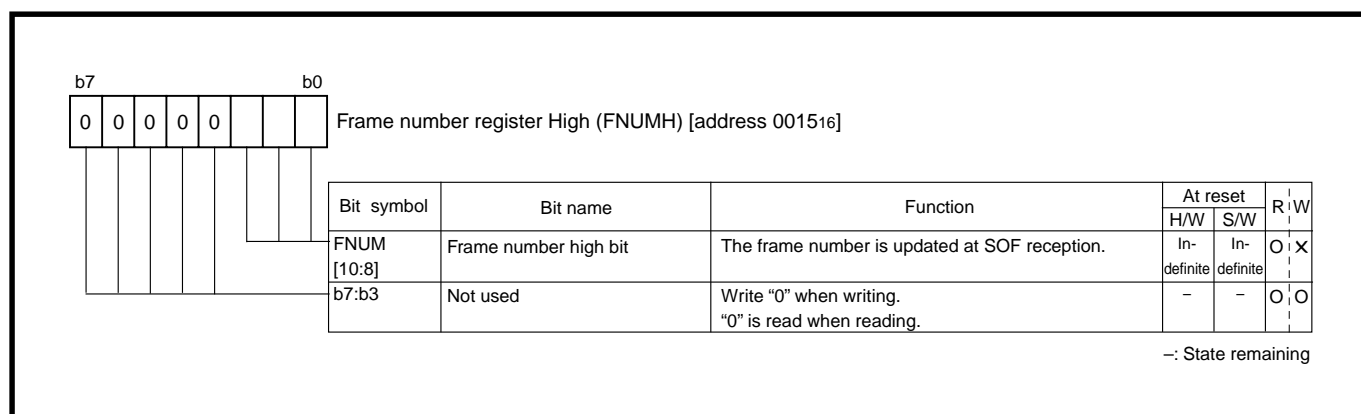


Fig. 3.5.7 Structure of Frame number register High

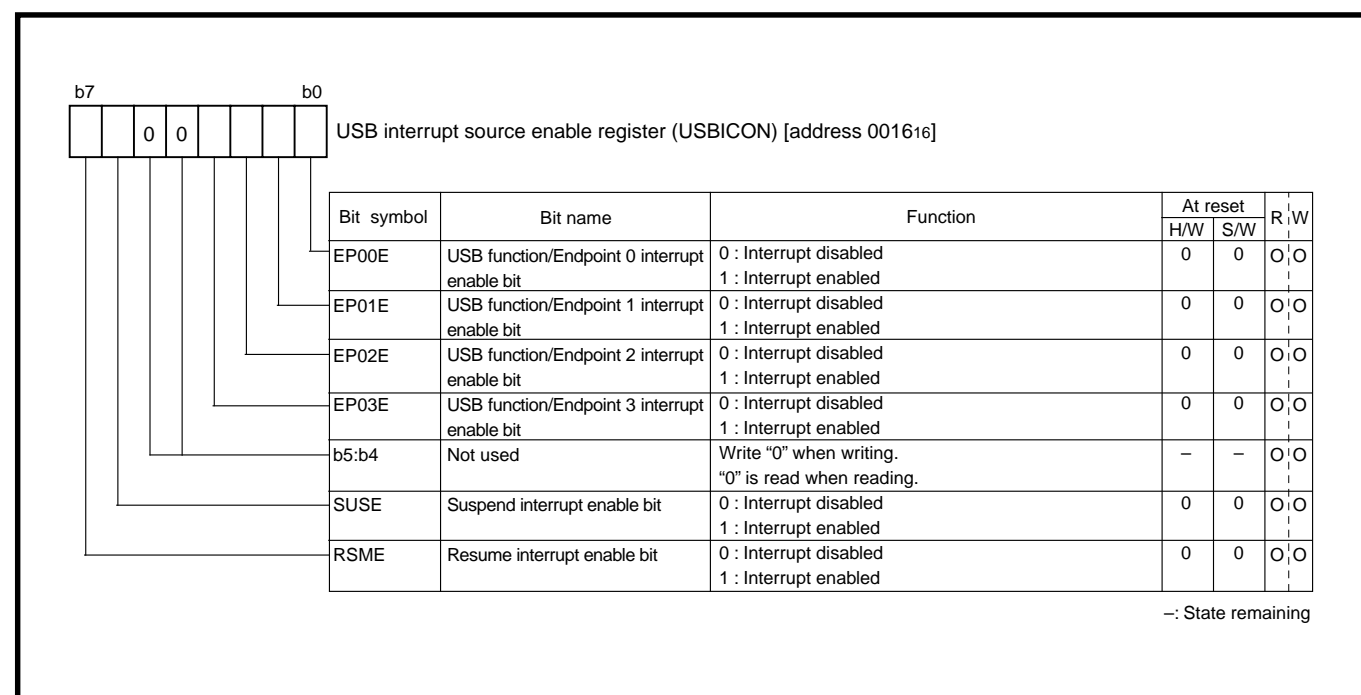


Fig. 3.5.8 Structure of USB interrupt source enable register

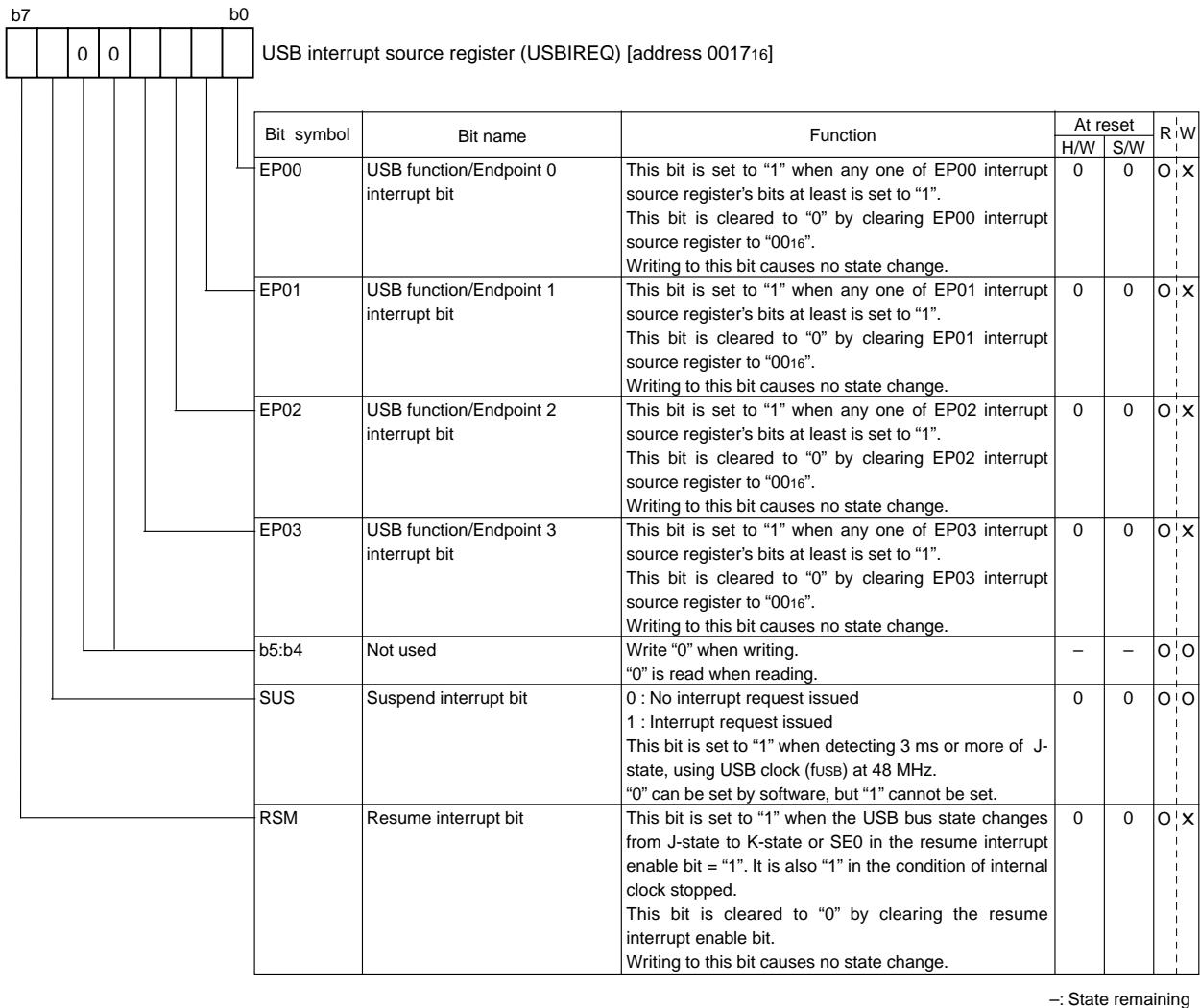


Fig. 3.5.9 Structure of USB interrupt source register

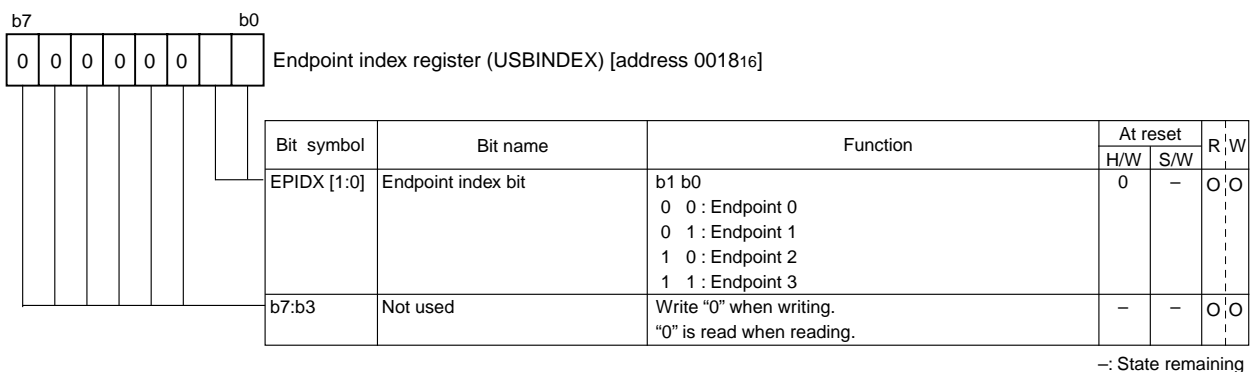


Fig. 3.5.10 Structure of Endpoint index register

APPENDIX

3.5 List of registers

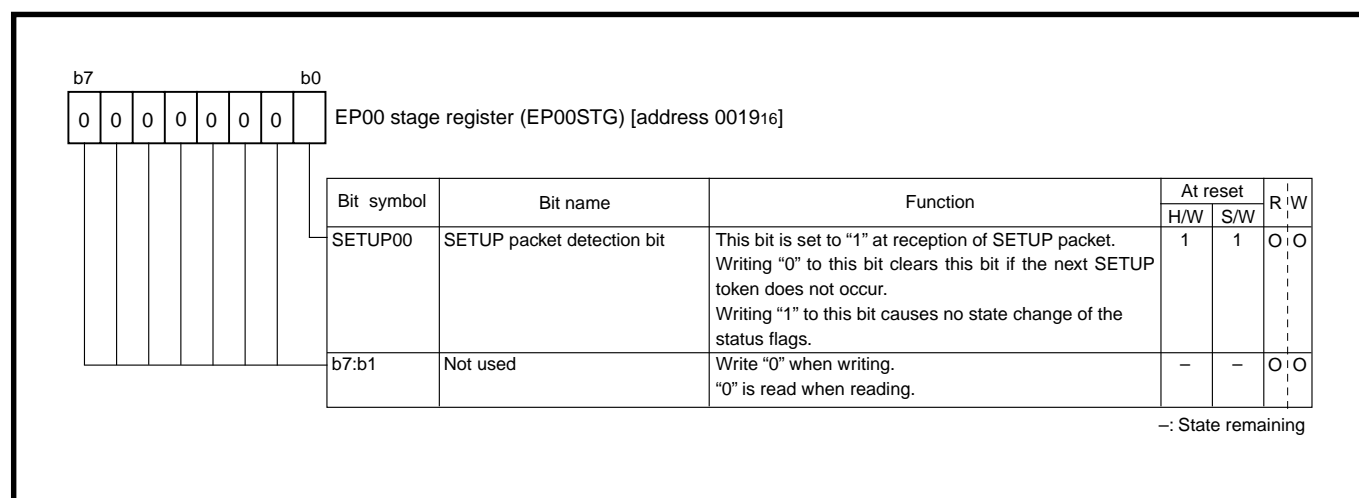


Fig. 3.5.11 Structure of EP00 stage register

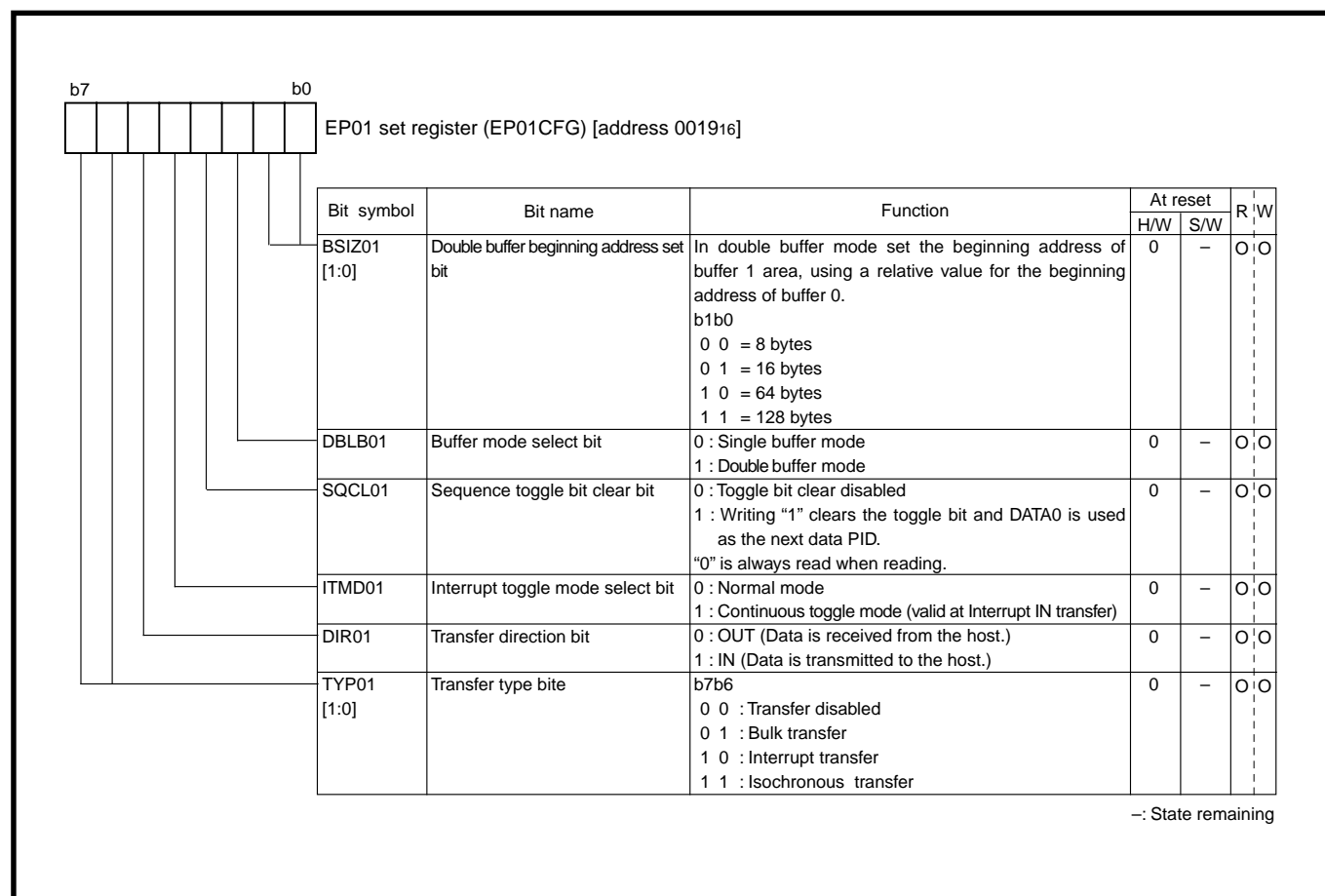


Fig. 3.5.12 Structure of EP01 set register

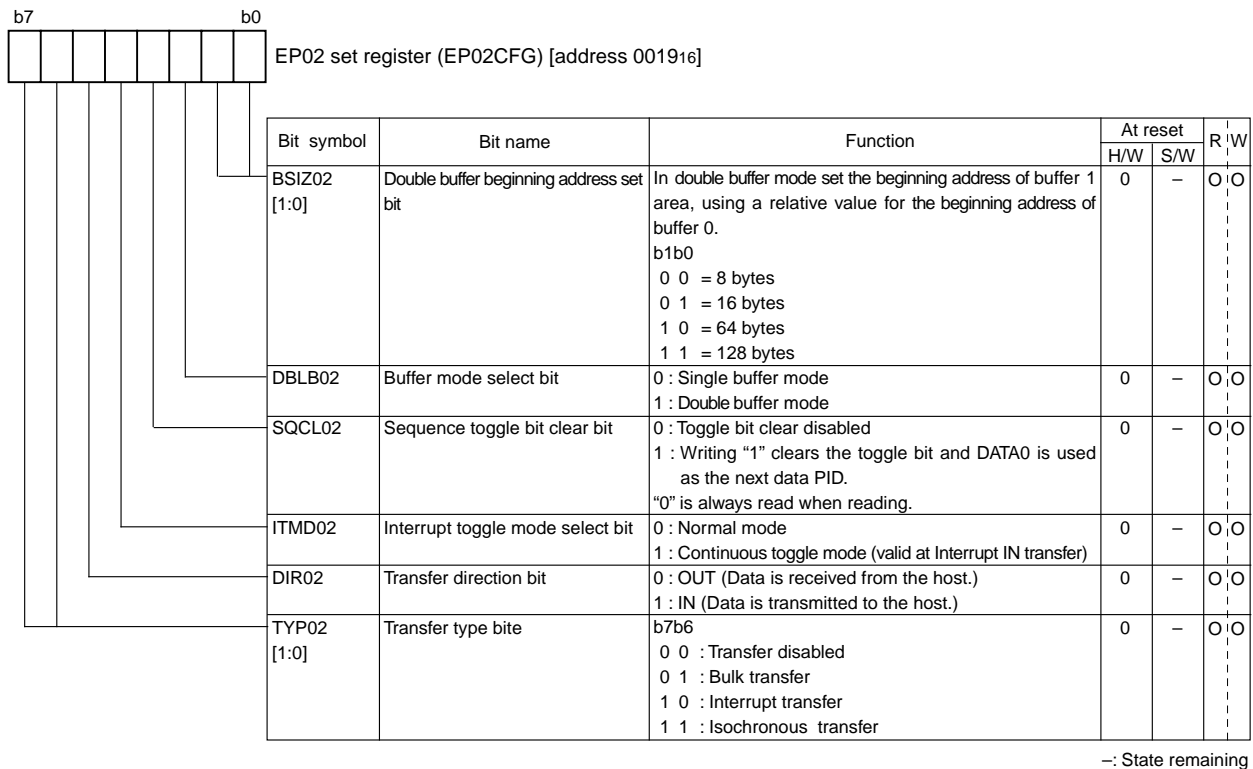


Fig. 3.5.13 Structure of EP02 set register

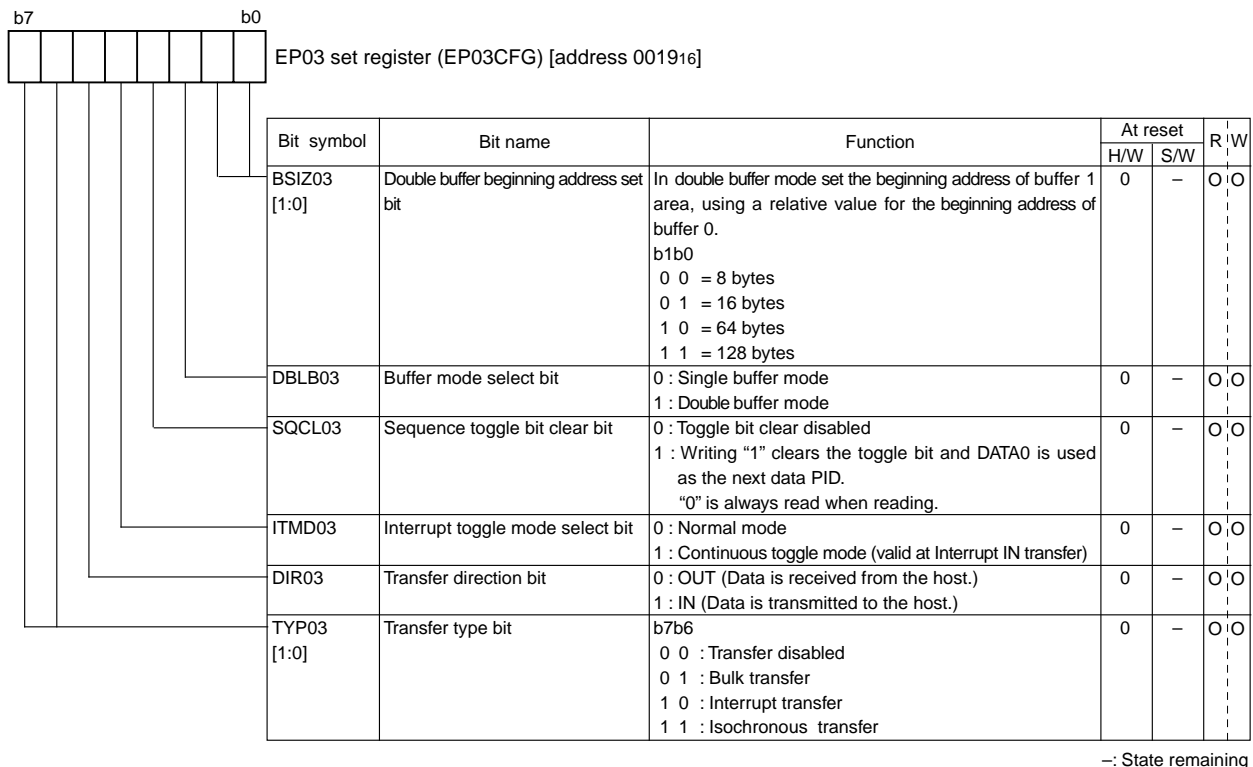


Fig. 3.5.14 Structure of EP03 set register

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3.5 List of registers

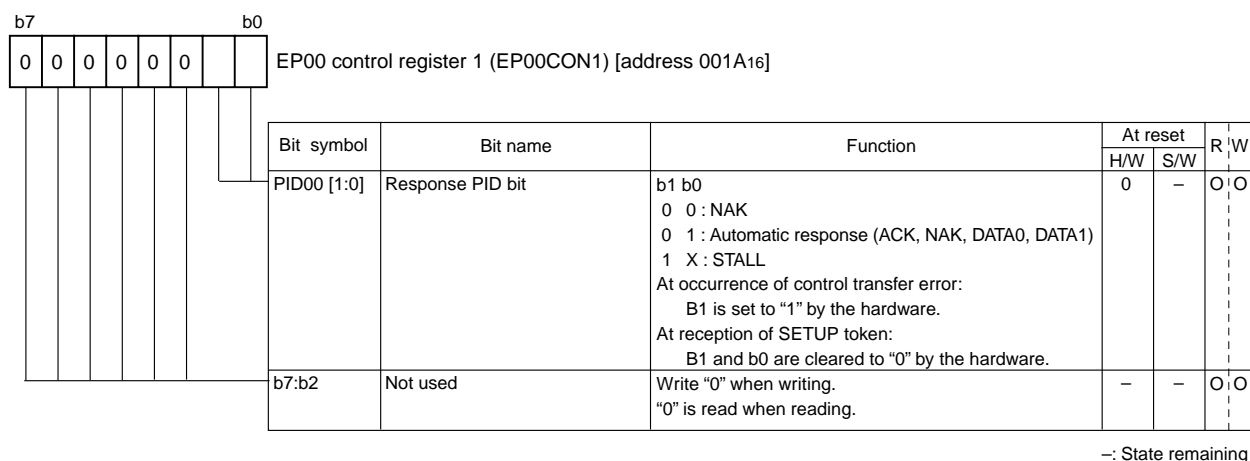


Fig. 3.5.15 Structure of EP00 control register 1

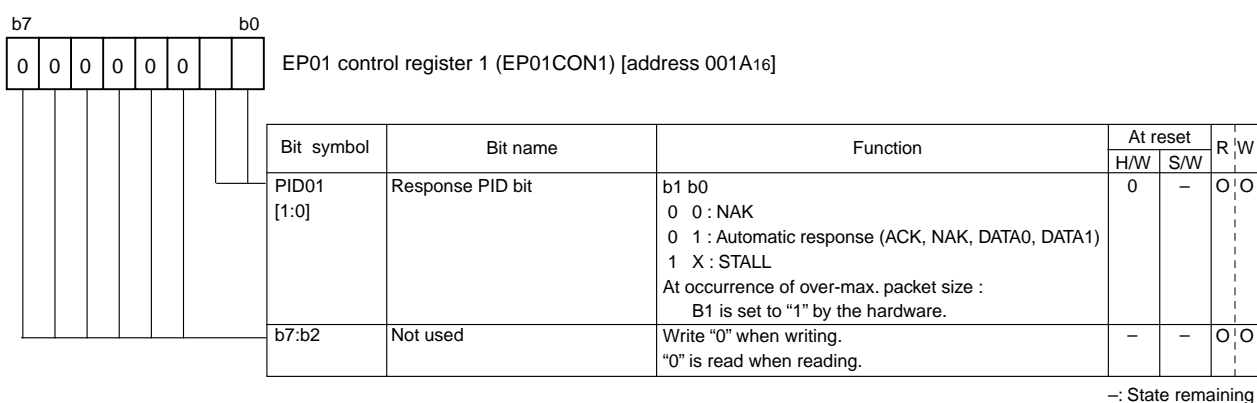


Fig. 3.5.16 Structure of EP01 control register 1

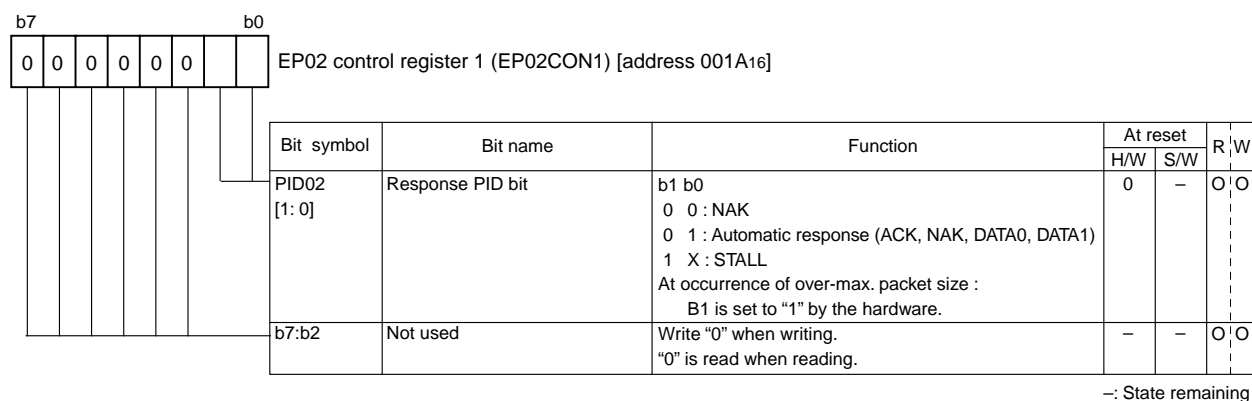


Fig. 3.5.17 Structure of EP02 control register 1

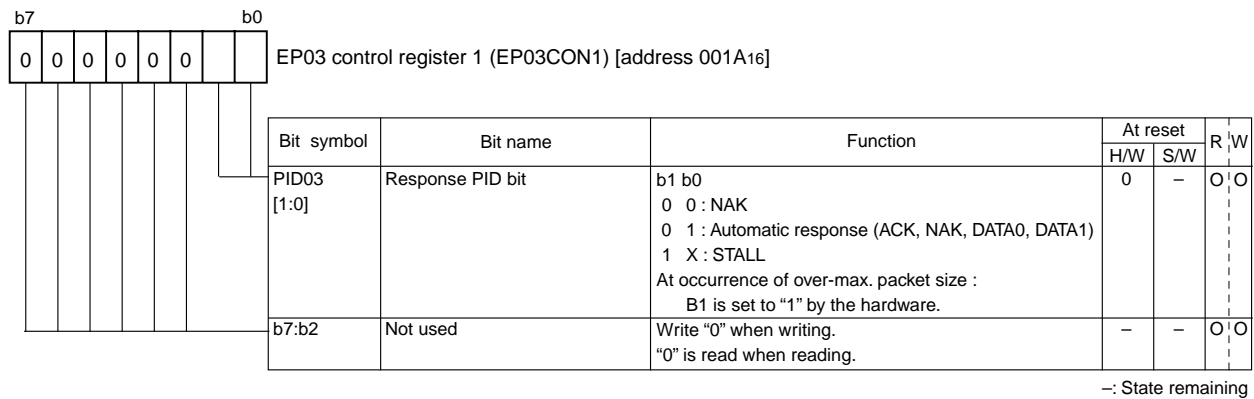


Fig. 3.5.18 Structure of EP03 control register 1

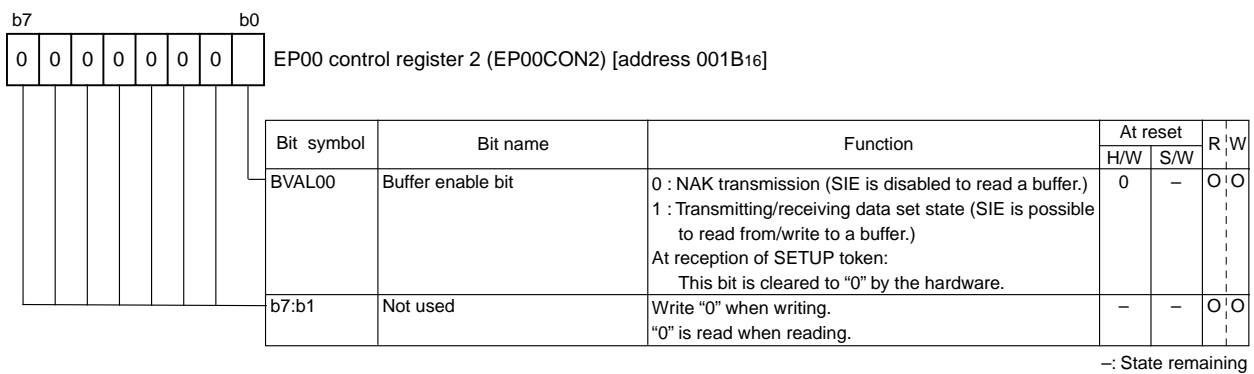


Fig. 3.5.19 Structure of EP00 control register 2

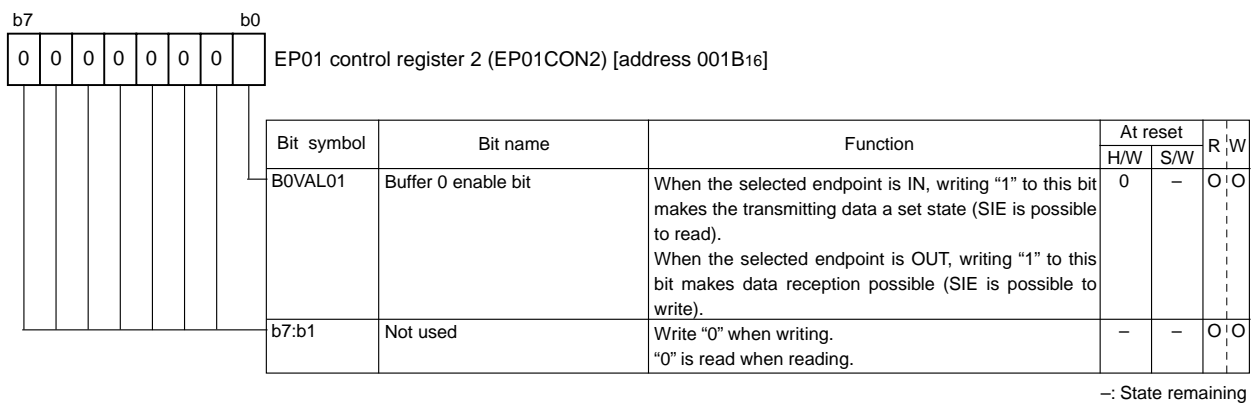


Fig. 3.5.20 Structure of EP01 control register 2

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3.5 List of registers

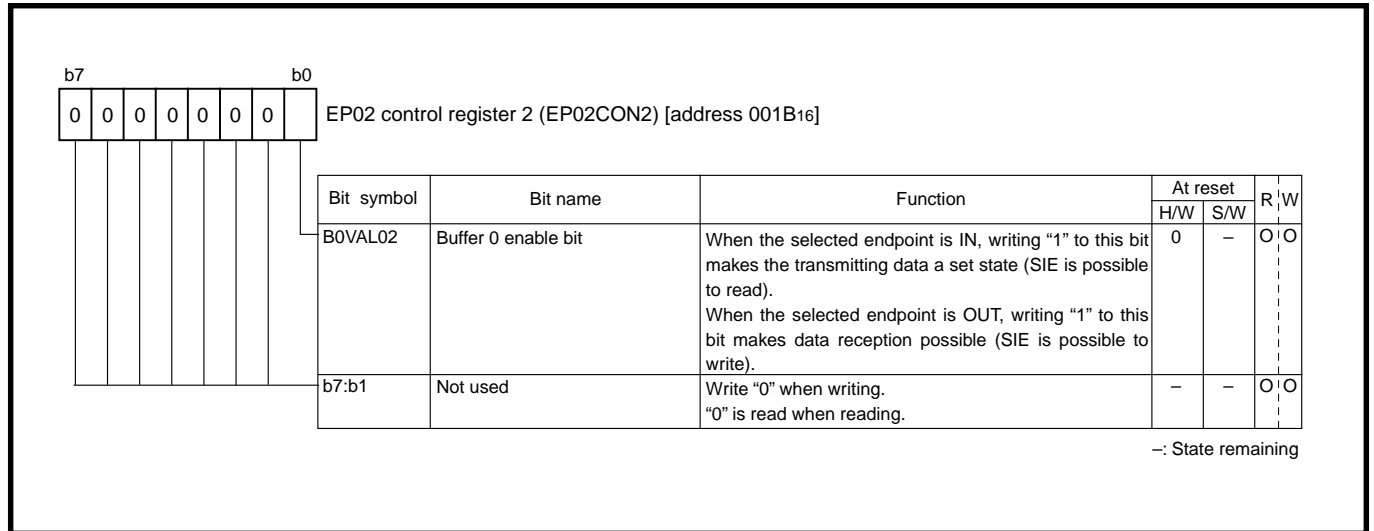


Fig. 3.5.21 Structure of EP02 control register 2

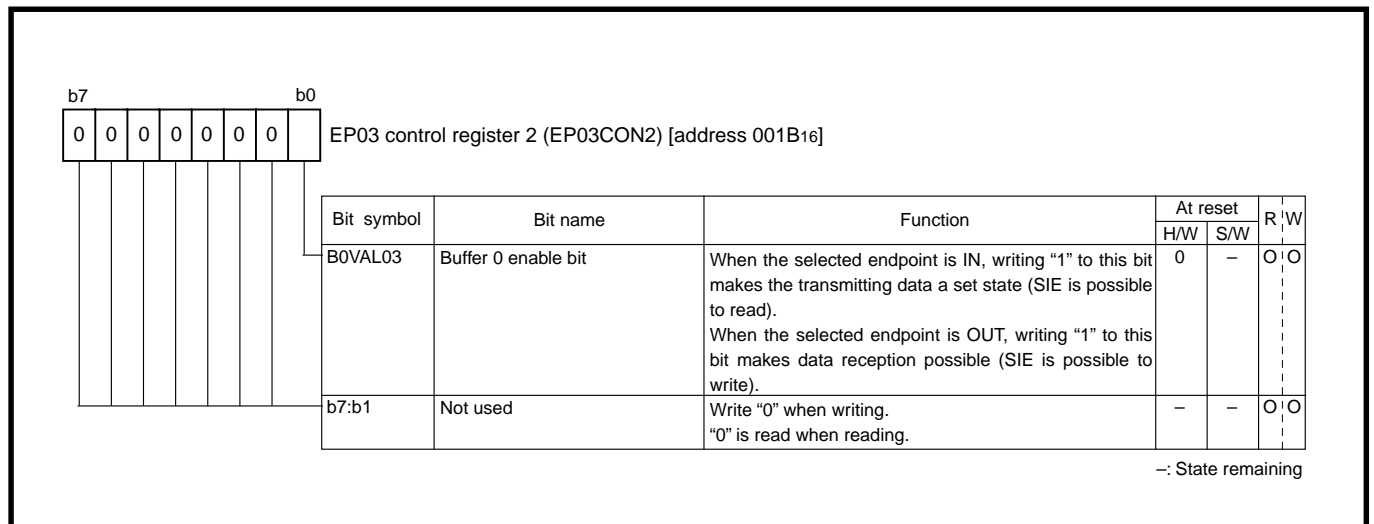


Fig. 3.5.22 Structure of EP03 control register 2

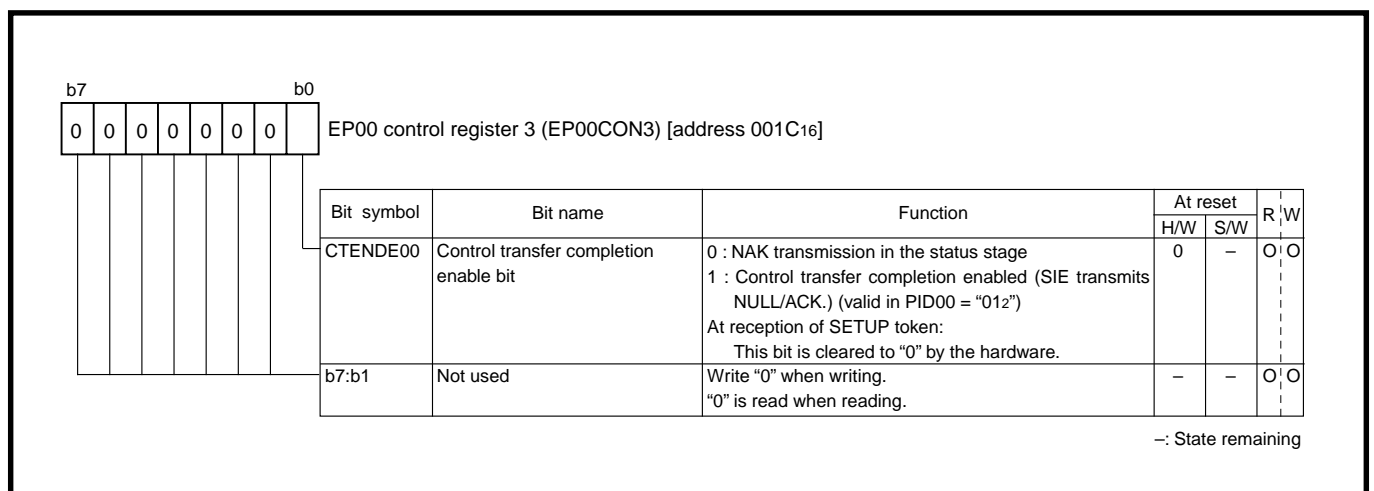


Fig. 3.5.23 Structure of EP00 control register 3

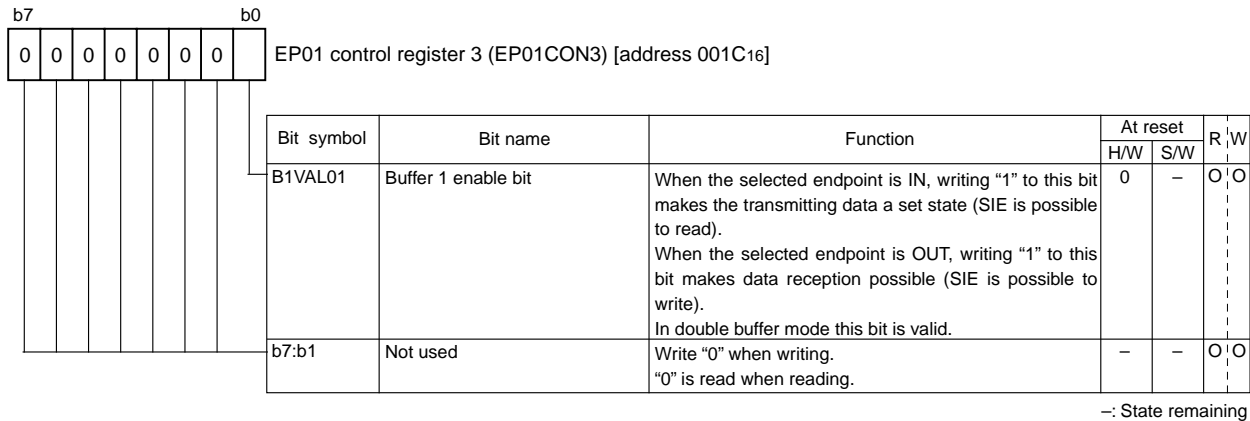


Fig. 3.5.24 Structure of EP01 control register 3

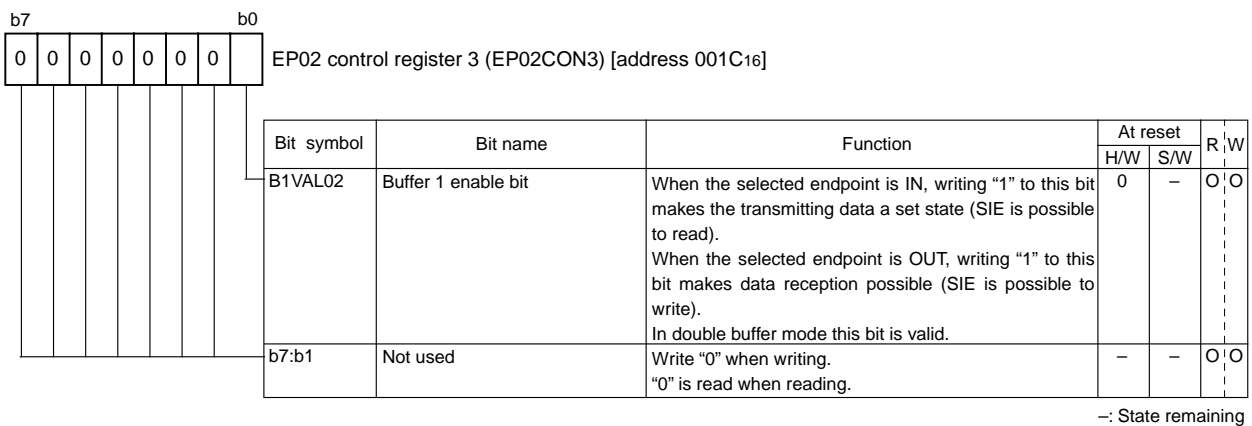


Fig. 3.5.25 Structure of EP02 control register 3

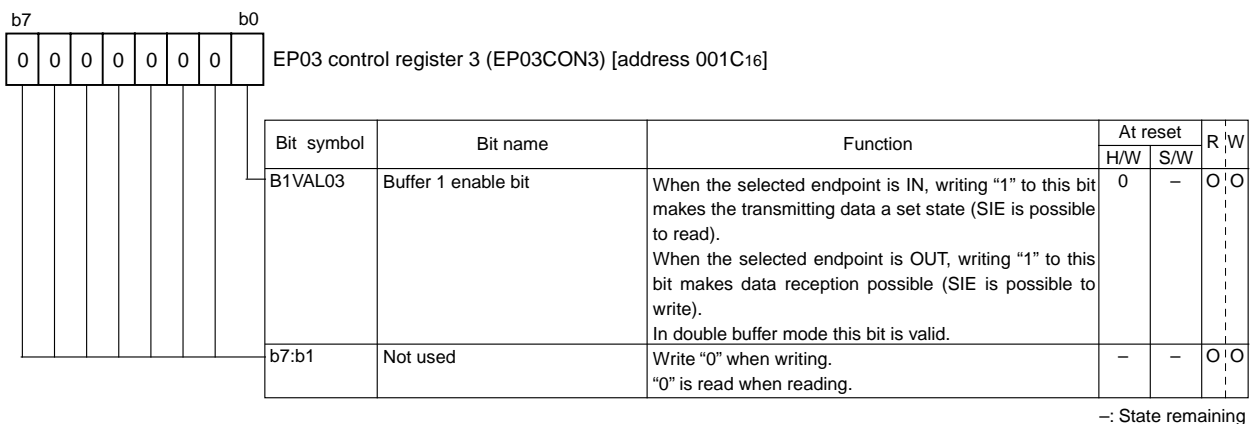


Fig. 3.5.26 Structure of EP03 control register 3

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3.5 List of registers

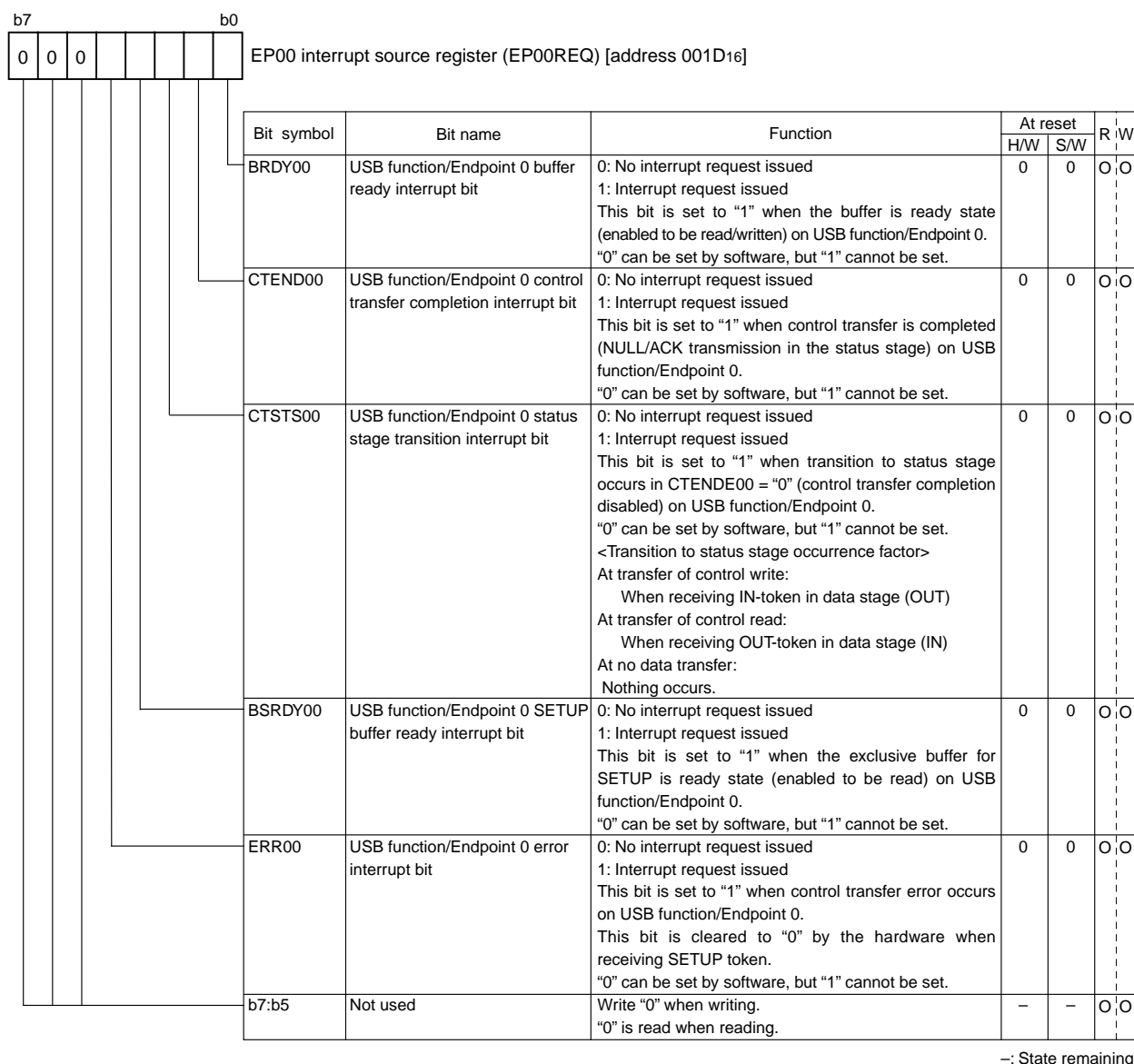


Fig. 3.5.27 Structure of EP00 interrupt source register

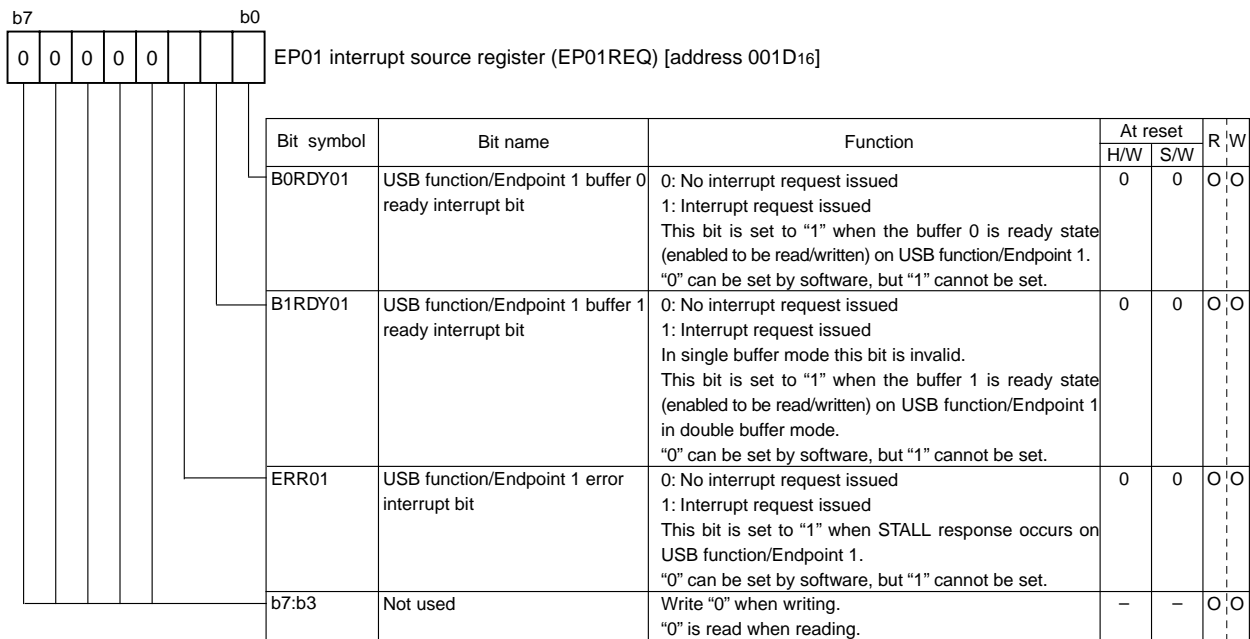


Fig. 3.5.28 Structure of EP01 interrupt source register

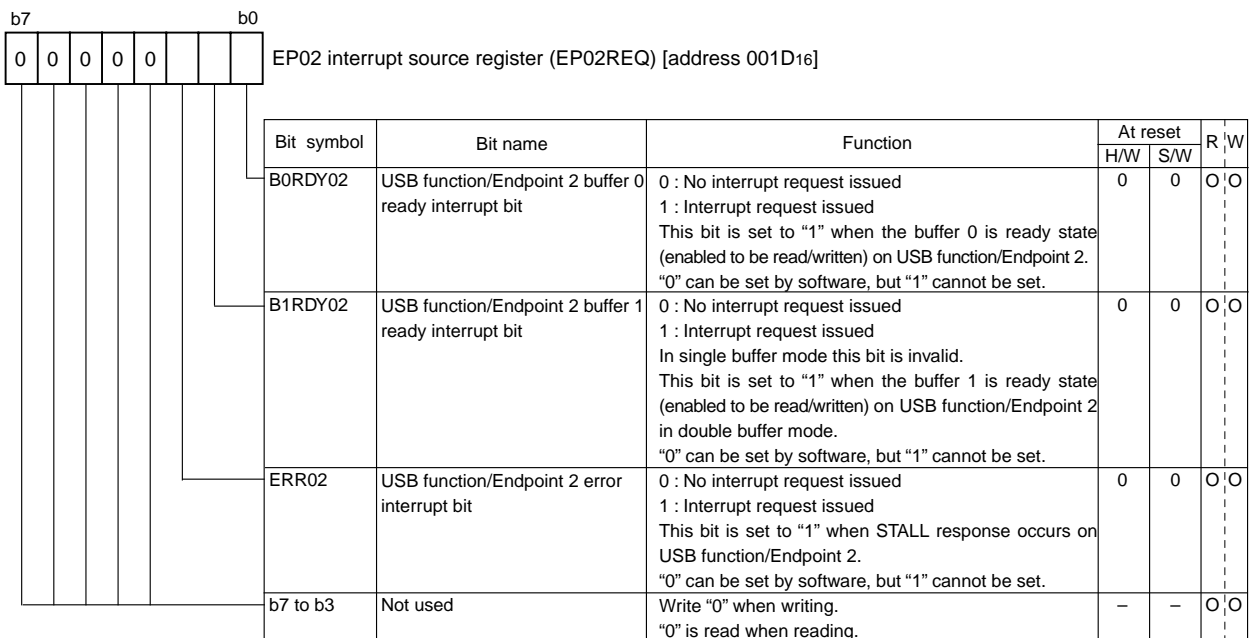


Fig. 3.5.29 Structure of EP02 interrupt source register

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3.5 List of registers

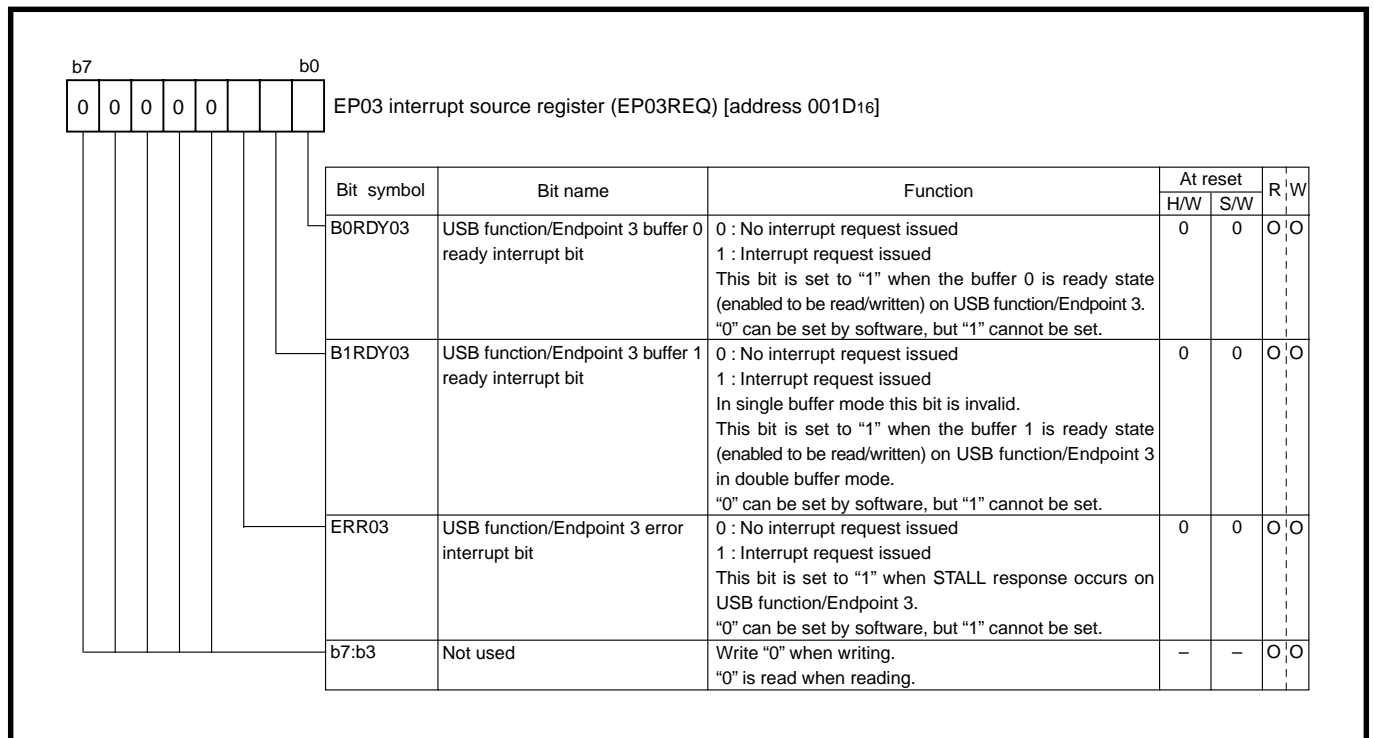


Fig. 3.5.30 Structure of EP03 interrupt source register

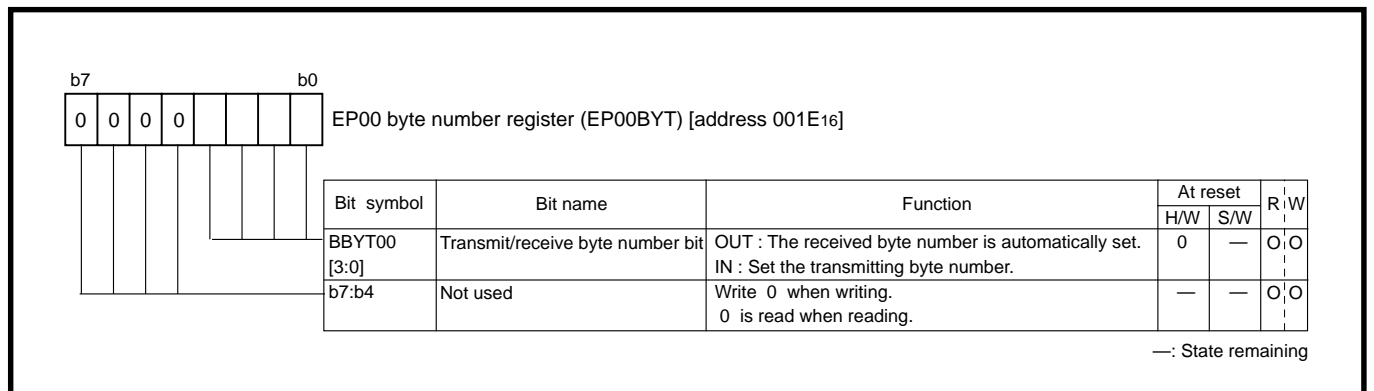


Fig. 3.5.31 Structure of EP00 byte number register

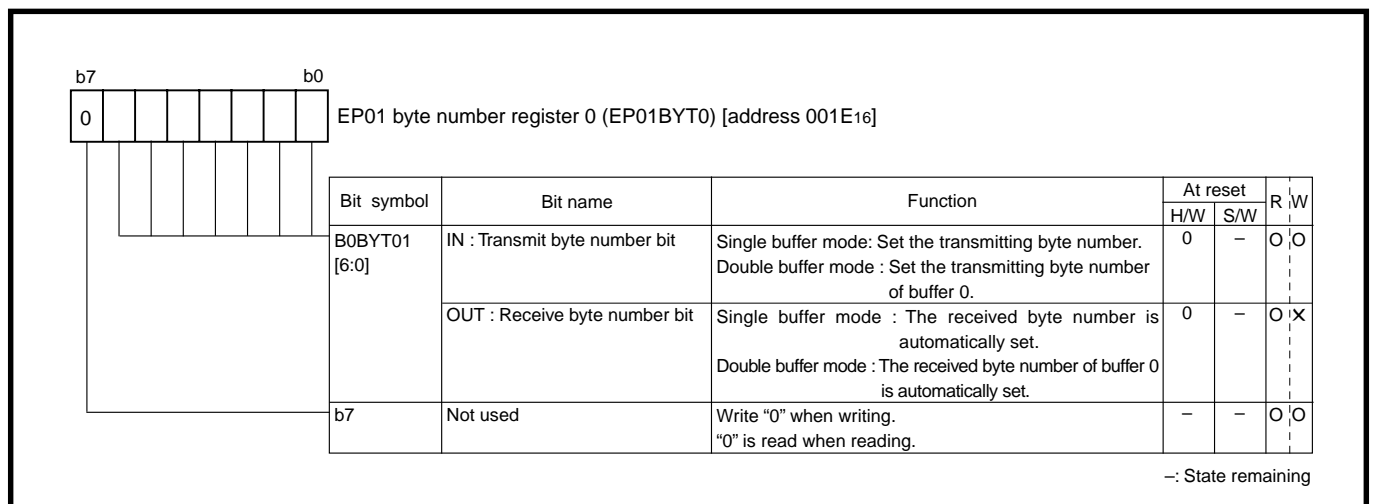


Fig. 3.5.32 Structure of EP01 byte number register 0

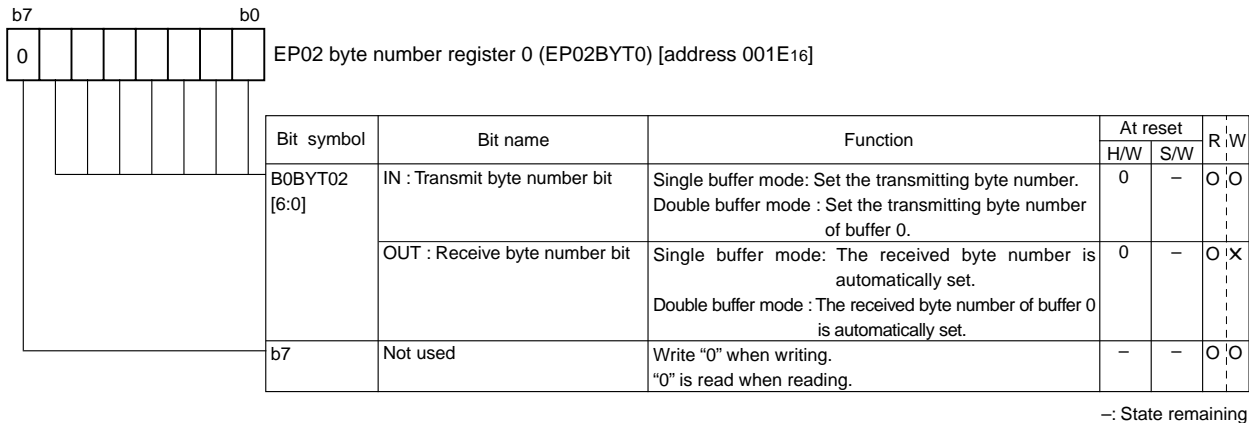


Fig. 3.5.33 Structure of EP02 byte number register 0

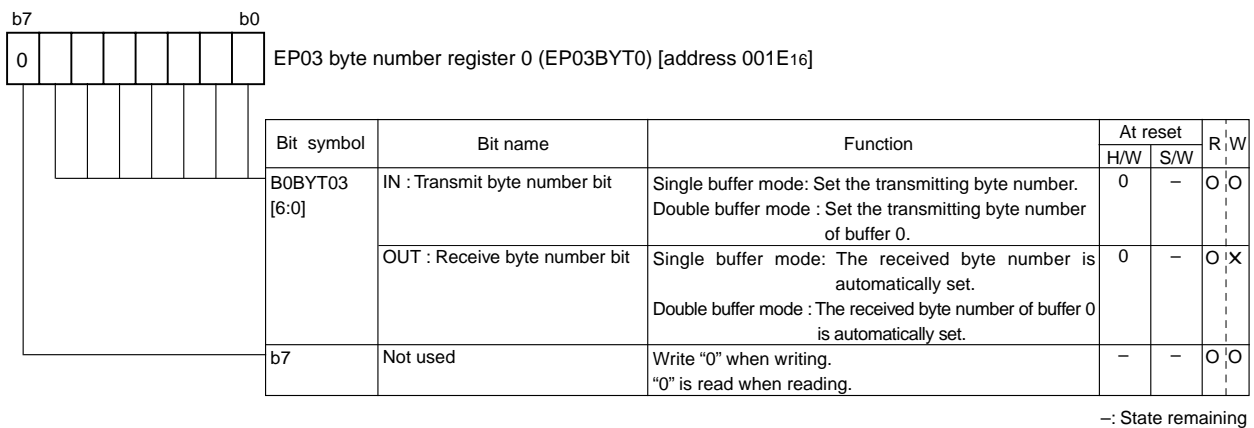


Fig. 3.5.34 Structure of EP03 byte number register 0

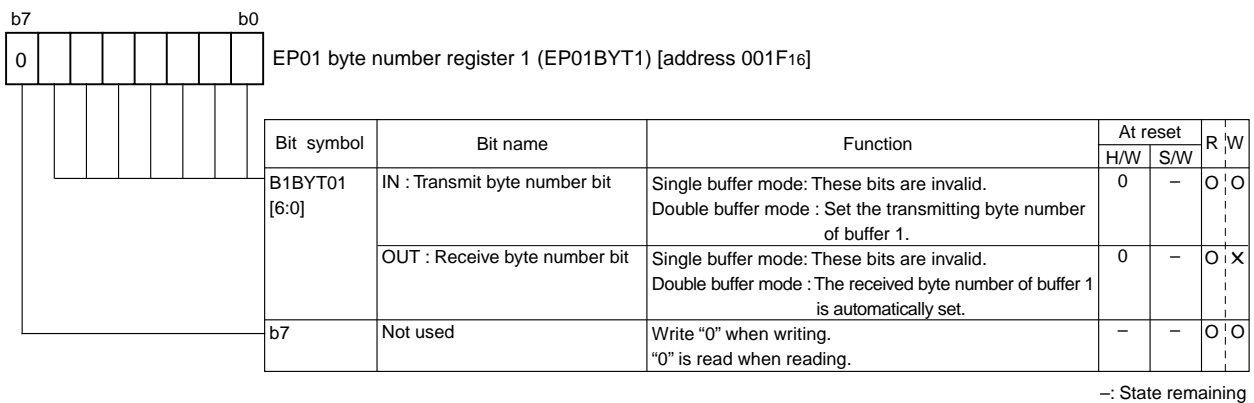
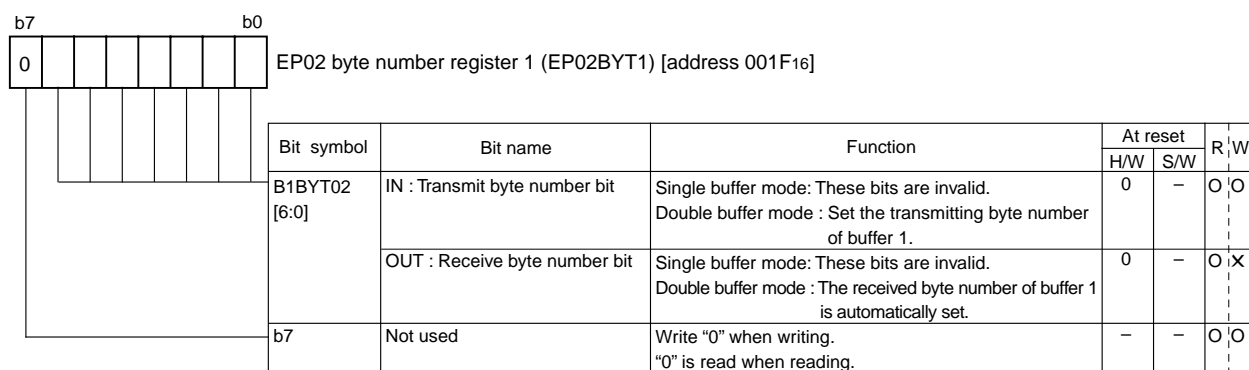


Fig. 3.5.35 Structure of EP01 byte number register 1

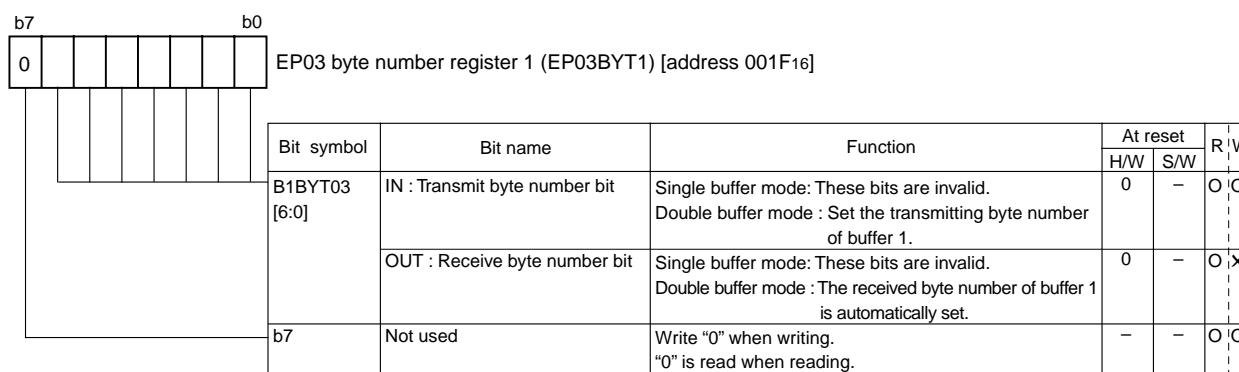
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3.5 List of registers



–: State remaining

Fig. 3.5.36 Structure of EP02 byte number register 1



–: State remaining

Fig. 3.5.37 Structure of EP03 byte number register 1

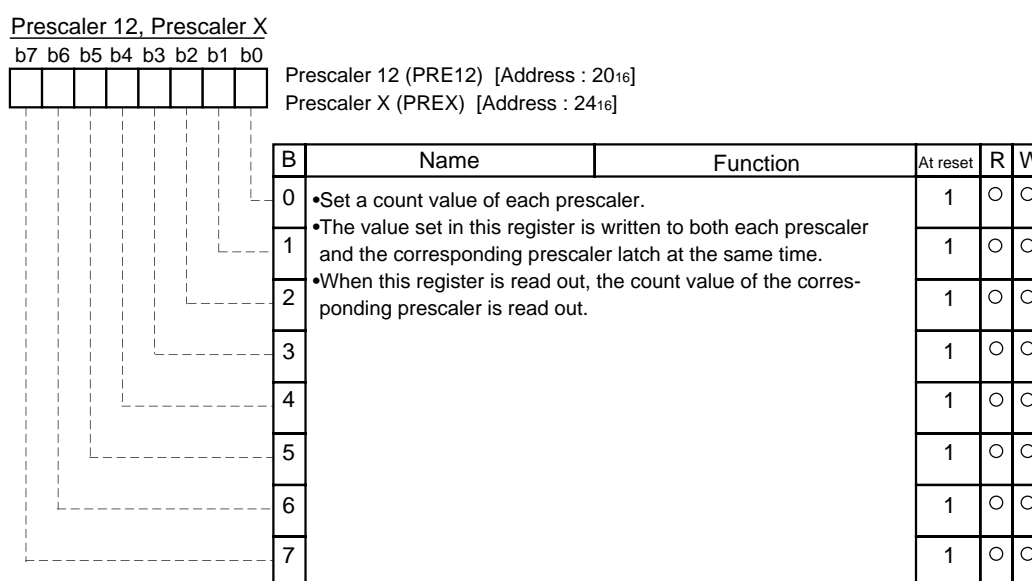
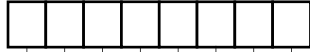


Fig. 3.5.38 Structure of Prescaler12, Prescaler X

Timer 1

b7 b6 b5 b4 b3 b2 b1 b0



Timer 1 (T1) [Address : 21₁₆]

B	Name	Function	At reset	R	W
0		•Set a count value of timer 1.	1	○	○
1		•The value set in this register is written to both timer 1 and timer 1 latch at the same time.	0	○	○
2		•When this register is read out, the timer 1's count value is read out.	0	○	○
3			0	○	○
4			0	○	○
5			0	○	○
6			0	○	○
7			0	○	○

Fig. 3.5.39 Structure of Timer 1

Timer 2, Timer X

b7 b6 b5 b4 b3 b2 b1 b0



Timer 2 (T2) [Address : 22₁₆]

Timer X (TX) [Address : 25₁₆]

B	Name	Function	At reset	R	W
0		•Set a count value of each timer.	1	○	○
1		•The value set in this register is written to both each timer and each timer latch at the same time.	1	○	○
2		•When this register is read out, each timer's count value is read out.	1	○	○
3			1	○	○
4			1	○	○
5			1	○	○
6			1	○	○
7			1	○	○

Fig. 3.5.40 Structure of Timer 2, Timer X

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3.5 List of registers

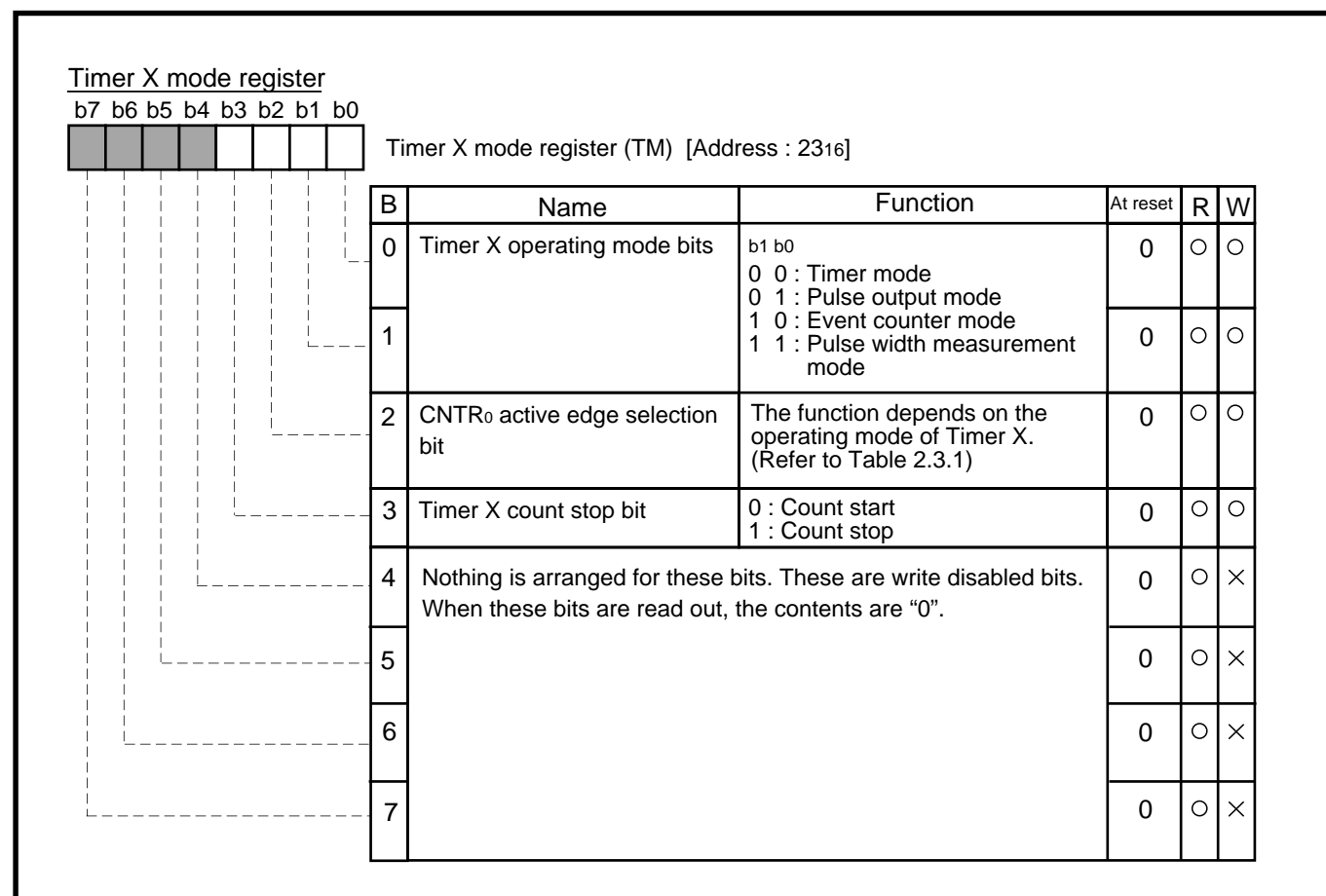


Fig. 3.5.41 Structure of Timer X mode register

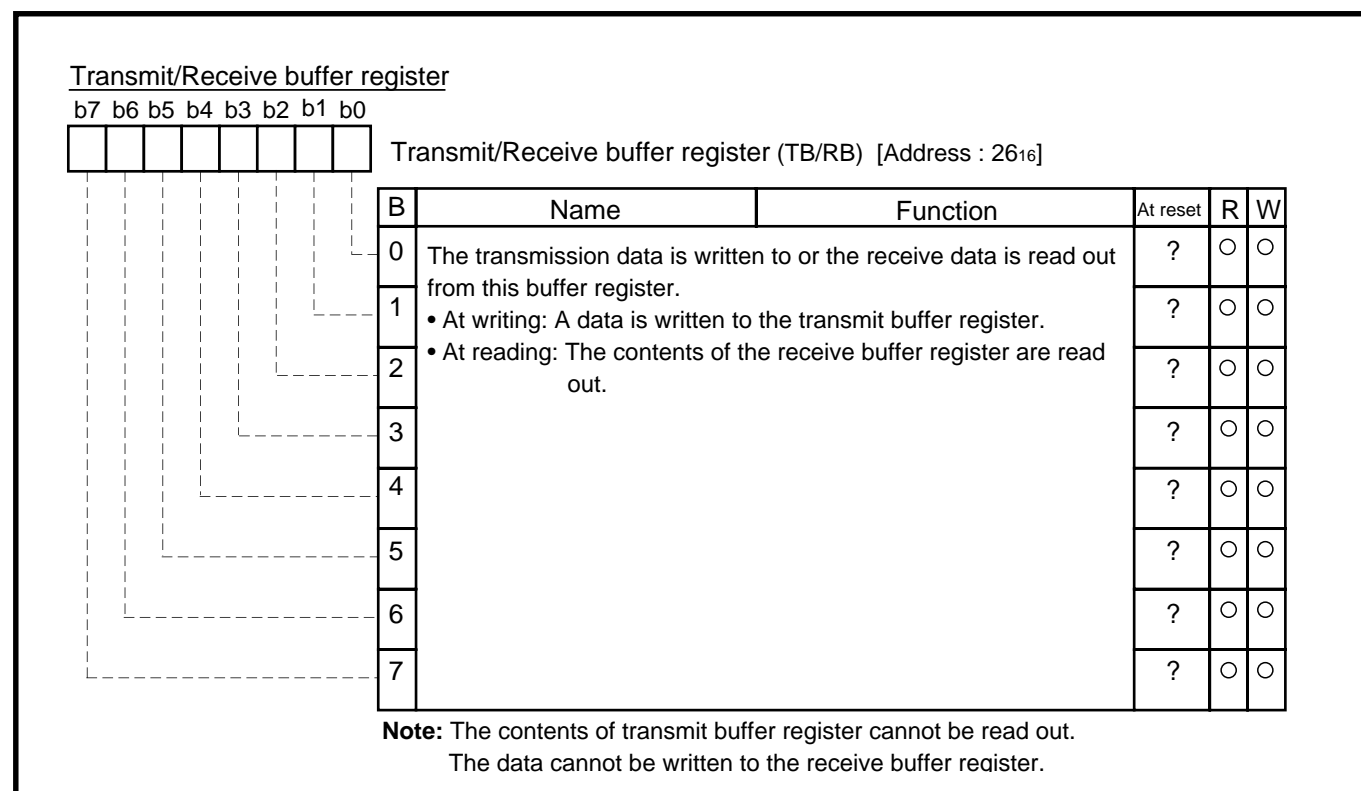
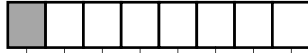


Fig. 3.5.42 Structure of Transmit/Receive buffer register

Serial I/O status register

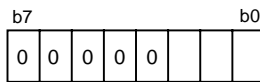
b7 b6 b5 b4 b3 b2 b1 b0



Serial I/O status register (SIOSTS) [Address : 27₁₆]

B	Name	Function	At reset	R	W
0	Transmit buffer empty flag (TBE)	0 : Buffer full 1 : Buffer empty	0	○	×
1	Receive buffer full flag (RBF)	0 : Buffer empty 1 : Buffer full	0	○	×
2	Transmit shift register shift completion flag (TSC)	0 : Transmit shift in progress 1 : Transmit shift completed	0	○	×
3	Overrun error flag (OE)	0 : No error 1 : Overrun error	0	○	×
4	Parity error flag (PE)	0 : No error 1 : Parity error	0	○	×
5	Framing error flag (FE)	0 : No error 1 : Framing error	0	○	×
6	Summing error flag (SE)	0 : (OE) U (PE) U (FE) = 0 1 : (OE) U (PE) U (FE) = 1	0	○	×
7	Nothing is allocated for this bit. This is a write disabled bit. When this bit is read out, the contents are "1".		1	○	×

Fig. 3.5.43 Structure of Serial I/O status register



EXB interrupt source enable register (EXBICON) [address 0030₁₆]
(Note)

Bit symbol	Bit name	Function	At reset		R	W
			H/W	S/W		
RXB_ENB	CPU channel receive enable bit	0 : Operation disabled (Interrupt disabled) 1 : Operation enabled (Receive buffer full interrupt enabled)	0	—	○	○
TXB_ENB	CPU channel transmit enable bit	0 : Operation disabled (Interrupt disabled) 1 : Operation enabled (Transmit buffer empty interrupt enabled)	0	—	○	○
MC_ENB	Memory channel operation enable bit	0 : Operation disabled (Memory channel operation end interrupt disabled) 1 : Operation enabled (Memory channel operation end interrupt disabled)	0	—	○	○
b7:b3	Not used	Write "0" when writing. "0" is read when reading.	—	—	○	○

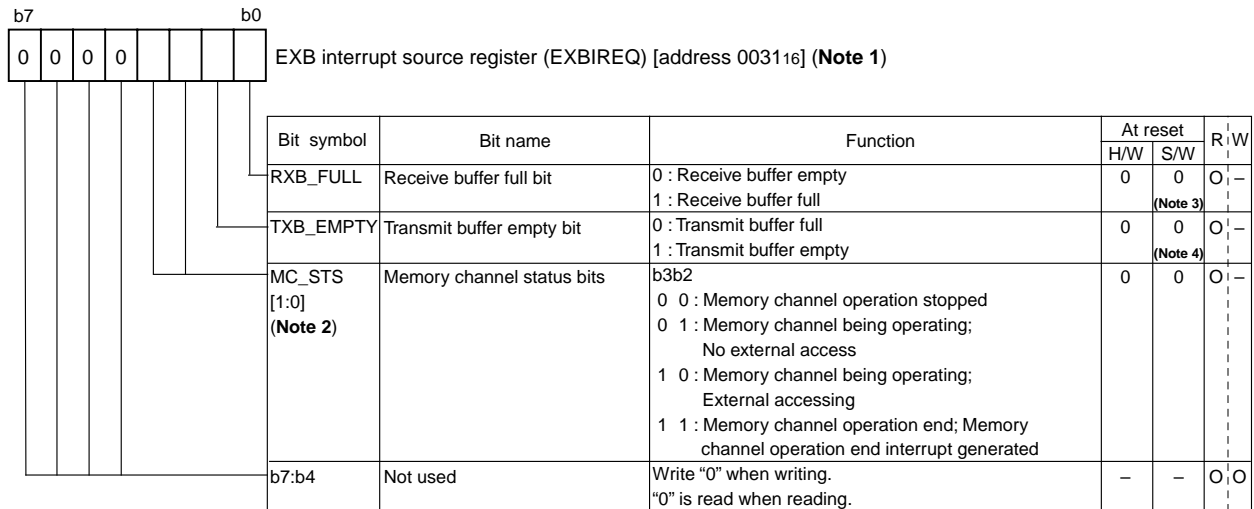
—: State remaining

Note: Do not set each bit simultaneously.

Fig. 3.5.44 Structure of EXB interrupt source enable register

APPENDIX

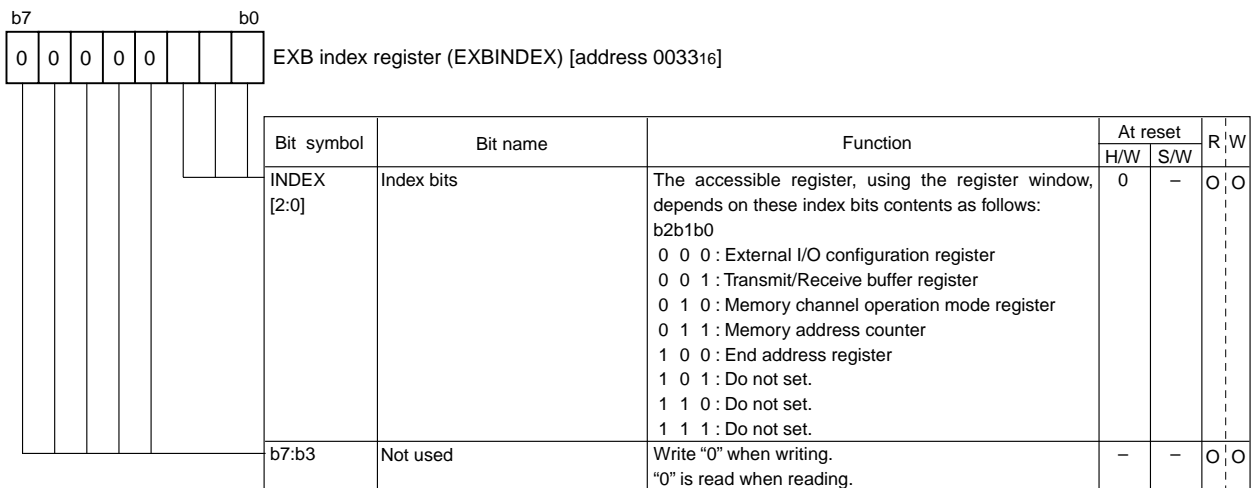
3.5 List of registers



—: State remaining

- Notes**
- 1: When the the ExA1 pin control bit of external I/O configuration register is "1", the external MCU bus can read this register contents by setting the ExA1 pin to "H".
 - 2: The memory channel status bits indicate the status of memory channel. In MC_ENB = "0" these bits are always "002". When the memory channel operation ends, these bits are set to "112" and the memory channel operation end interrupt is generated. These bits can be read out during operation, so that it will show that whether the external MCU bus is accessing or not.
 - 3: This bit is cleared to "0" when reading the transmit/receive buffer register in the CPU channel receive enable bit = "1" or when the CPU channel receive enable bit is "0".
 - 4: This bit is cleared to "0" when writing to the transmit/receive buffer register in the CPU channel transmit enable bit = "1" or when the CPU channel transmit enable bit is "0".

Fig. 3.5.45 Structure of EXB interrupt source register



—: State remaining

Fig. 3.5.46 Structure of EXB index register

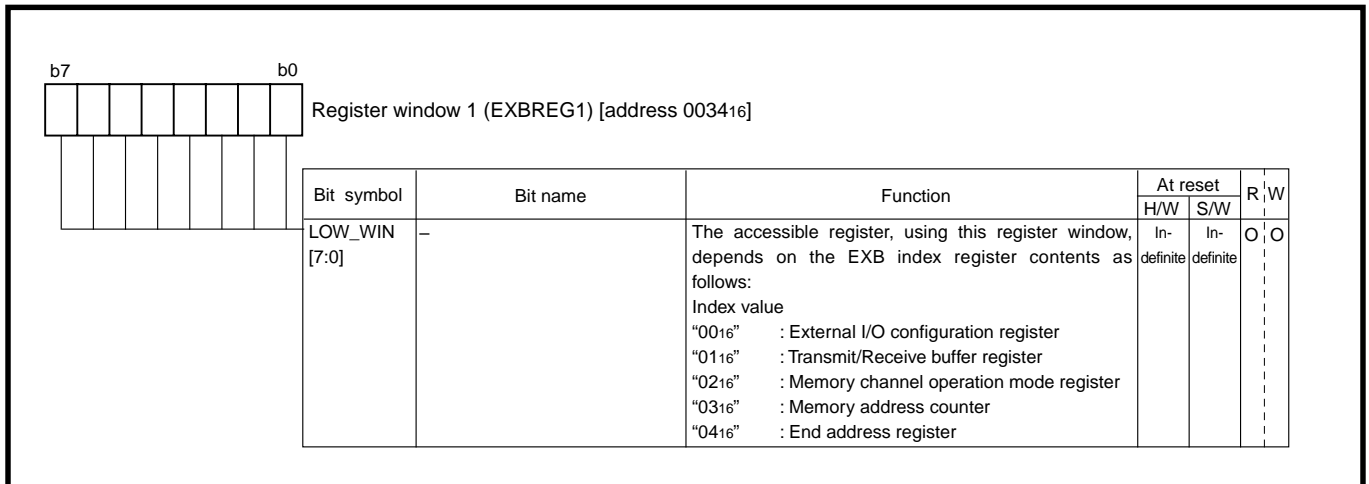


Fig. 3.5.47 Structure of Register window 1

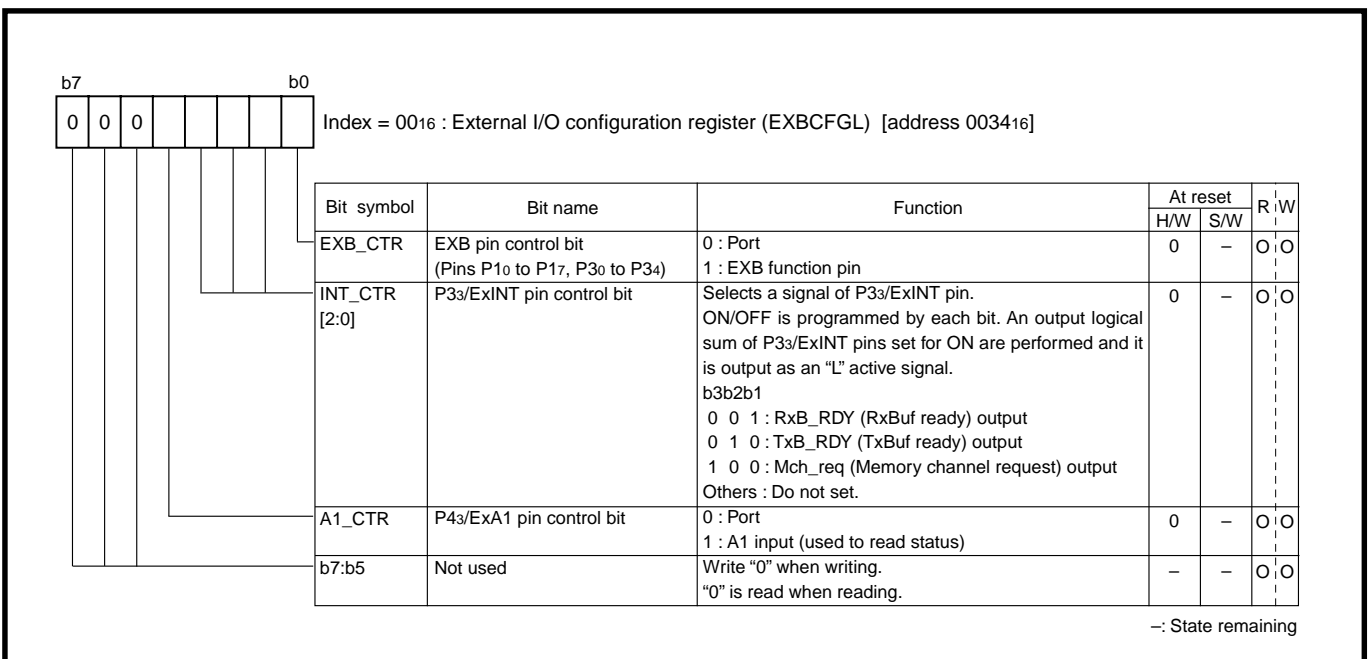


Fig. 3.5.48 Index00[low]; Structure of External I/O configuration register

APPENDIX

3.5 List of registers

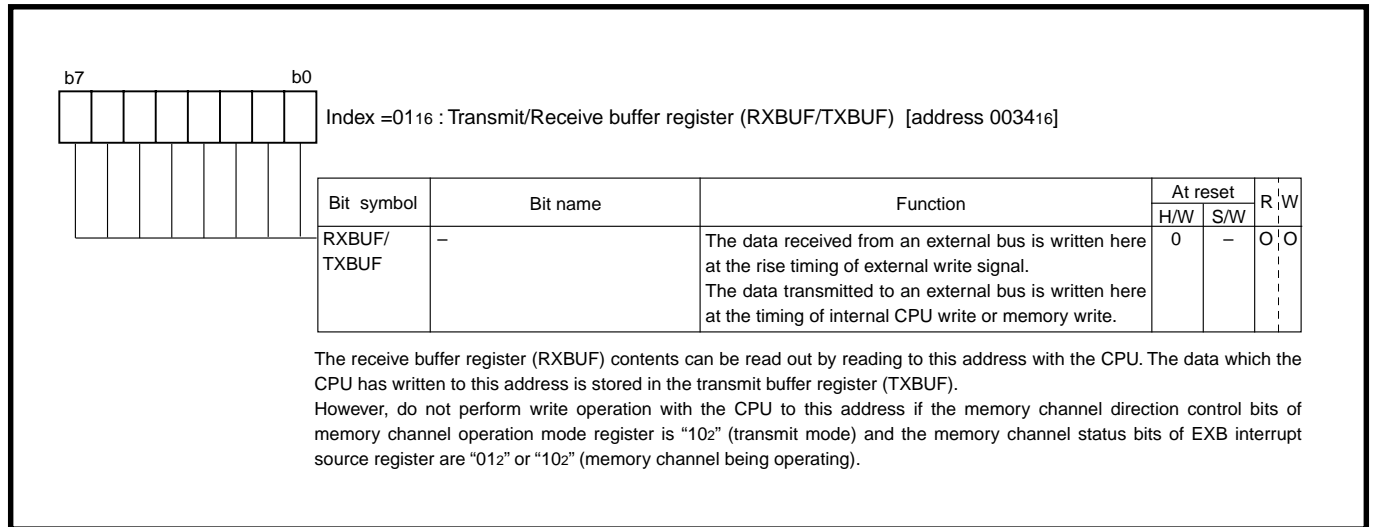


Fig. 3.5.49 Index01[low]; Structure of Transmit/Receive buffer register

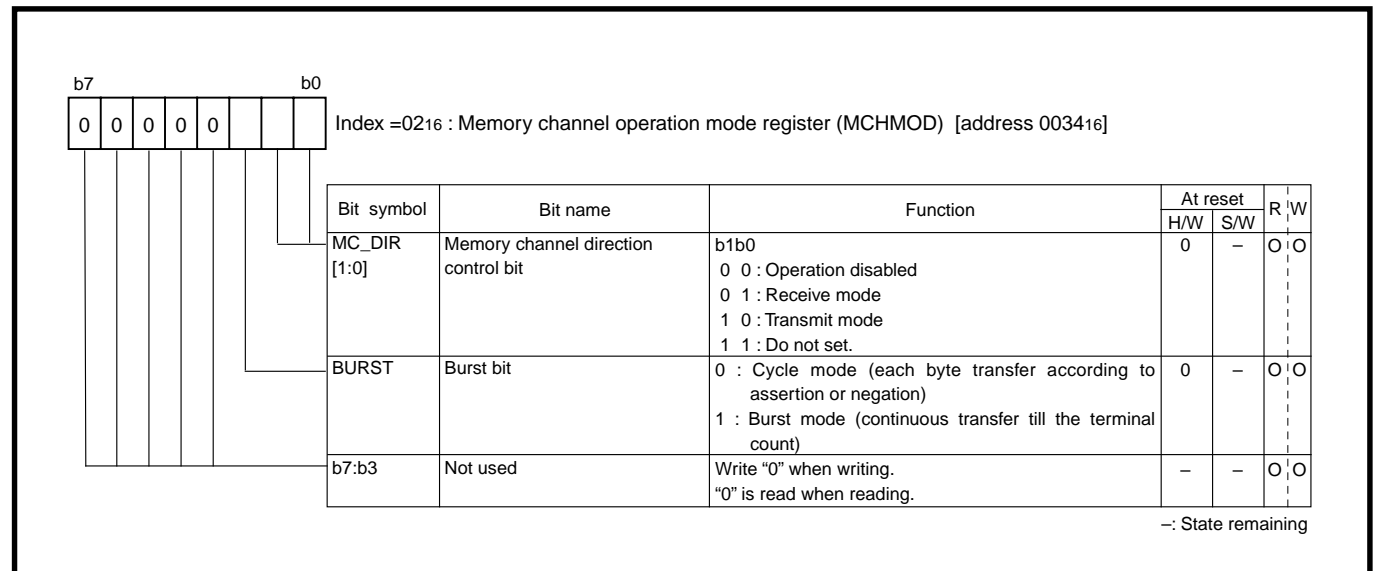


Fig. 3.5.50 Index02[low]; Structure of Memory channel operation mode register

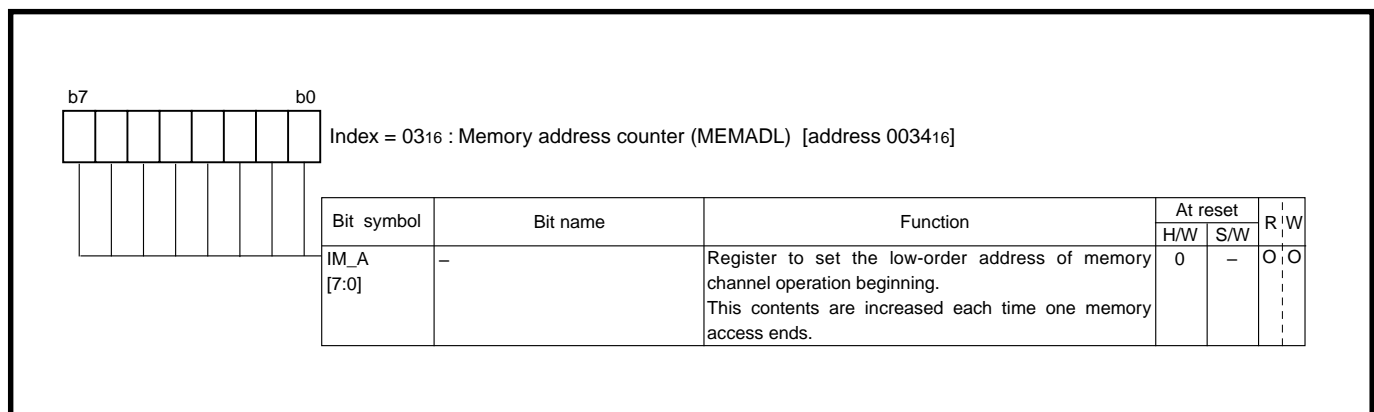


Fig. 3.5.51 Index03[low]; Structure of Memory address counter

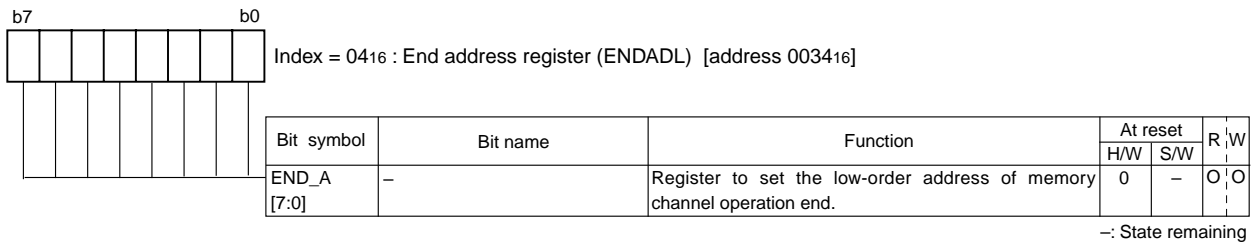


Fig. 3.5.52 Index04[low]; Structure of End address register

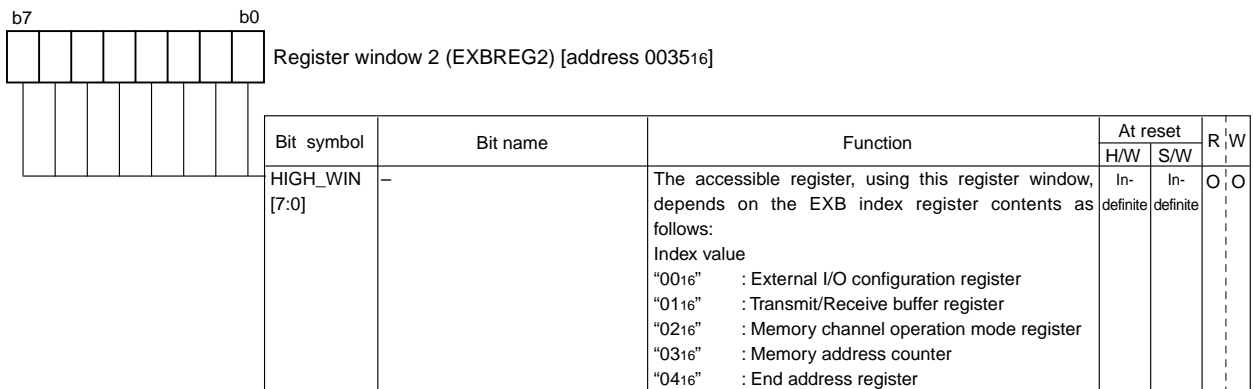


Fig. 3.5.53 Structure of Register window 2

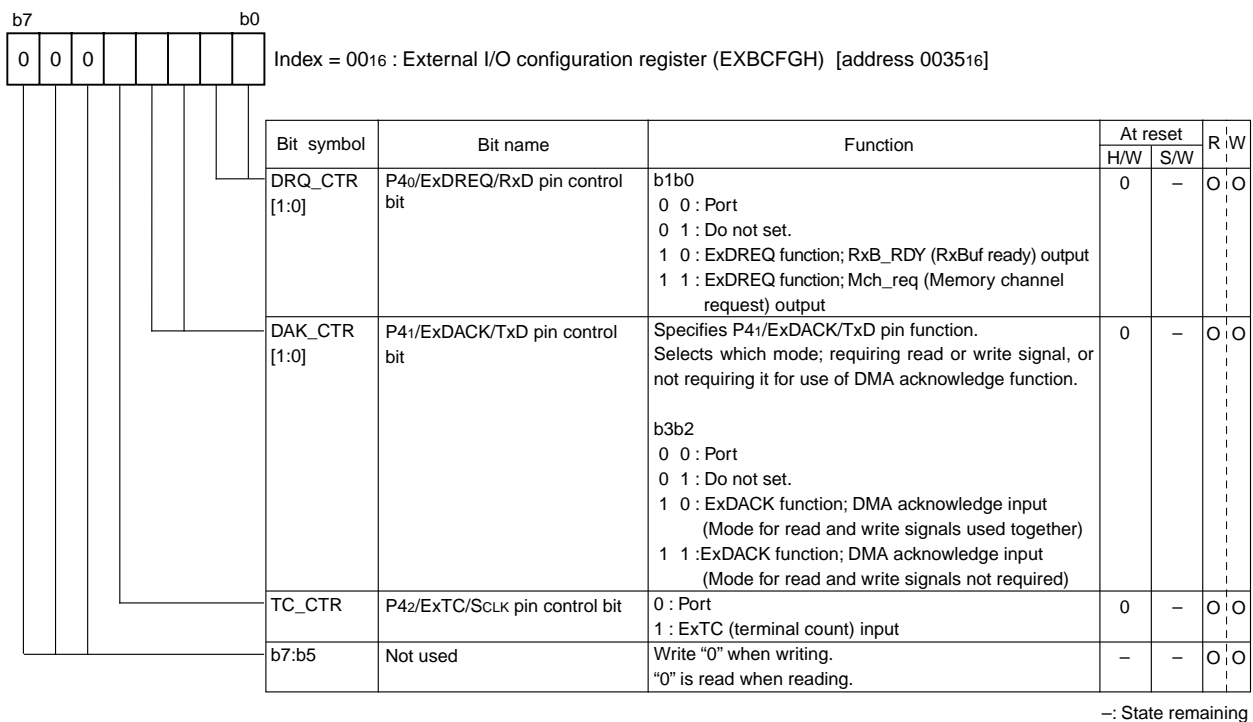


Fig. 3.5.54 Index00[high]; Structure of External I/O configuration register

APPENDIX

3.5 List of registers

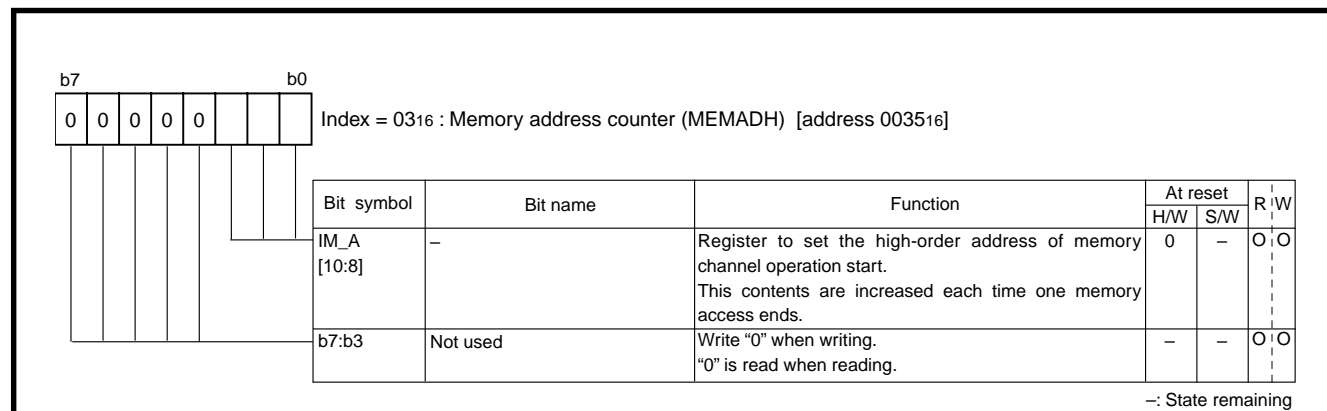


Fig. 3.5.55 Index03[high]; Structure of Memory address counter

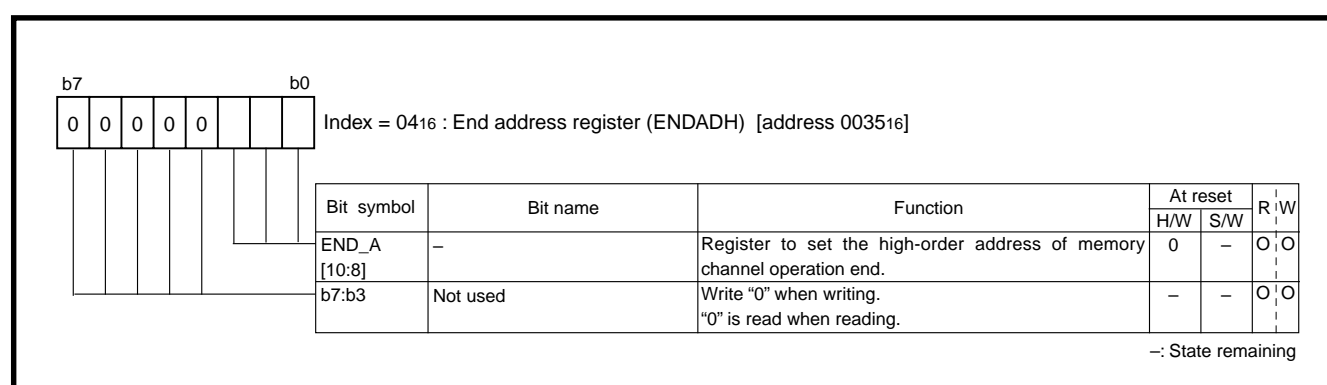


Fig. 3.5.56 Index04[high]; Structure of End address register

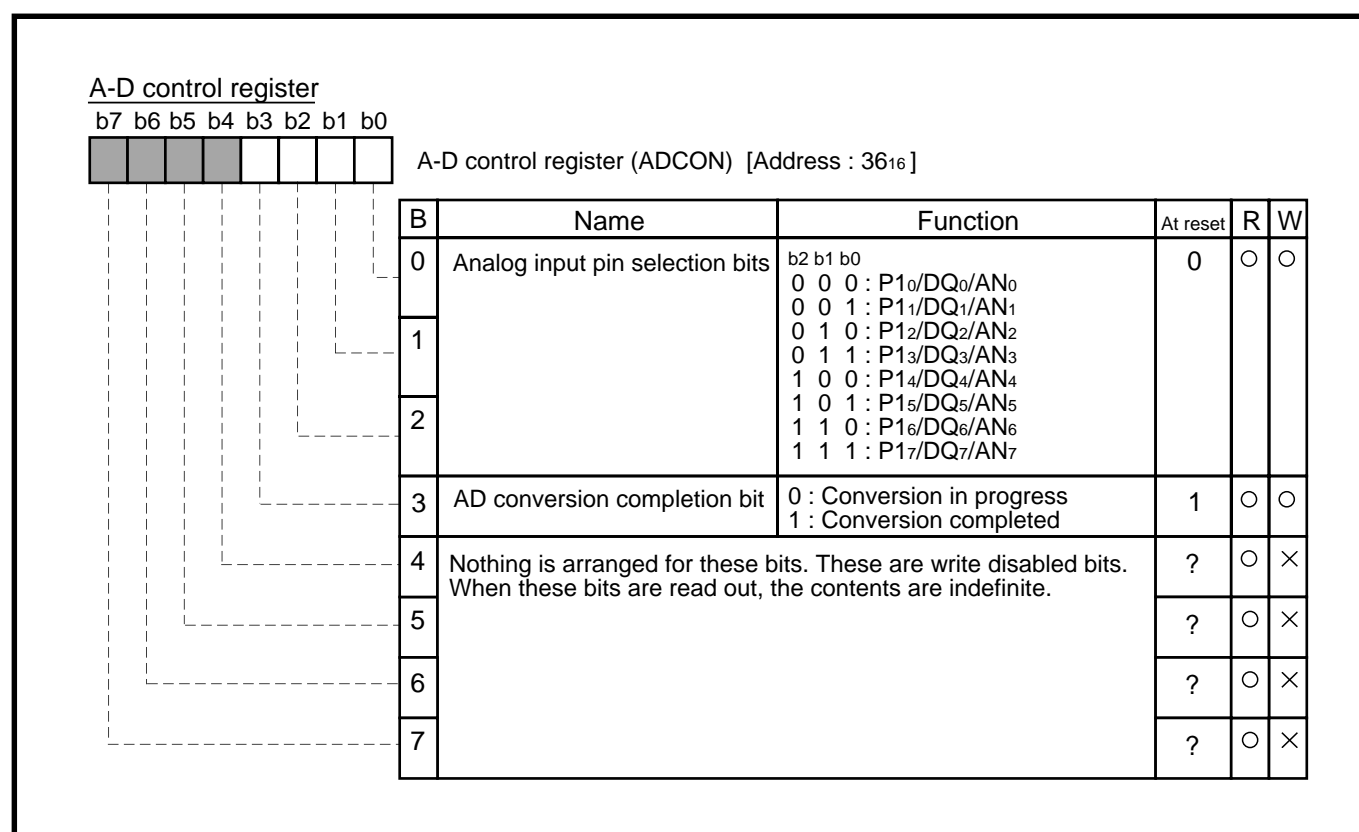
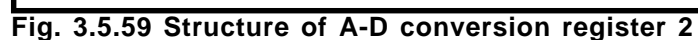


Fig. 3.5.57 Structure of A-D control register

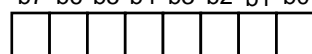


APPENDIX

3.5 List of registers

Watchdog timer control register

b7 b6 b5 b4 b3 b2 b1 b0



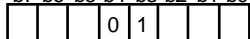
Watchdog timer control register (WDTCON) [Address : 39₁₆]

B	Name	Function	At reset	R	W
0	Watchdog timer H (for read-out of high-order 6 bits)		1	○	×
1			1	○	×
2			1	○	×
3			1	○	×
4			1	○	×
5			1	○	×
6	STP instruction disable bit	0 : STP instruction enabled 1 : STP instruction disabled	0	○	○
7	Watchdog timer H count source selection bit	0 : Watchdog timer L underflow 1 : System clock/16	0	○	○

Fig. 3.5.60 Structure of Watchdog timer control register

CPU mode register

b7 b6 b5 b4 b3 b2 b1 b0



CPU mode register
(CPUM: address 3B₁₆)

B	Name	Function	At reset	R	W
0	Processor mode bits	b1 b0 0 0 : Single-chip mode 0 1 : Not available 1 0 : Not available 1 1 : Not available	0	○	○
1			*	○	○
2			0	○	○
3			1	○	○
4	Fix this bit to "0".		0	○	○
5	System clock selection bit	0 : Main clock f(X _{IN}) 1 : f _{SYN}	0	○	○
6	System clock division ratio selection bits	b7 b6 0 0 : $\phi = f(\text{system clock})/8$ (8-divide mode) 0 1 : $\phi = f(\text{system clock})/4$ (4-divide mode) 1 0 : $\phi = f(\text{system clock})/2$ (2-divide mode) 1 1 : $\phi = f(\text{system clock})$ (Through mode)	0	○	○
7					

*: The initial value of bit 1 depends on the CNVss level.

Fig. 3.5.61 Structure of CPU mode register

Interrupt request register 1

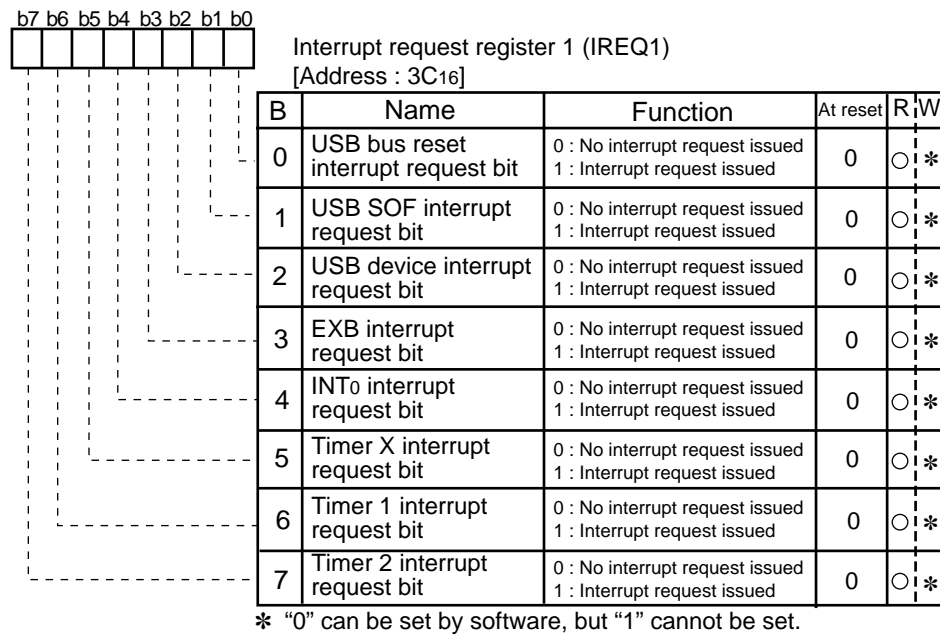


Fig. 3.5.62 Structure of Interrupt request register 1

Interrupt request register 2

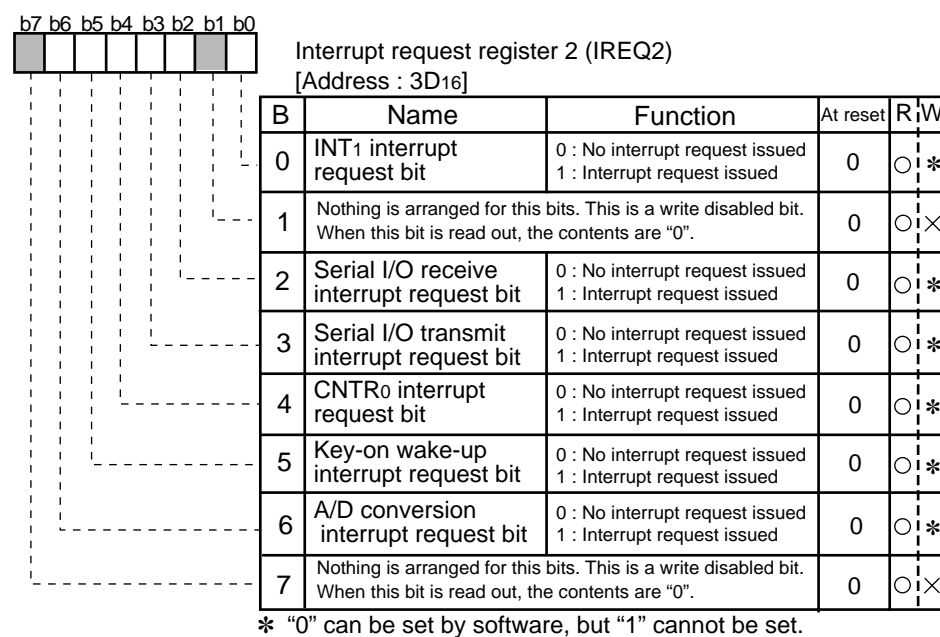


Fig. 3.5.63 Structure of Interrupt request register 2

APPENDIX

3.5 List of registers

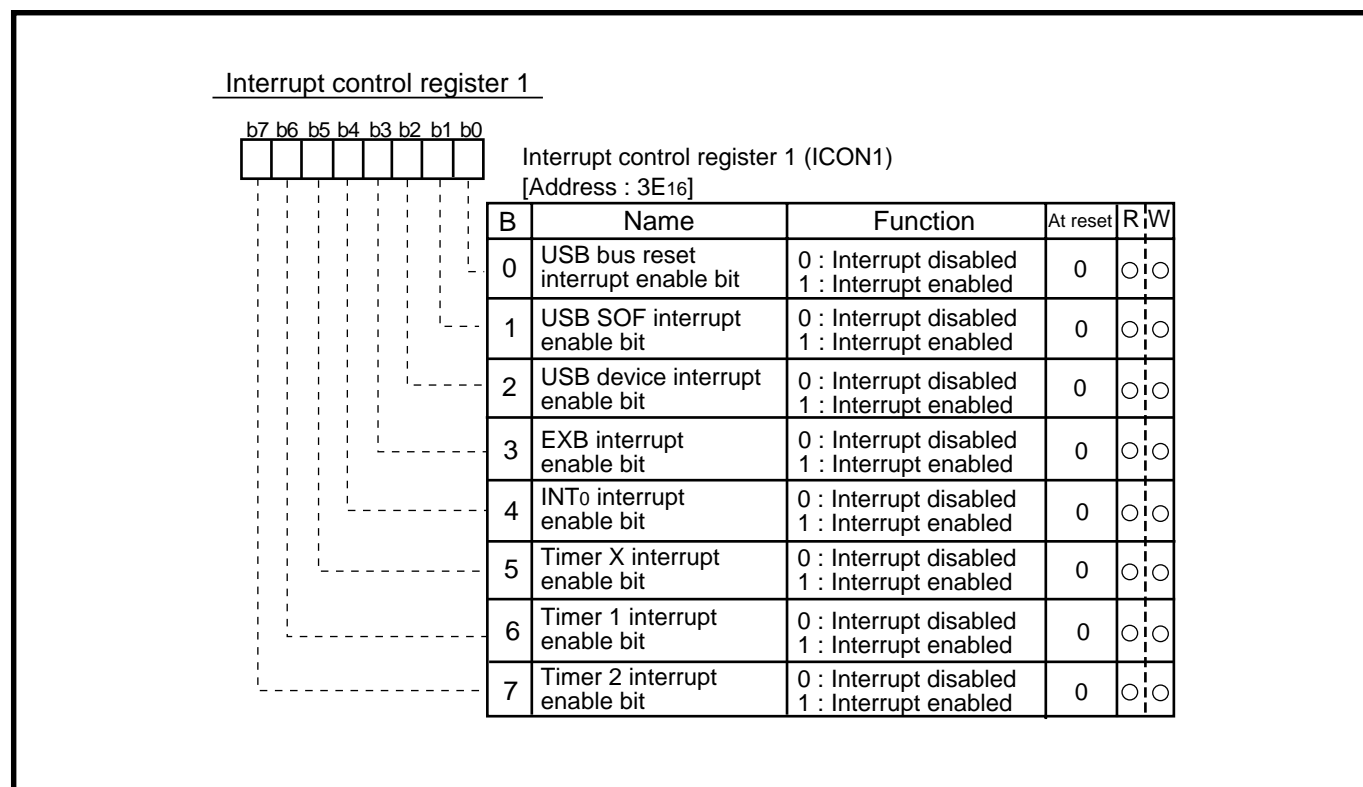


Fig. 3.5.64 Structure of Interrupt control register 1

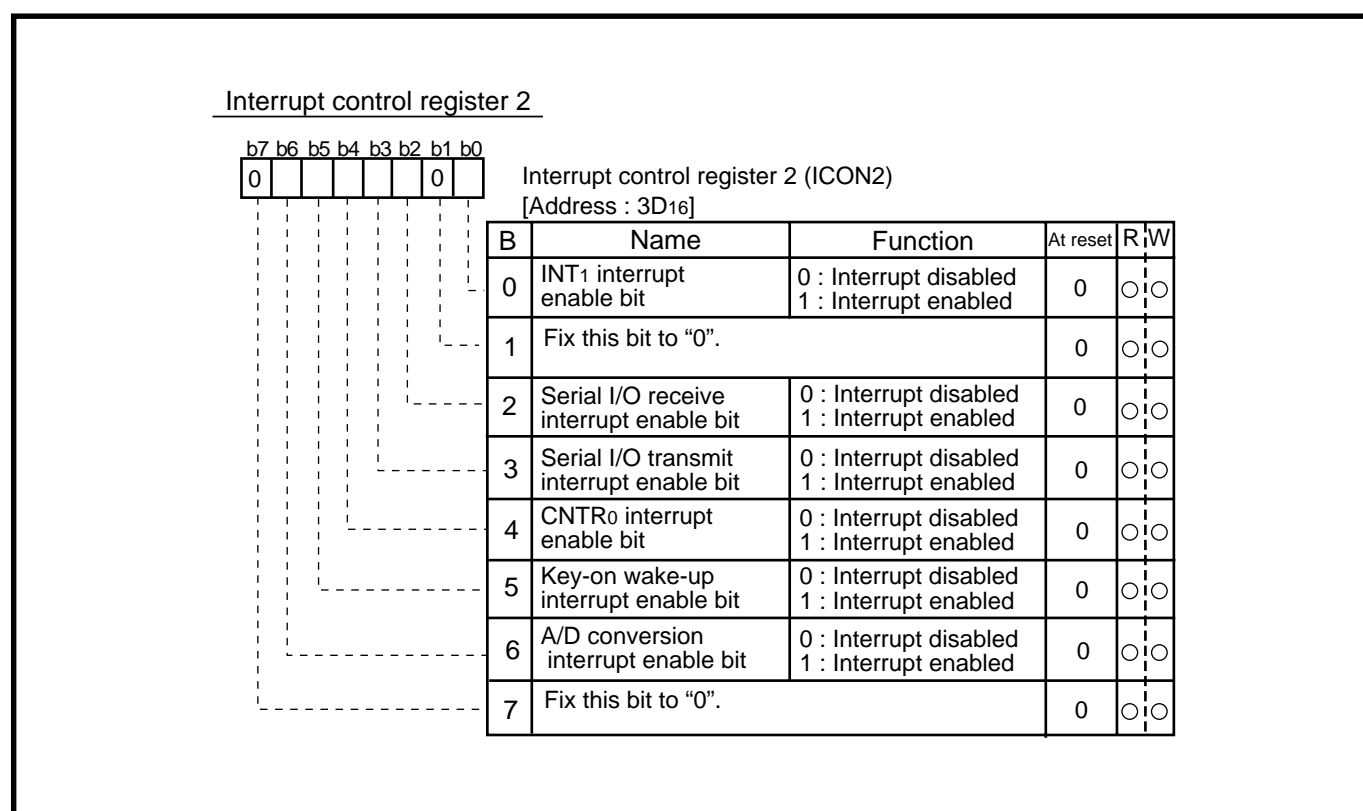
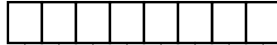


Fig. 3.5.65 Structure of Interrupt control register 2

Serial I/O control register

b7 b6 b5 b4 b3 b2 b1 b0



Serial I/O control register (SIOCON) [Address : 0FE0₁₆]

B	Name	Function	At reset	R	W
0	BRG count source selection bit (CSS)	0 : System clock 1 : System clock/4	0	○	○
1	Serial I/O synchronous clock selection bit (SCS)	<ul style="list-style-type: none"> In clock synchronous serial I/O 0 : BRG output divided by 4 1 : External clock input In UART 0 : BRG output divided by 16 1 : External clock input divided by 16 	0	○	○
2	SRDY output enable bit (SRDY)	0 : P43 pin operates as ordinary I/O pin 1 : P43 pin operates as SRDY output pin	0	○	○
3	Transmit interrupt source selection bit (TIC)	0 : Interrupt when transmit buffer has emptied 1 : Interrupt when transmit shift operation is completed	0	○	○
4	Transmit enable bit (TE)	0 : Transmit disabled 1 : Transmit enabled	0	○	○
5	Receive enable bit (RE)	0 : Receive disabled 1 : Receive enabled	0	○	○
6	Serial I/O mode selection bit (SIOM)	0 : Clock asynchronous(UART) serial I/O 1 : Clock synchronous serial I/O	0	○	○
7	Serial I/O enable bit (SIOE)	0 : Serial I/O disabled (pins P40 to P43 operate as ordinary I/O pins) 1 : Serial I/O enabled (pins P40 to P43 operate as serial I/O pins)	0	○	○

Fig. 3.5.66 Structure of Serial I/O control register

UART control register

b7 b6 b5 b4 b3 b2 b1 b0



UART control register (UARTCON) [Address : 0FE1₁₆]

B	Name	Function	At reset	R	W
0	Character length selection bit (CHAS)	0 : 8 bits 1 : 7 bits	0	○	○
1	Parity enable bit (PARE)	0 : Parity checking disabled 1 : Parity checking enabled	0	○	○
2	Parity selection bit (PARS)	0 : Even parity 1 : Odd parity	0	○	○
3	Stop bit length selection bit (STPS)	0 : 1 stop bit 1 : 2 stop bits	0	○	○
4	Nothing is allocated for this bit. This is a write disabled bit. When this bit is read out, the contents are "0".		0	○	X
5	Nothing is allocated for these bits. These are write disabled bits. When these bits are read out, the contents are "1".		1	○	X
6			1	○	X
7			1	○	X

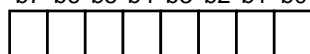
Fig. 3.5.67 Structure of UART control register

APPENDIX

3.5 List of registers

Baud rate generator

b7 b6 b5 b4 b3 b2 b1 b0



Baud rate generator (BRG) [Address : 0FE2₁₆]

B	Function	At reset	R	W
0	Set a count value of baud rate generator.	?	○	○
1		?	○	○
2		?	○	○
3		?	○	○
4		?	○	○
5		?	○	○
6		?	○	○
7		?	○	○

Fig. 3.5.68 Structure of Baud rate generator

b7 b0



EP01 MAX. packet size register (EP01MAX) [address 0FEC₁₆]

Bit symbol	Bit name	Function	At reset		R	W
			H/W	S/W		
MXPS01 [6:0]	Max. packet size bit	IN : These bits are invalid. OUT : Set the maximum packet size.	0	—	○	○
b7	Not used	Write "0" when writing. "0" is read when reading.	—	—	○	○

—: State remaining

Fig. 3.5.69 Structure of EP01 MAX. packet size register

b7 b0



EP02 MAX. packet size register (EP02MAX) [address 0FEC₁₆]

Bit symbol	Bit name	Function	At reset		R	W
			H/W	S/W		
MXPS02 [6:0]	Max. packet size bit	IN : These bits are invalid. OUT : Set the maximum packet size.	0	—	○	○
b7	Not used	Write "0" when writing. "0" is read when reading.	—	—	○	○

—: State remaining

Fig. 3.5.70 Structure of EP02 MAX. packet size register

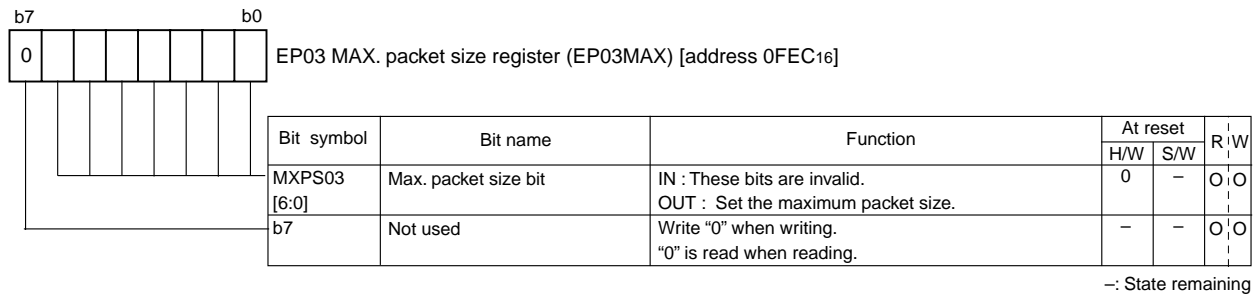


Fig. 3.5.71 Structure of EP03 MAX. packet size register

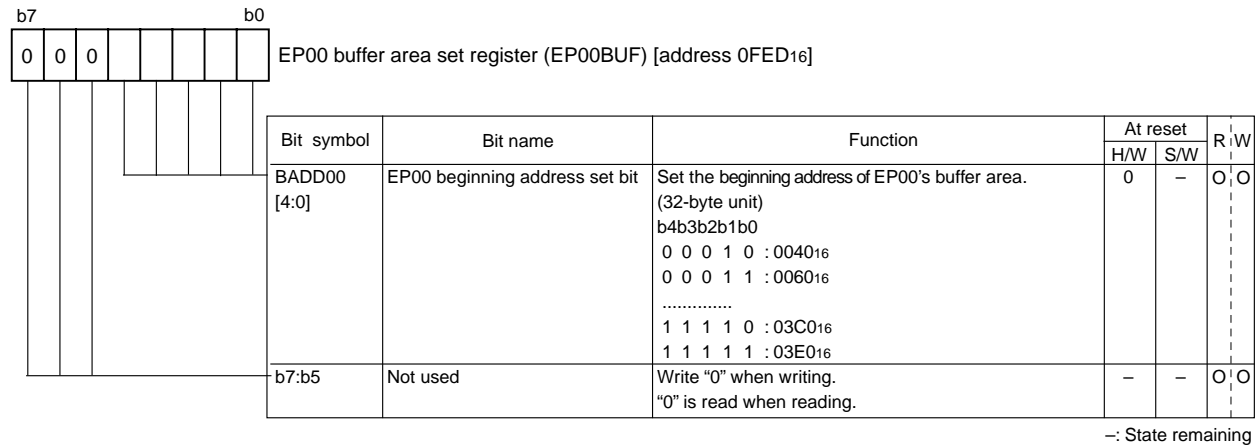


Fig. 3.5.72 Structure of EP00 buffer area set register

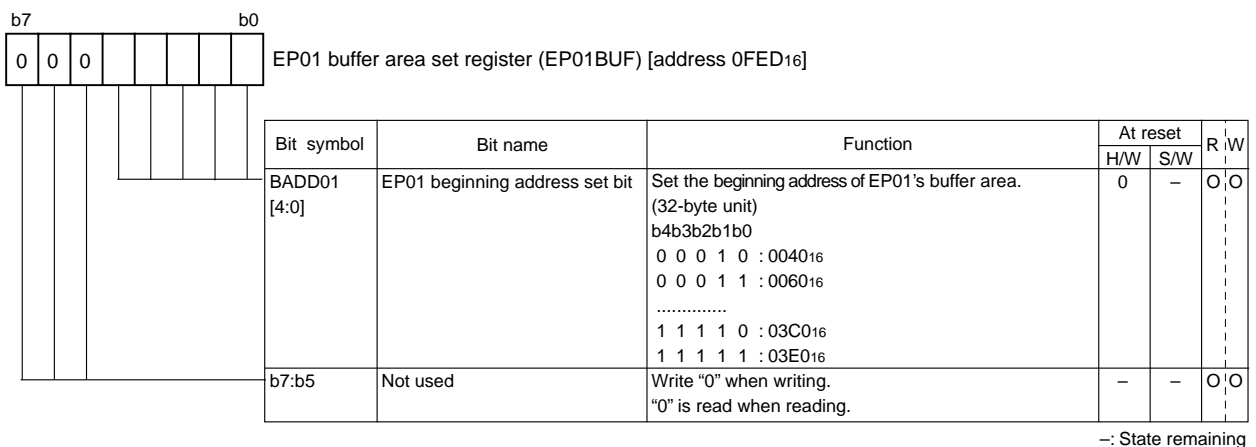


Fig. 3.5.73 Structure of EP01 buffer area set register

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3.5 List of registers

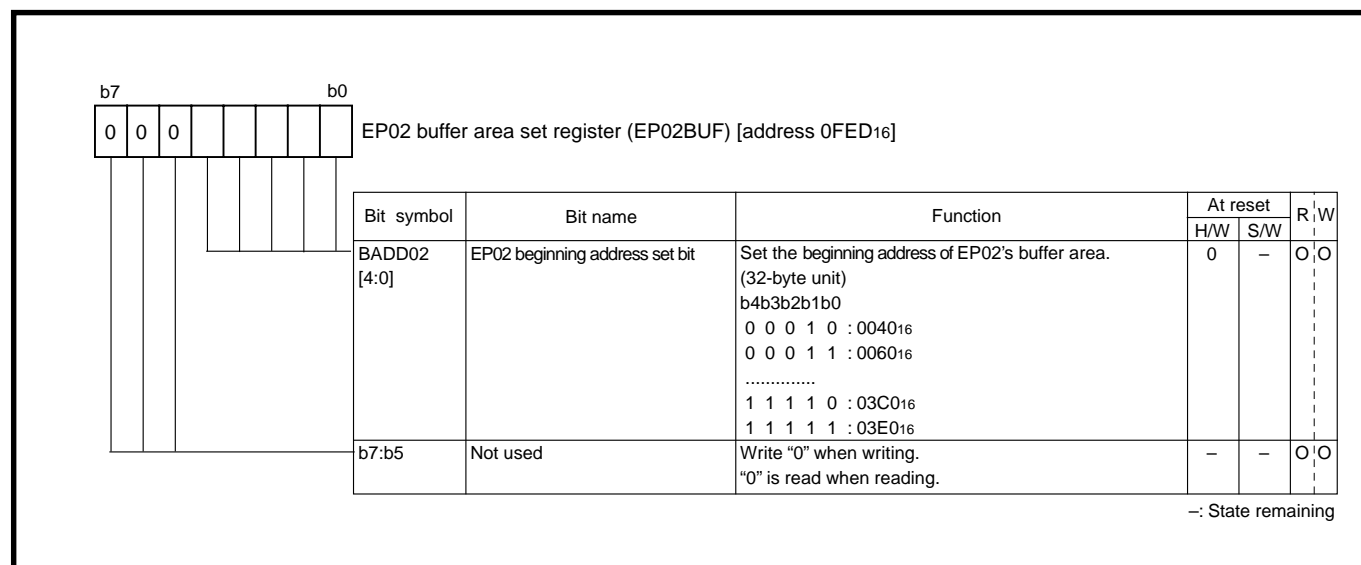


Fig. 3.5.74 Structure of EP02 buffer area set register

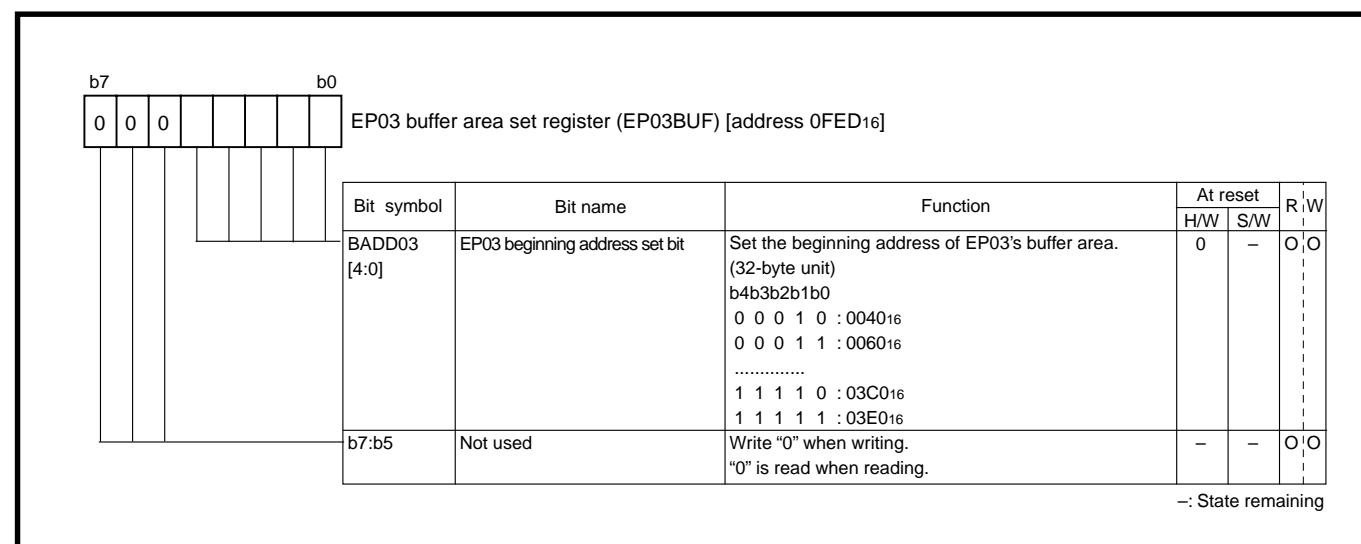
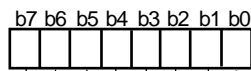


Fig. 3.5.75 Structure of EP03 buffer area set register

Port P0 pull-up control register

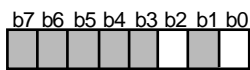


Port P0 pull-up control register (PULL0)
[Address : 0FF0₁₆]

B	Name	Function	At reset	R	W
0	P0 ₀ pul l-up control bit	0 : No pull-up 1 : Pull-up	0	○	○
1	P0 ₀ pul l-up control bit	0 : No pull-up 1 : Pull-up	0	○	○
2	P0 ₀ pul l-up control bit	0 : No pull-up 1 : Pull-up	0	○	○
3	P0 ₀ pul l-up control bit	0 : No pull-up 1 : Pull-up	0	○	○
4	P0 ₀ pul l-up control bit	0 : No pull-up 1 : Pull-up	0	○	○
5	P0 ₀ pul l-up control bit	0 : No pull-up 1 : Pull-up	0	○	○
6	P0 ₀ pul l-up control bit	0 : No pull-up 1 : Pull-up	0	○	○
7	P0 ₀ pul l-up control bit	0 : No pull-up 1 : Pull-up	0	○	○

Fig. 3.5.76 Structure of Port P0 pull-up control register

Port P5 pull-up control register



Port P5 pull-up control register (PULL5)
[Address : 0FF2₁₆]

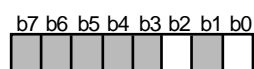
B	Name	Function	At reset	R	W
0	P5 ₀ pul l-up control bit	0 : No pull-up 1 : Pull-up	0	○	○
1	Nothing is arranged for this bit. This is a write disabled bit. When this bit is read out, the contents are "0".		0	○	×
2	P5 ₂ pul l-up control bit	0 : No pull-up 1 : Pull-up	0	○	○
3	Nothing is arranged for these bits. These are write disabled bits. When these bits are read out, the contents are "0".		0	○	×
4			0	○	×
5			0	○	×
6			0	○	×
7			0	○	×

Fig. 3.5.77 Structure of Port P5 pull-up control register

APPENDIX

3.5 List of registers

Interrupt edge selection register

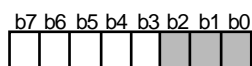


Interrupt edge selection register (INTEDGE)
[Address : 0FF316]

B	Name	Function	At reset	R	W
0	INT ₀ interrupt edge selection bit	0 : Falling edge active 1 : Rising edge active	0	○	○
1	Nothing is arranged for this bits. This is a write disabled bit. When this bit is read out, the contents are "0".		0	○	×
2	INT ₁ interrupt edge selection bit	0 : Falling edge active 1 : Rising edge active	0	○	○
3	Nothing is arranged for these bits. These are write disabled bits. When these bits are read out, the contents are "0".		0	○	×
4			0	○	×
5			0	○	×
6			0	○	×
7			0	○	×

Fig. 3.5.78 Structure of Interrupt edge selection register

PLL control register



PLL control register (PLLCON)
[Address : 0FF816]

B	Name	Function	At reset	R	W
0	Nothing is arranged for these bit. These are write disabled bits. When these bits are read out, the contents are "0".		0	○	×
1					
2					
3	USB clock division ratio selection bits	b4 b3 0 0 : Divided by 8 ($f_{\text{SYN}} = f_{\text{USB}}/8$) 0 1 : Divided by 6 ($f_{\text{SYN}} = f_{\text{USB}}/6$) 1 0 : Divided by 4 ($f_{\text{SYN}} = f_{\text{USB}}/4$) 1 1 : Not selected	0	○	○
4					
5	PLL operation mode selection bits	b6 b5 0 0 : Not multiplied ($f_{\text{VCO}} = f_{\text{XIN}}$) 0 1 : Double ($f_{\text{VCO}} = f_{\text{XIN}} \times 2$) 1 0 : Quadruple ($f_{\text{VCO}} = f_{\text{XIN}} \times 4$) 1 1 : Multiplied by 8 ($f_{\text{VCO}} = f_{\text{XIN}} \times 8$)	0	○	○
6					
7					
7	PLL enable bit	0 : Disabled 1 : Enabled	0	○	○

Fig. 3.5.79 Structure of PLL control register

MISRG

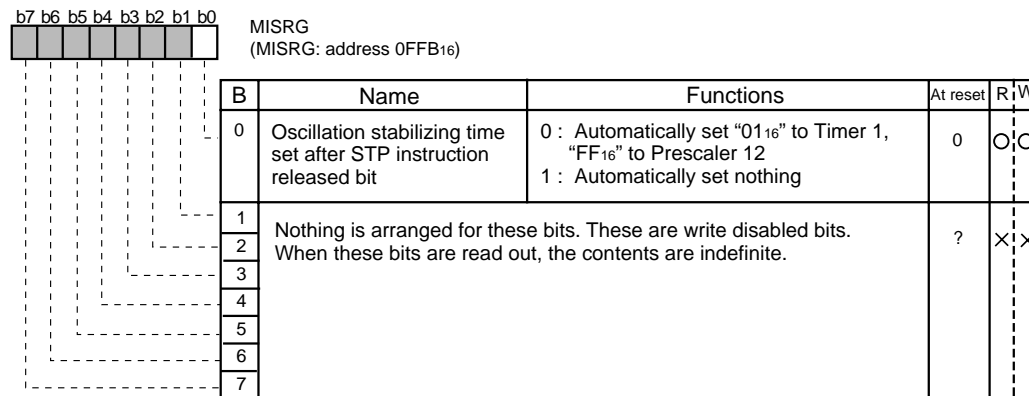
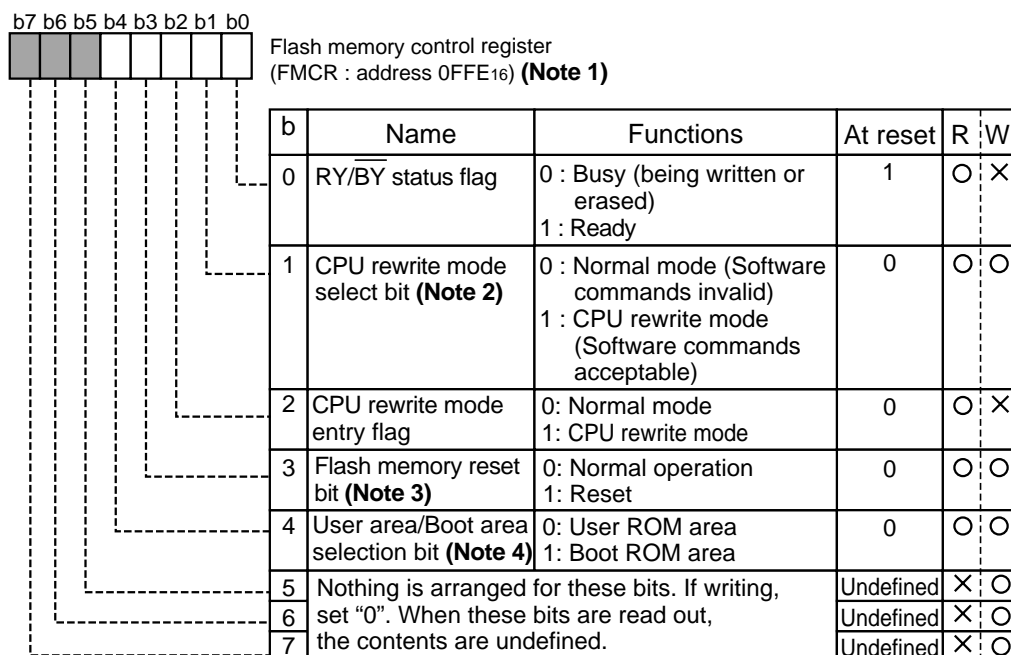


Fig. 3.5.80 Structure of MISRG

Flash memory control register



Notes 1: The contents of flash memory control register are "XXX00001" just after reset release.

2: For this bit to be set to "1", the user needs to write "0" and then "1" to it in succession. If it is not this procedure, this bit will not be set to "1". Additionally, it is required to ensure that no interrupt will be generated during that interval.

Use the control program in the area except the built-in flash memory for write to this bit.

3: This bit is valid when the CPU rewrite mode select bit is "1". Set this bit 3 to "0" subsequently after setting bit 3 to "1".

4: Use the control program in the area except the built-in flash memory for write to this bit.

Fig. 3.5.81 Structure of Flash memory control register

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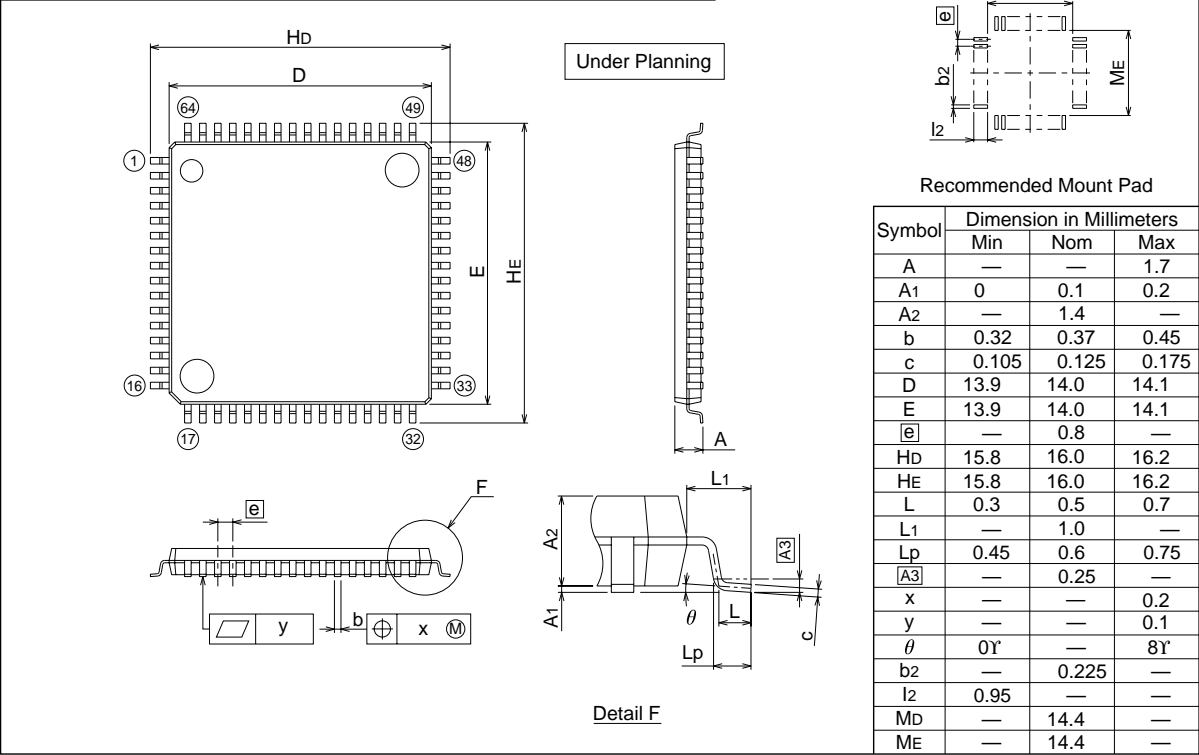
3.6 Package outline

3.6 Package outline

64P6U-A (MMP)

Plastic 64pin 14X14mm body LQFP

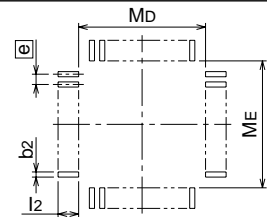
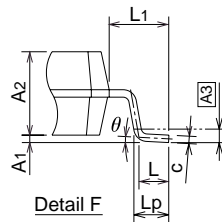
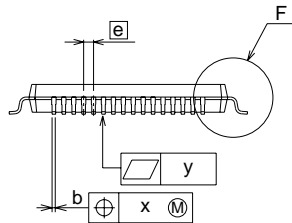
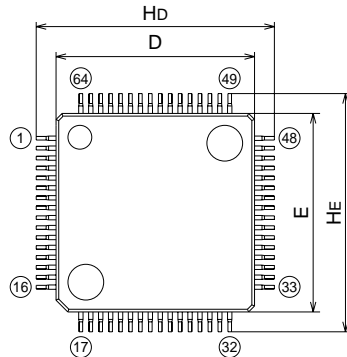
EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP64-P-1414-0.8	—		Cu Alloy



64P6Q-A (MMP)

Plastic 64pin 10X10mm body LQFP

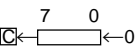
EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP64-P-1010-0.50	—	—	Cu Alloy



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.7
A1	0	0.1	0.2
A2	—	1.4	—
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	9.9	10.0	10.1
E	9.9	10.0	10.1
e	—	0.5	—
Hd	11.8	12.0	12.2
HE	11.8	12.0	12.2
L	0.3	0.5	0.7
L1	—	1.0	—
Lp	0.45	0.6	0.75
A3	—	0.25	—
x	—	—	0.08
y	—	—	0.1
θ	0°	—	10°
b2	—	0.225	—
l2	1.0	—	—
MD	—	10.4	—
ME	—	10.4	—

3.7 Machine instructions

Symbol	Function	Details	Addressing mode																	
			IMP			IMM			A			BIT, A, R			ZP			BIT, ZP, R		
			OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#
ADC (Note 1) (Note 5)	When T = 0 $A \leftarrow A + M + C$ When T = 1 $M(X) \leftarrow M(X) + M + C$	When T = 0, this instruction adds the contents M, C, and A; and stores the results in A and C. When T = 1, this instruction adds the contents of M(X), M and C; and stores the results in M(X) and C. When T=1, the contents of A remain unchanged, but the contents of status flags are changed. M(X) represents the contents of memory where is indicated by X.				69	2	2							65	3	2			
AND (Note 1)	When T = 0 $A \leftarrow A \wedge M$ When T = 1 $M(X) \leftarrow M(X) \wedge M$	When T = 0, this instruction transfers the contents of A and M to the ALU which performs a bit-wise AND operation and stores the result back in A. When T = 1, this instruction transfers the contents M(X) and M to the ALU which performs a bit-wise AND operation and stores the results back in M(X). When T = 1 the contents of A remain unchanged, but status flags are changed. M(X) represents the contents of memory where is indicated by X.				29	2	2							25	3	2			
ASL		This instruction shifts the content of A or M by one bit to the left, with bit 0 always being set to 0 and bit 7 of A or M always being contained in C.							0A	2	1				06	5	2			
BBC (Note 4)	Ai or Mi = 0?	This instruction tests the designated bit i of M or A and takes a branch if the bit is 0. The branch address is specified by a relative address. If the bit is 1, next instruction is executed.										13 20i	4	2				17 20i	5	3
BBS (Note 4)	Ai or Mi = 1?	This instruction tests the designated bit i of the M or A and takes a branch if the bit is 1. The branch address is specified by a relative address. If the bit is 0, next instruction is executed.										03 20i	4	2				07 20i	5	3
BCC (Note 4)	C = 0?	This instruction takes a branch to the appointed address if C is 0. The branch address is specified by a relative address. If C is 1, the next instruction is executed.																		
BCS (Note 4)	C = 1?	This instruction takes a branch to the appointed address if C is 1. The branch address is specified by a relative address. If C is 0, the next instruction is executed.																		
BEQ (Note 4)	Z = 1?	This instruction takes a branch to the appointed address when Z is 1. The branch address is specified by a relative address. If Z is 0, the next instruction is executed.																		
BIT	$A \wedge M$	This instruction takes a bit-wise logical AND of A and M contents; however, the contents of A and M are not modified. The contents of N, V, Z are changed, but the contents of A, M remain unchanged.													24	3	2			
BMI (Note 4)	N = 1?	This instruction takes a branch to the appointed address when N is 1. The branch address is specified by a relative address. If N is 0, the next instruction is executed.																		
BNE (Note 4)	Z = 0?	This instruction takes a branch to the appointed address if Z is 0. The branch address is specified by a relative address. If Z is 1, the next instruction is executed.																		

Addressing mode																								Processor status register																
ZP, X			ZP, Y			ABS			ABS, X			ABS, Y			IND			ZP, IND			IND, X			IND, Y			REL			SP			7	6	5	4	3	2	1	0
OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	N	V	T	B	D	I	Z	C			
75	4	2				6D	4	3	7D	5	3	79	5	3							61	6	2	71	6	2				N	V	•	•	•	•	Z	C			
35	4	2				2D	4	3	3D	5	3	39	5	3							21	6	2	31	6	2				N	•	•	•	•	•	Z	•			
16	6	2				0E	6	3	1E	7	3																		N	•	•	•	•	•	Z	C				
																															•	•	•	•	•	•	•	•		
																															•	•	•	•	•	•	•	•		
																															•	•	•	•	•	•	•	•		
																										90	2	2			•	•	•	•	•	•	•	•		
																										B0	2	2			•	•	•	•	•	•	•	•		
																										F0	2	2			•	•	•	•	•	•	•	•		
						2C	4	3																					M7	M6	•	•	•	•	•	Z	•			
																															•	•	•	•	•	•	•	•		
																										30	2	2			•	•	•	•	•	•	•	•		
																										D0	2	2			•	•	•	•	•	•	•	•		

Symbol	Function	Details	Addressing mode																	
			IMP			IMM			A			BIT, A			ZP			BIT, ZP		
			OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#
BPL (Note 4)	N = 0?	This instruction takes a branch to the appointed address if N is 0. The branch address is specified by a relative address. If N is 1, the next instruction is executed.																		
BRA	PC ← PC ± offset	This instruction branches to the appointed address. The branch address is specified by a relative address.																		
BRK	B ← 1 (PC) ← (PC) + 2 M(S) ← PCH S ← S − 1 M(S) ← PCL S ← S − 1 M(S) ← PS S ← S − 1 I ← 1 PCL ← ADL PCH ← ADH	When the BRK instruction is executed, the CPU pushes the current PC contents onto the stack. The BADRS designated in the interrupt vector table is stored into the PC.	00	7	1															
BVC (Note 4)	V = 0?	This instruction takes a branch to the appointed address if V is 0. The branch address is specified by a relative address. If V is 1, the next instruction is executed.																		
BVS (Note 4)	V = 1?	This instruction takes a branch to the appointed address when V is 1. The branch address is specified by a relative address. When V is 0, the next instruction is executed.																		
CLB	Ai or Mi ← 0	This instruction clears the designated bit i of A or M.										1B 20i	2	1				1F 20i	5	2
CLC	C ← 0	This instruction clears C.	18	2	1															
CLD	D ← 0	This instruction clears D.	D8	2	1															
CLI	I ← 0	This instruction clears I.	58	2	1															
CLT	T ← 0	This instruction clears T.	12	2	1															
CLV	V ← 0	This instruction clears V.	B8	2	1															
CMP (Note 3)	When T = 0 A − M When T = 1 M(X) − M	When T = 0, this instruction subtracts the contents of M from the contents of A. The result is not stored and the contents of A or M are not modified. When T = 1, the CMP subtracts the contents of M from the contents of M(X). The result is not stored and the contents of X, M, and A are not modified. M(X) represents the contents of memory where is indicated by X.				C9	2	2							C5	3	2			
COM	M ← M	This instruction takes the one's complement of the contents of M and stores the result in M.													44	5	2			
CPX	X − M	This instruction subtracts the contents of M from the contents of X. The result is not stored and the contents of X and M are not modified.				E0	2	2							E4	3	2			
CPY	Y − M	This instruction subtracts the contents of M from the contents of Y. The result is not stored and the contents of Y and M are not modified.				C0	2	2							C4	3	2			
DEC	A ← A − 1 or M ← M − 1	This instruction subtracts 1 from the contents of A or M.							1A	2	1				C6	5	2			

Addressing mode																											Processor status register													
ZP, X			ZP, Y			ABS			ABS, X			ABS, Y			IND			ZP, IND			IND, X			IND, Y			REL			SP			7	6	5	4	3	2	1	0
OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	N	V	T	B	D	I	Z	C			
																														•	•	•	•	•	•	•	•			
																														•	•	•	•	•	•	•	•			
																														•	•	•	1	•	1	•	•			
																														•	•	•	•	•	•	•	•			
																														•	•	•	•	•	•	•	•			
																														•	•	•	•	•	•	•	•			
																														•	•	•	•	•	•	•	•			
																														•	•	•	•	•	•	•	•			
																														•	•	•	•	•	•	•	•			
																														•	•	•	•	•	•	•	•			
																														•	•	•	•	•	•	•	•			
																														•	•	•	•	•	•	•	•			
																														•	•	•	•	•	•	•	•			
D5	4	2							CD	4	3	DD	5	3	D9	5	3													N	•	•	•	•	•	•	Z	C		
														</																										

Symbol	Function	Details	Addressing mode																	
			IMP			IMM			A			BIT, A			ZP			BIT, ZP		
			OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#
DEX	$X \leftarrow X - 1$	This instruction subtracts one from the current contents of X.	CA	2	1															
DEY	$Y \leftarrow Y - 1$	This instruction subtracts one from the current contents of Y.	88	2	1															
DIV	$A \leftarrow (M(zz + X + 1), M(zz + X)) / A$ $M(S) \leftarrow \text{one's complement of Remainder}$ $S \leftarrow S - 1$	Divides the 16-bit data in M(zz+(X)) (low-order byte) and M(zz+(X)+1) (high-order byte) by the contents of A. The quotient is stored in A and the one's complement of the remainder is pushed onto the stack.																		
EOR (Note 1)	When T = 0 $A \leftarrow A \vee M$ When T = 1 $M(X) \leftarrow M(X) \vee M$	When T = 0, this instruction transfers the contents of the M and A to the ALU which performs a bit-wise Exclusive OR, and stores the result in A. When T = 1, the contents of M(X) and M are transferred to the ALU, which performs a bit-wise Exclusive OR and stores the results in M(X). The contents of A remain unchanged, but status flags are changed. M(X) represents the contents of memory where is indicated by X.				49	2	2							45	3	2			
INC	$A \leftarrow A + 1$ or $M \leftarrow M + 1$	This instruction adds one to the contents of A or M.							3A	2	1				E6	5	2			
INX	$X \leftarrow X + 1$	This instruction adds one to the contents of X.	E8	2	1															
INY	$Y \leftarrow Y + 1$	This instruction adds one to the contents of Y.	C8	2	1															
JMP	If addressing mode is ABS $PCL \leftarrow ADL$ $PCH \leftarrow ADH$ If addressing mode is IND $PCL \leftarrow M(ADH, ADL)$ $PCH \leftarrow M(ADH, ADL + 1)$ If addressing mode is ZP, IND $PCL \leftarrow M(00, ADL)$ $PCH \leftarrow M(00, ADL + 1)$	This instruction jumps to the address designated by the following three addressing modes: Absolute Indirect Absolute Zero Page Indirect Absolute																		
JSR	$M(S) \leftarrow PCH$ $S \leftarrow S - 1$ $M(S) \leftarrow PCL$ $S \leftarrow S - 1$ After executing the above, if addressing mode is ABS, $PCL \leftarrow ADL$ $PCH \leftarrow ADH$ if addressing mode is SP, $PCL \leftarrow ADL$ $PCH \leftarrow FF$ If addressing mode is ZP, IND, $PCL \leftarrow M(00, ADL)$ $PCH \leftarrow M(00, ADL + 1)$	This instruction stores the contents of the PC in the stack, then jumps to the address designated by the following addressing modes: Absolute Special Page Zero Page Indirect Absolute																		
LDA (Note 2)	When T = 0 $A \leftarrow M$ When T = 1 $M(X) \leftarrow M$	When T = 0, this instruction transfers the contents of M to A. When T = 1, this instruction transfers the contents of M to (M(X)). The contents of A remain unchanged, but status flags are changed. M(X) represents the contents of memory where is indicated by X.				A9	2	2							A5	3	2			
LDM	$M \leftarrow nn$	This instruction loads the immediate value in M.													3C	4	3			
LDX	$X \leftarrow M$	This instruction loads the contents of M in X.				A2	2	2							A6	3	2			
LDY	$Y \leftarrow M$	This instruction loads the contents of M in Y.				A0	2	2							A4	3	2			

Addressing mode																											Processor status register													
ZP, X			ZP, Y			ABS			ABS, X			ABS, Y			IND			ZP, IND			IND, X			IND, Y			REL			SP			7	6	5	4	3	2	1	0
OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	N	V	T	B	D	I	Z	C			
																														N	•	•	•	•	•	•	Z	•		
																														N	•	•	•	•	•	•	Z	•		
E2	16	2																												•	•	•	•	•	•	•	•	•		
55	4	2				4D	4	3	5D	5	3	59	5	3							41	6	2	51	6	2				N	•	•	•	•	•	•	Z	•		
F6	6	2				EE	6	3	FE	7	3																			N	•	•	•	•	•	•	Z	•		
																															N	•	•	•	•	•	•	Z	•	
																															N	•	•	•	•	•	•	Z	•	
						4C	3	3							6C	5	3	B2	4	2										•	•	•	•	•	•	•	•	•		
						20	6	3										02	7	2								22	5	2	•	•	•	•	•	•	•	•	•	
B5	4	2				AD	4	3	BD	5	3	B9	5	3							A1	6	2	B1	6	2				N	•	•	•	•	•	•	Z	•		
																															•	•	•	•	•	•	•	•	•	
																															•	•	•	•	•	•	•	•	•	
																															N	•	•	•	•	•	•	Z	•	
B4	4	2				AC	4	3	BC	5	3																			N	•	•	•	•	•	•	Z	•		

Symbol	Function	Details	Addressing mode											
			IMP			IMM			A			BIT, A		
			OP	n	#	OP	n	#	OP	n	#	OP	n	#
LSR	$7 \quad 0$ $0 \rightarrow \boxed{} \rightarrow \boxed{C}$	This instruction shifts either A or M one bit to the right such that bit 7 of the result always is set to 0, and the bit 0 is stored in C.							4A	2	1			
MUL	$M(S) \bullet A \leftarrow A * M(zz + X)$ $S \leftarrow S - 1$	Multiplies Accumulator with the memory specified by the Zero Page X address mode and stores the high-order byte of the result on the Stack and the low-order byte in A.												
NOP	$PC \leftarrow PC + 1$	This instruction adds one to the PC but does no other operation.	EA	2	1									
ORA (Note 1)	When $T = 0$ $A \leftarrow A \vee M$ When $T = 1$ $M(X) \leftarrow M(X) \vee M$	When $T = 0$, this instruction transfers the contents of A and M to the ALU which performs a bit-wise "OR", and stores the result in A. When $T = 1$, this instruction transfers the contents of M(X) and the M to the ALU which performs a bit-wise OR, and stores the result in M(X). The contents of A remain unchanged, but status flags are changed. M(X) represents the contents of memory where is indicated by X.				09	2	2				05	3	2
PHA	$S \leftarrow S - 1$	This instruction pushes the contents of A to the memory location designated by S, and decrements the contents of S by one.	48	3	1									
PHP	$M(S) \leftarrow PS$ $S \leftarrow S - 1$	This instruction pushes the contents of PS to the memory location designated by S and decrements the contents of S by one.	08	3	1									
PLA	$S \leftarrow S + 1$ $A \leftarrow M(S)$	This instruction increments S by one and stores the contents of the memory designated by S in A.	68	4	1									
PLP	$S \leftarrow S + 1$ $PS \leftarrow M(S)$	This instruction increments S by one and stores the contents of the memory location designated by S in PS.	28	4	1									
ROL	$7 \quad 0$ $\leftarrow \boxed{} \leftarrow \boxed{C}$	This instruction shifts either A or M one bit left through C. C is stored in bit 0 and bit 7 is stored in C.							2A	2	1			
ROR	$7 \quad 0$ $\boxed{C} \rightarrow \boxed{} \rightarrow$	This instruction shifts either A or M one bit right through C. C is stored in bit 7 and bit 0 is stored in C.							6A	2	1			
RRF	$7 \quad 0$ $\rightarrow \boxed{} \rightarrow$	This instruction rotates 4 bits of the M content to the right.												
RTI	$S \leftarrow S + 1$ $PS \leftarrow M(S)$ $S \leftarrow S + 1$ $PCL \leftarrow M(S)$ $S \leftarrow S + 1$ $PCH \leftarrow M(S)$	This instruction increments S by one, and stores the contents of the memory location designated by S in PS. S is again incremented by one and stores the contents of the memory location designated by S in PCL. S is again incremented by one and stores the contents of memory location designated by S in PCH.	40	6	1									
RTS	$S \leftarrow S + 1$ $PCL \leftarrow M(S)$ $S \leftarrow S + 1$ $PCH \leftarrow M(S)$ $(PC) \leftarrow (PC) + 1$	This instruction increments S by one and stores the contents of the memory location designated by S in PCL. S is again incremented by one and the contents of the memory location is stored in PCH. PC is incremented by 1.	60	6	1									

Addressing mode																												Processor status register												
ZP, X			ZP, Y			ABS			ABS, X			ABS, Y			IND			ZP, IND			IND, X			IND, Y			REL			SP			7	6	5	4	3	2	1	0
OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	N	V	T	B	D	I	Z	C			
56	6	2				4E	6	3	5E	7	3																		0	Z	C			
62	15	2																													
																															
15	4	2				0D	4	3	1D	5	3	19	5	3						01	6	2	11	6	2				N	Z	.			
																															
																															
																													N	Z	.			
																													(Value saved in stack)											
36	6	2				2E	6	3	3E	7	3																		N	Z	C			
76	6	2				6E	6	3	7E	7	3																		N	Z	C			
																															
																													(Value saved in stack)											
																															

Symbol	Function	Details	Addressing mode																	
			IMP			IMM			A			BIT, A			ZP			BIT, ZP		
			OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#
SBC (Note 1) (Note 5)	When T = 0 $A \leftarrow A - M - C$ When T = 1 $M(X) \leftarrow M(X) - M - C$	When T = 0, this instruction subtracts the value of M and the complement of C from A, and stores the results in A and C. When T = 1, the instruction subtracts the contents of M and the complement of C from the contents of M(X), and stores the results in M(X) and C. A remain unchanged, but status flag are changed. M(X) represents the contents of memory where is indicated by X.				E9	2	2							E5	3	2			
SEB	A_i or $M_i \leftarrow 1$	This instruction sets the designated bit i of A or M.										0B 20i	2	1				0F 20i	5	2
SEC	$C \leftarrow 1$	This instruction sets C.	38	2	1															
SED	$D \leftarrow 1$	This instruction set D.	F8	2	1															
SEI	$I \leftarrow 1$	This instruction set I.	78	2	1															
SET	$T \leftarrow 1$	This instruction set T.	32	2	1															
STA	$M \leftarrow A$	This instruction stores the contents of A in M. The contents of A does not change.													85	4	2			
STP		This instruction resets the oscillation control F/ F and the oscillation stops. Reset or interrupt input is needed to wake up from this mode.	42	2	1															
STX	$M \leftarrow X$	This instruction stores the contents of X in M. The contents of X does not change.													86	4	2			
STY	$M \leftarrow Y$	This instruction stores the contents of Y in M. The contents of Y does not change.													84	4	2			
TAX	$X \leftarrow A$	This instruction stores the contents of A in X. The contents of A does not change.	AA	2	1															
TAY	$Y \leftarrow A$	This instruction stores the contents of A in Y. The contents of A does not change.	A8	2	1															
TST	$M = 0?$	This instruction tests whether the contents of M are "0" or not and modifies the N and Z.													64	3	2			
TSX	$X \leftarrow S$	This instruction transfers the contents of S in X.	BA	2	1															
TXA	$A \leftarrow X$	This instruction stores the contents of X in A.	8A	2	1															
TXS	$S \leftarrow X$	This instruction stores the contents of X in S.	9A	2	1															
TYA	$A \leftarrow Y$	This instruction stores the contents of Y in A.	98	2	1															
WIT		The WIT instruction stops the internal clock but not the oscillation of the oscillation circuit is not stopped. CPU starts its function after the Timer X over flows (comes to the terminal count). All registers or internal memory contents except Timer X will not change during this mode. (Of course needs VDD).	C2	2	1															

Notes 1 : The number of cycles "n" is increased by 3 when T is 1.
2 : The number of cycles "n" is increased by 2 when T is 1.
3 : The number of cycles "n" is increased by 1 when T is 1.
4 : The number of cycles "n" is increased by 2 when branching has occurred.
5 : N, V, and Z flags are invalid in decimal operation mode.

Addressing mode																					Processor status register																			
ZP, X			ZP, Y			ABS			ABS, X			ABS, Y			IND			ZP, IND			IND, X			IND, Y			REL			SP			7	6	5	4	3	2	1	0
OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	N	V	T	B	D	I	Z	C			
F5	4	2				ED	4	3	FD	5	3	F9	5	3							E1	6	2	F1	6	2				N	V	•	•	•	•	Z	C			
																														•	•	•	•	•	•	•	•	•		
																														•	•	•	•	•	•	•	•	1		
																														•	•	•	•	•	1	•	•	•		
																														•	•	•	•	•	1	•	•	•		
																														•	•	1	•	•	•	•	•	•		
95	5	2				8D	5	3	9D	6	3	99	6	3							81	7	2	91	7	2				•	•	•	•	•	•	•	•	•		
																														•	•	•	•	•	•	•	•	•		
			96	5	2	8E	5	3																					•	•	•	•	•	•	•	•	•			
94	5	2				8C	5	3																					•	•	•	•	•	•	•	•	•			
																														N	•	•	•	•	•	•	Z	•		
																														N	•	•	•	•	•	•	Z	•		
																														N	•	•	•	•	•	•	Z	•		
																														N	•	•	•	•	•	•	Z	•		
																														N	•	•	•	•	•	•	Z	•		
																														•	•	•	•	•	•	•	•	•		
																														N	•	•	•	•	•	•	Z	•		
																														•	•	•	•	•	•	•	•	•		

APPENDIX

3.7 Machine instructions

Symbol	Contents	Symbol	Contents
IMP	Implied addressing mode	+	Addition
IMM	Immediate addressing mode	−	Subtraction
A	Accumulator or Accumulator addressing mode	*	Multiplication
BIT, A	Accumulator bit addressing mode	/	Division
BIT, A, R	Accumulator bit relative addressing mode	∧	Logical OR
ZP	Zero page addressing mode	∨	Logical AND
BIT, ZP	Zero page bit addressing mode	⊕	Logical exclusive OR
BIT, ZP, R	Zero page bit relative addressing mode	—	Negation
ZP, X	Zero page X addressing mode	←	Shows direction of data flow
ZP, Y	Zero page Y addressing mode	X	Index register X
ABS	Absolute addressing mode	Y	Index register Y
ABS, X	Absolute X addressing mode	S	Stack pointer
ABS, Y	Absolute Y addressing mode	PC	Program counter
IND	Indirect absolute addressing mode	PS	Processor status register
		PCH	8 high-order bits of program counter
ZP, IND	Zero page indirect absolute addressing mode	PCL	8 low-order bits of program counter
		ADH	8 high-order bits of address
IND, X	Indirect X addressing mode	ADL	8 low-order bits of address
IND, Y	Indirect Y addressing mode	FF	FF in Hexadecimal notation
REL	Relative addressing mode	nn	Immediate value
SP	Special page addressing mode	zz	Zero page address
C	Carry flag	M	Memory specified by address designation of any addressing mode
Z	Zero flag	M(X)	Memory of address indicated by contents of index register X
I	Interrupt disable flag	M(S)	Memory of address indicated by contents of stack pointer
D	Decimal mode flag	M(ADH, ADL)	Contents of memory at address indicated by ADH and ADL, in ADH is 8 high-order bits and ADL is 8 low-order bits.
B	Break flag	M(00, ADL)	Contents of address indicated by zero page ADL
T	X-modified arithmetic mode flag	Ai	Bit i (i = 0 to 7) of accumulator
V	Overflow flag	Mi	Bit i (i = 0 to 7) of memory
N	Negative flag	OP	Opcode
		n	Number of cycles
		#	Number of bytes

3.8 List of instruction code

D3 – D0 D7 – D4	Hexadecimal notation	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000	0	BRK	ORA IND, X	JSR ZP, IND	BBS 0, A	—	ORA ZP	ASL ZP	BBS 0, ZP	PHP	ORA IMM	ASL A	SEB 0, A	—	ORA ABS	ASL ABS	SEB 0, ZP
0001	1	BPL	ORA IND, Y	CLT	BBC 0, A	—	ORA ZP, X	ASL ZP, X	BBC 0, ZP	CLC	ORA ABS, Y	DEC A	CLB 0, A	—	ORA ABS, X	ASL ABS, X	CLB 0, ZP
0010	2	JSR ABS	AND IND, X	JSR SP	BBS 1, A	BIT ZP	AND ZP	ROL ZP	BBS 1, ZP	PLP	AND IMM	ROL A	SEB 1, A	BIT ABS	AND ABS	ROL ABS	SEB 1, ZP
0011	3	BMI	AND IND, Y	SET	BBC 1, A	—	AND ZP, X	ROL ZP, X	BBC 1, ZP	SEC	AND ABS, Y	INC A	CLB 1, A	LDM ZP	AND ABS, X	ROL ABS, X	CLB 1, ZP
0100	4	RTI	EOR IND, X	STP	BBS 2, A	COM ZP	EOR ZP	LSR ZP	BBS 2, ZP	PHA	EOR IMM	LSR A	SEB 2, A	JMP ABS	EOR ABS	LSR ABS	SEB 2, ZP
0101	5	BVC	EOR IND, Y	—	BBC 2, A	—	EOR ZP, X	LSR ZP, X	BBC 2, ZP	CLI	EOR ABS, Y	—	CLB 2, A	—	EOR ABS, X	LSR ABS, X	CLB 2, ZP
0110	6	RTS	ADC IND, X	MUL ZP, X	BBS 3, A	TST ZP	ADC ZP	ROR ZP	BBS 3, ZP	PLA	ADC IMM	ROR A	SEB 3, A	JMP IND	ADC ABS	ROR ABS	SEB 3, ZP
0111	7	BVS	ADC IND, Y	—	BBC 3, A	—	ADC ZP, X	ROR ZP, X	BBC 3, ZP	SEI	ADC ABS, Y	—	CLB 3, A	—	ADC ABS, X	ROR ABS, X	CLB 3, ZP
1000	8	BRA	STA IND, X	RRF ZP	BBS 4, A	STY ZP	STA ZP	STX ZP	BBS 4, ZP	DEY	—	TXA	SEB 4, A	STY ABS	STA ABS	STX ABS	SEB 4, ZP
1001	9	BCC	STA IND, Y	—	BBC 4, A	STY ZP, X	STA ZP, X	STX ZP, Y	BBC 4, ZP	TYA	STA ABS, Y	TXS	CLB 4, A	—	STA ABS, X	—	CLB 4, ZP
1010	A	LDY IMM	LDA IND, X	LDX IMM	BBS 5, A	LDY ZP	LDA ZP	LDX ZP	BBS 5, ZP	TAY	LDA IMM	TAX	SEB 5, A	LDY ABS	LDA ABS	LDX ABS	SEB 5, ZP
1011	B	BCS	LDA IND, Y	JMP ZP, IND	BBC 5, A	LDY ZP, X	LDA ZP, X	LDX ZP, Y	BBC 5, ZP	CLV	LDA ABS, Y	TSX	CLB 5, A	LDY ABS, X	LDA ABS, X	LDX ABS, Y	CLB 5, ZP
1100	C	CPY IMM	CMP IND, X	WIT	BBS 6, A	CPY ZP	CMP ZP	DEC ZP	BBS 6, ZP	INY	CMP IMM	DEX	SEB 6, A	CPY ABS	CMP ABS	DEC ABS	SEB 6, ZP
1101	D	BNE	CMP IND, Y	—	BBC 6, A	—	CMP ZP, X	DEC ZP, X	BBC 6, ZP	CLD	CMP ABS, Y	—	CLB 6, A	—	CMP ABS, X	DEC ABS, X	CLB 6, ZP
1110	E	CPX IMM	SBC IND, X	DIV ZP, X	BBS 7, A	CPX ZP	SBC ZP	INC ZP	BBS 7, ZP	INX	SBC IMM	NOP	SEB 7, A	CPX ABS	SBC ABS	INC ABS	SEB 7, ZP
1111	F	BEQ	SBC IND, Y	—	BBC 7, A	—	SBC ZP, X	INC ZP, X	BBC 7, ZP	SED	SBC ABS, Y	—	CLB 7, A	—	SBC ABS, X	INC ABS, X	CLB 7, ZP

 : 3-byte instruction

 : 2-byte instruction

 : 1-byte instruction

APPENDIX

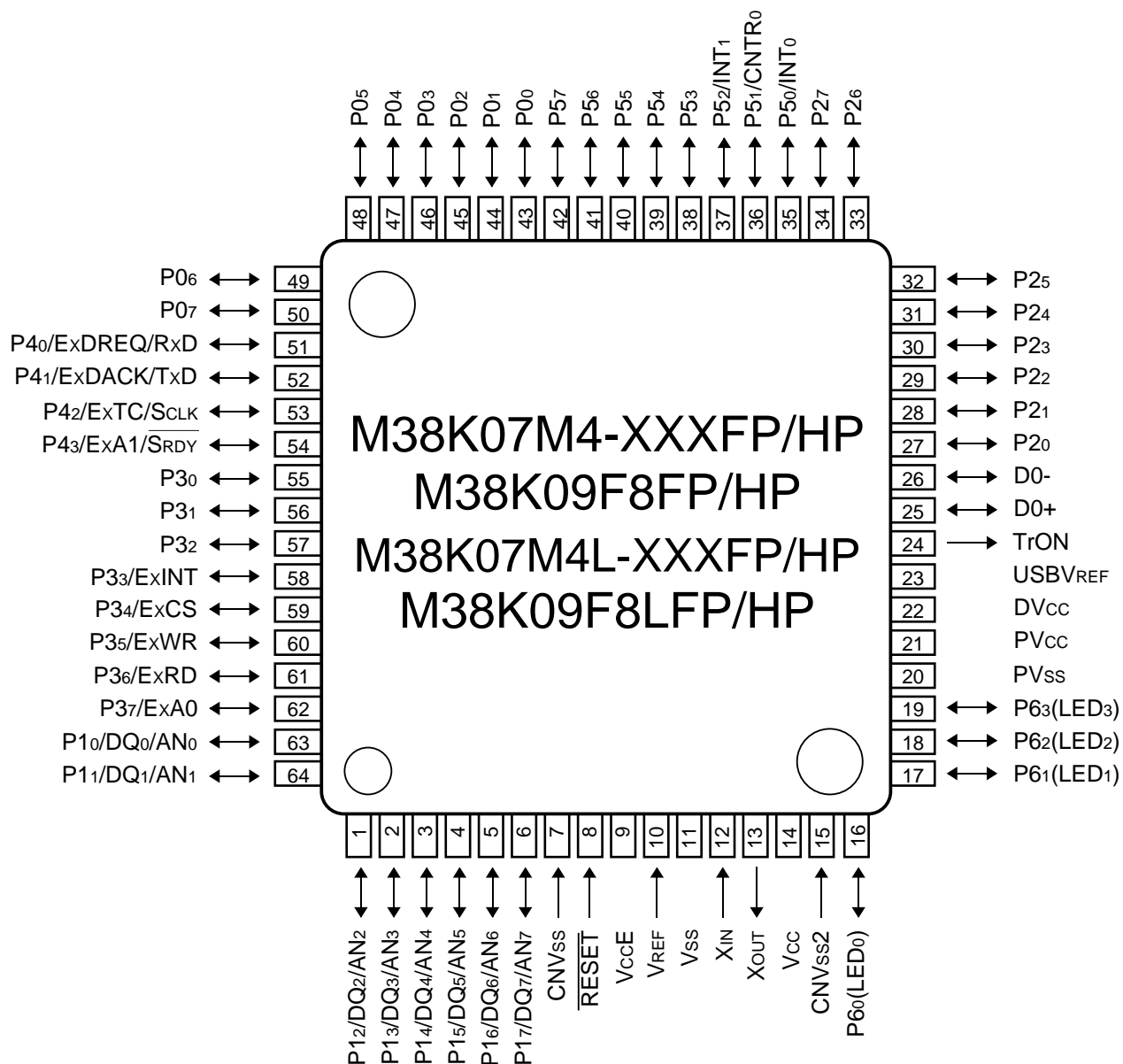
3.9 SFR memory map

3.9 SFR memory map

0000 ₁₆	Port P0 (P0)	0020 ₁₆	Prescaler 12 (PRE12)
0001 ₁₆	Port P0 direction register (P0D)	0021 ₁₆	Timer 1 (T1)
0002 ₁₆	Port P1 (P1)	0022 ₁₆	Timer 2 (T2)
0003 ₁₆	Port P1 direction register (P1D)	0023 ₁₆	Timer X mode register (TM)
0004 ₁₆	Port P2 (P2)	0024 ₁₆	Prescaler X (PREX)
0005 ₁₆	Port P2 direction register (P2D)	0025 ₁₆	Timer X (TX)
0006 ₁₆	Port P3 (P3)	0026 ₁₆	Transmit/Receive buffer register (TB/RB)
0007 ₁₆	Port P3 direction register (P3D)	0027 ₁₆	Serial I/O status register (SIOSTS)
0008 ₁₆	Port P4 (P4)	0028 ₁₆	Reserved (Note)
0009 ₁₆	Port P4 direction register (P4D)	0029 ₁₆	Reserved (Note)
000A ₁₆	Port P5 (P5)	002A ₁₆	Reserved (Note)
000B ₁₆	Port P5 direction register (P5D)	002B ₁₆	Reserved (Note)
000C ₁₆	Port P6 (P6)	002C ₁₆	Reserved (Note)
000D ₁₆	Port P6 direction register (P6D)	002D ₁₆	Reserved (Note)
000E ₁₆	Reserved (Note)	002E ₁₆	Reserved (Note)
000F ₁₆	Reserved (Note)	002F ₁₆	Reserved (Note)
0010 ₁₆	USB control register (USBCON)	0030 ₁₆	EXB interrupt source enable register (EXBICON)
0011 ₁₆	USB function enable register (USBAE)	0031 ₁₆	EXB interrupt source register (EXBIREQ)
0012 ₁₆	USB function address register (USBA0)	0032 ₁₆	Reserved (Note)
0013 ₁₆	Reserved (Note)	0033 ₁₆	EXB index register (EXBINDEX)
0014 ₁₆	Frame number register Low (FNUML)	0034 ₁₆	EXB field register 1 (EXBREG1)
0015 ₁₆	Frame number register High (FNUMH)	0035 ₁₆	EXB field register 2 (EXBREG2)
0016 ₁₆	USB interrupt source enable register (USBICON)	0036 ₁₆	A-D control register (ADCON)
0017 ₁₆	USB interrupt source register (USBIREQ)	0037 ₁₆	A-D conversion register 1 (AD1)
0018 ₁₆	Endpoint index register (USBINDEX)	0038 ₁₆	A-D conversion register 2 (AD2)
0019 ₁₆	Endpoint field register 1 (EPXXREG1)	0039 ₁₆	Watchdog timer control register (WDTCON)
001A ₁₆	Endpoint field register 2 (EPXXREG2)	003A ₁₆	Reserved (Note)
001B ₁₆	Endpoint field register 3 (EPXXREG3)	003B ₁₆	CPU mode register (CPUM)
001C ₁₆	Endpoint field register 4 (EPXXREG4)	003C ₁₆	Interrupt request register 1(IREQ1)
001D ₁₆	Endpoint field register 5 (EPXXREG5)	003D ₁₆	Interrupt request register 2(IREQ2)
001E ₁₆	Endpoint field register 6 (EPXXREG6)	003E ₁₆	Interrupt control register 1(ICON1)
001F ₁₆	Endpoint field register 7 (EPXXREG7)	003F ₁₆	Interrupt control register 2(ICON2)
0FE0 ₁₆	Serial I/O control register (SIOCON)	0FF0 ₁₆	Port P0 pull-up control register (PULL0)
0FE1 ₁₆	UART control register (UARTCON)	0FF1 ₁₆	Reserved (Note)
0FE2 ₁₆	Baud rate generator (BRG)	0FF2 ₁₆	Port P5 pull-up control register (PULL5)
0FE3 ₁₆	Reserved (Note)	0FF3 ₁₆	Interrupt edge selection register (INTEDGE)
0FE4 ₁₆	Reserved (Note)	0FF4 ₁₆	Reserved (Note)
0FE5 ₁₆	Reserved (Note)	0FF5 ₁₆	Reserved (Note)
0FE6 ₁₆	Reserved (Note)	0FF6 ₁₆	Reserved (Note)
0FE7 ₁₆	Reserved (Note)	0FF7 ₁₆	Reserved (Note)
0FE8 ₁₆	Reserved (Note)	0FF8 ₁₆	PLL control register (PLLCON)
0FE9 ₁₆	Reserved (Note)	0FF9 ₁₆	Reserved (Note)
0FEA ₁₆	Reserved (Note)	0FFA ₁₆	Reserved (Note)
0FEB ₁₆	Reserved (Note)	0FFB ₁₆	MISRG
0FEC ₁₆	Endpoint field register 8 (EPXXREG8)	0FFC ₁₆	Reserved (Note)
0FED ₁₆	Endpoint field register 9 (EPXXREG9)	0FFD ₁₆	Reserved (Note)
0FEE ₁₆	Reserved (Note)	0FFE ₁₆	Flash memory control register (FMCR)
0FEF ₁₆	Reserved (Note)	0FFF ₁₆	Reserved (Note)

Note: Do not write any data to these addresses, because these areas are reserved.

3.10 Pin configurations



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