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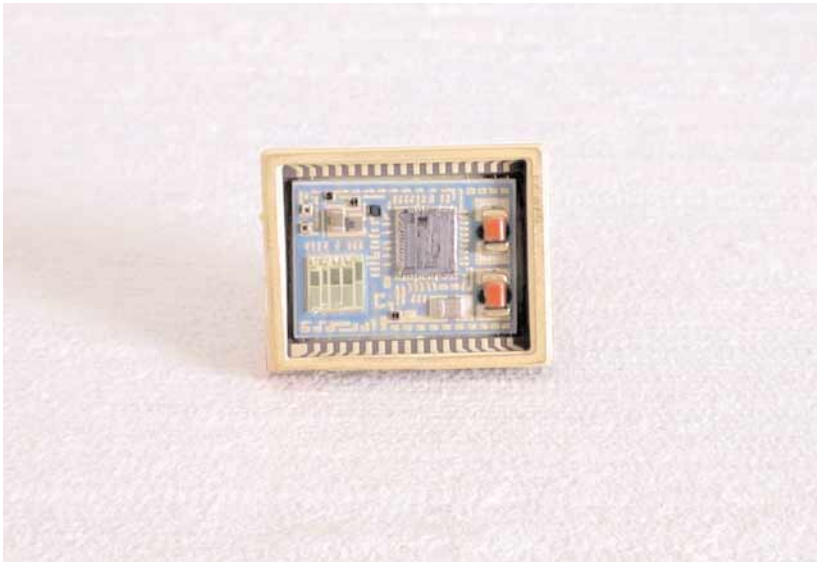
DDC on Board™

SD-14550 Series

Programmable Synchro/Resolver-to-Digital Converters



FEATURES

- Synthesized Reference Option
- 1 Minute Accuracy Available ("S" Option only)
- Single +5 V Power Supply
- 10-, 12-, 14-, or 16-Bit Programmable Resolution
- Small 34-Pin Ceramic Package
- $\overline{\text{BIT}}$ Output
- Velocity Output Eliminates Tachometer
- High Reliability Single Chip Monolithic
- -55°C to +125°C Operating Temperature Range
- MIL-PRF-38534 Processing Available

DESCRIPTION

The SD-14550 Series are small complete low cost hybrid synchro- or resolver-to-digital converters based on a single-chip monolithic. The SD-14550X "S" option offers synthesized reference circuitry to correct for phase shifts between the reference and signal voltage. The completely self-contained unit offers programmable resolution and +5 VDC operation. The package is a 34-pin, 1.0 x 0.78 x 0.21 inch ceramic package.

Resolution programming allows selection of 10-, 12-, 14-, or 16-bit modes. This feature allows selection of either low resolution for fast tracking or higher resolution for higher accuracy.

The velocity output (VEL) from the SD-14550, which can be used to replace a tachometer, is a ±4 V signal referenced to analog ground with a linearity of 1% of output voltage.

This converter series also offers a Built-In-Test output ($\overline{\text{BIT}}$). The SD-14550 converters are available with operating temperature ranges of 0°C to +70°C, -40°C to +85°C and -55°C to +125°C. These converters are also available with MIL-PRF-38534 processing.

APPLICATIONS

With its low cost, small size, high accuracy, and versatile performance, the SD-14550 Series converters are ideal for use in modern high-performance military, commercial and space position control systems. Typical applications include radar antenna positioning, navigation and fire control systems, motor control, and robotics.

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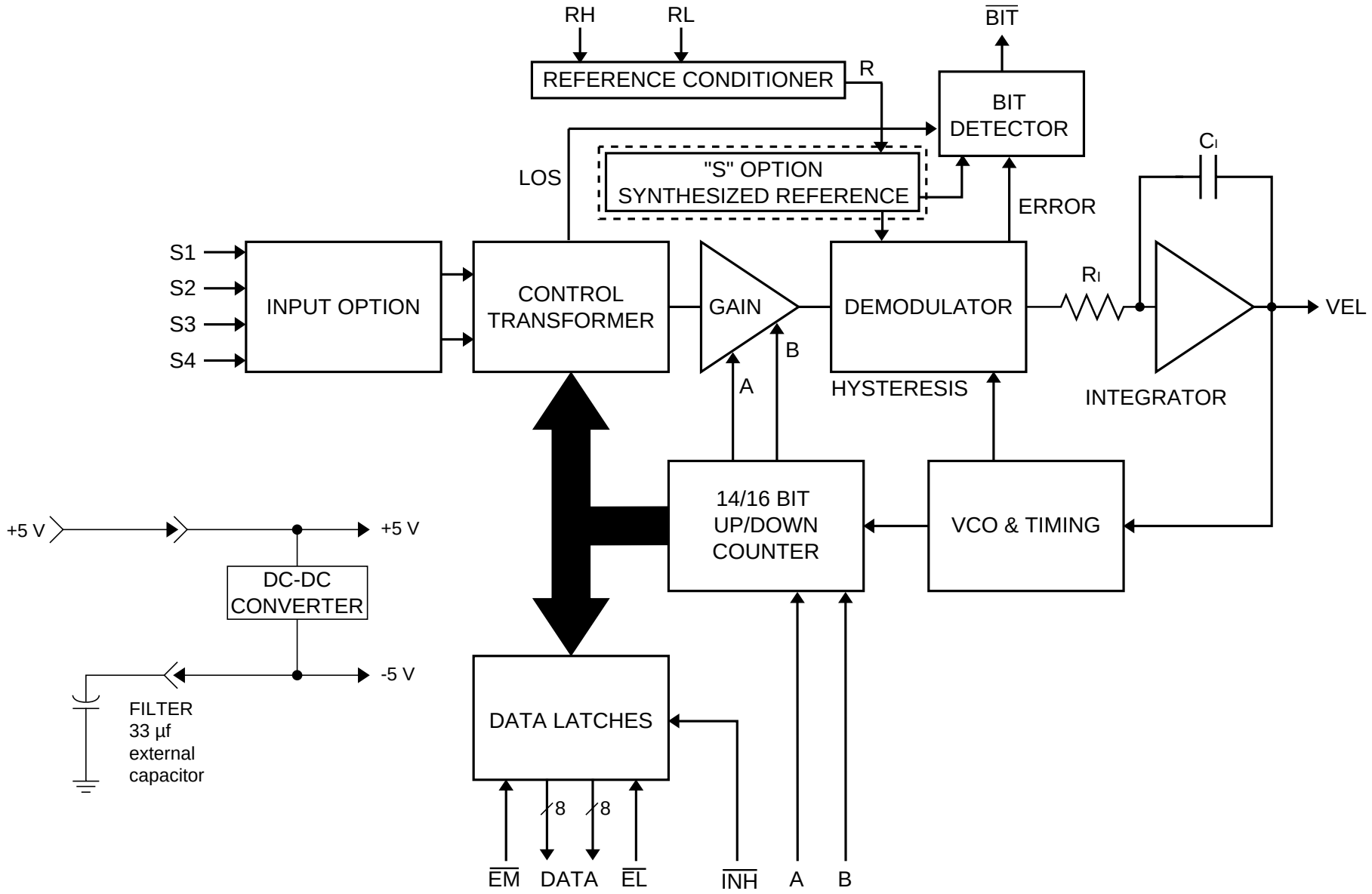


FIGURE 1. SD-14550 SERIES BLOCK DIAGRAM

TABLE 1. SD-14550 SERIES SPECIFICATIONS

These specs apply over the rated power supply, temperature, and reference frequency ranges; 10% signal amplitude variation, and 10% harmonic distortion.

PARAMETER	UNIT	VALUE	
RESOLUTION	Bits	programmable 10, 12, 14, or 16	
ACCURACY	Min	1, 2 or 4, + 1 LSB (see TABLE 4)	
REPEATABILITY	LSB	1 max.	
DIFFERENTIAL LINEARITY	LSB	1 max.	
REFERENCE INPUT		(RH, RL)	
Type		differential	
SD-14550		**2 & 11.8 V UNITS**	**90 V UNIT**
Voltage Range	Vrms	2-35	10-130
Frequency	Hz	360 - 5K	60 (47-5K) 400 (360-5K)
Input Impedance			
single ended	Ohm	60K	270K min.
differential	Ohm	120K	540K min.
Common-Mode Range	Vpeak	50, 100 transient	200, 300 transient
SD-14550XS			
Voltage Range	Vrms	2-35	—
Frequency	Hz	1K - 5K	—
Input Impedance			
single ended	Ohm	40K	—
differential	Ohm	80K	—
Common-Mode Range	Vpeak	50, 100 transient	—
±Sig/Ref Phase Shift	deg.	45 max.	—
SIGNAL INPUT CHARACTERISTICS			
90 V Synchro Input (L-L)			
Zin line-to-line	Ohm	123K	
Zin line-to-ground	Ohm	80K	
Common-Mode Voltage	V	180 max.	
11.8 V Synchro Input (L-L)			
Zin line-to-line	Ohm	52K	
Zin line-to-ground	Ohm	34K	
Common-Mode Voltage	V	30 max.	
11.8 V Resolver Input (L-L)		(same for “S” option)	
Zin line-to-line	Ohm	140K	
Zin line-to-ground	Ohm	70K	
Common-Mode Voltage	V	30 max.	
2 V Direct Input (L-L)			
Voltage Range	Vrms	2 nom, 2.3 max.	
Max. Voltage w/o Damage	V	25 cont, 100 pk transient	
Input Impedance	Ohm	20 M || 10 pF min.	
2 V Resolver Input (L-L)		(“S” option only)	
Zin line-to-line	Ohm	11K	
Zin line-to-ground	Ohm	22K	
Common-Mode Voltage	V	4.9 max.	
DIGITAL INPUT/OUTPUT			
LOGIC TYPE		TTL/CMOS compatible	
INPUTS		Logic 0 = 0.8 V max. Logic 1 = 2.0 V min. Loading =10 µA max P.U. current source to +5 V || 5 pF max. CMOS transient protected.	
Resolution Control		See TABLE 2.	

TABLE 1. SD-14550 SERIES SPECS. (CONTINUED)

PARAMETER	UNIT	VALUE	
DIGITAL INPUT/OUTPUT INPUTS (CONTINUED)			
Inhibit ($\overline{\text{INH}}$)		Logic 0 inhibits; Data stable within 0.5 µs	
Enable Bits 1 to 8 ($\overline{\text{EM}}$)		Logic 0 enables; Data stable within 150 ns	
Enable Bits 9 to 16 ($\overline{\text{EL}}$)		Logic 1 = High Impedance Data High Z within 100 ns	
OUTPUTS			
Parallel Data	bits	16 parallel lines; 2 bytes natural binary angle, positive logic.	
Built-In-Test		LOGIC 0 = BIT condition. ~ ± 100 LSBs of error with a filter of 500 µs for LOS. (LOS and LOR for “S” option)	
Drive Capability	TTL	50 PF + Logic 0; 1 TTL load, 1.6 mA at 0.4 V max Logic 1; 10 TTL loads, -0.4 mA at 2.8 V min	
	CMOS	Logic 0; 100mV max. driving Logic 1; +5 V supply minus 100 mV min.	
VELOCITY CHARACTERISTICS (see Note 1.)			
Polarity		Positive for increasing angle	
Voltage Range (Full Scale)	±V	4.0 typ.	3.5 min.
Scale Factor	±%	10 typ.	20 max.
Scale Factor TC	ppm/°C	100 typ.	200 max.
Reversal Error	±%	1 typ.	2 max.
Linearity	±%	0.5 typ.	1 max.
Zero Offset	mV	5 typ.	10 max.
Zero Offset TC	µV/°C	15 typ.	30 max.
Load	KOhm		20 max.
Noise	(Vp/V)%	1 typ.	2 max.
POWER SUPPLIES			
Nominal Voltage	V	+5	
Voltage Tolerance	%	±5	
Max. Voltage w/o Damage	V	+7	
Current	mA	30 typ.	35 max.
“S” option	mA	30 typ.	35 max.
TEMPERATURE RANGE			
Operating			
-30X	°C	0 to +70	
-20X	°C	-40 to +85	
-10X	°C	-55 to +125	
Storage	°C	-65 to +150	
PHYSICAL CHARACTERISTICS			
Size	in (mm)	1.00 x 0.78 x 0.21 (25.4 x 19.81 x 5.33)	
Weight	oz (g)	0.44 (12.47)	

NOTES:
1. Refer to TABLE 3 for full-scale tracking rate.

THEORY OF OPERATION

The SD-14550 Series of converters are based upon a single chip CMOS custom monolithic. They are implemented using the latest IC technology, which merges precision analog circuitry with digital logic to form a complete high performance tracking synchro/resolver-to-digital converter.

CONVERTER OPERATION

FIGURE 1 is the functional block diagram of the SD-14550 Series. The converter operates with a single +5 V DC power supply and internally generates a negative voltage of approximately 5 volts. This negative voltage comes out on pin 5 (filter point) — see GENERAL SETUP CONSIDERATIONS.

The converter is made up of three main sections; an input front-end, an error processor, and a digital interface. The converter front-end differs for synchro, resolver and direct inputs. An electronic Scott-T is used for synchro inputs, a resolver conditioner for resolver inputs, and a sine and cosine voltage follower for direct inputs. These amplifiers feed the high accuracy Control Transformer (CT). Its other input is the 16-bit digital angle ϕ. Its output is an analog error angle, or difference angle, between the two inputs. The CT performs the ratiometric trigonometric computation of $SIN\theta COS\phi - COS\theta SIN\phi = SIN(\theta - \phi)$ using amplifiers, switches, logic, and capacitors in precision ratios.

The converter accuracy is limited by the precision of the computing elements in the CT. In these converters ratioed capacitors are used in the CT, instead of the more conventional precision ratioed resistors. Capacitors used as computing elements with op-amps need to be sampled to eliminate voltage drifting. Therefore, the circuits are sampled at a high rate to eliminate this drifting and at the same time to cancel out the op-amp offsets.

The error processing is performed using the industry standard technique for type II tracking R/D converters. The DC error is integrated yielding a velocity voltage which in turn drives a voltage controlled oscillator (VCO). This VCO is an incremental integrator (constant voltage input to position rate output) which together with the velocity integrator forms a type II servo feedback loop. A lead in the frequency response is introduced to stabilize the loop and another lag at higher frequency is introduced to reduce the gain and ripple at the carrier frequency and above.

GENERAL SETUP CONSIDERATIONS

The following recommendations should be considered when using the SD-14550 Series converters:

1) The power supply is +5 V DC.

2) Direct inputs are referenced to AGND.

3) Connect (close to hybrid) pin 31 (Analog Ground) to pin 7 (GND).

4) Connect a 33 µF/10 VDC tantalum filter capacitor externally between pin 5 (filter point) to pin 7 (ground).

PROGRAMMABLE RESOLUTION

Resolution is controlled by pins 27 and 28. The resolution can be changed during converter operation so that the appropriate resolution and velocity dynamics can be set as needed. To insure that a race condition does not exist between counting and changing the resolution, the resolution control is latched internally. Refer to TABLE 2 for resolution control.

TABLE 2. RESOLUTION CONTROL (A AND B)

RESOLUTION	B	A
10 bit	0	0
12 bit	0	1
14 bit	1	0
16 bit	1	1

BIT (BUILT-IN-TEST)

This output is a logic line that will flag an internal fault condition or LOS (Loss-Of-Signal). The internal fault detector monitors the internal loop error and, when it exceeds approximately ±100 LSBs, will set the line to a logic 0; this condition will occur during a large-step input and will reset to a logic 1 after the converter settles out. (The error voltage is filtered with a 500 µs filter.) $\overline{BIT}$ will set for an over velocity condition because the converter loop cannot maintain input/output sync. $\overline{BIT}$ will also be set if a total LOS (loss of all signals) occurs. Additionally, in the SD-14550XS version, $\overline{BIT}$ will set when a Loss-of-Reference (LOR) condition occurs.

NO FALSE 180° HANGUP

This feature eliminates the “false 180° reading” during instantaneous 180° step changes; this condition most often occurs when the input is “electronically switched” from a digital-to-synchro converter. If the “MSB” (or 180° bit) is “toggled” on and off, a converter without the “false 180° hangup” feature may fail to respond.

The condition is artificial, as a “real” synchro or resolver cannot change its output 180° instantaneously. The condition is most often noticed during wraparound verification tests, simulations, or troubleshooting.

SYNTHESIZED REFERENCE

The synthesized reference section (“S” option) eliminates errors due to phase shift between the reference and signal inputs. Quadrature voltages in a resolver or synchro are by definition the resulting 90° fundamental signal in the nulled out error voltage (e) in the converter. Due to the inductive nature of synchros and resolvers, their output signals lead the reference input signal (RH and RL). When an uncompensated reference signal is used to demodulate the control transformer’s output, quadrature voltages are not completely eliminated. As shown in FIGURE 1, the converter synthesizes its own internal reference signal based on the SIN and COS signal inputs. Therefore, the phase of the synthesized (internal) reference is determined by the signal input, resulting in reduced quadrature errors. The synthesized reference circuit also eliminates the 180 degree false error null hang up.

INTERFACING

SOLID-STATE BUFFER PROTECTION - TRANSIENT VOLTAGE SUPPRESSION

The solid-state signal and reference inputs are true differential inputs with high AC and DC common rejection, so most applications will not require units with isolation transformers. Input impedance is maintained with power off. The recurrent AC peak + DC common mode voltage should not exceed the values in TABLE 1.

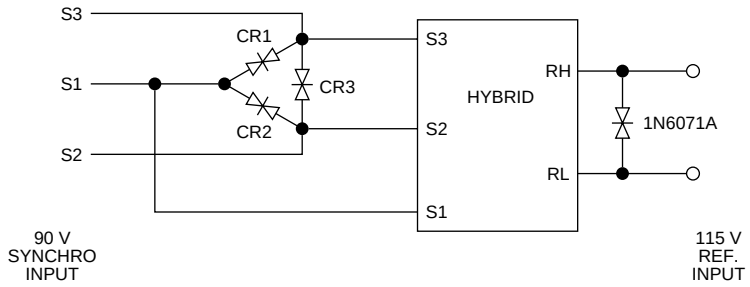
The 90 V line-to-line systems may have voltage transients which exceed the 300 V specification listed in TABLE 1. **These transients can destroy the thin-film input resistor network in the hybrid.** Therefore, 90 V L-L solid-state input modules may be protected by installing voltage suppressors as shown in FIGURE 2. Voltage transients are likely to occur whenever a synchro is switched on and off. For instance, a 1000 V transient can be generated when the primary of a CX or TX input is opened.

INHIBIT AND ENABLE TIMING

The Inhibit ($\overline{\text{INH}}$) signal is used to freeze the digital output angle in the transparent output data latch while the data is being transferred. Application of an inhibit signal does not interfere with the continuous tracking of the converter. As shown in FIGURE 3, angular output data is valid 500 nanoseconds maximum after the application of the low-going inhibit pulse.

Output angle data is enabled onto the tri-state data bus in 2 bytes. This Enable MSB ($\overline{\text{EM}}$) is used for the most significant 8 bits and Enable LSB ($\overline{\text{EL}}$) is used for the least significant bits. As

FOR 90 V SYNCHRO INPUTS



CR1, CR2, AND CR3 ARE IN6068A, BIPOLAR TRANSIENT VOLTAGE SUPRESSORS OR EQUIVALENT.

FIGURE 2. CONNECTIONS FOR VOLTAGE TRANSIENT SUPPRESSORS

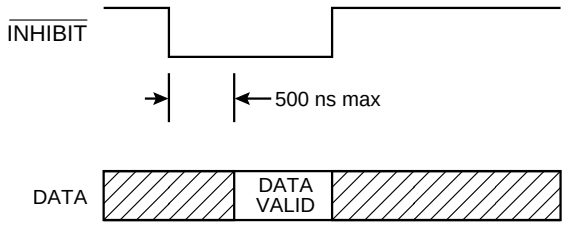


FIGURE 3. INHIBIT TIMING

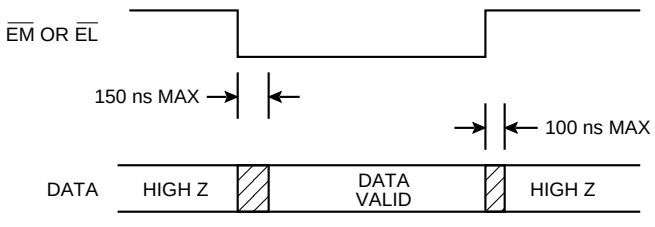


FIGURE 4. ENABLE TIMING

TABLE 3. DYNAMIC CHARACTERISTICS													
PARAMETER	**UNITS**	**DEVICE TYPE**											
		60 Hz				**400 Hz**				**"S" OPTION**			
Input Frequency	Hz	47 - 5K				360 - 5K				1K - 5K			
Bandwidth (Closed Loop)	Hz	15				56				150			
Ka	$1/s^2$	830				53K				110K			
A1	1/s	0.17				0.41				2.47			
A2	1/s	5K				41K				44.4K			
A	1/s	29				130				333			
B	1/s	14.5				81				166			
RESOLUTION	**BITS**	**10**	**12**	**14**	**16**	**10**	**12**	**14**	**16**	**10**	**12**	**14**	**16**
Tracking Rate (rps)													
typical	rps	32	8	2	0.5	160	40	10	2.5	160	40	10	2.5
minimum	rps	25.6	6.4	1.6	0.4	128	32	8	2	128	32	8	2
Acceleration (1 LSB lag)	deg/s^2	720	180	45	11.3	5950	1490	372	93	39K	9760	2440	610
Settling Time (179° step max)	msec	400	500	1100	2500	90	100	180	360	51	78	150	232

shown in FIGURE 4, output data is valid 150 nanoseconds maximum after the application of a low-going enable pulse. The tri-state data bus returns to the high impedance state 100 nanoseconds maximum after the rising edge of the enable signal.

DYNAMIC PERFORMANCE

A type II servo loop (Kv = ∞) and very high acceleration constants give the SD-14550 superior dynamic performance.

TRANSFER FUNCTION AND BODE PLOT

The dynamic performance of the converter can be determined from its functional block diagram (FIGURE 1), its transfer function block diagram (FIGURE 5), and its bode plots (open and closed loop - FIGURE 6). Values for the transfer function block can be obtained from TABLE 3.

The open loop transfer function is as follows:

$$\text{Open Loop Transfer Function} = \frac{A^2\left(\frac{S}{B}+1\right)}{S^2\left(\frac{S}{10B}+1\right)}$$

where A is the gain coefficient
and B is the frequency of lead compensation

ACCURACY AND RESOLUTION

TABLE 4 lists the total accuracy including quantitation for the various resolutions and accuracy grades.

TABLE 4. ACCURACY/RESOLUTION					
VERSION	**ACCURACY (minutes) See Note 1**	**RESOLUTION VS ACCURACY (In LSB's - See Note 2)**			
		10 BIT	**12 BIT**	**14 BIT**	**16 BIT**
SD-1455X-XX	4 +1 LSB	2	2	4	13
	2 +1 LSB	2	2	3	7
SD-1455X-XS ("S" option)	4 +1 LSB	2	2	4	13
	2 +1 LSB	2	2	3	7
	1 +1 LSB	2	2	2	4*

* 1.3 minute (4 LSB) accuracy available for "S" option only. Inclusive of 1 bit of jitter.

Note 1: Accuracy Base measured in 16 bit mode.

Note 2: Accuracy in Resolution rounded up to next LSB:
LSB in 16 Bit mode = 0.3 minutes
LSB in 14 Bit mode = 1.3 minutes
LSB in 12 bit mode = 5.3 minutes
LSB in 10 Bit mode = 21.1 minutes

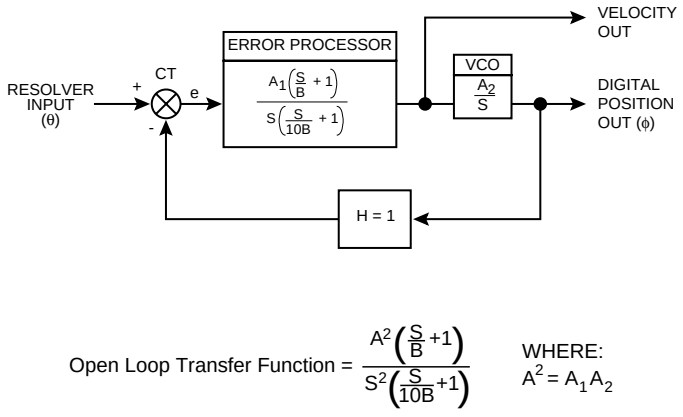


FIGURE 5. TRANSFER FUNCTION BLOCK DIAGRAM

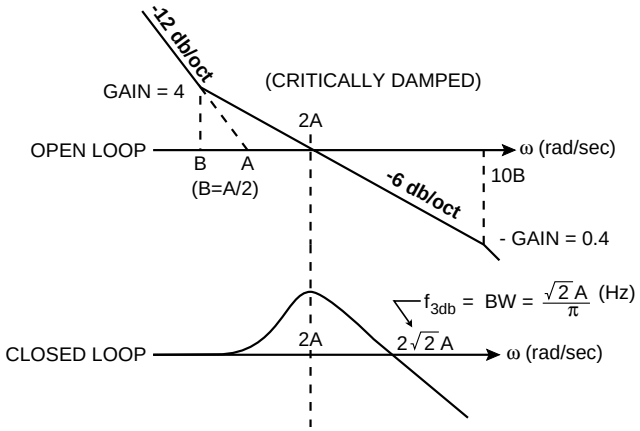
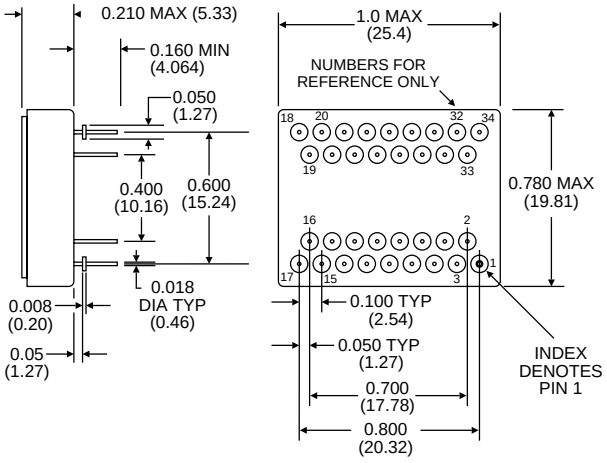


FIGURE 6. BODE PLOTS

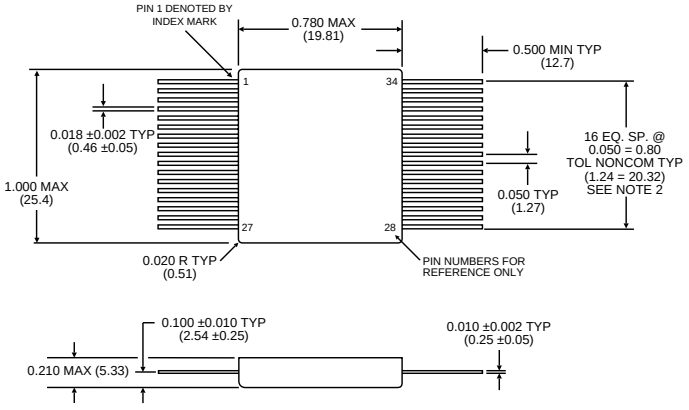
TABLE 5. PINOUTS (DIP AND FLAT PACK)					
PIN	**FUNCTION**			**PIN**	**FUNCTION**
1	S1 (R)	S1 (S)	N.C.	34	RH (+Reference input)
2	S2 (R)	S2 (S)	COS (D)	33	RL (-Reference input)
3	S3 (R)	S3 (S)	SIN (D)	32	N.C.
4	S4 (R)	N.C.	N.C.	31	AGND (Analog Ground)
5	Filter Point			30	VEL (Velocity Output)
6	+5 V (Power Supply)			29	$\overline{\text{INH}}$ (Inhibit)
7	GND (ground)			28	B (Resolution Control B)
8	$\overline{\text{EM}}$ (Enable MSBs)			27	A (Resolution Control A)
9	$\overline{\text{BIT}}$ (Built-In-Test)			26	$\overline{\text{EL}}$ (Enable LSBs)
10	Bit 1 (MSB)			25	Bit 16 (LSB, 16-bit mode)
11	Bit 9			24	Bit 8
12	Bit 2			23	Bit 15
13	Bit 10 (LSB, 10-bit mode)			22	Bit 7
14	Bit 3			21	Bit 14 (LSB, 14-bit mode)
15	Bit 11			20	Bit 6
16	Bit 4			19	Bit 13
17	Bit 12 (LSB, 12-bit mode)			18	Bit 5

Notes:
1. (S) = Synchro; (R) = Resolver; (D) = 2 V Resolver Direct.
2. Connect (close to the hybrid) pin 31 to pin 7.
3. Connect a 33 µF/10 VDC tantalum filter cap from pin 5 to pin 7.



Notes:
1. Dimensions are in inches (mm).
2. Lead identification numbers are for reference only
3. Lead cluster shall be centered within ±0.005 (0.13) of outline dimensions. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements to MIL-STD-202E, Method 208C.
5. Case is hermetically sealed ceramic package.

FIGURE 7. SD-14550 MECHANICAL OUTLINE (DIP)



Notes:
1. Dimensions are in inches (mm).
2. Lead cluster shall be centralized about case centerline within ±0.010 (±2.54).

FIGURE 8. SD-14550 MECHANICAL OUTLINE (FLAT PACK)

ORDERING INFORMATION

SD-1455X X X - X X X X

Supplemental Process Requirements:
- S = Pre-Cap Source Inspection
- L = Pull Test
- Q = Pull Test and Pre-Cap Inspection
- K = One Lot Date Code
- W = One Lot Date Code and Pre-Cap Source
- Y = One Lot Date Code and 100% Pull Test
- Z = One Lot Date Code, Pre-Cap Source and 100% Pull Test
- Blank = None of the Above

Accuracy:
- 2 = 4 min + 1 LSB
- 4 = 2 min + 1 LSB
- 5 = 1 min + 1 LSB (available with “S” option only)

Reliability Grade:
- 0 = Standard DDC Processing, no Burn-In (See table on next page.)
- 1 = MIL-PRF-38534 Compliant
- 2 = B*
- 3 = MIL-PRF-38534 Compliant with PIND Testing
- 4 = MIL-PRF-38534 Compliant with Solder Dip
- 5 = MIL-PRF-38534 Compliant with PIND Testing and Solder Dip
- 6 = B* with PIND Testing
- 7 = B* with Solder Dip
- 8 = B* with PIND Testing and Solder Dip
- 9 = Standard DDC Processing with Solder Dip, no Burn-In (See table on next page.)

Temperature Grade/Data Requirements:
- 1 = -55°C to +125°C
- 2 = -40°C to +85°C
- 3 = 0°C to +70°C
- 4 = -55°C to +125°C + Variables Test Data
- 5 = -40°C to +85°C + Variables Test Data
- 8 = 0°C to +70°C + Variables Test Data

Options:
- X = None
- S = Synthesized Reference

Package Type:
- D = DIP
- F = Flat Pack

Input Options:
- 0 = 11.8 V, Synchro, 400 Hz
- 1 = 11.8 V, Resolver, 400 Hz
- 2 = 90 V, Synchro, 400 Hz
- 3 = 2 V, Direct, 400 Hz
- 4 = 90 V, Synchro, 60 Hz

Input Options (“S” Option):
- 1 = 11.8 V, Resolver, 1 KHz
- 3 = 2 V, Resolver (Differential), 1 KHz

*Standard DDC Processing with burn-in and full temperature test — see table on next page.

STANDARD DDC PROCESSING		
TEST	**MIL-STD-883**	
	METHOD(S)	**CONDITION(S)**
INSPECTION	2009, 2010, 2017, and 2032	—
SEAL	1014	A and C
TEMPERATURE CYCLE	1010	C
CONSTANT ACCELERATION	2001	A
BURN-IN	1015, Table 1	—

NOTES:

NOTES:

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