Military 10H581

4-Bit Arithmetic Logic Unit/Function Generator

ELECTRICALLY TESTED PER: MPG 10H581

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The 10H581 is a high speed arithmetic logic unit capable of performing 16 logic operations and 16 arithmetic operations on two 4-bit words. Full internal carry is incorporated for ripple-through operation. Arithmetic logic operations are selected by applying the appropriate binary word to the select inputs (S0 through S3) as indicated in the tables of arithmetic/logic functions. Group carry propagate (P_G) and carry generate (G_G) are provided allowing fast operations on very long words using a second order look ahead. The internal carry is enabled by applying a low level voltage to the mode control input (M).

When used with the 10579, full-carry look-ahead, as a second order look ahead block, the 10H581 provides high speed arithmetic operations on very long words.

This 10H part is a functional/pinout duplication of the standard MECL 10K family part with 100% improvement in propagation delay and not increase in power supply current.

- Improved Noise Margin, 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: 10H581/BXAJC
X = CASE OUTLINE AS FOLLOWS:

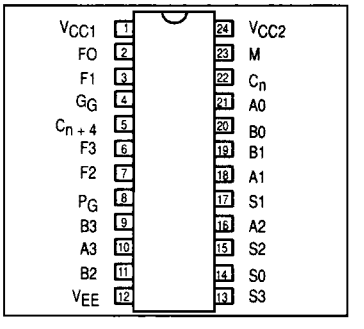
PACKAGE: CERDIP: K
CERFLAT: J

The letter "M" appears before the slash on LCC.

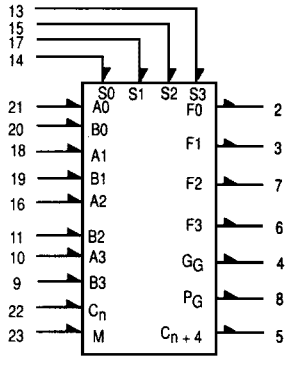
PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	BURN-IN (CONDITION C)
V_{CC1}	1	7	GND
F0	2	8	51 Ω to V_{TT}
F1	3	9	51 Ω to V_{TT}
G_G	4	10	51 Ω to V_{TT}
C_{n+4}	5	11	51 Ω to V_{TT}
F3	6	12	51 Ω to V_{TT}
F2	7	13	51 Ω to V_{TT}
P_G	8	14	51 Ω to V_{TT}
B3	9	15	50 Ω to V_{EE}
A3	10	16	GND
B2	11	17	50 Ω to V_{EE}
V_{EE}	12	18	V_{EE}
S3	13	19	50 Ω to V_{EE}
S0	14	20	GND
S2	15	21	50 Ω to V_{EE}
A2	16	22	GND
S1	17	23	GND
A1	18	24	50 Ω to V_{EE}
B1	19	1	V_{EE}
B0	20	2	50 Ω to V_{EE}
A0	21	3	GND
C_n	22	4	50 Ω to V_{EE}
M	23	5	GND
V_{CC2}	24	6	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN



LOGIC DIAGRAM



ARITHMETIC/LOGIC FUNCTIONS

Function Select				Logic Function M is High C = D. C.	Arithmetic Operation M is Low C_n is low
S_3	S_2	S_1	S_0	F	F
L	L	L	L	$F = \overline{A}$	F = A
L	L	L	H	$F = \overline{A} + \overline{B}$	F = A plus $(A \bullet \overline{B})$
L	L	H	L	$F = \overline{A} + B$	F = A plus (A • B)
L	L	H	H	F = Logical "1"	F = A times 2
L	H	L	L	$F = \overline{A} \bullet B$	F = (A + B) plus 0
L	H	L	H	$F = \overline{B}$	F = (A + B) plus $(A \bullet \overline{B})$
L	H	H	L	$F = A \oplus B$	F = A plus B
L	H	H	H	$F = A + \overline{B}$	F = A plus (A + B)
H	L	L	L	$F = \overline{A} \bullet B$	F = $(A + \overline{B})$ plus 0
H	L	L	H	$F = A \oplus B$	F = A minus B minus 1
H	L	H	L	F = B	F = $(A + \overline{B})$ plus $(A \bullet B)$
H	L	H	H	F = A + B	F = A plus $(A + \overline{B})$
H	H	L	L	F = Logical "0"	F = minus 1 (two's complement)
H	H	L	H	$F = A \bullet \overline{B}$	F = $(A \bullet \overline{B})$ minus 1
H	H	H	L	F = A • B	F = (A • B) minus 1
H	H	H	H	F = A	F = minus 1

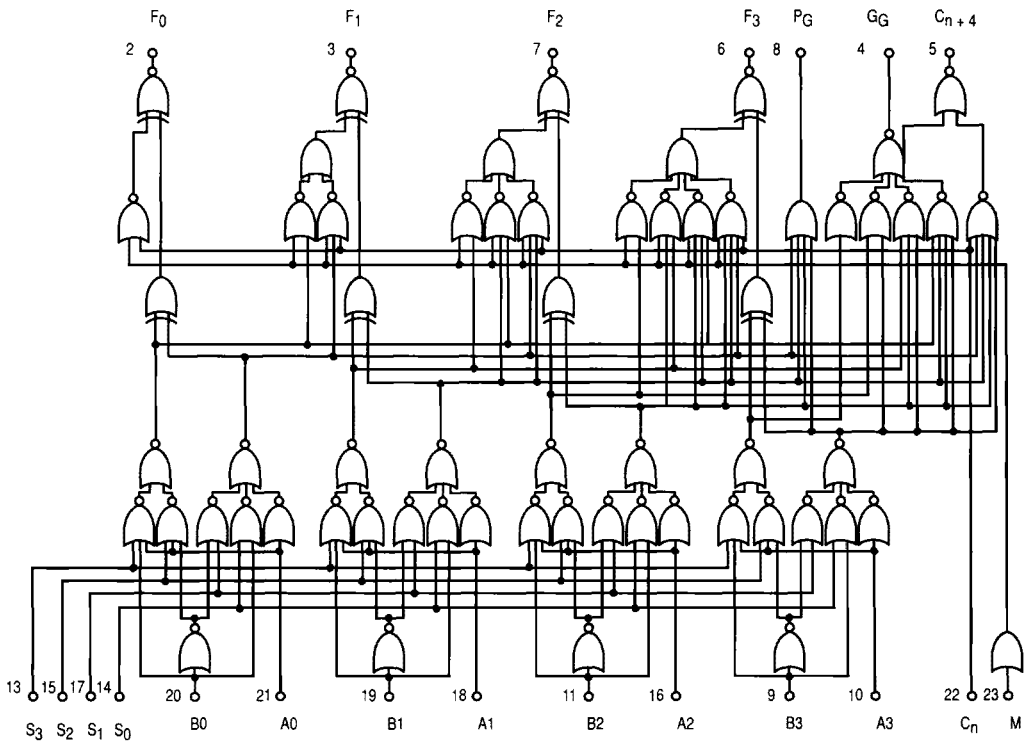
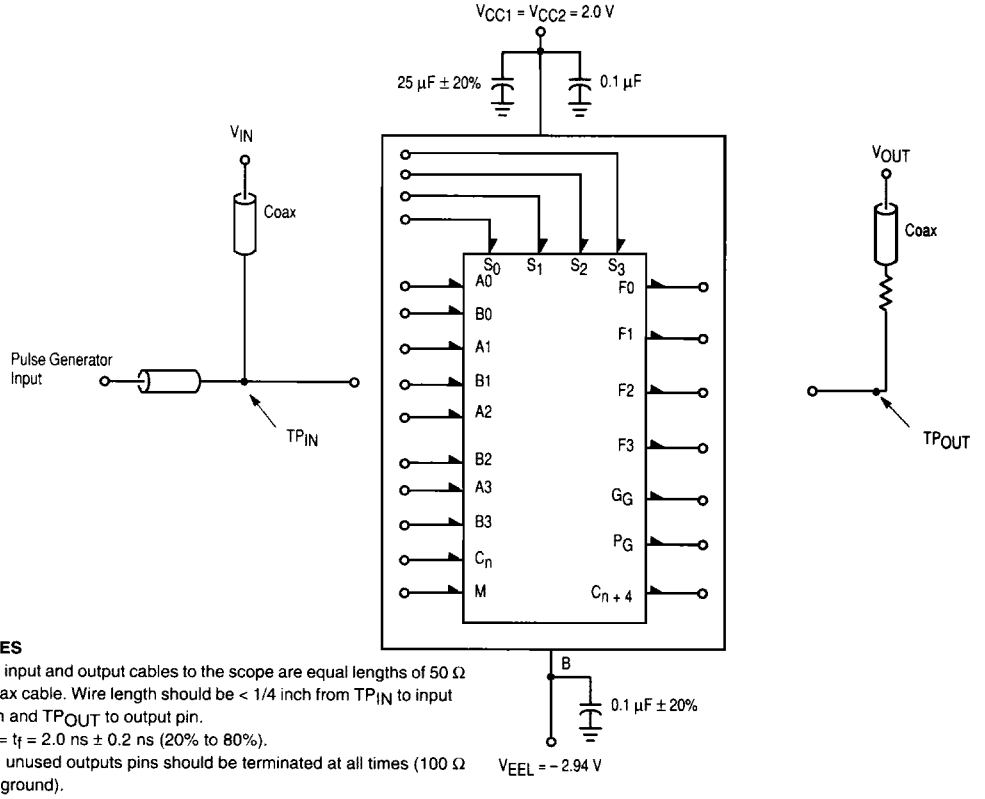


Figure 1. Logic Diagram



NOTES

1. All input and output cables to the scope are equal lengths of 50 Ω coax cable. Wire length should be < 1/4 inch from TP_{IN} to input pin and TP_{OUT} to output pin.
2. $t_r = t_f = 2.0$ ns ± 0.2 ns (20% to 80%).
3. All unused outputs pins should be terminated at all times (100 Ω to ground).
4. V_{IN} waveform has the following characteristics:
   a) Pulse width ≥ 20 ns.
   b) Frequency = 1.0 MHz.

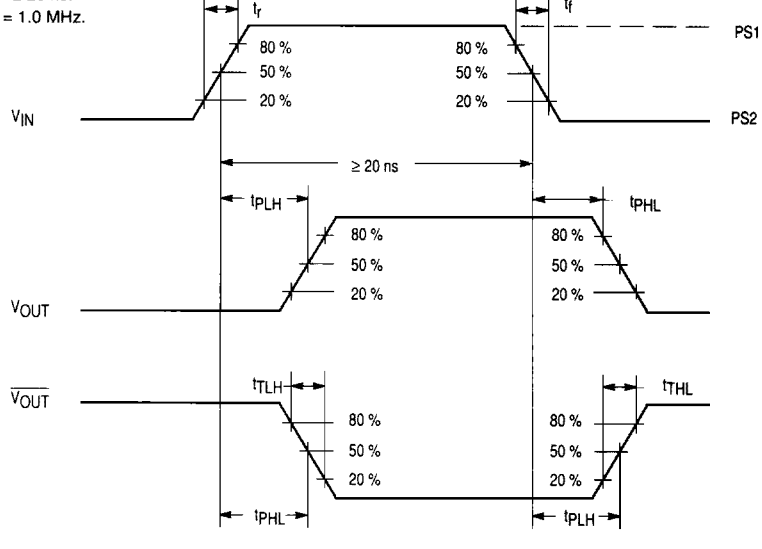


Figure 2. Switching Test Circuit and Waveforms

10H581
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}
T_A = 25 °C	-0.78	-1.950	-1.105	-1.475	+1.11	+0.31	-5.46	-4.94
T_A = 125 °C	-0.65	-1.950	-1.000	-1.400	+1.24	+0.36	-5.46	-4.94
T_A = -55 °C	-0.88	-1.950	-1.255	-1.510	+1.01	+0.28	-5.46	-4.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	$V_{EE1/2}$	V_{CC}	P.U.T.
V_{OH}	High Output Voltage	- 0.93	- 0.78	- 0.825	- 0.63	- 1.09	- 0.88	V	9 - 11 16 - 23	13 - 15			12	1, 24	2 - 8
V_{OL1}	Low Output Voltage	- 1.85	- 1.620	- 1.82	- 1.545	- 1.92	- 1.655	V	9 - 11, 14, 16 18, 19, 21 - 23	9, 10, 13, 15 16, 17, 19, 21			12	1, 24	2, 3, 5 - 8
V_{OHA}	High Output Voltage	- 0.95	- 0.78	- 0.845	- 0.63	- 1.10	- 0.88	V	9 - 11, 13 16 - 23	13 - 23	16 - 23	13 - 15 22, 23	12	1, 24	2 - 8
V_{OLA}	Low Output Voltage	- 1.85	- 1.60	- 1.88	- 1.525	- 1.92	- 1.635	V		9 - 11, 13 - 23	14, 15	9 - 11 16 - 23	12	1, 24	2 - 8
V_{OL2}	Low Output Voltage	- 1.99	- 1.620	- 1.88	- 1.545	- 2.10	- 1.655	V	11, 14, 16, 18 20, 22, 23	9, 10, 13, 15 17, 19, 21	8		12	1, 24	4
I_{EE}	Power Supply Current	- 145		- 160		- 160		mA	9 - 11, 16 18 - 21				12	1, 24	12
I_{IH1}	Input Current High		200		340		340	µA	13, 23				12	1, 24	13, 23
I_{IH2}	Input Current High		220		375		375	µA	10, 16, 18 21				12	1, 24	10, 16, 18 21
I_{IH3}	Input Current High		245		415		415	µA	9, 11 19, 20				12	1, 24	9, 11, 19, 20
I_{IH4}	Input Current High		265		450		450	µA	14, 15, 17				12	1, 24	14, 15, 17
I_{IH5}	Input Current High		290		580		495	µA	22				12	1, 24	22
I_{IL}	Input Current Low	0.5		0.3		0.5		mA	9 - 11 13 - 23				1, 16		9 - 11, 13 - 23

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Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-5.2	-4.94	-2.94
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2	-4.94	-2.94
T_A = -55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EE1}	P_{S1}	P. U. T.
t_{TLH}/ t_{THL}	Rise & Fall Time	0.5	2.3	0.764	2.64	0.62	2.4	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay C_n to C_{n+4}	0.6	2.2	0.74	2.64	0.74	2.4	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	0.6	2.2	0.74	2.88	0.7	2.2	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay C_n to F	1.0	3.0	1.44	3.96	1.8	3.6	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	0.6	2.0	0.74	2.64	0.84	2.4	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay A to F	1.5	3.7	1.92	4.8	1.8	4.44	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	0.8	2.4	1.08	3.12	1.0	2.88	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay A to P_G	1.5	3.7	1.92	4.8	1.8	4.44	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	0.6	2.2	0.74	2.88	0.74	2.764	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay A to G_G	1.5	3.7	1.92	4.68	1.8	4.44	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	0.6	2.0	0.74	2.64	0.74	2.4	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay A to C_{n+4}	1.5	3.6	1.92	4.68	1.8	4.32	ns	"	"	"	"	"	"

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T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2	-4.94	-2.94
T_A = -55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EE1}	P_{S1}	P. U. T.
t_{TLH}/ t_{THL}	Rise & Fall Time	0.6	2.3	0.74	3.0	0.74	2.76	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay B to F	2.0	4.5	2.52	5.76	2.2	5.0	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	0.6	2.2	0.74	2.88	0.74	2.64	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay B to P_G	1.5	3.8	1.92	4.8	1.8	4.56	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	0.6	2.2	0.74	2.88	0.74	2.64	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay B to G_G	1.5	3.7	1.92	4.8	1.8	4.44	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	0.5	2.0	0.5	2.64	0.5	2.4	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay B to Cn + 4	2.0	4.0	2.52	5.16	2.4	4.8	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	0.7	2.3	0.86	3.0	0.86	2.76	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay M to F	1.5	4.2	1.92	5.4	1.8	5.04	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	0.6	2.0	0.74	2.64	0.74	2.4	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay S to F	1.5	4.5	1.92	5.76	1.8	5.4	ns	"	"	"	"	"	"

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		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EE1}	P_{S1}	P. U. T.
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t_{pd}	Propagation Delay S to P_G	1.5	4.0	1.92	5.16	1.8	4.8	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	0.6	2.2	0.74	2.88	0.74	2.64	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay S to C_{n+4}	1.5	4.1	1.92	5.28	1.8	4.92	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	0.5	3.2	0.5	4.0	0.5	3.84	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14 16, 18, 19. 21 22	2 - 7
t_{pd}	Propagation Delay S to G_G	1.3	4.5	1.68	5.76	1.56	5.4	ns	"	"	"	"	"	"