



Hex "D" Master-Slave Flip-Flop with Reset

ELECTRICALLY TESTED PER: 5962-8756301

The 10H586 is a hex D type flip-flop with common reset and clock lines. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in clock toggle frequency and propagation delay and no increase in power supply current.

- Propagation Delay, 1.7 ns Typical
- 660 mW Max/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

FUNCTION	PIN ASSIGNMENTS			BURN-IN (CONDITION C)
	DIL	FLATS	LCC	
VCC1	1	5	2	GND
Q0	2	6	3	51 Ω to V _{TT}
Q1	3	7	4	51 Ω to V _{TT}
Q2	4	8	5	51 Ω to V _{TT}
D0	5	9	7	GND
D1	6	10	8	GND
D2	7	11	9	GND
VEE	8	12	10	VEE
Clock	9	13	12	CP1
D3	10	14	13	GND
D4	11	15	14	GND
D5	12	16	15	GND
Q3	13	1	17	51 Ω to V _{TT}
Q4	14	2	18	51 Ω to V _{TT}
Q5	15	3	19	51 Ω to V _{TT}
VCC2	16	4	20	GND

BURN - IN CONDITIONS:

V_{TT} = - 2.0 V MAX/ - 2.2 V MIN

V_{EE} = - 5.7 V MAX/ - 5.2 V MIN

Military 10H586

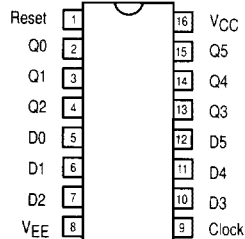


AVAILABLE AS

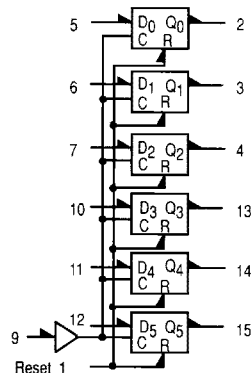
- 1) JAN: N/A
 - 2) SMD: 5962-8756301
 - 3) 883: 10H586/BXAJC
- X = CASE OUTLINE AS FOLLOWS:**

**PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2**

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM



10H586

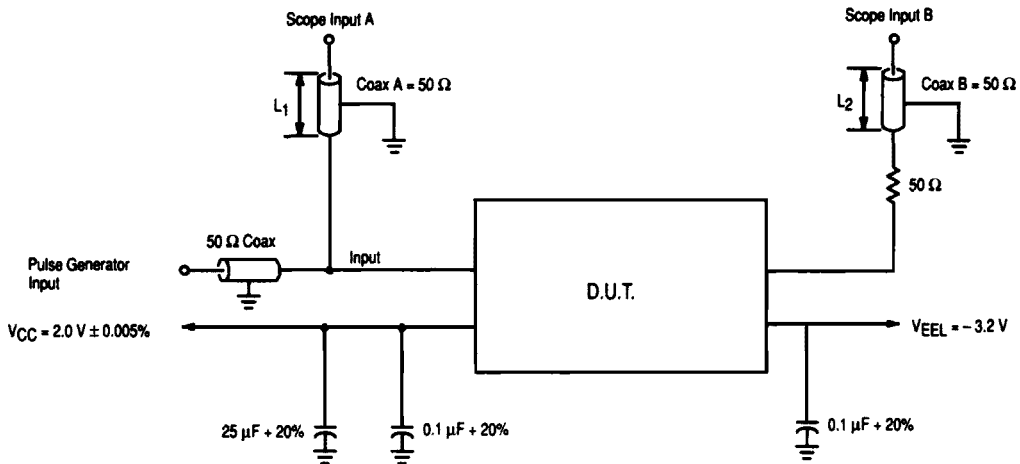
CLOCKED TRUTH TABLE

R	C	Q	Q _{n+1}
L	L	∅	Q _n
L	H*	L	L
L	H*	H	H
H	L	∅	L

∅ = Don't Care

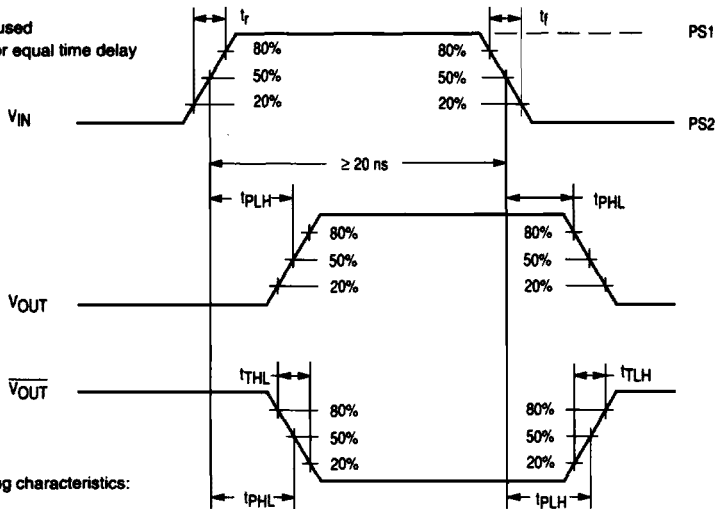
* A clock H is a clock transition from a low to a high state

2



NOTES

1. Pulse generator must be capable of rise and fall time of $1.0 \text{ ns} \pm 0.1 \text{ ns}$
2. Unused outputs connected to 100Ω resistor to ground
3. 2:1 divider may be used
4. $L_1 = L_2$: matched for equal time delay

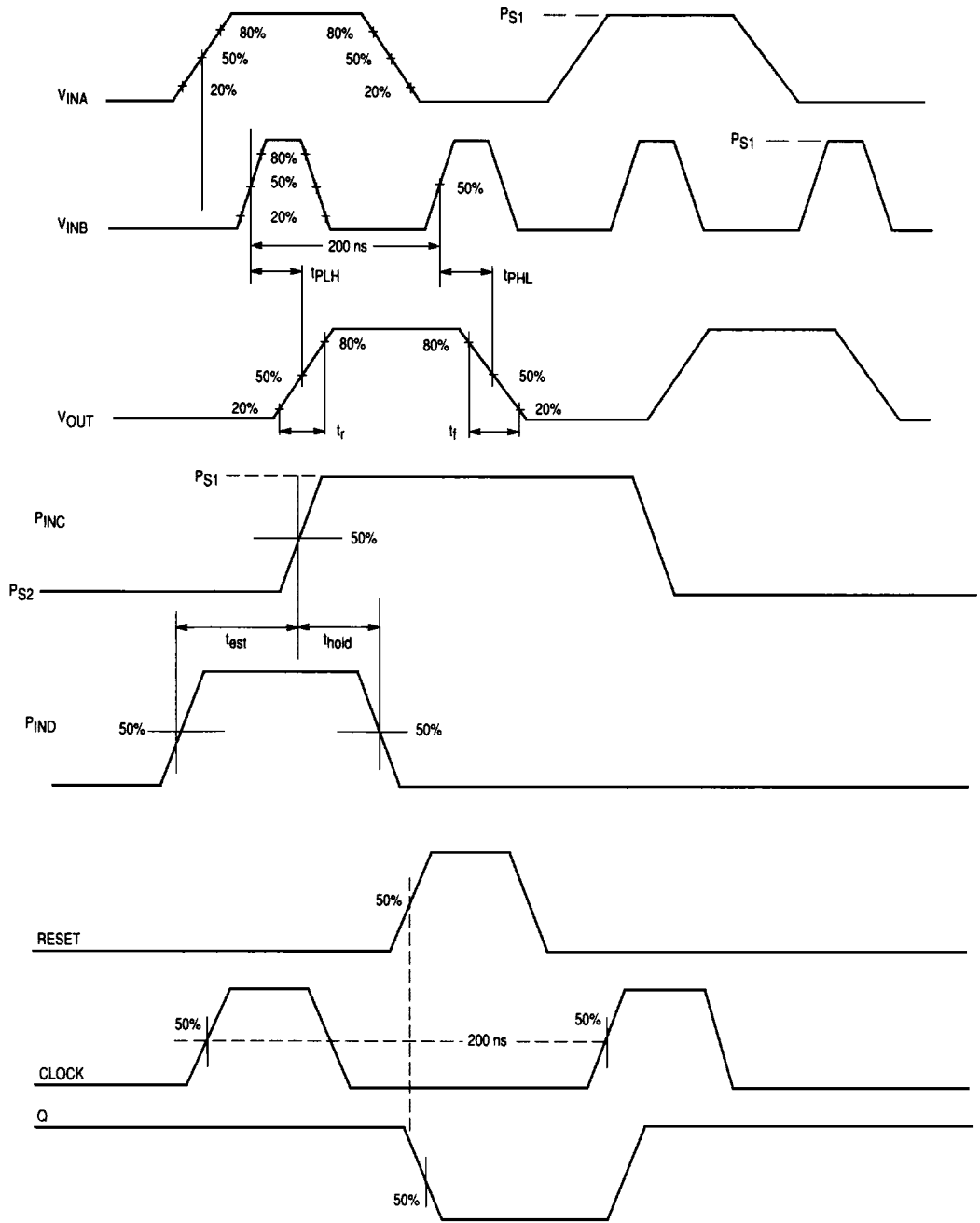


NOTES

1. V_{IN} has the following characteristics:
 - a) $PW \geq 20 \text{ ns}$
 - b) $f = 1.0 \text{ MHz}$

Figure 1. Switching Test Circuit and Waveforms

10H586



2

Figure 2. Switching Test Circuit and Waveforms

10H586

2

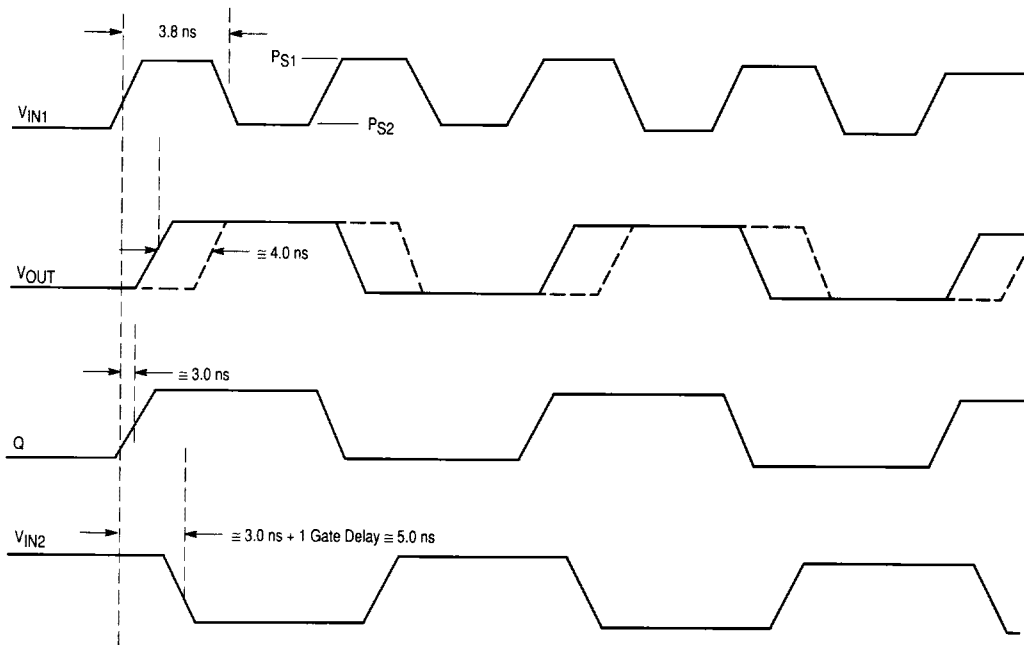


Figure 3. t_{TOGGLE} Waveforms

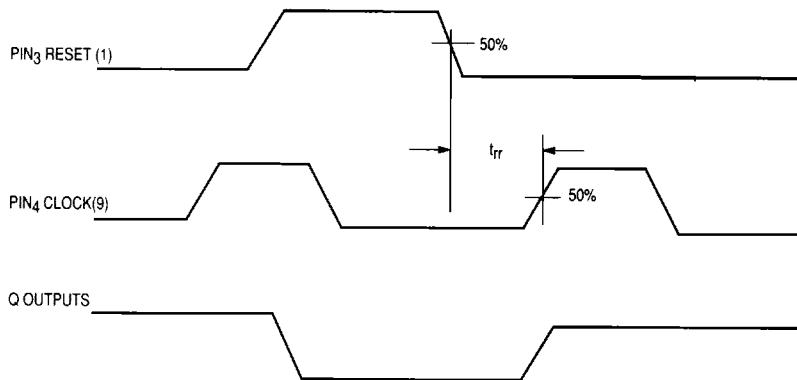


Figure 4. t_{rr} Waveforms

10H586 QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)									
	V _{IH1}	V _{IL1}	V _{IH2}	V _{IL2}	PS1	PS2	V _{EE1}	V _{EE2}	VEEL	VEEL
T _A = 25 °C	-0.78	-1.95	-1.11	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94	-2.94
T _A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94	-2.94
T _A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW													
		+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments VCC = 0 V, Output Load = 100 Ω to - 2.0 V													
		Subgroup 1		Subgroup 2		Subgroup 3			V _{IH1}	V _{IL1}	V _{IH2}	V _{IL2}	V _{EE1}	V _{EE2}	VCC	P. U. T.						
V _{OH}	High Output Voltage	Min	-1.01	Max	-0.78	Min	-0.86	Max	-0.65	Min	-1.06	Max	-0.84	V	5-7 9-12	5-7 9-12			8		16	2-4, 13-15
V _{OL}	Low Output Voltage	Min	-1.95	Max	-1.58	Min	-1.95	Max	-1.565	Min	-1.95	Max	-1.61	V	5-7 9-12	5-7 9-12			8		16	2-4, 13-15
V _{OH1}	High Output Voltage	Min	-1.01	Max	-0.78	Min	-0.86	Max	-0.65	Min	-1.06	Max	-0.84	V	5-7 9-12	1,5-7 10-12	5-7, 10-12	1	8	8	16	2-4, 13-15
V _{OL1}	Low Output Voltage	Min	-1.95	Max	-1.58	Min	-1.95	Max	-1.565	Min	-1.95	Max	-1.61	V	5-7 10-12	1,5-7 9-12	1	5-7, 10-12	8	8	16	2-4, 13-15
I _{EE}	Power Supply Current	Min	-110	Max		Min	-121	Max		Min	-121	Max		mA					8		16	8
I _{IH}	Input Current High	Min		Max	420	Min		Max	670	Min		Max	670	μA		9			8		16	9
I _{IH1}	Input Current High	Min		Max	265	Min		Max	430	Min		Max	430	μA	5-7 10-12				8		16	5-7, 10-12
I _{IH2}	Input Current High	Min		Max	1200	Min		Max	1900	Min		Max	1900	μA	1				8		16	1
I _{IL}	Input Current Low	Min	0.5	Max		Min	0.3	Max		Min	0.5	Max		μA						8	16	1,5-7 9-12

NOTES

1. Hold power during all V_{OH} and V_{OL} tests.



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	V _{IH1}	V _{IL1}	V _{IH2}	V _{IL2}	PS1	PS2	VEE1	VEE2	VEEL	VEEL
T _A = 25 °C	-0.78	-1.95	-1.11	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94	-2.94
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Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW											
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Functional Parameters:		Subgroup 9		Subgroup 10		Subgroup 11				V _{IN}		V _{OUT}		V _{CC}		V _{EEL}		P. U. T.		
		Min	Max	Min	Max	Min	Max			PS1										
t _{TLH}	Rise Time	0.7	2.4	0.7	2.6	0.7	2.6	ns			5-7, 9-12	2-4, 13-15	16	8					2-4, 13-15	
t _{THL}	Fall Time	0.7	2.4	0.7	2.6	0.7	2.6	ns			5-7, 9-12	2-4, 13-15	16	8					2-4, 13-15	
t _{PLH}	Propagation Delay Clk or Reset to Q	0.7	2.7	0.7	3.0	0.7	3.0	ns		5-7 10-12	5-7, 9-12	2-4, 13-15	16	8					2-4, 13-15	
t _{PLH}	Propagation Delay Clk or Reset to Q	0.7	2.7	0.7	3.0	0.7	3.0	ns		5-7 10-12	5-7, 9-12	2-4, 13-15	16	8					2-4, 13-15	
t _{SET}	Setup Time	1.5		1.5		1.5		ns			5-7, 9-12	2-4, 13-15	16	8					2-4, 13-15	
t _{HOLD}	Hold Time	1.0		1.0		1.0		ns			5-7, 9-12	2-4, 13-15	16	8					2-4, 13-15	
t _{RR}	Reset Recovery Time	3.0		3.0		3.0		ns			5-7, 9-12	2-4, 13-15	16	8					2-4, 13-15	
t _{TOGGLE}	Toggle Frequency	250		250		250		MHz			9	2-4, 13-15	16	8					2-4, 13-15	
				250		250					5-7, 9-12	2-4, 13-15	16	8					2-4, 13-15	