

### Features

- **Operating with Single 5V or 12V Input**
- **Drives N-Channel MOSFETs**
- **Simple Single-Loop Control Design**
  - Voltage-Mode PWM Control
  - Full 0% to 100% Duty Ratio
  - Fast Transient Response
- **±2% Output Voltage Accuracy Over Temperature**
- **Under-Voltage Protection for Output**
- **200/400kHz Constant Frequency Operation**
  - 200kHz for APW7037B
  - 400kHz for APW7037A
- **Small size, 8-PIN Package (SOIC or TSSOP)**
- **Lead Free and Green Devices Available (RoHS Compliant)**

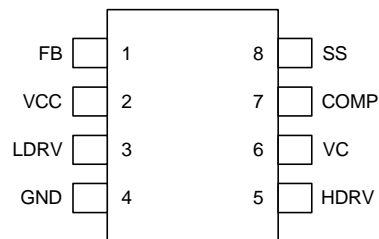
### Applications

- **Graphics Cards**
- **DDR Memory Power Supply**
- **DDR Memory Termination Voltage**
- **Low-Voltage Distributed Power Supplies**

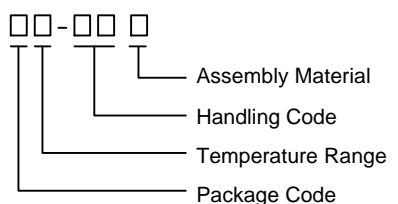
### General Description

The APW7037 series are designed to provide a low cost synchronous Buck regulator for on-board DC to DC converter applications. The APW7037 series together with dual N-channel MOSFETs such as APM7313, provide a low cost solution for such applications. Each device features an internal 200/400kHz oscillator, Power-On-Reset (POR) for both VCC and VC supplies, an external programmable soft-start function as well as output under-voltage detection that latches off the device when an output short is detected.

### Pin Configuration



## Ordering and Marking Information

<p>APW7037A/B</p>  <p>Assembly Material Handling Code Temperature Range Package Code</p>	<p>Package Code K : SOP-8                      O : TSSOP-8 Operating Junction Temperature Range C : 0 to 70°C Handling Code TR : Tape &amp; Reel Assembly Material L : Lead Free Device G : Halogen and Lead Free Device</p>	
<p>APW7037A/B K :</p>	<table border="1" data-bbox="427 609 598 660"> <tr> <td>APW7037A/B XXXXX</td> </tr> </table> <p>XXXXX - Date Code</p>	APW7037A/B XXXXX
APW7037A/B XXXXX		
<p>APW7037A/B O :</p>	<table border="1" data-bbox="427 698 614 750"> <tr> <td>APW7037A/B XXXXX</td> </tr> </table> <p>XXXXX - Date Code</p>	APW7037A/B XXXXX
APW7037A/B XXXXX		

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020C for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

## Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
$V_{CC}$	VCC to GND	-0.2~30	V
$V_C$	VC to GND	-0.2~30	V
$T_J$	Operating Junction Temperature	0~125	°C
$T_{STG}$	Storage Temperature	-65~150	°C
$T_{SDR}$	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

## Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
$\theta_{JA}$	Thermal Resistance in Free Air	SOP-8 160 TSSOP-8 124	°C/W

## Electrical Characteristics

Unless otherwise specified, these specifications apply over  $V_{CC}=5V$ ,  $V_C=12V$  and  $T_A=0$  to  $70^\circ C$ . Typical values refer to  $T_A=25^\circ C$ .

Symbol	Parameter	Test Conditions	APW7037/A/B			Unit
			Min.	Typ.	Max.	
<b>SUPPLY CURRENT</b>						
ICC	VCC Dynamic Supply Current	FOSC=200kHz, CL=1500pF	2	3	5	mA
IC	VC Dynamic Supply Current	FOSC=200kHz, CL=1500pF	2	5.5	8	mA
ICCQ	VCC Static Supply Current	SS=GND	0.5	1.5	3	mA
ICQ	VC Static Supply Current	SS=GND	0.2	0.4	1	mA
<b>POWER-ON-RESET</b>						
	Rising VCC Threshold		4.0	4.2	4.4	V
	VCC POR Hysteresis		-	0.25	-	V
	Rising VC Threshold		3.1	3.3	3.5	V
	VC POR Hysteresis		-	0.2	-	V
<b>OSCILLATOR</b>						
FOSC	Free Running Frequency	APW7037A APW7037B	360 180	400 200	440 220	kHz
$\Delta V_{osc}$	Ramp Amplitude		-	1.10	-	V
<b>ERROR AMPLIFIER</b>						
IFB1	FB Pin Input Bias Current	SS=3V, VFB=1V	-	1	-	nA
IFB2	FB Pin Input Bias Current	SS=0V, VFB=1V	-	-64	-	$\mu A$
GM	Transconductance		450	600	750	$\mu mho$
<b>REFERENCE VOLTAGE</b>						
VFB	FB Pin Regulation Voltage	APW7037A APW7037B	0.784 0.784	0.800 0.800	0.816 0.816	V
LREG	VFB Line Regulation	VCC = 5~12V	-	0.2	0.35	%
<b>GATE DRIVERS</b>						
	HDRV Rising Time	CL = 1500pF	-	20	50	nS
	HDRV Falling Time	CL = 1500pF	-	15	50	nS
	LDRV Rising Time	CL = 1500pF	-	25	50	nS
	LDRV Falling Time	CL = 1500pF	-	25	50	nS
	Dead Band Time		50	150	250	nS
<b>PROTECTION</b>						
VFBUV	FB Under-Voltage Threshold	VFB Falling APW7037A APW7037B	0.3 0.3	0.4 0.4	0.5 0.5	V
VSD	Shutdown Threshold Voltage	Pull the voltage of SS pin	-	0.5	-	V
ISS	Soft-Start Current	SS=0	10	20	30	$\mu A$

## Function Pin Description

### FB (Pin 1)

Connect this pin to the output (VOUT) of the PWM converter via an external resistor divider to provide a voltage feedback path for the converter. The output voltage set by the resistor divider is determined using the following formula :

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{OUT}}{R_{GND}}\right)$$

where ROUT is the resistor connected from VOUT to FB , and RGND is the resistor connected from FB to ground. The voltage at this pin is also monitored for Under-Voltage protection.

### VCC (Pin 2)

Connect this pin to input voltage from 5V to 20V. This pin provides the bias for the control circuitry and the low-side power MOSFET driver (LDRV). The voltage at this pin is monitored for Power-On-Reset (POR) purpose.

### LDRV (Pin 3)

Connect this pin to the gate of the low-side power MOSFET. This pin provides the gate drive for the MOSFET.

### GND (Pin 4)

Signal and power ground for the IC. All voltage levels are measured with respect to this pin.

### HDRV (Pin 5)

Connect this pin to the gate of the high-side power MOSFET. This pin provides the gate drive for the MOSFET.

### VC (Pin 6)

This pin provides bias voltage to the high-side MOSFET driver. A bootstrap circuit may be used to pump a boot voltage for enforcing the driving capability of the gate driver and improving the performance of the MOSFET.

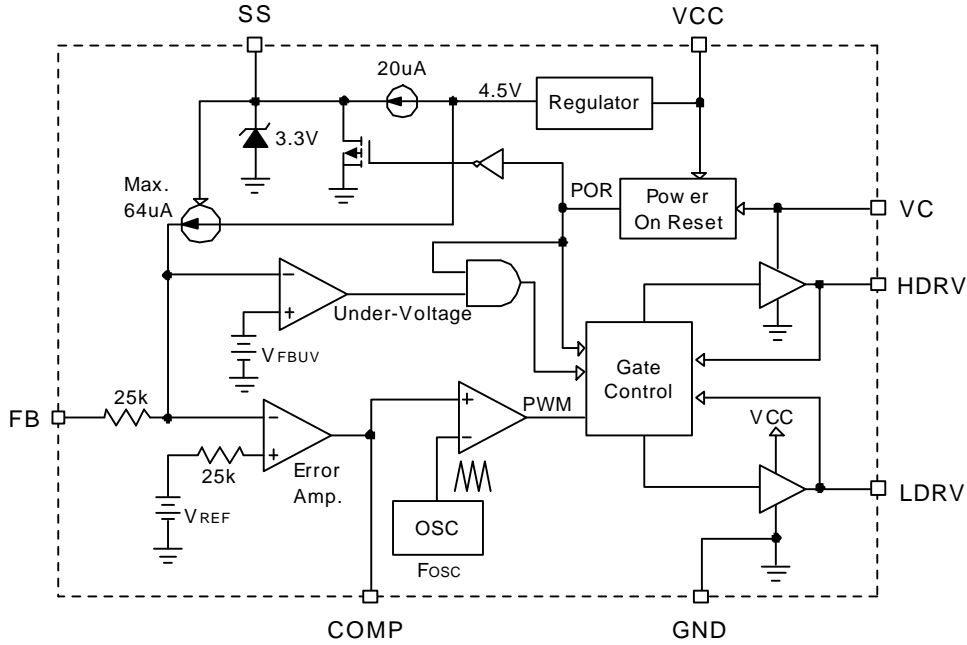
### COMP (Pin 7)

This pin is the output of the error amplifier. Add an external resistor-capacitor network to provide a loop compensation for the PWM converter.

### SS (Pin 8)

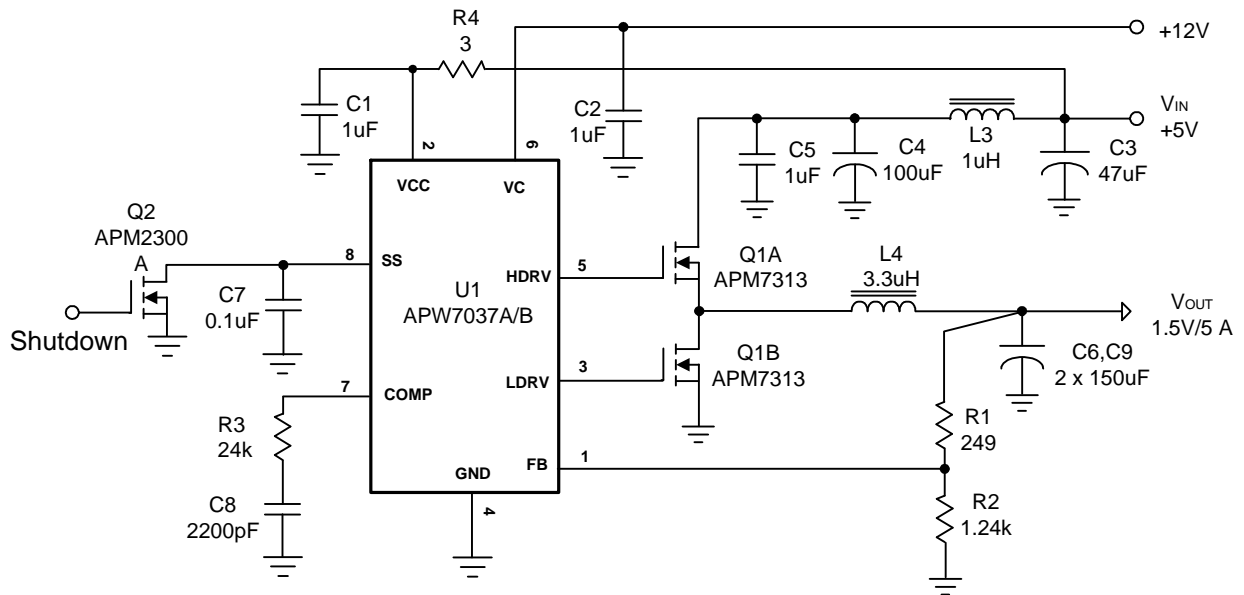
Connect a capacitor from this pin to ground. This capacitor, along with an internal 20µA current source, sets the soft-start interval of the PWM converter and prevents the outputs from overshoot as well as limits the input current. Pull this pin below 0.5V can shutdown the converter.

### Block Diagram



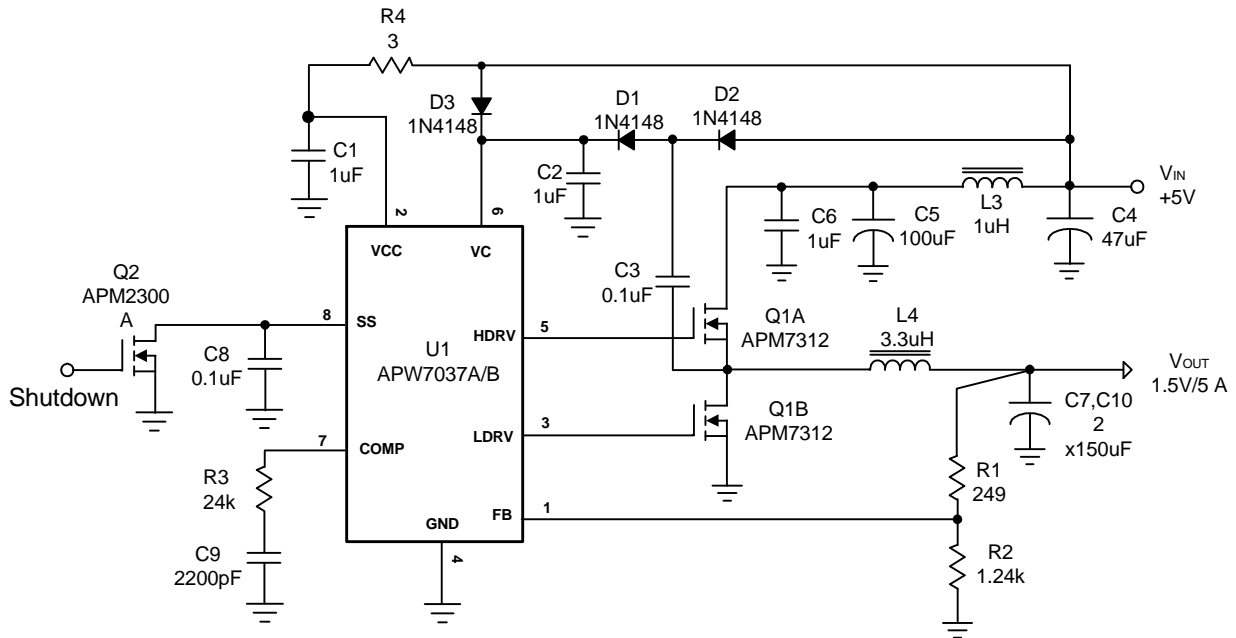
### Typical Application Circuit

1. Dual supply voltage(5V and 12V) application

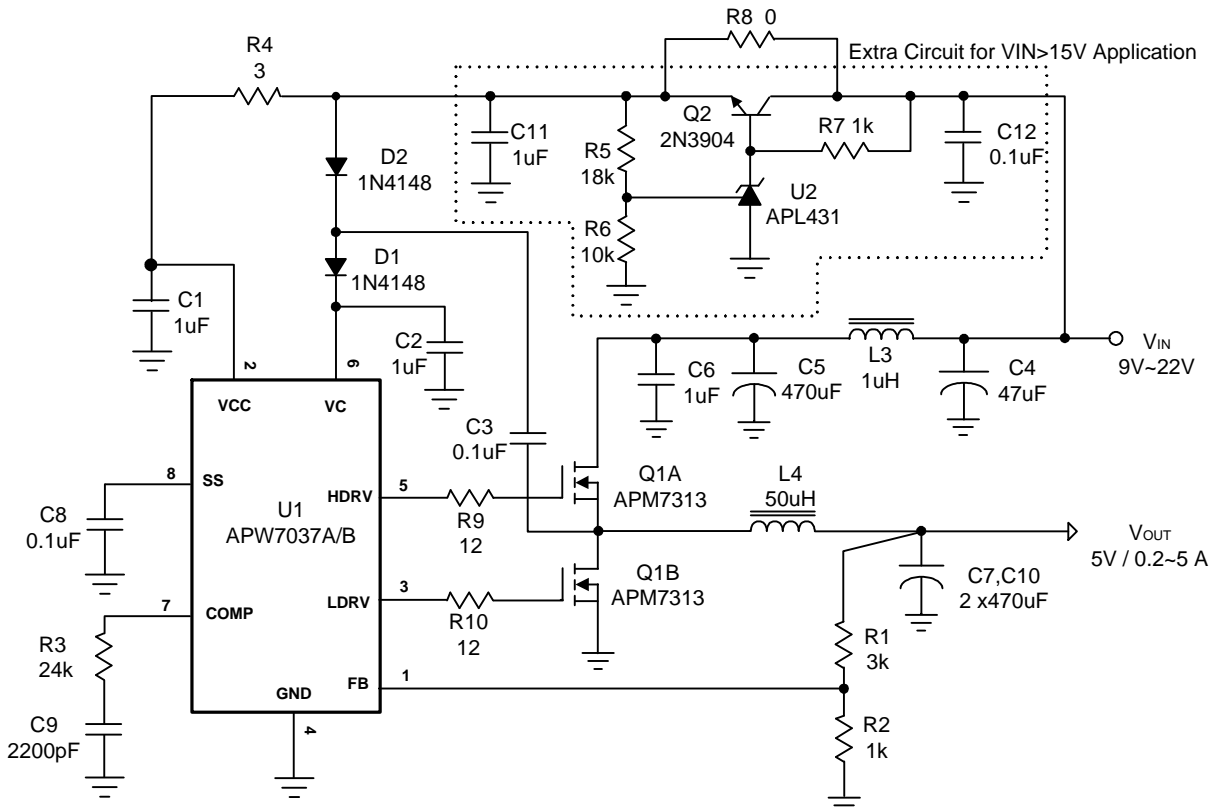


## Typical Application Circuit (Cont.)

### 2. Single supply voltage(5V) application

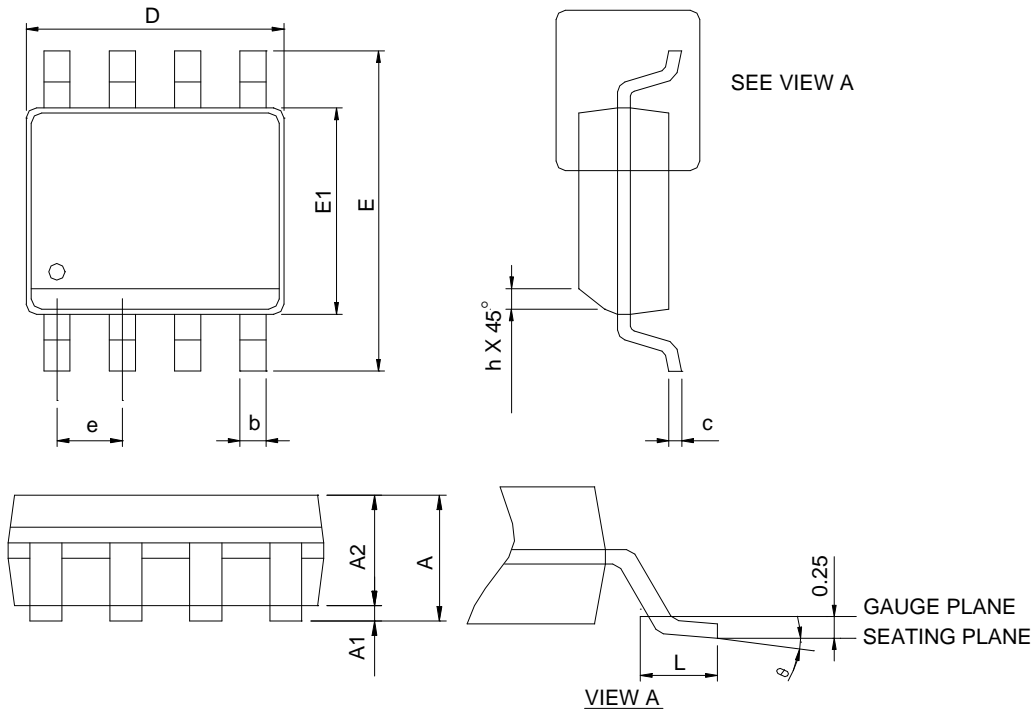


### 3. LCD Monitor Application Circuit



Package Information

SOP-8

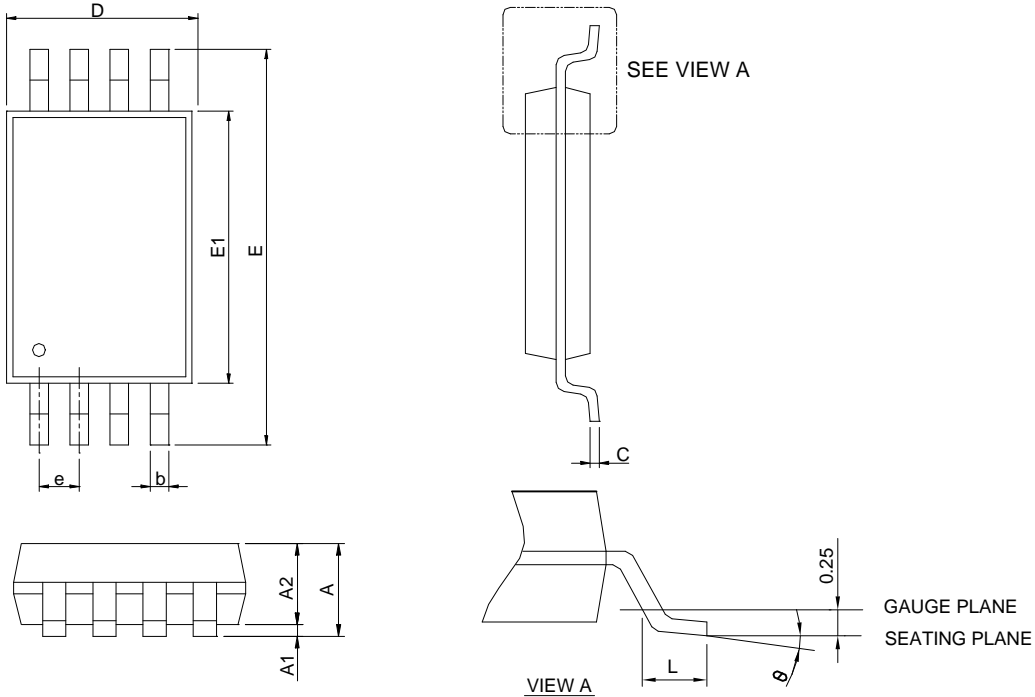


SYMBOL	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.10	0.25	0.004	0.010
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
$\theta$	0°	8°	0°	8°

- Note: 1. Follow JEDEC MS-012 AA.  
 2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.  
 3. Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Package Information

TSSOP-8

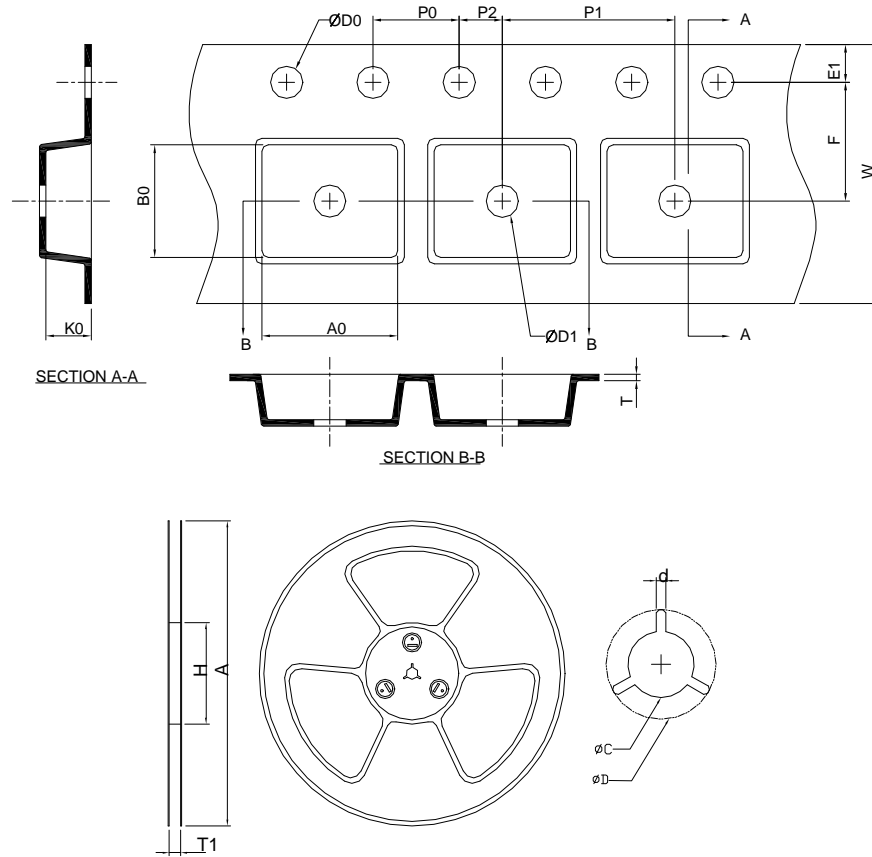


SYMBOL	TSSOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.20		0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.031	0.041
b	0.19	0.30	0.007	0.012
c	0.09	0.20	0.004	0.008
D	2.90	3.10	0.114	0.122
E	6.20	6.60	0.244	0.260
E1	4.30	4.50	0.169	0.177
e	0.65 BSC		0.026 BSC	
L	0.45	0.75	0.018	0.030
θ	0°	8°	0°	8°

- Note : 1. Follow JEDEC MO-153 AA  
 2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.  
 3. Dimension "E1" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.



### Carrier Tape & Reel Dimensions



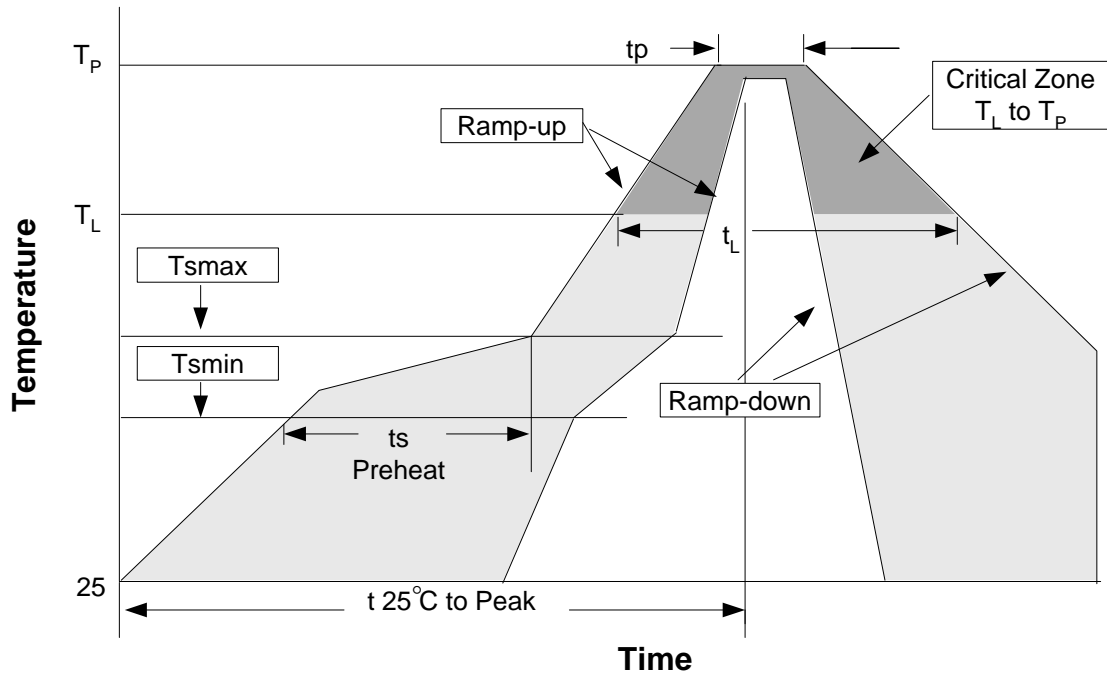
Application	A	H	T1	C	d	D	W	E1	F
SOP-8	330.0 ±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0 ±0.30	1.75 ±0.10	5.5 ±0.05
	<b>P0</b>	<b>P1</b>	<b>P2</b>	<b>D0</b>	<b>D1</b>	<b>T</b>	<b>A0</b>	<b>B0</b>	<b>K0</b>
	4.0 ±0.10	8.0 ±0.10	2.0 ±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40 ±0.20	5.20 ±0.20	2.10 ±0.20
Application	A	H	T1	C	d	D	W	E1	F
TSSOP-8	330.0 ±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0 ±0.30	1.75 ±0.10	5.5 ±0.10
	<b>P0</b>	<b>P1</b>	<b>P2</b>	<b>D0</b>	<b>D1</b>	<b>T</b>	<b>A0</b>	<b>B0</b>	<b>K0</b>
	4.00 ±0.10	8.00 ±0.10	2.00 ±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.90 ±0.20	3.40 ±0.20	1.60 ±0.20

(mm)

### Devices Per Unit

Package Type	Unit	Quantity
SOP-8	Tape & Reel	2500
TSSOP-8	Tape & Reel	2500

**Reflow Condition (IR/Convection or VPR Reflow)**



**Reliability Test Program**

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C, 5 sec
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @125°C
PCT	JESD-22-B, A102	168 Hrs, 100%RH, 121°C
TST	MIL-STD-883D-1011.9	-65°C~150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms, 1 <sub>tr</sub> > 100mA

**Classification Reflow Profiles**

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T <sub>L</sub> to T <sub>P</sub> )	3°C/second max.	3°C/second max.
Preheat		
- Temperature Min (T <sub>min</sub> )	100°C	150°C
- Temperature Max (T <sub>max</sub> )	150°C	200°C
- Time (min to max) (t <sub>s</sub> )	60-120 seconds	60-180 seconds
Time maintained above:		
- Temperature (T <sub>L</sub> )	183°C	217°C
- Time (t <sub>L</sub> )	60-150 seconds	60-150 seconds
Peak/Classification Temperature (T <sub>p</sub> )	See table 1	See table 2
Time within 5°C of actual Peak Temperature (t <sub>p</sub> )	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Note: All temperatures refer to topside of the package. Measured on the body surface.

## Classification Reflow Profiles (Cont.)

Table 1. SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm <sup>3</sup> <350	Volume mm <sup>3</sup> ≥350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

Table 2. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm <sup>3</sup> <350	Volume mm <sup>3</sup> 350-2000	Volume mm <sup>3</sup> >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*

\*Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.

## Customer Service

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