ANALOG DEVICES

Octal 8-Bit CMOS D/A Converter

DAC8800

FEATURES
±1/2 LSB Total Unadjusted Error
2 μs Settling Time
Serial Data Input
±Full-Scale Output Set by $V_{REF}H$ and $V_{REF}L$
Unipolar and Bipolar Operation
TTL Input Compatible
20-Pin DIP or SOL Package
Low Cost

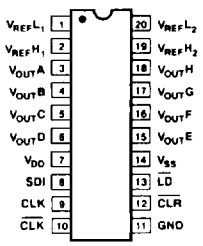
APPLICATIONS
Voltage Setpoint Control
Digital Offset & Gain Adjustment
Microprocessor Controlled Calibration
General Purpose Trimming Adjustments

GENERAL DESCRIPTION

The DAC8800 TrimDAC® is designed to be a general purpose digitally controlled voltage adjustment device. The output voltage range can be independently set for each set of four D/A converters. In addition, both unipolar and bipolar output voltage ranges are easy to establish by external reference input high and low terminals. The digitally-programmed output voltages are ideal for op amp trimming, voltage-controlled amplifier gain setting and any general purpose trimming tasks.

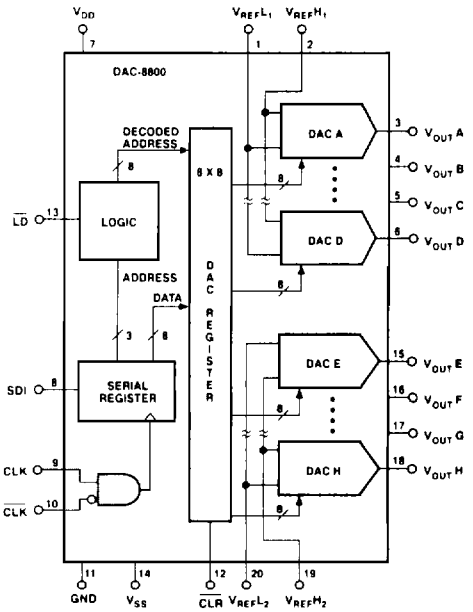
A three-wire serial digital interface loads the contents of eight internal DAC registers which establish the output voltage levels. An asynchronous Clear (CLR) input places all DACs in a zero code output condition, very handy for system power-up. An internal regulator provides TTL input compatibility over a wide range of V_{DD} supply voltages. Single supply operation is available by connecting V_{SS} to GND.

PIN CONNECTIONS



TrimDAC is a registered trademark of Analog Devices, Inc.

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION[1]

Model	Temperature Range	Package Description[2]
DAC8800BR[3]	–55°C to +125°C	Q-20 Cerdip
DAC8800FR	–40°C to +85°C	Q-20 Cerdip
DAC8800FP	–40°C to +85°C	N-20 Plastic DIP
DAC8800FS	–40°C to +85°C	R-20 SOL

NOTES
[1]Burn in is available on commercial and industrial temperature range parts in Cerdip and plastic DIP packages.
[2]For outline information see Package Information section.
[3]For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

DAC8800–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS[1]

Single Supply; V_{DD} = +12 V, V_{SS} = 0 V, $V_{REF}H$ = +5 V, $V_{REF}L$ = 0 V; or Dual Supply; V_{DD} = +12 V, V_{SS} = –5 V, $V_{REF}H$ = +2.5 V, $V_{REF}L$ = –2.5 V; F Grade; –40°C ≤ T_A ≤ +85°C; B Grade; –55°C ≤ T_A ≤ +125°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
STATIC ACCURACY (All specifications apply for DACs A, B, C, D, E, F, G, H)						
Resolution	N		8			Bits
Total Unadjusted Error[2]	TUE				±1/2	LSB
Differential Nonlinearity[3]	DNL				±1	LSB
Full Scale Error	G_{FSE}				±1/2	LSB
Zero Code Error	V_{ZSE}				±1/2	LSB
DAC Output Resistance	R_{OUT}		8	12	16	kΩ
DAC Output Resistance Match	$\Delta R_{OUT}/R_{OUT}$			0.5		%
REFERENCE INPUT						
Voltage Range[5]	$V_{REF}H$	Pins 2 & 19	$V_{REF}L$		(V_{DD} – 4)	V
	$V_{REF}L$	Pins 1 & 20	V_{SS}		$V_{REF}H$	V
Input Resistance	$V_{REF}H$	Digital Inputs = 55_H	2	3		kΩ
Input Resistance Match	$\Delta R_{REF}H/R_{REF}H$	Digital Inputs = 55_H		0.5		%
Reference Input Capacitance[4]	C_{REF}	Digital Inputs All Zeros		50	75	pF
	C_{REF}	Digital Inputs All Ones		75	100	pF
DIGITAL INPUTS						
Logic High	V_{INH}		2.4			V
Logic Low	V_{INL}				0.8	V
Input Current	I_{IN}	V_{IN} = 0 V or +5 V			±1	μA
Input Capacitance[4]	C_{IN}			4	8	pF
Input Coding				Binary		
POWER SUPPLIES[6]						
Positive Supply Current	I_{DD}	Dual Supply TTL		1	2	mA
		Dual Supply CMOS		0.2	0.4	mA
Negative Supply Current	I_{SS}	Dual Supply		0.01	0.2	mA
Power Dissipation	P_{DISS}	Single Supply Operation		12	24	mW
		Dual Supply Operation		12	25	mW
DC Power Supply Rejection Ratio	PSRR	ΔV_{DD} = ±5%		0.001	0.01	%/%
DYNAMIC PERFORMANCE[4]						
V_{OUT} Settling Time	t_S	±1/2 LSB Error Band		0.8	2	μs
Channel-to-Channel Crosstalk[7]	CT	Measured Between Adjacent DAC Outputs		80		nVs
SWITCHING CHARACTERISTICS[4, 8]						
Input Clock Pulse Width	t_{CH}, t_{CL}	Clock Level High or Low	60			ns
Data Setup Time	t_{DS}		30			ns
Data Hold Time	t_{DH}		30			ns
DAC Register Load Pulse Width	t_{LD}		50			ns
Clear Pulse Width	t_{CLR}		50			ns
Clock Edge to Load Time	t_{CKLD}		50			ns
Edge Time	t_{TDCK}		50			ns

NOTES

[1]Testing performed in SINGLE SUPPLY mode, except I_{DD}, I_{SS} and PSRR which are tested in DUAL SUPPLY mode.

[2]Includes Full Scale Error, Relative Accuracy, and Zero Code Error.

[3]All devices guaranteed monotonic over the full operating temperature range.

[4]Guaranteed by design and not subject to production test.

[5]V_{DD} – 4 volts is the maximum reference voltage for the above specifications. Also $V_{REF}H > V_{REF}L$.

[6]Digital Input voltages V_{IS} = V_{INL} or V_{INH} for TTL condition; V_{IS} = 0 V or +5 V for CMOS condition. DAC outputs unloaded. P_{DISS} is calculated from (I_{DD} × V_{DD}) + (I_{SS} × V_{SS}).

[7]Measured at V_{OUT} pin where an adjacent V_{OUT} pin is making a full-scale voltage change.

[8]See timing diagram for location of measured values.

Specifications subject to change without notice.