**DALLAS SEMICONDUCTOR**

# DS1000
## 5-Tap Silicon Delay Line

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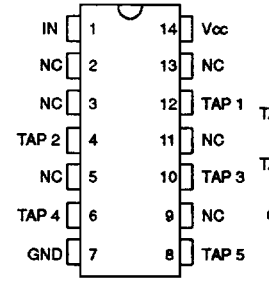
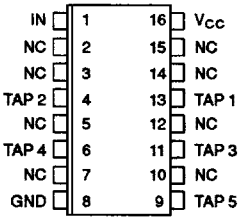
### FEATURES

- All-silicon time delay
- 5 taps equally spaced
- Delays are stable and precise
- Both leading and trailing edge accuracy
- Delay tolerance ±5% or ±2 ns, whichever is greater
- Economical
- Auto-insertable, low profile
- Low-power CMOS
- TTL/CMOS-compatible
- Vapor phase, IR and wave solderable
- Custom delays available
- Fast turn prototypes
- Extended temperature range available

### PIN ASSIGNMENT

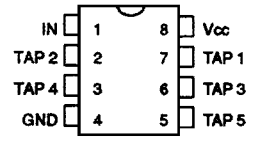



DS1000 14-PIN DIP (300 MIL)
DS1000G 14-PIN GULLWING (300 MIL)
DS1000K 14-PIN SHEARED NC
See Mech. Drawings Sect. 16, Pgs. 1 & 3

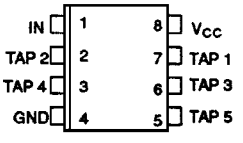



DS1000S 16-PIN SOIC
(300 MIL)
See Mech. Drawing
Sect. 16, Pg. 6

Also Available
In Die Form




DS1000M 8-PIN DIP (300 MIL)
DS1000H 8-PIN GULLWING (300 MIL)
See Mech. Drawings
Section 16, Pgs. 1 & 3




DS1000Z 8-PIN SOIC
(150 MIL)
See Mech. Drawing
Sect. 16, Pg. 5

### PIN DESCRIPTION

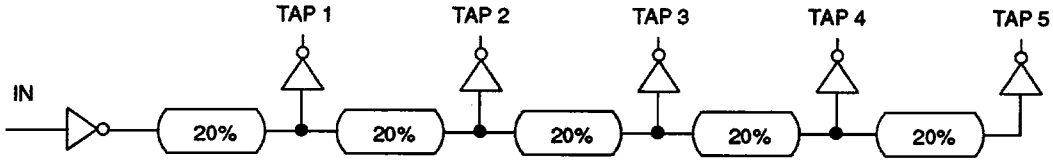
| | |
|---|---|
| TAP 1-TAP 5 | - Tap Output Number |
| $V_{CC}$ | - +5 Volts |
| GND | - Ground |
| NC | - No Connection |
| IN | - Input |

### DESCRIPTION

The DS1000 series delay lines have five equally spaced taps providing delays from 4 ns to 500 ns. These devices are offered in a standard 14-pin DIP that is pin-compatible with hybrid delay lines. Alternatively, 8-pin DIPs and surface mount packages are available to save PC board area. Low cost and superior reliability over hybrid technology is achieved by the combination of a 100% silicon delay line and industry standard DIP and SOIC packaging. In order to maintain complete pin compatibility, DIP packages are available with hybrid lead configurations. The DS1000 series delay lines provide a nominal accuracy of ±5% or ±2 ns, whichever is greater. The DS1000 5-Tap Silicon Delay Line reproduces the input logic state at the output after a fixed delay as specified by the extension of the part number after the dash. The DS1000 is designed to reproduce both leading and trailing edges with equal precision. Each tap is capable of driving up to ten 74LS loads.

Dallas Semiconductor can customize standard products to meet special needs. For special requests and rapid delivery, call (214) 450-5348.

## LOGIC DIAGRAM Figure 1




## PART NUMBER DELAY TABLE ($t_{PHL}$, $t_{PLH}$) Table 1

| PART NO. | TAP 1 | TAP 2 | TAP 3 | TAP 4 | TAP 5 |
|---|---|---|---|---|---|
| DS1000-20* | 4 ns | 8 ns | 12 ns | 16 ns | 20 ns |
| DS1000-25 | 5 ns | 10 ns | 15 ns | 20 ns | 25 ns |
| DS1000-30 | 6 ns | 12 ns | 18 ns | 24 ns | 30 ns |
| DS1000-35 | 7 ns | 14 ns | 21 ns | 28 ns | 35 ns |
| DS1000-40 | 8 ns | 16 ns | 24 ns | 32 ns | 40 ns |
| DS1000-45 | 9 ns | 18 ns | 27 ns | 36 ns | 45 ns |
| DS1000-50 | 10 ns | 20 ns | 30 ns | 40 ns | 50 ns |
| DS1000-60 | 12 ns | 24 ns | 36 ns | 48 ns | 60 ns |
| DS1000-75 | 15 ns | 30 ns | 45 ns | 60 ns | 75 ns |
| DS1000-100 | 20 ns | 40 ns | 60 ns | 80 ns | 100 ns |
| DS1000-125 | 25 ns | 50 ns | 75 ns | 100 ns | 125 ns |
| DS1000-150 | 30 ns | 60 ns | 90 ns | 120 ns | 150 ns |
| DS1000-175 | 35 ns | 70 ns | 105 ns | 140 ns | 175 ns |
| DS1000-200 | 40 ns | 80 ns | 120 ns | 160 ns | 200 ns |
| DS1000-250 | 50 ns | 100 ns | 150 ns | 200 ns | 250 ns |
| DS1000-350 | 70 ns | 140 ns | 210 ns | 280 ns | 350 ns |
| DS1000-450 | 90 ns | 180 ns | 270 ns | 360 ns | 450 ns |
| DS1000-500 | 100 ns | 200 ns | 300 ns | 400 ns | 500 ns |

Custom delays available.
*Consult Dallas Semiconductor for availability.

## ABSOLUTE MAXIMUM RATINGS*

| | |
|---|---|
| Voltage on Any Pin Relative to Ground | -1.0V to 7.0V |
| Operating Temperature | -40°C to +85°C |
| Storage Temperature | -55°C to 125°C |
| Soldering Temperature | 260°C for 10 seconds |
| Short Circuit Output Current | 50 mA for 1 second |

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

## DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, $V_{CC}$ = 5.0V ± 5%)

| PARAMETER | SYM | TEST CONDITION | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | | 4.75 | 5.00 | 5.25 | V | 1 |
| High Level Input Voltage | $V_{IH}$ | | 2.2 | | $V_{CC}$ + 0.5 | V | 1 |
| Low Level Input Voltage | $V_{IL}$ | | -0.5 | | 0.8 | V | 1 |
| Input Leakage Current | $I_I$ | $0.0V \le V_I \le V_{CC}$ | -1.0 | | 1.0 | uA | |
| Active Current | $I_{CC}$ | $V_{CC}$= Max; Period= Min. | | 35 | 75 | mA | 2,8 |
| High Level Output Current | $I_{OH}$ | $V_{CC}$=Min. $V_{OH}$=4 | | | -1 | mA | |
| Low Level Output Current | $I_{OL}$ | $V_{CC}$=Min. $V_{OL}$=0.5 | 12 | | | mA | |

## AC ELECTRICAL CHARACTERISTICS

($t_A$ = 25°C, $V_{CC}$ = 5V ± 5%)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Pulse Width | $t_{WI}$ | 40% of Tap 5 $t_{PLH}$ | | | ns | 7 |
| Input to Tap Delay (leading edge) | $t_{PLH}$ | | Table 1 | | ns | 3, 4, 5, 6, 9 |
| Input to Tap Delay (trailing edge) | $t_{PHL}$ | | Table 1 | | ns | 3, 4, 5, 6, 9 |
| Power-up Time | $t_{PU}$ | | | 100 | ms | |
| | Period | 4 ($t_{WI}$) | | | ns | 7 |

## CAPACITANCE

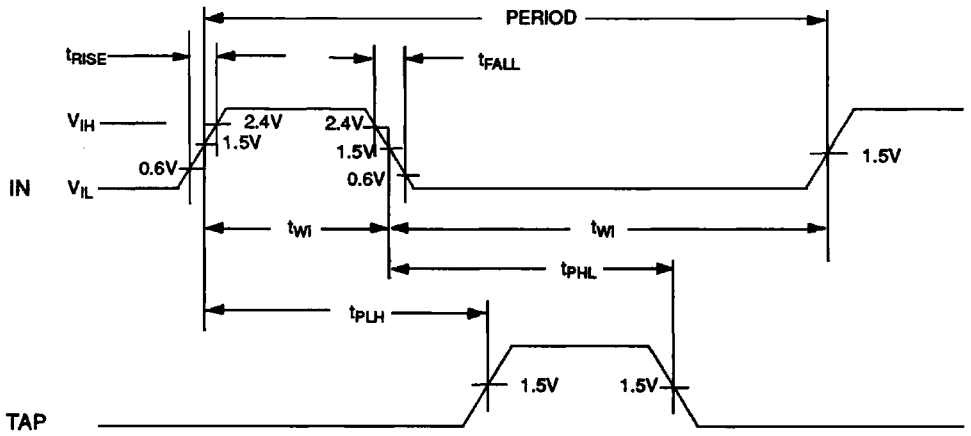
($t_A$ = 25°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | | 5 | 10 | pF | |

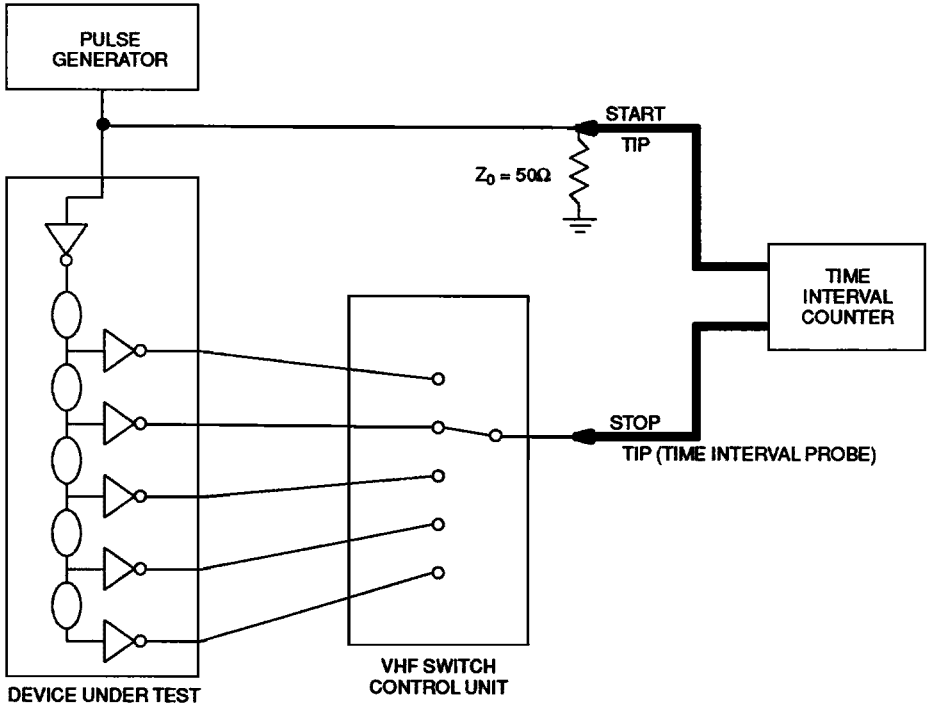
**NOTES:**

1. All voltages are referenced to ground.
2. Measured with outputs open.
3. $V_{CC}$= 5V @25°C. Delays accurate on both rising and falling edges within ±2 ns or 5%, whichever is greater.
4. For DS1000 delay lines with a TAP 5 delay of 50 ns or greater, temperature variations from 25°C to 0°C or 70°C may produce an additional input to tap delay shiift of ± 1 ns or ± 3%, whichever is greater.
5. For DS1000 delay lines with a TAP 5 delay less than 50 ns, temperature variations from 25°C to 0°C or 70° may produce an additional input to tap delay shift of ± 1 ns or ± 10%, whichever is greater.
6. All tap delays tend to vary unidirectionally with temperature or voltage changes. For example, if TAP 1 slows down, all other taps also slow down; TAP3 can never be faster than TAP2.
7. Pulse width and period specifications may be exceeded; however, accuracy will be application-sensitive (decoupling, layout, etc.).
8. $I_{CC}$ is a function of frequency and TAP 5 delay. Only a -25 operating with a 40 ns period and $V_{CC}$ = 5.25V will have an $I_{CC}$ = 75 mA. For example a -100 will never exceed 30 mA, etc.
9. See "Test Conditions" section at the end of this data sheet.

**TIMING DIAGRAM-SILICON DELAY LINE** Figure 2



**TEST CIRCUIT** Figure 3




## TERMINOLOGY

**Period:** The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

**$t_{WI}$ (Pulse Width):** The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

**$t_{RISE}$ (Input Rise Time):** The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

**$t_{FALL}$ (Input Fall Time):** The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

**$t_{PLH}$ (Time Delay, Rising):** The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of any tap output pulse.

**$t_{PHL}$ (Time Delay, Falling):** The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of any tap output pulse.

## TEST SETUP DESCRIPTION

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1000. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter ( 20 ps resolution) connected between the input and each tap. Each tap is selected and connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

## TEST CONDITIONS

### INPUT :

| | |
|---|---|
| Ambient Temperature: | 25°C ± 3°C |
| Supply Voltage ($V_{CC}$): | 5.0V ± 0.1V |
| Input Pulse: | High = 3.0V ± 0.1V |
| | Low = 0.0V ± 0.1V |
| Source Impedance: | 50 ohm Max. |
| Rise and Fall Time: | 3.0ns Max. (measured between 0.6V and 2.4V) |
| Pulse Width: | 500ns (1us for -500) |
| Period: | 1 us (2us for -500) |

### OUTPUT:

Each output is loaded with the equivalent of one 74F04 input gate. Delay is measured at the 1.5V level on the rising and falling edge.

### NOTE:

Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.