GENERAL DESCRIPTION

The EM23C1000 series high performance Read Only Memory is organized as 131,072 words by 8 bits. It is designed to be compatible with all microprocessor and similar applications where high performance large bit storage and simple interface are important design considerations.
The EM23C1000 series have two type. The one is offer the simplest operation (no power down). Its programmable chip selects allow up to four 1M ROMs to be Wired-OR without external decoding.
The other one has the automatic power down feature. The power down capability is controlled by the Chip Enable (CE/$\overline{CE}$) input. When $\overline{CE}$ goes to high or CE goes low, the device will automatically goes to power down mode and remains in a low power standby mode as long as $\overline{CE}$ remains high. This unique feature provides system level power savings as much as 90%. An additional feature of this type is the Output Enable (OE/$\overline{OE}$) function. This eliminates bus connection in multiple bus microprocessor systems.

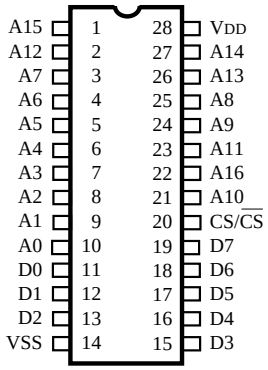
FEATURES

- 131,072 x 8 bit organization
- Access time 150 ns (max.) at $4.5V \leq V_{CC} \leq 5.5V$
- Low-power consumption:
  Operating: 193 mW (max.)
  Standby: 165 μW (max.)
- Fully-static operation
- Three-state outputs
- Completely TTL compatible.
- EM23C1000BP, EM23C1000FP.
  EM23C1000BM, EM23C1000FM.
  - Non power down version.
  - Two programmable chip selects (CS/$\overline{CS}$).
- EM23C1000AP, EM23C1000EP.
  EM23C1000AM, EM23C1000EM.
  - Automatic power down (CE/$\overline{CE}$).
  - Output Enable function (OE/$\overline{OE}$).
- Package:

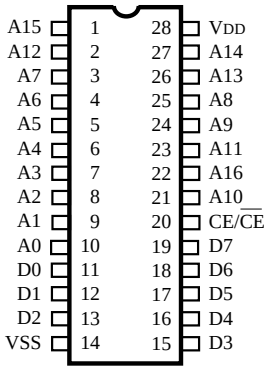
EM23C1000AP/BP	- 28 pins 600 mil plastic DIP.
EM23C1000AM/BM	- 28 pins 450 mil plastic SOP.
EM23C1000EP/FP	- 32 pins 600 mil plastic DIP.

PIN ASSIGNMENTS

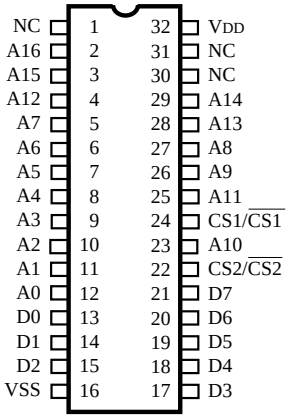
EM23C1000BP, EM23C1000BM



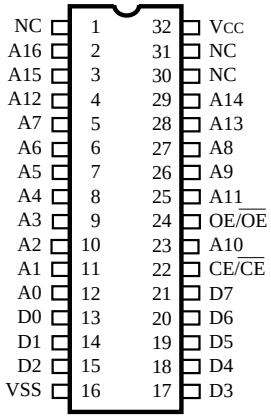
EM23C1000AP, EM23C1000AM



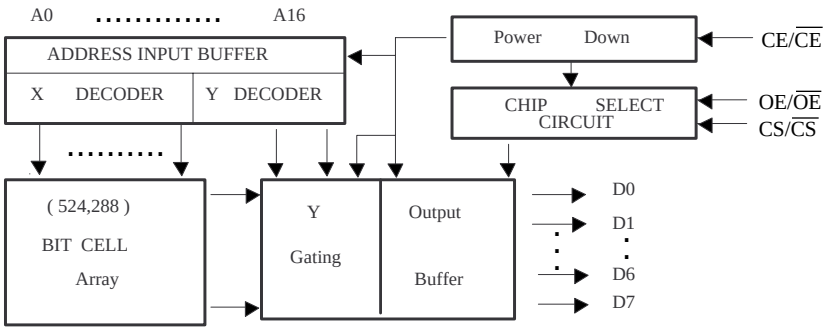
EM23C1000FP, EM23C1000FM



EM23C1000EP, EM23C1000EM



BLOCK DIAGRAM



FUNCTION DESCRIPTIONS

EM23C1000A/E

MODE	CE	OE	A0-A16	D0-D7	POWER
READ	ACTIVE	ACTIVE	VALID	DATA OUT	I_{CC}
STANDBY	INACTIVE	*	*	HIGH-Z	I_{SB}
OUTPUT DISABLE	ACTIVE	INACTIVE	*	HIGH-Z	I_{CC}

EM23C1000B/F

MODE	CS1	CS2	A0-A16	D0-D7	POWER
READ	ACTIVE	ACTIVE	VALID	DATA OUT	I_{CC}
OUTPUT DISABLE	INACTIVE	*	*	HIGH-Z	I_{CC}
OUTPUT DISABLE	*	INACTIVE	*	HIGH-Z	I_{CC}

NOTE : " * " MEANS ACTIVE (VALID) OR INACTIVE (INVALID)

ABSOLUTE MAXIMUM RATINGS

Items	Sym.	Condition	Rating
Supply voltage	V_{CC}		- 0.3V to 7 V
Input voltage	V_{IN}		- 0.3V to V_{CC}+0.3V
Output voltage	V_{OUT}		- 0.3V to V_{CC}+0.3V
Operating temperature	T_{OPR}		0 to 70°C
Storage temperature	T_{STR}		-65°C to 150°C

RECOMMENDED OPERATING CONDITIONS (T_{OPR}=0~70°C)

Parameter	Sym.	Min.	Max.	Unit
SUPPLY VOLTAGE	V_{CC}	4.5	5.5	V

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5V to 5.5V, T_{OPR}=0~70°C)

Parameter	Sym.	Condition	Min.	Max.	Unit	Note
Input "Low" voltage	V_{IL}		-0.3	0.8	V	
Input "High" voltage	V_{IH}		2.2	V_{CC}+0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 400mA		0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -100mA	2.4		V	
Input leakage current	I_{LI}	V_{IN} = 0V to V_{CC}		10	µA	
Output leakage current	I_{LO}	V_{OUT}=0V to V_{CC}		10	µA	1
Operating current	I_{CC}	t_{RC} = 150ns		35	mA	
Standby current	I_{SB}	$\overline{CE}$ = V_{IH}		2	mA	
		$\overline{CE}$ = V_{CC} -0.2V		30	µA	2
Input capacitance	C_{IN}	f = 1MHz,		10	pF	
Output capacitance	C_{OUT}	t_A = 25°C		10	pF	

Note:
1. $\overline{CE}$ /$\overline{OE}$ =V_{IH}, OE = V_{IL}, outputs open
2.Automatic power down version

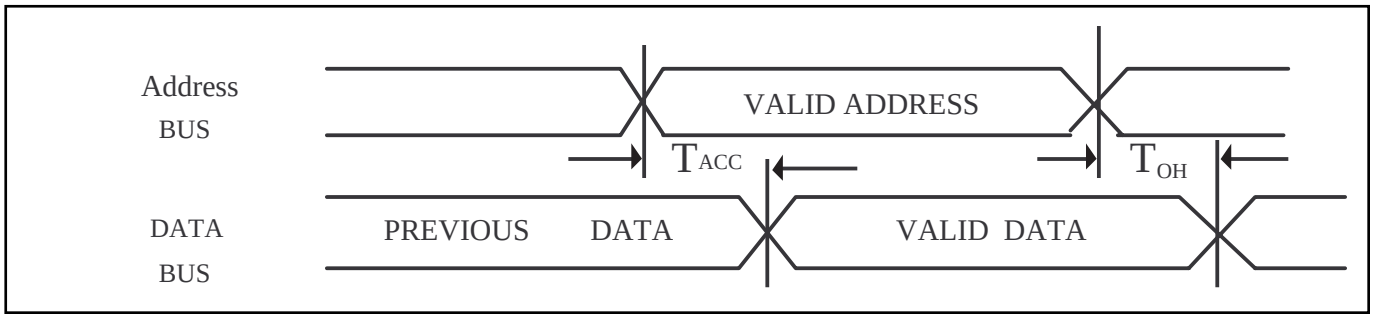
(V_{CC} = 4.5V to 5.5V T_{OPR}=0~70°C)

Parameter	Sym.	Condition	Min.	Max.	Unit
Cycle time	t_{CYC}		150		ns
Address access time	t_{ACC}			150	ns
Output hold after address change	t_{OH}		10		ns
Chip enable access time	t_{CE}	1		150	ns
Chip select access time	t_{CS}	3		70	ns
Output enable access time	t_{OE}	1,3		70	ns
Output disable delay	t_{DF}	2		50	ns

Note: 1. Power down type only. (A/E).
2. Outputs high impedence delay (t_{DF}) is measure from either $\overline{CE}$ or OE going high or CS going inactive, whichever occurs first.
3. Functions of $\overline{CS}$/CS & $\overline{OE}$/OE are identical.

TIMING DIAGRAM

Propagation delay from Address (CE/ $\overline{CE}$=Enable or CS/ $\overline{CS}$=Active)



Propagation delay from Chip Enable or Chip Select (Address Valid)