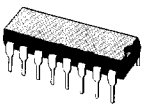
SGS-THOMSON MICROELECTRONICS

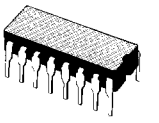
HCC4724B
HCF4724B

8 BIT ADDRESSABLE LATCH

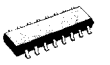
- SERIAL DATA INPUT - ACTIVE PARALLEL OUTPUT
- STORAGE REGISTER CAPABILITY - MASTER CLEAR
- CAN FUNCTION AS DEMULTIPLEXER
- STANDARDIZED, SYMMETRICAL OUTPUT CHARACTER
- 100% TESTED FOR QUIESCENT CURRENT AT 20V
- MAXIMUM INPUT CURRENT OF 1μA AT 18V (full package-temperature range), 100nA AT 18V AND 25°C
- NOISE MARGIN (full package-temperature range) = 1V AT V_{DD} = 5V, 2V AT V_{DD} = 10V, 2.5V AT V_{DD} = 15V
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N. 13A, " STANDARD SPECIFICATIONS FOR DESCRIPTION OF ' B ' SERIES CMOS DEVICES "



EY
(Plastic Package)



F
(Ceramic Package)



M1
(Micro Package)

C1
(Chip Carrier)

ORDER CODES :

HCC4724BF HCF4724BM1
HCF4724BEY HCF4724BC1

APPLICATION

- MULTI-LINE DECODERS
- A/D CONVERTERS

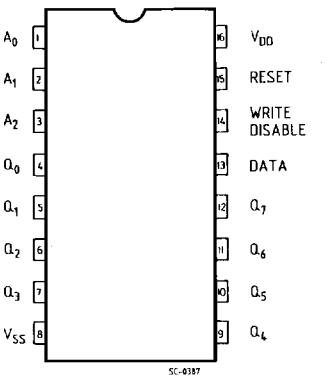
DESCRIPTION

The **HCC/HCF4724B** 8-bit addressable latch is a serial-input, parallel-output storage register that can perform a variety of functions.

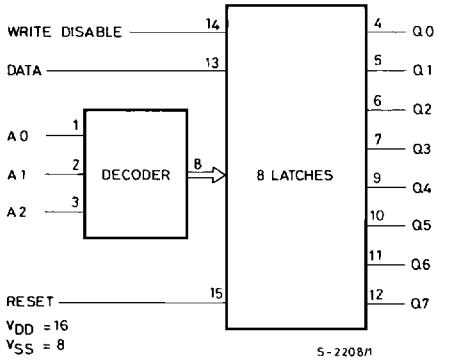
Data are inputted to a particular bit in the latch when that bit is addressed (by means of inputs A0, A1, A2) and when WRITE DISABLE is at low level. When WRITE DISABLE is high, data entry is inhibited however, all 8 outputs can be continuously read independent of WRITE DISABLE and address inputs.

A master RESET input is available, which resets all bits to a logic " 0 " level when RESET and WRITE DISABLE are at a high level. When RESET is at a high level, and WRITE DISABLE is at a low level, the latch acts as a 1-of-8 demultiplexer ; the bit that is addressed has an active output which follows the data input, while all unaddressed bits are held to a logic " 0 " level.

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{DD} *	Supply Voltage: **HCC** Types **HCF** Types	-0.5 to +20 -0.5 to +18	V V
V_i	Input Voltage	-0.5 to V_{DD} + 0.5	V
I_I	DC Input Current (any one input)	± 10	mA
P_{tot}	Total Power Dissipation (per package) Dissipation per Output Transistor for Top = Full Package Temperature Range	200 100	mW mW
T_{op}	Operating Temperature: **HCC** Types **HCF** Types	-55 to +125 -40 to +85	°C °C
T_{stg}	Storage Temperature	-65 to +150	°C

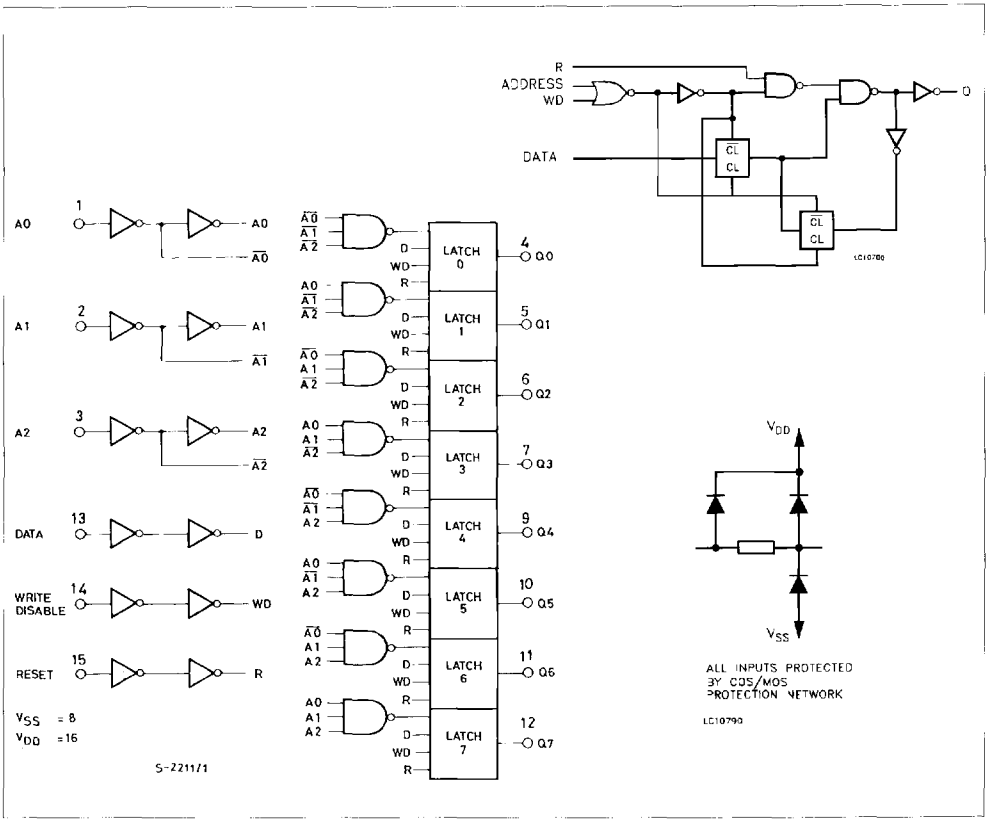
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

* All voltage values are referred to V_{SS} pin voltage.

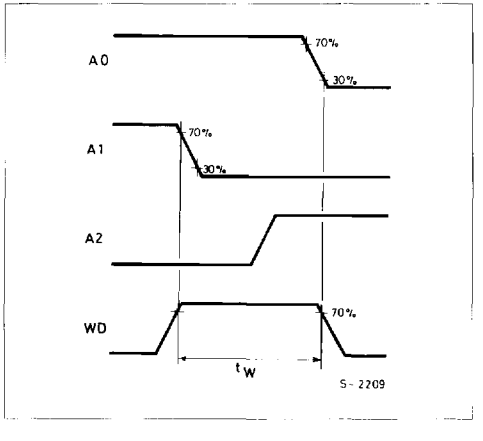
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage: **HCC** Types **HCF** Types	3 to 18 3 to 15	V V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature: **HCC** Types **HCF** Types	-55 to +125 -40 to +85	°C °C

LOGIC DIAGRAM



Definition of WRITE DISABLE ON Time



MODE SELECTION

TYPE	WD	R	Addressed Latch	Unaddressed Latch
A	0	0	Follows Data	Hold Previous State
B	0	1	Follows Data (Active High 8-Channel De-multiplexer)	Reset to "0"
C	1	0	Hold Previous State	
D	1	1	Reset to "0"	Reset to "0"

WD = WRITE DISABLE R= RESET

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Symbol	Parameter		Test Conditios V_I (V)	V_O (V)	$\|I_O\|$ (µA)	V_{DD} (V)	Value T_{LOW} * Min.	T_{LOW} * Max.	25 °C Min.	25 °C Typ.	25 °C Max.	T_{HIGH} * Min.	T_{HIGH} * Max.	Unit
I_L	Quiescent Current	HCC Types	0/5			5		5		0.04	5		150	µA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		HCF Types	0/5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output High Voltage		0/5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output Low Voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input High Voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input Low Voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output Drive Current	HCC Types	0/5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF Types	0/5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output Sink Current	HCC Types	0/5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF Types	0/5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH}, I_{IL}	Input Leakage Current		0/18	Any Input		18		±0.1		$±10^{-5}$	±0.1		±1	µA
C_I	Input Capacitance			Any Input						5	7.5			pF

* T_{LOW} = -55 °C for **HCC** device: -40 °C for **HCF** device.

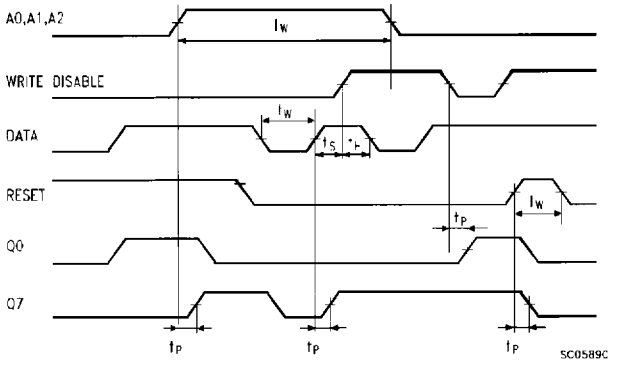
* T_{HIGH} = +125 °C for **HCC** device: +85 °C for **HCF** device.

The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5 V, 2 V min. with V_{DD} = 10 V, 2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C, C_L = 50 pF, R_L = 200 KΩ, typical temperature coefficent for all V_{DD} values is 03 %/°C, all input rise and fall times= 20 ns)

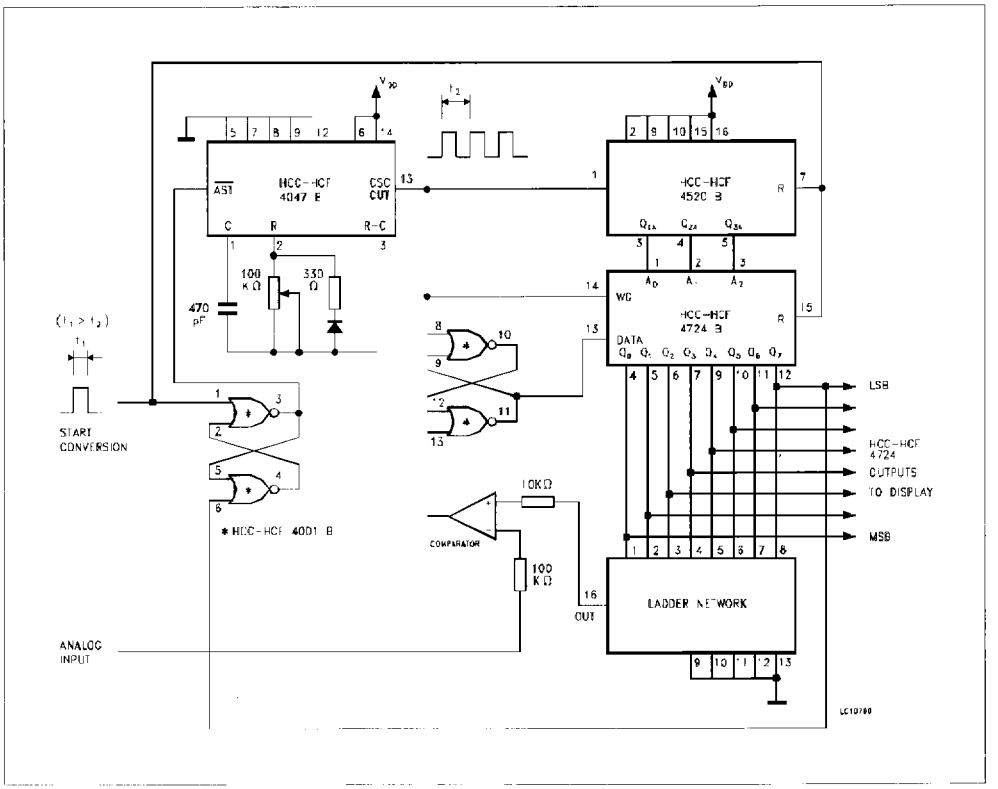
Symbol	Parameter	Test Conditions		Value			Unit
			V_{DD} (V)	Min.	Typ.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time Data to Output	(See Figure 1)	5		200	400	ns
			10		75	150	
			15		50	100	
t_{PLH} t_{PHL}	Propagation Delay Time Write Disable to Output	(See Figure 1)	5		200	400	ns
			10		80	160	
			15		60	120	
t_{PHL}	Propagation Delay Time Reset to Output	(See Figure 1)	5		175	350	ns
			10		80	160	
			15		65	130	
t_{PLH} t_{PHL}	Propagation Delay Time Address to Output	(See Figure 1)	5		225	450	ns
			10		100	200	
			15		75	150	
t_{TLH} t_{THL}	Transition Time Any Output		5		100	200	ns
			10		50	100	
			15		40	80	
t_W	Minimum Pulse Width Data	(See Figure 1)	5		100	200	ns
			10		50	100	
			15		40	80	
	Minimum Pulse Width Address	(See Figure 1)	5		200	400	ns
			10		100	200	
			15		65	125	
	Minimum Pulse Width Reset	(See Figure 1)	5		75	150	ns
			10		40	75	
			15		25	50	
t_S	Minimum Setup Time Data to Write Disable	(See Figure 1)	5		50	100	ns
			10		25	50	
			15		20	35	
t_H	Minimum Holf Time Data to Write Disable	(See Figure 1)	5		75	150	ns
			10		40	75	
			15		25	50	
C_{IN}	Input Capacitance		Any Input		5	7.5	pF

Figure 1: Master Timing Diagram

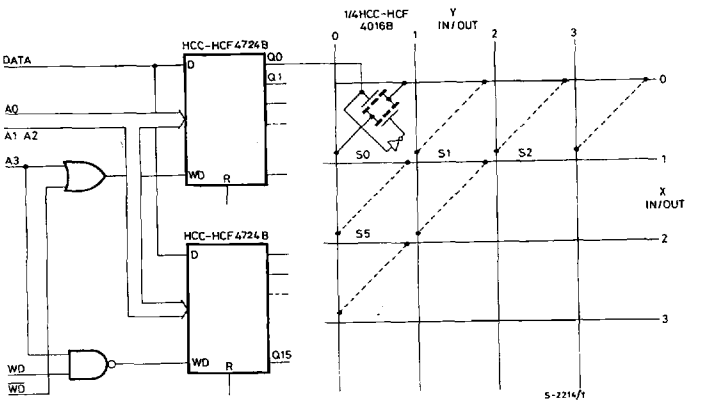


TYPICAL APPLICATIONS

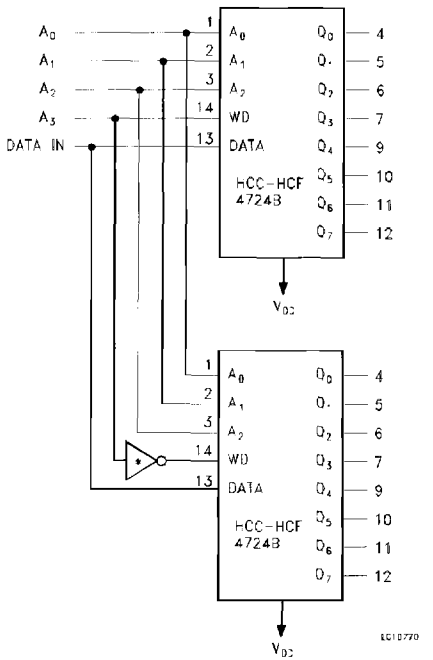
A/D Converter



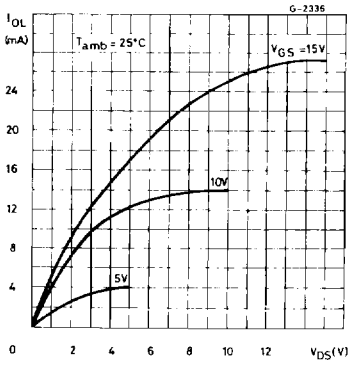
Multiple Selection Decoding - 4 x 4 Crosspoint Switch



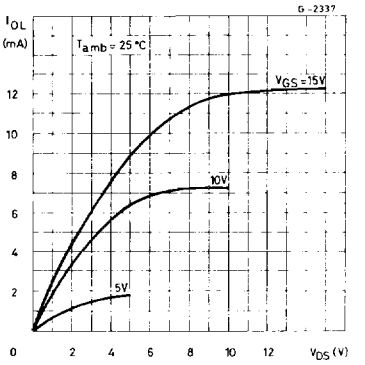
1 of 6 Decoder/Demultiplexer



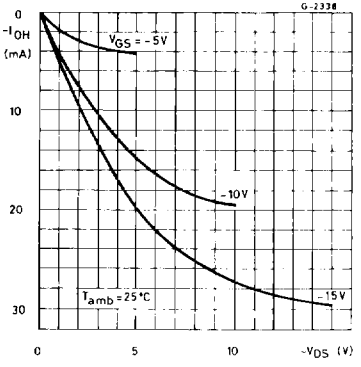
Typical Output Low (sink) Current Characteristics



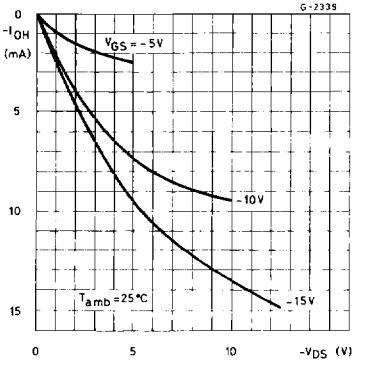
Minimum Output Low (sink) Current Characteristics



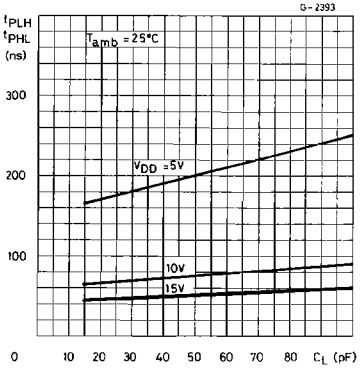
Typical Output High (source) Current Characteristics



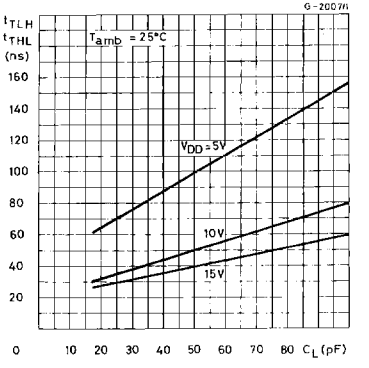
Minimum Output High (source) Current Characteristics



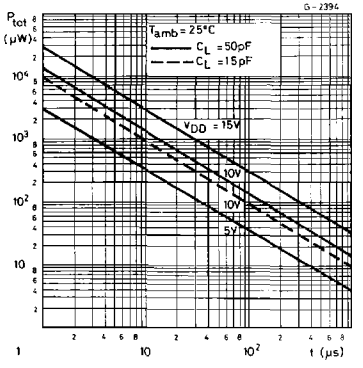
Typical Propagation Delay Time (data to Qn) vs Load Capacitance



Typical Transition Time vs Load Capacitance

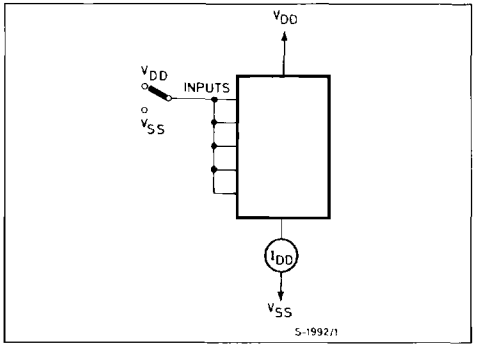


Typical Dynamic Power Dissipation vs Address Cycle Time

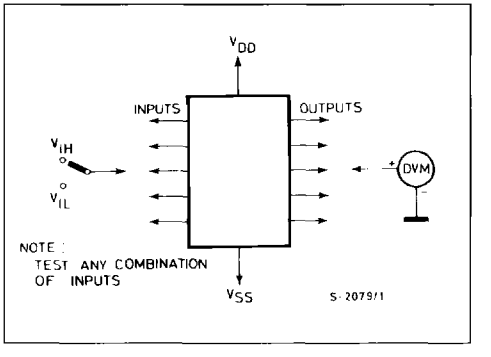


TEST CIRCUITS

Quiescent Device Current.



Noise Immunity.



Input Leakage Current.