

HYS72T64000HR-[3.7/5]-B
HYS72T1280x0HR-[3.7/5]-B
HYS72T256220HR-[3.7/5]-B

240-Pin Registered DDR2 SDRAM Modules

RDIMM SDRAM
DDR2 SDRAM
RoHS Compliant

Memory Products



Never stop thinking

Edition 2006-03

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Page	Subjects (major changes since last revision)
Previous Revision: 2005-07,1.00	
5	removed product types for DDR800,DDR667 these are to be found in a separate data sheet
8	removed DDR800, DDR667 raw card figures
23,25,35, 36	removed DDR800, DDR667 tables
45	removed DDR800, DDR667 package outlines

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240-Pin Registered DDR2 SDRAM Modules RDIMM SDRAM

HYS72T6400HR-[3.7/5]-B
HYS72T1280x0HR-[3.7/5]-B
HYS72T256220HR-[3.7/5]-B

1 Overview

This chapter gives an overview of the 1.8 V 240-Pin Registered DDR2 SDRAM Modules product family and describes its main characteristics.

1.1 Features

- 240-Pin PC2-6400, PC2-5300PC2-4200 and PC2-3200 DDR2 SDRAM memory modules for PC, Workstation and Server main memory applications.
- One rank 64M ×72, 128M ×72, and two ranks 128M ×72, 256M ×72 module organization, and 512M ×8, 512M ×4 chip organization
- Standard Double-Data-Rate-Two Synchronous DRAMs (DDR2 SDRAM) with a single + 1.8 V (± 0.1 V) power supply
- Built with 512 Mbit DDR2 SDRAMs in P-TFBGA-60 chipsize packages.
- Programmable CAS Latencies (3, 4, 5, 6), Burst Length (4 & 8) and Burst Type
- Auto Refresh (CBR) and Self Refresh
- Programmable self refresh rate via EMRS2 setting
- Programmable partial array refresh via EMRS2 settings
- DCC enabling via EMRS2 setting
- All inputs and outputs SSTL_18 compatible
- Off-Chip Driver Impedance Adjustment (OCD) and On-Die Termination (ODT)
- Serial Presence Detect with E²PROM
- RDIMM Dimensions (nominal):
30,00 mm high, 133.35 mm wide
- Based on standard reference card layouts Raw Card "A", "B", "C", "J"
- All speed grades faster than DDR400 comply with DDR400 timing specifications.
- RoHS compliant products¹⁾

Table 1 Performance for PC2-4200-444

Product Type Speed Code			-3.7	Unit
Speed Grade			PC2-4200 4-4-4	—
max. Clock Frequency	@CL5	f_{CK5}	266	MHz
	@CL4	f_{CK4}	266	MHz
	@CL3	f_{CK3}	200	MHz
min. RAS-CAS-Delay		t_{RCD}	15	ns
min. Row Precharge Time		t_{RP}	15	ns
min. Row Active Time		t_{RAS}	45	ns
min. Row Cycle Time		t_{RC}	60	ns

1) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.

Table 2 High Performance for PC2-3200

Product Type Speed Code			-5	Unit
Speed Grade			PC2-3200 3-3-3	—
max. Clock Frequency	@CL5	f_{CK5}	200	MHz
	@CL4	f_{CK4}	200	MHz
	@CL3	f_{CK3}	200	MHz
min. RAS-CAS-Delay		t_{RCD}	15	ns
min. Row Precharge Time		t_{RP}	15	ns
min. Row Active Time		t_{RAS}	40	ns
min. Row Cycle Time		t_{RC}	55	ns

1.2 Description

The INFINEON HYS72T[64/128/256]xxxHR-[3.7/5]-B module family are Registered DIMM modules with 30,0 mm height based on DDR2 technology. DIMMs are available as ECC modules in 64M x72 (512 MB), 128M x72 (1 GB), 256M x72 (2GB) organization and density, intended for mounting into 240-Pin connector sockets. The memory array is designed with 512-Mbit Double-Data-Rate-Two (DDR2) Synchronous DRAMs. All control and address signals are re-driven on the DIMM using register devices and a PLL for the clock distribution. This reduces capacitive loading to the system bus, but adds one cycle to the SDRAM timing. Decoupling capacitors are mounted on the PCB board. The DIMMs feature serial presence detect based on a serial E²PROM device using the 2-pin I²C protocol. The first 128 bytes are programmed with configuration data and the second 128 bytes are available to the customer.


Table 3 Ordering Information for RoHS Compliant Products

Product Type ¹⁾	Compliance Code ²⁾	Description	SDRAM Technology
PC2-4200			
HYS72T64000HR-3.7-B	512 MB 1Rx8 PC2-4200R-444-12-A0	1 Rank ECC	512 Mbit (x8)
HYS72T128000HR-3.7-B	1 GB 1Rx4 PC2-4200R-444-12-C0	1 Rank ECC	512 Mbit (x4)
HYS72T128020HR-3.7-B	1 GB 2Rx8 PC2-4200R-444-12-B0	2 Ranks, ECC	512 Mbit (x8)
HYS72T256220HR-3.7-B	2 GB 2Rx4 PC2-4200R-444-12-J1	2 Ranks, ECC	512 Mbit (x4)
PC2-3200			
HYS72T64000HR-5-B	512 MB 1Rx8 PC2-3200R-333-12-A0	1 Rank ECC	512 Mbit (x8)
HYS72T128000HR-5-B	1 GB 1Rx4 PC2-3200R-333-12-C0	1 Rank ECC	512 Mbit (x4)
HYS72T128020HR-5-B	1 GB 2Rx8 PC2-3200R-333-12-B0	2 Ranks, ECC	512 Mbit (x8)
HYS72T256220HR-5-B	2 GB 2Rx4 PC2-3200R-333-12-J1	2 Ranks, ECC	512 Mbit (x4)

1) All part numbers end with a place code, designating the silicon die revision. Example: HYS72T64000HR-3.7-B, indicating Rev. "B" dies are used for DDR2 SDRAM components. For all INFINEON DDR2 module and component nomenclature see [Chapter 6](#) of this data sheet.

2) The Compliance Code is printed on the module label and describes the speed grade, for example "PC2-4200R-444-12-A0", where 4200R means Registered DIMM modules with 4.26 GB/sec Module Bandwidth and "444-12" means Column Address Strobe (CAS) latency = 4, Row Column Delay (RCD) latency = 4 and Row Precharge (RP) latency = 4 using the latest JEDEC SPD Revision 1.2 and produced on the Raw Card "A"

Table 4 Address Format

DIMM Density	Module Organization	Memory Ranks	ECC/ Non-ECC	# of SDRAMs	# of row/bank/column bits	Raw Card
512 MB	64M ×72	1	ECC	9	14/2/10	F
1 GB	128M ×72	1	ECC	18	14/2/11	H
1 GB	128M ×72	2	ECC	18	14/2/10	G
2 GB	256M ×72	2	ECC	36	14/2/11	J

Table 5 Components on Modules ¹⁾

Product Type ²⁾	DRAM Components ²⁾	DRAM Density	DRAM Organisation
HYS72T64000HR	HYB18T512800BF	512 Mbit	512M ×8
HYS72T128000HR	HYB18T512400BF	512 Mbit	512M ×4
HYS72T128020HR	HYB18T512800BF	512 Mbit	512M ×8
HYS72T256220HR	HYB18T512400BF	512 Mbit	512M ×4

1) For a detailed description of all functionalities of the DRAM components on these modules see the component data sheet.

2) Green Product

2 Pin Configuration and Block Diagrams

2.1 Pin Configuration

The pin configuration of the Registered DDR2 SDRAM DIMM is listed by function in [Table 6](#) (240 pins). The abbreviations used in columns Pin and Buffer Type are

explained in [Table 7](#) and [Table 8](#) respectively. The pin numbering is depicted in [Figure 1](#).

Table 6 Pin Configuration of RDIMM

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
Clock Signals				
185	CK0	I	SSTL	Clock Signal CK0, Complementary Clock Signal CK0
186	$\overline{\text{CK0}}$	I	SSTL	The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and the falling edge of $\overline{\text{CK}}$. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.
52	CKE0	I	SSTL	Clock Enables 1:0
171	CKE1	I	SSTL	Activates the DDR2 SDRAM CK signal when HIGH and deactivates the CK signal when LOW. By deactivating the clocks, CKE0 initiates the Power Down Mode or the Self Refresh Mode. <i>Note: 2-Ranks module</i>
	NC	NC	—	Not Connected <i>Note: 1-Rank module</i>
Control Signals				
193	$\overline{\text{S0}}$	I	SSTL	Chip Select Rank 1:0
76	$\overline{\text{S1}}$	I	SSTL	Enables the associated DDR2 SDRAM command decoder when LOW and disables the command decoder when HIGH. When the command decoder is disabled, new commands are ignored but previous operations continue. Rank 0 is selected by $\overline{\text{S0}}$; Rank 1 is selected by $\overline{\text{S1}}$. The input signals also disable all outputs (except CKE and ODT) of the register(s) on the DIMM when both inputs are high. When $\overline{\text{S}}$ is HIGH, all register outputs (except CK, ODT and Chip select) remain in the previous state. <i>Note: 2-Ranks module</i>
	NC	NC	—	Not Connected <i>Note: 1-Rank module</i>
192	$\overline{\text{RAS}}$	I	SSTL	Row Address Strobe (RAS), Column Address Strobe (CAS), Write Enable (WE)
74	$\overline{\text{CAS}}$	I	SSTL	When sampled at the cross point of the rising edge of CK, and falling edge of $\overline{\text{CK}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ define the operation to be executed by the SDRAM.
73	$\overline{\text{WE}}$	I	SSTL	

Table 6 Pin Configuration of RDIMM (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
18	RESET	I	CMOS	Register Reset The RESET pin is connected to the RST pin on the register and to the OE pin on the PLL. When LOW, all register outputs will be driven LOW and the PLL clocks to the DRAMs and the register(s) will be set to low-level. The PLL will remain synchronized with the input clock.
Address Signals				
71	BA0	I	SSTL	Bank Address Bus 1:0 Selects internal SDRAM memory bank
190	BA1	I	SSTL	
54	BA2	I	SSTL	Bank Address Bus 2 Greater than 512Mb DDR2 SDRAMS
	NC	I	SSTL	Not Connected Less than 1Gb DDR2 SDRAMS
188	A0	I	SSTL	Address Bus 12:0, Address Signal 10/AutoPrecharge During a Bank Activate command cycle, defines the row address when sampled at the crosspoint of the rising edge of CK and falling edge of \overline{CK} . During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of \overline{CK} . In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is HIGH, autoprecharge is selected and BA[1:0] defines the bank to be precharged. If AP is LOW, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA[1:0] to control which bank(s) to precharge. If AP is HIGH, all banks will be precharged regardless of the state of BA[1:0] inputs. If AP is LOW, then BA[1:0] are used to define which bank to precharge.
183	A1	I	SSTL	
63	A2	I	SSTL	
182	A3	I	SSTL	
61	A4	I	SSTL	
60	A5	I	SSTL	
180	A6	I	SSTL	
58	A7	I	SSTL	
179	A8	I	SSTL	
177	A9	I	SSTL	
70	A10	I	SSTL	
	AP	I	SSTL	
57	A11	I	SSTL	
176	A12	I	SSTL	
196	A13	I	SSTL	Address Signal 13 <i>Note: modules based on $\times 4$, $\times 8$</i>
	NC	NC	—	Not Connected <i>Note: modules based on $\times 16$</i>
174	A14	I	SSTL	Address Signal 14 <i>Note: 2 Gbit based module</i>
	NC	NC	—	Not Connected <i>Note: 1 Gbit based module or smaller</i>

Table 6 Pin Configuration of RDIMM (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
Data Signals				
3	DQ0	I/O	SSTL	Data Bus 63:0 Data Input/Output pins
4	DQ1	I/O	SSTL	
9	DQ2	I/O	SSTL	
10	DQ3	I/O	SSTL	
122	DQ4	I/O	SSTL	
123	DQ5	I/O	SSTL	
128	DQ6	I/O	SSTL	
129	DQ7	I/O	SSTL	
12	DQ8	I/O	SSTL	
13	DQ9	I/O	SSTL	
21	DQ10	I/O	SSTL	
22	DQ11	I/O	SSTL	
131	DQ12	I/O	SSTL	
132	DQ13	I/O	SSTL	
140	DQ14	I/O	SSTL	
141	DQ15	I/O	SSTL	
24	DQ16	I/O	SSTL	
25	DQ17	I/O	SSTL	
30	DQ18	I/O	SSTL	
31	DQ19	I/O	SSTL	
143	DQ20	I/O	SSTL	
144	DQ21	I/O	SSTL	
149	DQ22	I/O	SSTL	
150	DQ23	I/O	SSTL	
33	DQ24	I/O	SSTL	
34	DQ25	I/O	SSTL	
39	DQ26	I/O	SSTL	
40	DQ27	I/O	SSTL	
152	DQ28	I/O	SSTL	
153	DQ29	I/O	SSTL	
158	DQ30	I/O	SSTL	
159	DQ31	I/O	SSTL	
80	DQ32	I/O	SSTL	
81	DQ33	I/O	SSTL	
86	DQ34	I/O	SSTL	
87	DQ35	I/O	SSTL	
199	DQ36	I/O	SSTL	
200	DQ37	I/O	SSTL	
205	DQ38	I/O	SSTL	

Table 6 Pin Configuration of RDIMM (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
206	DQ39	I/O	SSTL	Data Bus 63:0
89	DQ40	I/O	SSTL	
90	DQ41	I/O	SSTL	
95	DQ42	I/O	SSTL	
96	DQ43	I/O	SSTL	
208	DQ44	I/O	SSTL	
209	DQ45	I/O	SSTL	
214	DQ46	I/O	SSTL	
215	DQ47	I/O	SSTL	
98	DQ48	I/O	SSTL	
99	DQ49	I/O	SSTL	
107	DQ50	I/O	SSTL	
108	DQ51	I/O	SSTL	
217	DQ52	I/O	SSTL	
218	DQ53	I/O	SSTL	
226	DQ54	I/O	SSTL	
227	DQ55	I/O	SSTL	
110	DQ56	I/O	SSTL	
111	DQ57	I/O	SSTL	
116	DQ58	I/O	SSTL	
117	DQ59	I/O	SSTL	
229	DQ60	I/O	SSTL	
230	DQ61	I/O	SSTL	
235	DQ62	I/O	SSTL	
236	DQ63	I/O	SSTL	
Check Bits				
42	CB0	I/O	SSTL	Check Bits 7:0 Check Bit Input / Output pins <i>Note: NC on Non-ECC module</i>
43	CB1	I/O	SSTL	
48	CB2	I/O	SSTL	
49	CB3	I/O	SSTL	
161	CB4	I/O	SSTL	
162	CB5	I/O	SSTL	
167	CB6	I/O	SSTL	
168	CB7	I/O	SSTL	

Table 6 Pin Configuration of RDIMM (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
Data Strobe Bus				
7	DQS0	I/O	SSTL	Data Strobes 17:0 The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode the data strobe is sourced by the DDR2 SDRAM and is sent at the leading edge of the data window. DQS signals are complements, and timing is relative to the crosspoint of respective DQS and DQS. If the module is to be operated in single ended strobe mode, all DQS signals must be tied on the system board to V_{SS} through a 20 ohm to 10 Kohm resistor and DDR2 SDRAM mode registers programmed appropriately. <i>Note: See block diagram for corresponding DQ signals</i>
6	$\overline{\text{DQS0}}$	I/O	SSTL	
16	DQS1	I/O	SSTL	
15	$\overline{\text{DQS1}}$	I/O	SSTL	
28	DQS2	I/O	SSTL	
27	$\overline{\text{DQS2}}$	I/O	SSTL	
37	DQS3	I/O	SSTL	
36	$\overline{\text{DQS3}}$	I/O	SSTL	
84	DQS4	I/O	SSTL	
83	$\overline{\text{DQS4}}$	I/O	SSTL	
93	DQS5	I/O	SSTL	
92	$\overline{\text{DQS5}}$	I/O	SSTL	
105	DQS6	I/O	SSTL	
104	$\overline{\text{DQS6}}$	I/O	SSTL	
114	DQS7	I/O	SSTL	
113	$\overline{\text{DQS7}}$	I/O	SSTL	
46	DQS8	I/O	SSTL	
45	$\overline{\text{DQS8}}$	I/O	SSTL	
126	DQS9	I/O	SSTL	Not Connected <i>Note: x8 based DIMMs only</i>
	NC	NC	—	Not Connected <i>Note: x4 based DIMMs</i>
135	$\overline{\overline{\text{DQS10}}}$	I/O	SSTL	Not Connected <i>Note: x8 based DIMMs only</i>
	NC	NC	—	Not Connected <i>Note: x4 based DIMMs</i>
147	$\overline{\overline{\text{DQS11}}}$	I/O	SSTL	Not Connected <i>Note: x8 based DIMMs only</i>
	NC	NC	—	Not Connected <i>Note: x4 based DIMMs</i>
156	$\overline{\overline{\text{DQS12}}}$	I/O	SSTL	Not Connected <i>Note: x8 based DIMMs only</i>
	NC	NC	—	Not Connected <i>Note: x4 based DIMMs</i>
203	$\overline{\overline{\text{DQS13}}}$	I/O	SSTL	Not Connected <i>Note: x8 based DIMMs only</i>
	NC	NC	—	Not Connected <i>Note: x4 based DIMMs</i>

Table 6 Pin Configuration of RDIMM (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
212	DQS14	I/O	SSTL	Not Connected <i>Note: x8 based DIMMs only</i>
	NC	NC	—	Not Connected <i>Note: x4 based DIMMs</i>
224	DQS15	I/O	SSTL	Not Connected <i>Note: x8 based DIMMs only</i>
	NC	NC	—	Not Connected <i>Note: x4 based DIMMs</i>
233	DQS16	I/O	SSTL	Not Connected <i>Note: x8 based DIMMs only</i>
	NC	NC	—	Not Connected <i>Note: x4 based DIMMs</i>
165	DQS17	I/O	SSTL	Not Connected <i>Note: x8 based DIMMs only</i>
	NC	NC	—	Not Connected <i>Note: x4 based DIMMs</i>
125	DQS9	I/O	SSTL	Data Strobes 17:9 <i>Note: x4 based module</i>
134	DQS10	I/O	SSTL	
146	DQS11	I/O	SSTL	
155	DQS12	I/O	SSTL	
202	DQS13	I/O	SSTL	
211	DQS14	I/O	SSTL	
223	DQS15	I/O	SSTL	
232	DQS16	I/O	SSTL	
164	DQS17	I/O	SSTL	
125	DM0	I	SSTL	
134	DM1	I	SSTL	
146	DM2	I	SSTL	
155	DM3	I	SSTL	
202	DM4	I	SSTL	
211	DM5	I	SSTL	
223	DM6	I	SSTL	
232	DM7	I	SSTL	
164	DM8	I	SSTL	

Table 6 Pin Configuration of RDIMM (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
EEPROM				
120	SCL	I	CMOS	Serial Bus Clock This signal is used to clock data into and out of the SPD EEPROM.
119	SDA	I/O	OD	Serial Bus Data This is a bidirectional pin used to transfer data into or out of the SPD EEPROM. A resistor must be connected from SDA to V_{DDSPD} on the motherboard to act as a pull-up.
239	SA0	I	CMOS	Serial Address Select Bus 2:0 These signals are tied at the system planar to either V_{SS} or V_{DDSPD} to configure the serial SPD EEPROM address range
240	SA1	I	CMOS	
101	SA2	I	CMOS	
Power Supplies				
1	V_{REF}	AI	—	I/O Reference Voltage Reference voltage for the SSTL-18 inputs.
238	V_{DDSPD}	PWR	—	EEPROM Power Supply Serial EEPROM positive power supply, wired to a separated power pin at the connector which supports from 1.7 Volt to 3.6 Volt.
51, 56, 62, 72, 75, 78, 170, 175,, 181, 191, 194	V_{DDQ}	PWR	—	I/O Driver Power Supply Power and ground for the DDR SDRAM
53, 59, 64, 67, 69, 172, 178, 184,, 187, 189, 197	V_{DD}	PWR	—	Power Supply Power and ground for the DDR SDRAM
2, 5, 8, 11, 14, 17, 20, 23, 26, 29, 32, 35, 38, 41, 44, 47, 50, 65, 66, 79, 82, 85, 88, 91, 94, 97, 100, 103, 106, 109, 112, 115, 118, 121, 124, 127, 130, 133, 136, 139, 142, 145, 148, 151, 154, 157, 160, 163, 166, 169, 198, 201, 204, 207, 210, 213, 216, 219, 222, 225, 228, 231, 234, 237	V_{SS}	GND	—	Ground Plane Power and ground for the DDR SDRAM

Table 6 Pin Configuration of RDIMM (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
Other Pins				
19, 55, 68, 102, 137, 138, 173, 220, 221	NC	NC	—	Not connected Pins not connected on Infineon RDIMM's
195	ODT0	I	SSTL	On-Die Termination Control 1:0 Asserts on-die termination for DQ, DM, DQS, and $\overline{\text{DQS}}$ signals if enabled via the DDR2 SDRAM mode register. <i>Note: 2-Ranks module</i>
77	ODT1	I	SSTL	
	NC	NC	—	<i>Note: 1-Rank modules</i>

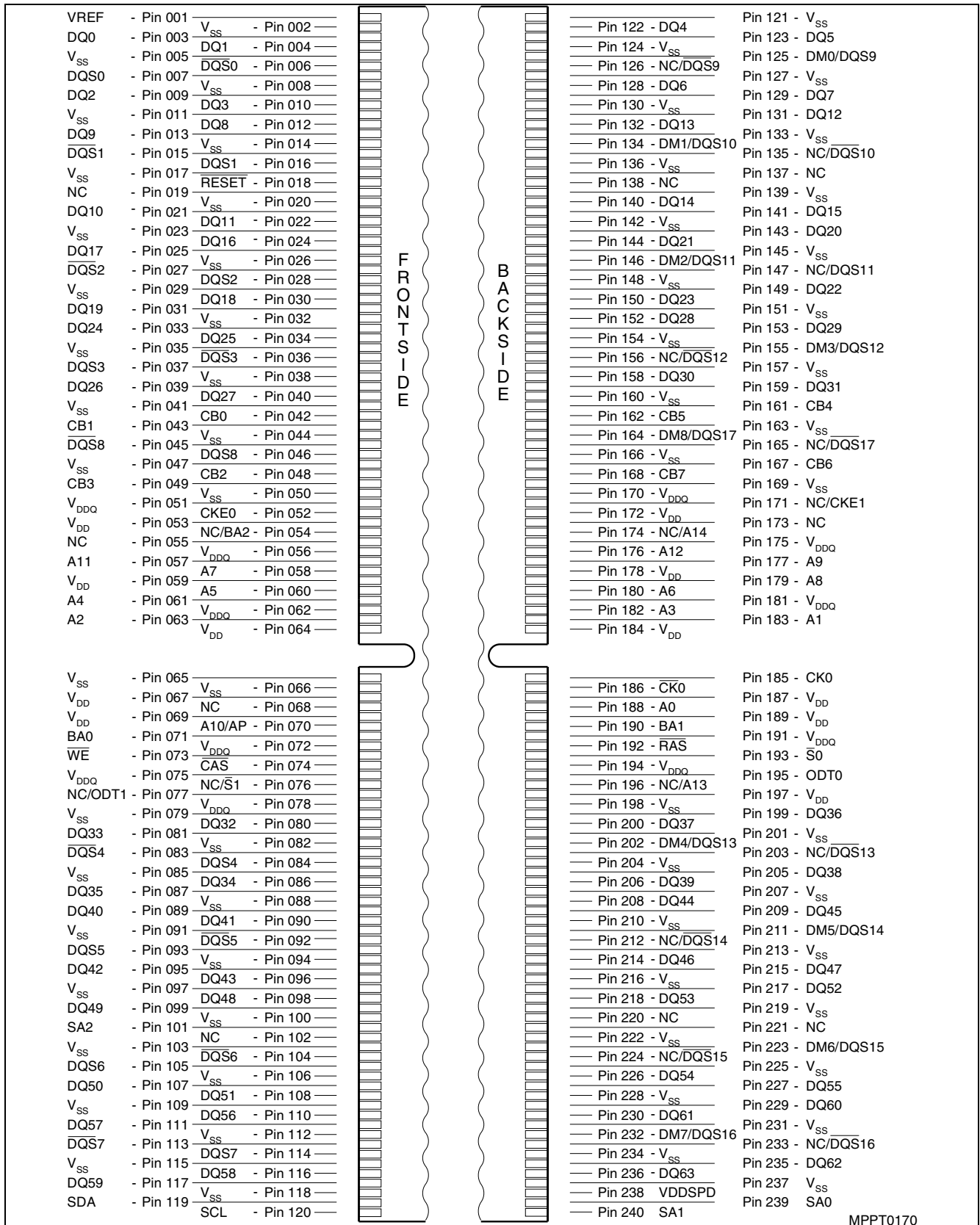
Table 7 Abbreviations for Buffer Type

Abbreviation	Description
SSTL	Serial Stub Terminated Logic (SSTL_18)
CMOS	CMOS Levels
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR.

Table 8 Abbreviations for Pin Type

Abbreviation	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
PWR	Power
GND	Ground
NU	Not Usable
NC	Not Connected

Pin Configuration and Block Diagrams



MPPT0170

Figure 1 Pin Configuration for RDIMM (240 pins)

2.2 Block Diagrams

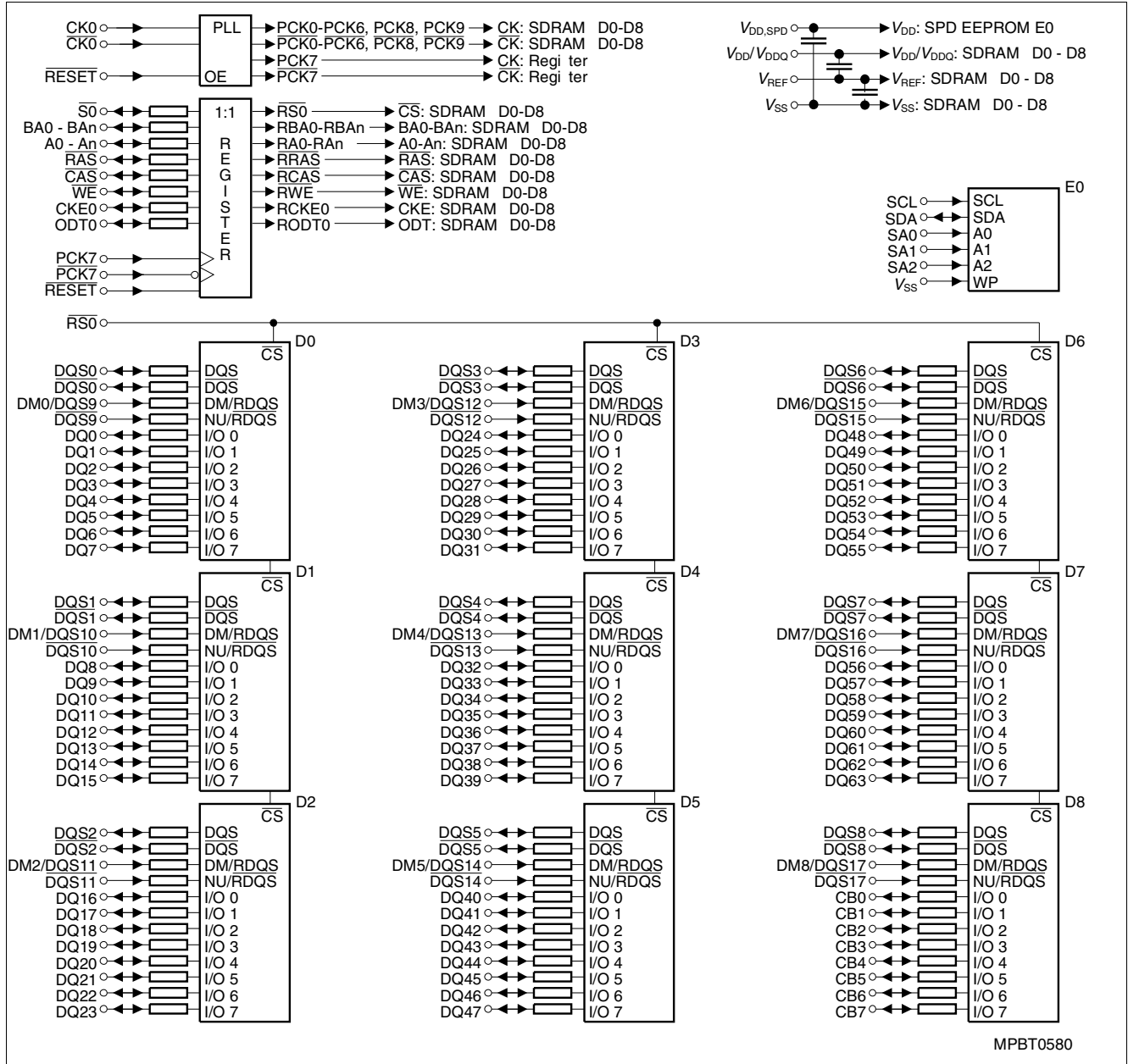


Figure 2 Block Diagram Raw Card A RDIMM (x72, 1 Rank, x8)

Notes

1. Unless otherwise noted, resistors are $22 \Omega \pm 5 \%$
2. $\overline{S0}$ connects to \overline{DCS} and V_{DD} connects to \overline{CSR} on the register.

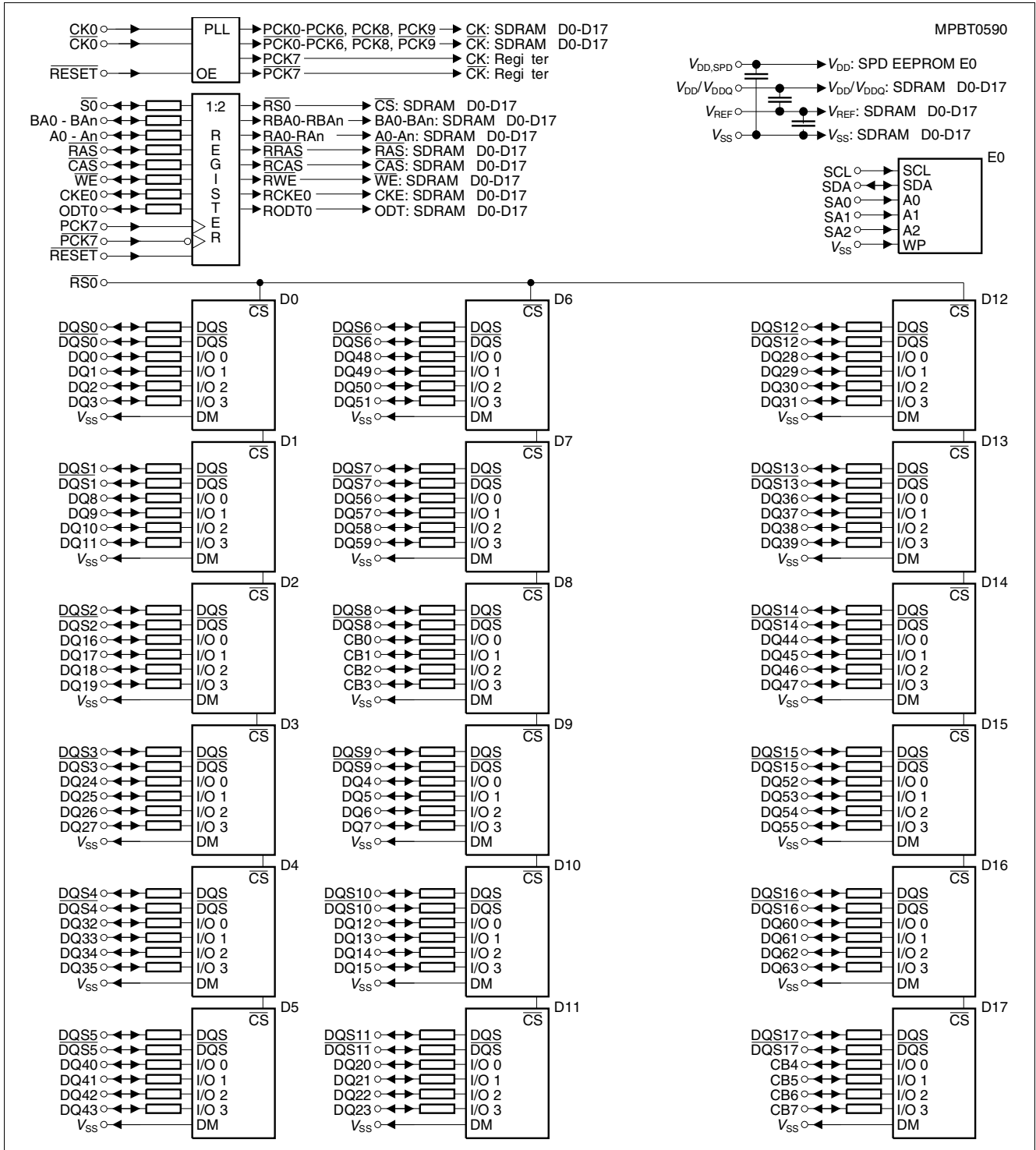


Figure 3 Block Diagram Raw Card C RDIMM (x72, 1 Rank, x4)

Notes

1. Unless otherwise noted, resistors are $22 \Omega \pm 5 \%$
2. $\overline{S0}$ connects to \overline{DCS} of register1 and \overline{CSR} of register2.
3. \overline{CSR} of register1 and \overline{DCS} of register2 connects to $\overline{V_{DD}}$.
4. \overline{RESET} , $\overline{PCK7}$ and $\overline{PCK7}$ connect to both registers.

Pin Configuration and Block Diagrams

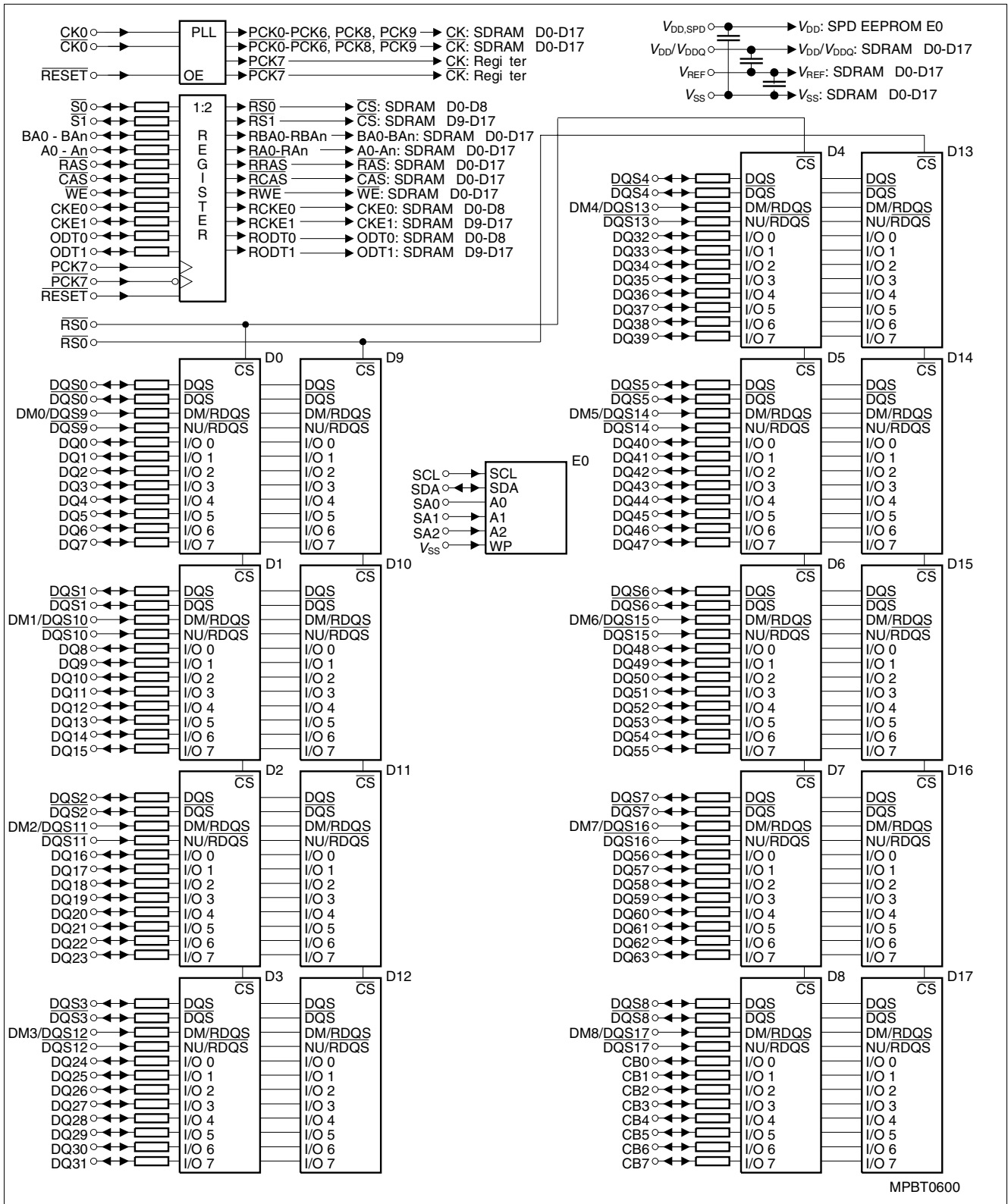


Figure 4 Block Diagram Raw Card B RDIMM (x72, 2 Ranks, x8)

Notes

1. Unless otherwise noted, resistors are $22 \Omega \pm 5 \%$

2. $\overline{RS0}$ and $\overline{RS1}$ alternate between the back and front sides of the DIMM.

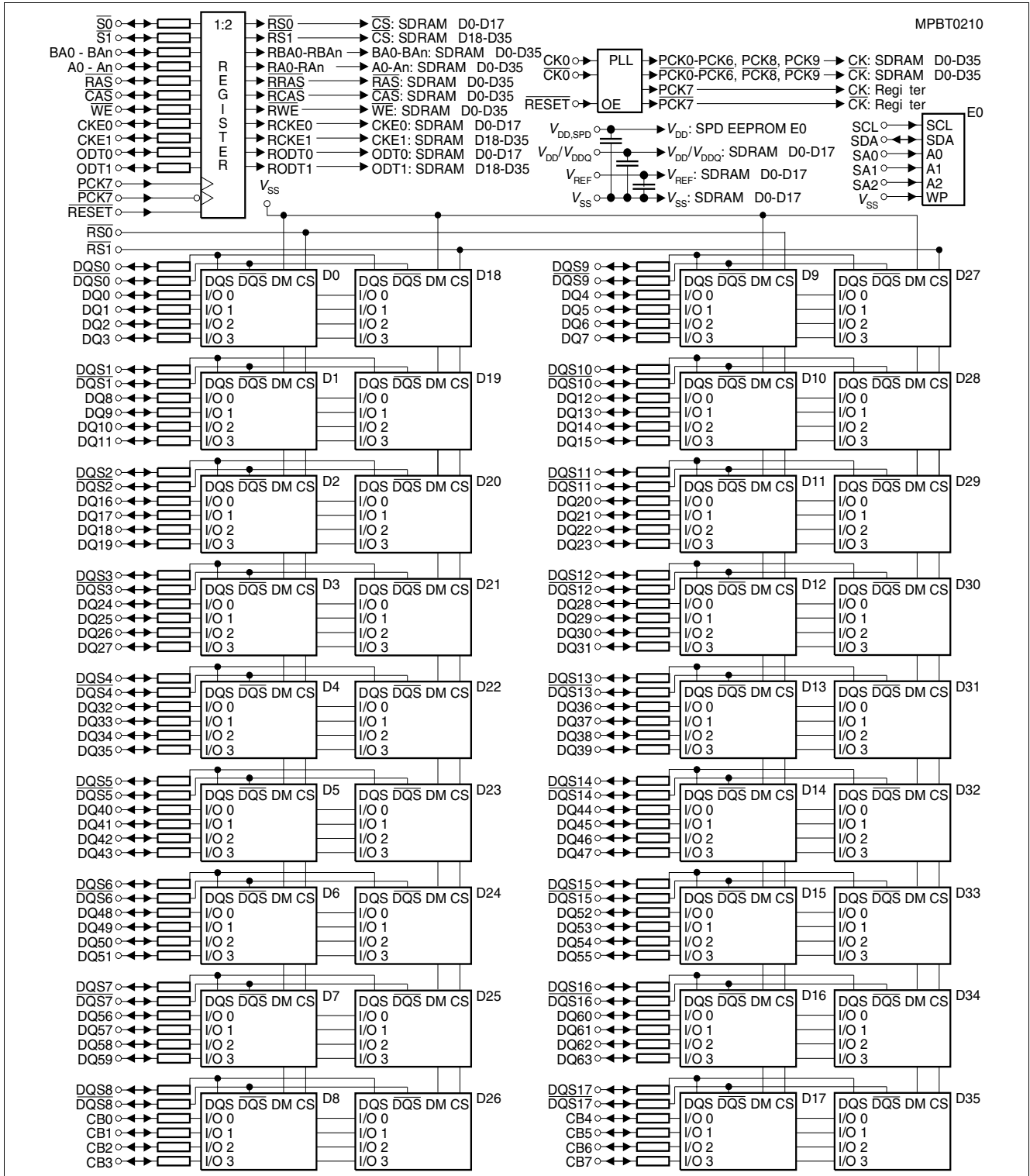


Figure 5 Block Diagram Raw Card J RDIMM (x72, 2Ranks, x4)

Notes

1. Unless otherwise noted, resistors are $22 \Omega \pm 5 \%$
2. $\overline{RS0}$ and $\overline{RS1}$ alternate between the bottom and surface sides of the DIMM.
3. $\overline{S0}$ connects to \overline{DCS} and $\overline{S1}$ connects to \overline{CSR} on a pair of registers. $\overline{S1}$ connects to \overline{DCS} and $\overline{S0}$ connects to \overline{CSR} on another pair of registers.
4. \overline{RESET} , $\overline{PCK7}$ and $\overline{PCK7}$ connect to all registers.

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Caution is needed not to exceed absolute maximum ratings of the DRAM device listed in [Table 9](#) at any time.

Table 9 Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit	Notes
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	-1.0 to +2.3	V	1)2)
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	-0.5 to +2.3	V	2)3)
V_{DDL}	Voltage on V_{DDL} pin relative to V_{SS}	-0.5 to +2.3	V	2)3)
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	-0.5 to +2.3	V	2)
T_{STG}	Storage Temperature	-55 to +100	°C	2)3)

- 1) Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- 2) When V_{DD} and V_{DDQ} and V_{DDL} are less than 500 mV; V_{REF} may be equal to or less than 300 mV.
- 3) Storage Temperature is the case surface temperature on the center/top side of the DRAM.

Table 10 DRAM Component Operating Temperature Range

Symbol	Parameter	Rating	Unit	Notes
T_{OPER}	Operating Temperature	0 to 95	°C	1)2)3)

- 1) Operating Temperature is the case surface temperature on the center / top side of the DRAM.
- 2) The operating temperature range are the temperatures where all DRAM specification will be supported. During operation, the DRAM case temperature must be maintained between 0 - 95 °C under all other specification parameters.
- 3) Self-Refresh period is hard-coded in the chip and therefore it is imperative that the system ensures the DRAM is below 85 °C case temperature before initiating self-refresh operation.

3.2 DC Characteristics

Table 11 Recommended DC Operating Conditions (SSTL_18)

Symbol	Parameter	Rating			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	Supply Voltage	1.7	1.8	1.9	V	1)
V_{DDDL}	Supply Voltage for DLL	1.7	1.8	1.9	V	1)
V_{DDQ}	Supply Voltage for Output	1.7	1.8	1.9	V	1)
V_{REF}	Input Reference Voltage	$0.49 \times V_{DDQ}$	$0.5 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V	2)3)
V_{TT}	Termination Voltage	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$	V	4)

- 1) V_{DDQ} tracks with V_{DD} , V_{DDDL} tracks with V_{DD} . AC parameters are measured with V_{DD} , V_{DDQ} and V_{DDDL} tied together.
- 2) The value of V_{REF} may be selected by the user to provide optimum noise margin in the system. Typically the value of V_{REF} is expected to be about $0.5 \times V_{DDQ}$ of the transmitting device and V_{REF} is expected to track variations in V_{DDQ} .
- 3) Peak to peak ac noise on V_{REF} may not exceed $\pm 2\% V_{REF}$ (dc)
- 4) V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} , and must track variations in die dc level of V_{REF} .

Table 12 ODT DC Electrical Characteristics

Parameter / Condition	Symbol	Min.	Nom.	Max.	Unit	Notes
Termination resistor impedance value for EMRS(1)[A6,A2] = [0,1]; 75 Ohm	Rtt1(eff)	60	75	90	Ω	1)
Termination resistor impedance value for EMRS(1)[A6,A2] = [1,0]; 150 Ohm	Rtt2(eff)	120	150	180	Ω	1)
Termination resistor impedance value for EMRS(1)(A6,A2)=[1,1]; 50 Ohm	Rtt3(eff)	40	50	60	Ω	1)
Deviation of V_M with respect to $V_{DDQ} / 2$	delta V_M	-6.00	—	+ 6.00	%	2)

- 1) Measurement Definition for Rtt(eff): Apply $V_{IH(ac)}$ and $V_{IL(ac)}$ to test pin separately, then measure current $I(V_{IHac})$ and $I(V_{ILac})$ respectively. $Rtt(eff) = (V_{IH(ac)} - V_{IL(ac)}) / (I(V_{IHac}) - I(V_{ILac}))$.
- 2) Measurement Definition for V_M : Turn ODT on and measure voltage (V_M) at test pin (midpoint) with no load:
delta $V_M = ((2 \times V_M / V_{DDQ}) - 1) \times 100\%$

Table 13 Input and Output Leakage Currents

Symbol	Parameter / Condition	Min.	Max.	Unit	Notes
IIL	Input Leakage Current; any input $0\text{ V} < V_{IN} < V_{DD}$	-2	+2	μA	1)
IOL	Output Leakage Current; $0\text{ V} < V_{OUT} < V_{DDQ}$	-5	+5	μA	2)

- 1) All other pins not under test = 0 V
- 2) DQ's, LDQS, LDQS, UDQS, UDQS, DQS, DQS, RDQS, RDQS are disabled and ODT is turned off

Table 14 Input / Output Capacitance

Symbol	Parameter	Min.	Max.	Unit
CCK	Input capacitance, CK and \overline{CK}			pF
CDCK	Input capacitance delta, CK and \overline{CK}	—		pF
CI	Input capacitance, all other input-only pins			pF
CDI	Input capacitance delta, all other input-only pins	—		pF
CIO	Input/output capacitance, DQ, DM, \overline{DQS} , \overline{DQS} , RDQS, RDQS			pF
CDIO	Input/output capacitance delta, DQ, DM, DQS, \overline{DQS} , RDQS, RDQS	—		pF

3.3 AC Characteristics

3.3.1 Speed Grade Definitions

All Speed grades faster than DDR2-DDR400B comply with DDR2-DDR400B timing specifications ($t_{CK} = 5\text{ns}$ with $t_{RAS} = 40\text{ns}$).

List of Speed Grade Definition tables:

- [Table 15 “Speed Grade Definition Speed Bins for DDR2–533C” on Page 23](#)
- [Table 16 “Speed Grade Definition Speed Bins for DDR2–400B” on Page 24](#)

Table 15 Speed Grade Definition Speed Bins for DDR2–533C

Speed Grade		DDR2–533C		Unit	Note	
IFX Sort Name		–3.7				
CAS-RCD-RP latencies		4–4–4		t_{CK}		
Parameter	Symbol	Min.	Max.	—		
Clock Frequency	@ CL = 3	t_{CK}	5	8	ns	1)2)3)4)
	@ CL = 4	t_{CK}	3.75	8	ns	1)1)1)1)
	@ CL = 5	t_{CK}	3.75	8	ns	1)1)1)1)
Row Active Time	t_{RAS}	45	70000	ns	1)1)1)1)5)	
Row Cycle Time	t_{RC}	60	—	ns	1)1)1)1)	
RAS-CAS-Delay	t_{RCD}	15	—	ns	1)1)1)1)	
Row Precharge Time	t_{RP}	15	—	ns	1)1)1)1)	

- 1) Timings are guaranteed with $\overline{CK}/\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0) only.
- 2) The $\overline{CK}/\overline{CK}$ input reference level (for timing reference to $\overline{CK}/\overline{CK}$) is the point at which CK and \overline{CK} cross. The $\overline{DQS} / \overline{DQS}$, $\overline{RDQS} / \overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode
- 3) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, $CKE = 0.2 \times V_{DDQ}$ is recognized as low.
- 4) The output timing reference voltage level is V_{TT} .
- 5) $t_{RAS,MAX}$ is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to $9 \times t_{REFI}$.

Table 16 Speed Grade Definition Speed Bins for DDR2-400B

Speed Grade		DDR2-400B		Unit	Note	
IFX Sort Name		-5				
CAS-RCD-RP latencies		3-3-3		t_{CK}		
Parameter		Symbol	Min.	Max.	—	
Clock Frequency	@ CL = 3	t_{CK}	5	8	ns	1)2)3)4)
	@ CL = 4	t_{CK}	5	8	ns	1)2)3)4)
	@ CL = 5	t_{CK}	5	8	ns	1)2)3)4)
Row Active Time		t_{RAS}	40	70000	ns	1)2)3)4)5)
Row Cycle Time		t_{RC}	55	—	ns	1)2)3)4)
RAS-CAS-Delay		t_{RCD}	15	—	ns	1)2)3)4)
Row Precharge Time		t_{RP}	15	—	ns	1)2)3)4)

- 1) Timings are guaranteed with CK/ \overline{CK} differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0) only.
- 2) The CK/ \overline{CK} input reference level (for timing reference to CK/ \overline{CK}) is the point at which CK and \overline{CK} cross. The DQS / \overline{DQS} , RDQS / \overline{RDQS} , input reference level is the crosspoint when in differential strobe mode
- 3) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, $CKE = 0.2 \times V_{DDQ}$ is recognized as low.
- 4) The output timing reference voltage level is V_{TT} .
- 5) $t_{RAS,MAX}$ is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to $9 \times t_{REFI}$.

3.3.2 AC Timing Parameters

List of AC timing parameter tables.

- [Table 17 “Timing Parameter by Speed Grade - DDR2-533” on Page 25](#)
- [Table 18 “Timing Parameter by Speed Grade - DDR2-400” on Page 27](#)

Table 17 Timing Parameter by Speed Grade - DDR2-533

Parameter	Symbol	DDR2-533		Unit	Notes ¹⁾²⁾³⁾⁴⁾⁵⁾⁶⁾⁷⁾
		Min.	Max.		
DQ output access time from CK / $\overline{\text{CK}}$	t_{AC}			ps	
CAS A to CAS B command period	t_{CCD}	2	—	t_{CK}	
CK, $\overline{\text{CK}}$ high-level width	t_{CH}	0.45	0.55	t_{CK}	
CKE minimum high and low pulse width	t_{CKE}	3	—	t_{CK}	
CK, $\overline{\text{CK}}$ low-level width	t_{CL}	0.45	0.55	t_{CK}	
Auto-Precharge write recovery + precharge time	t_{DAL}	$WR + t_{RP}$	—	t_{CK}	
Minimum time clocks remain ON after CKE asynchronously drops LOW	t_{DELAY}	$t_{IS} + t_{CK} + t_{IH}$	—	ns	
DQ and DM input hold time (differential data strobe)	$t_{DH}(\text{base})$	225	—	ps	
DQ and DM input hold time (single ended data strobe)	$t_{DH1}(\text{base})$	-25	—	ps	
DQ and DM input pulse width (each input)	t_{DIPW}	0.35	—	t_{CK}	
DQS output access time from CK / $\overline{\text{CK}}$	t_{DQSK}			ps	
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	t_{CK}	
DQS-DQ skew (for DQS & associated DQ signals)	t_{DQSQ}	—	300	ps	
Write command to 1st DQS latching transition	t_{DQSS}	- 0.25	+ 0.25	t_{CK}	
DQ and DM input setup time (differential data strobe)	$t_{DS}(\text{base})$	100	—	ps	
DQ and DM input setup time (single ended data strobe)	$t_{DS1}(\text{base})$	-25	—	ps	
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	t_{CK}	
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	t_{CK}	
Clock half period	t_{HP}	MIN. (t_{CL}, t_{CH})			
Data-out high-impedance time from CK / $\overline{\text{CK}}$	t_{HZ}	—	$t_{AC,MAX}$	ps	
Address and control input hold time	$t_{IH}(\text{base})$	375	—	ps	
Address and control input pulse width (each input)	t_{IPW}	0.6	—	t_{CK}	
Address and control input setup time	$t_{IS}(\text{base})$	250	—	ps	

Table 17 Timing Parameter by Speed Grade - DDR2-533 (cont'd)

Parameter	Symbol	DDR2-533		Unit	Notes ¹⁾²⁾³⁾⁴⁾⁵⁾⁶⁾⁷⁾
		Min.	Max.		
DQ low-impedance time from CK / $\overline{\text{CK}}$	$t_{\text{LZ(DQ)}}$	$2 \times t_{\text{AC.MIN}}$	$t_{\text{AC.MAX}}$	ps	
DQS low-impedance from CK / $\overline{\text{CK}}$	$t_{\text{LZ(DQS)}}$	$t_{\text{AC.MIN}}$	$t_{\text{AC.MAX}}$	ps	
Mode register set command cycle time	t_{MRD}	2	—	t_{CK}	
OCD drive mode output delay	t_{OIT}	0	12	ns	
Data output hold time from DQS	t_{QH}	$t_{\text{HP}} - t_{\text{QHS}}$	—		
Data hold skew factor	t_{QHS}	—	400	ps	
Average periodic refresh Interval	t_{REFI}	—	7.8	μs	8)
		—	3.9	μs	9)
Precharge-All (4 banks) command period	t_{RP}	t_{RP}	—	ns	
Read preamble	t_{RPRE}	0.9	1.1	t_{CK}	
Read postamble	t_{RPST}	0.40	0.60	t_{CK}	
Active bank A to Active bank B command period	t_{RRD}	7.5	—	ns	
		10	—	ns	
Internal Read to Precharge command delay	t_{RTP}	7.5	—	ns	
Write preamble	t_{WPRE}	$0.25 \times t_{\text{CK}}$	—	t_{CK}	
Write postamble	t_{WPST}	0.40	0.60	t_{CK}	
Write recovery time for write without Auto-Precharge	t_{WR}	15	—	ns	
Write recovery time for write with Auto-Precharge	WR	$t_{\text{WR}}/t_{\text{CK}}$	—	t_{CK}	
Internal Write to Read command delay	t_{WTR}	7.5	—	ns	
Exit power down to any valid command (other than NOP or Deselect)	t_{XARD}	2	—	t_{CK}	
Exit active power-down mode to Read command (slow exit, lower power)	t_{XARDS}	6 – AL	—	t_{CK}	
Exit precharge power-down to any valid command (other than NOP or Deselect)	t_{XP}	2	—	t_{CK}	
Exit Self-Refresh to non-Read command	t_{XSNR}	$t_{\text{RFC}} + 10$	—	ns	
Exit Self-Refresh to Read command	t_{XSRD}	200	—	t_{CK}	

- 1) For details and notes see the relevant INFINEON component data sheet
- 2) $V_{\text{DDQ}} = 1.8 \text{ V} \pm 0.1 \text{ V}$; $V_{\text{DD}} = 1.8 \text{ V} \pm 0.1 \text{ V}$. See notes 4)5)6)7)
- 3) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
- 4) Timings are guaranteed with CK/ $\overline{\text{CK}}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.
- 5) The CK/ $\overline{\text{CK}}$ input reference level (for timing reference to CK/ $\overline{\text{CK}}$) is the point at which CK and $\overline{\text{CK}}$ cross. The DQS/ $\overline{\text{DQS}}$, RDQS/ $\overline{\text{RDQS}}$, input reference level is the crosspoint when in differential strobe mode.
- 6) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, $\text{CKE} = 0.2 \times V_{\text{DDQ}}$ is recognized as low.
- 7) The output timing reference voltage level is V_{TT} .
- 8) $0 \text{ }^\circ\text{C} \leq T_{\text{CASE}} \leq 85 \text{ }^\circ\text{C}$

9) $85\text{ }^{\circ}\text{C} < T_{\text{CASE}} \leq 95\text{ }^{\circ}\text{C}$
Table 18 Timing Parameter by Speed Grade - DDR2-400

Parameter	Symbol	DDR2-400		Unit	Notes ¹⁾²⁾³⁾⁴⁾⁵⁾⁶⁾⁷⁾
		Min.	Max.		
DQ output access time from CK / $\overline{\text{CK}}$	t_{AC}			ps	
CAS A to CAS B command period	t_{CCD}	2	—	t_{CK}	
CK, $\overline{\text{CK}}$ high-level width	t_{CH}	0.45	0.55	t_{CK}	
CKE minimum high and low pulse width	t_{CKE}	3	—	t_{CK}	
CK, $\overline{\text{CK}}$ low-level width	t_{CL}	0.45	0.55	t_{CK}	
Auto-Precharge write recovery + precharge time	t_{DAL}	WR + t_{RP}	—	t_{CK}	
Minimum time clocks remain ON after CKE asynchronously drops LOW	t_{DELAY}	$t_{\text{IS}} + t_{\text{CK}} + t_{\text{IH}}$	—	ns	
DQ and DM input hold time (differential data strobe)	$t_{\text{DH}}(\text{base})$	275	—	ps	
DQ and DM input hold time (single ended data strobe)	$t_{\text{DH1}}(\text{base})$	-25	—	ps	
DQ and DM input pulse width (each input)	t_{DIPW}	0.35	—	t_{CK}	
DQS output access time from CK / $\overline{\text{CK}}$	t_{DQSCK}			ps	
DQS input low (high) pulse width (write cycle)	$t_{\text{DQSL,H}}$	0.35	—	t_{CK}	
DQS-DQ skew (for DQS & associated DQ signals)	t_{DQSQ}	—	350	ps	
Write command to 1st DQS latching transition	t_{DQSS}	- 0.25	+ 0.25	t_{CK}	
DQ and DM input setup time (differential data strobe)	$t_{\text{DS}}(\text{base})$	150	—	ps	
DQ and DM input setup time (single ended data strobe)	$t_{\text{DS1}}(\text{base})$	-25	—	ps	
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	t_{CK}	
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	t_{CK}	
Clock half period	t_{HP}	MIN. ($t_{\text{CL}}, t_{\text{CH}}$)			
Data-out high-impedance time from CK / $\overline{\text{CK}}$	t_{HZ}	—	$t_{\text{AC,MAX}}$	ps	
Address and control input hold time	$t_{\text{IH}}(\text{base})$	475	—	ps	
Address and control input pulse width (each input)	t_{IPW}	0.6	—	t_{CK}	
Address and control input setup time	$t_{\text{IS}}(\text{base})$	350	—	ps	
DQ low-impedance time from CK / $\overline{\text{CK}}$	$t_{\text{LZ}}(\text{DQ})$	$2 \times t_{\text{AC,MIN}}$	$t_{\text{AC,MAX}}$	ps	
DQS low-impedance from CK / $\overline{\text{CK}}$	$t_{\text{LZ}}(\text{DQS})$	$t_{\text{AC,MIN}}$	$t_{\text{AC,MAX}}$	ps	
Mode register set command cycle time	t_{MRD}	2	—	t_{CK}	

Table 18 Timing Parameter by Speed Grade - DDR2-400

Parameter	Symbol	DDR2-400		Unit	Notes ¹⁾²⁾³⁾⁴⁾⁵⁾⁶⁾⁷⁾
		Min.	Max.		
OCD drive mode output delay	t_{OIT}	0	12	ns	
Data output hold time from DQS	t_{QH}	$t_{HP} - t_{QHS}$	—		
Data hold skew factor	t_{QHS}	—	450	ps	
Average periodic refresh Interval	t_{REFI}	—	7.8	μ s	8)
		—	3.9	μ s	9)
Precharge-All (4 banks) command period	t_{RP}	t_{RP}	—	ns	
Read preamble	t_{RPRE}	0.9	1.1	t_{CK}	
Read postamble	t_{RPST}	0.40	0.60	t_{CK}	
Active bank A to Active bank B command period	t_{RRD}	7.5	—	ns	
		10	—	ns	
Internal Read to Precharge command delay	t_{RTP}	7.5	—	ns	
Write preamble	t_{WPRE}	$0.25 \times t_{CK}$	—	t_{CK}	
Write postamble	t_{WPST}	0.40	0.60	t_{CK}	
Write recovery time for write without Auto-Precharge	t_{WR}	15	—	ns	
Write recovery time for write with Auto-Precharge	WR	t_{WR}/t_{CK}	—	t_{CK}	
Internal Write to Read command delay	t_{WTR}	10	—	ns	
Exit power down to any valid command (other than NOP or Deselect)	t_{XARD}	2	—	t_{CK}	
Exit active power-down mode to Read command (slow exit, lower power)	t_{XARDS}	6 – AL	—	t_{CK}	
Exit precharge power-down to any valid command (other than NOP or Deselect)	t_{XP}	2	—	t_{CK}	
Exit Self-Refresh to non-Read command	t_{XSNR}	$t_{RFC} + 10$	—	ns	
Exit Self-Refresh to Read command	t_{XSRD}	200	—	t_{CK}	

- 1) For details and notes see the relevant INFINEON component data sheet
- 2) $V_{DDQ} = 1.8 \text{ V} \pm 0.1 \text{ V}$; $V_{DD} = 1.8 \text{ V} \pm 0.1 \text{ V}$. See notes ⁴⁾⁵⁾⁶⁾⁷⁾
- 3) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
- 4) Timings are guaranteed with CK/ $\overline{\text{CK}}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.
- 5) The CK/ $\overline{\text{CK}}$ input reference level (for timing reference to CK/ $\overline{\text{CK}}$) is the point at which CK and $\overline{\text{CK}}$ cross. The DQS/ $\overline{\text{DQS}}$, RDQS/ $\overline{\text{RDQS}}$, input reference level is the crosspoint when in differential strobe mode.
- 6) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = $0.2 \times V_{DDQ}$ is recognized as low.
- 7) The output timing reference voltage level is V_{TT} .
- 8) $0 \text{ }^\circ\text{C} \leq T_{CASE} \leq 85 \text{ }^\circ\text{C}$
- 9) $85 \text{ }^\circ\text{C} < T_{CASE} \leq 95 \text{ }^\circ\text{C}$

3.3.3 ODT AC Electrical Characteristics

Table 19 ODT AC Characteristics and Operating Conditions for DDR2-533 and DDR2-400

Symbol	Parameter / Condition	Values		Unit	Note
		Min.	Max.		
t_{AOND}	ODT turn-on delay	2	2	t_{CK}	
t_{AON}	ODT turn-on	$t_{AC.MIN}$	$t_{AC.MAX} + 1 \text{ ns}$	ns	1)
t_{AONPD}	ODT turn-on (Power-Down Modes)	$t_{AC.MIN} + 2 \text{ ns}$	$2 t_{CK} + t_{AC.MAX} + 1 \text{ ns}$	ns	
t_{AOFD}	ODT turn-off delay	2.5	2.5	t_{CK}	
t_{AOF}	ODT turn-off	$t_{AC.MIN}$	$t_{AC.MAX} + 0.6 \text{ ns}$	ns	2)
t_{AOFPD}	ODT turn-off (Power-Down Modes)	$t_{AC.MIN} + 2 \text{ ns}$	$2.5 t_{CK} + t_{AC.MAX} + 1 \text{ ns}$	ns	
t_{ANPD}	ODT to Power Down Mode Entry Latency	3	—	t_{CK}	
t_{AXPD}	ODT Power Down Exit Latency	8	—	t_{CK}	

- 1) ODT turn on time min. is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measure from t_{AOND} .
- 2) ODT turn off time min. is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from t_{AOFD} .

3.4 I_{DD} Specifications and Conditions

List of tables defining I_{DD} Specifications and Conditions.

- [Table 20 “IDD Measurement Conditions” on Page 30](#)
- [Table 22 “IDD Specification for HYS72T\[64/128/256\]xxxHR-3.7-B” on Page 32](#)
- [Table 23 “IDD Specification for HYS72T\[64/128/256\]xxxHR-5-B” on Page 33](#)

Table 20 I_{DD} Measurement Conditions ¹⁾²⁾³⁾⁴⁾⁵⁾⁶⁾

Parameter	Symbol
Operating Current 0 One bank Active - Precharge; $t_{CK} = t_{CK.MIN}$, $t_{RC} = t_{RC.MIN}$, $t_{RAS} = t_{RAS.MIN}$, CKE is HIGH, \overline{CS} is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.	I_{DD0}
Operating Current 1 One bank Active - Read - Precharge; $I_{OUT} = 0$ mA, BL = 4, $t_{CK} = t_{CK.MIN}$, $t_{RC} = t_{RC.MIN}$, $t_{RAS} = t_{RAS.MIN}$, $t_{RCD} = t_{RCD.MIN}$, AL = 0, CL = CL _{MIN} ; CKE is HIGH, \overline{CS} is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.	I_{DD1}
Precharge Standby Current All banks idle; \overline{CS} is HIGH; CKE is HIGH; $t_{CK} = t_{CK.MIN}$; Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD2N}
Precharge Power-Down Current Other control and address inputs are STABLE, Data bus inputs are FLOATING.	I_{DD2P}
Precharge Quiet Standby Current All banks idle; \overline{CS} is HIGH; CKE is HIGH; $t_{CK} = t_{CK.MIN}$; Other control and address inputs are STABLE, Data bus inputs are FLOATING.	I_{DD2Q}
Active Standby Current Burst Read: All banks open; Continuous burst reads; BL = 4; AL = 0, CL = CL _{MIN} ; $t_{CK} = t_{CK.MIN}$; $t_{RAS} = t_{RAS.MAX}$, $t_{RP} = t_{RP.MIN}$; CKE is HIGH, \overline{CS} is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING; $I_{OUT} = 0$ mA.	I_{DD3N}
Active Power-Down Current All banks open; $t_{CK} = t_{CK.MIN}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to LOW (Fast Power-down Exit);	$I_{DD3P(0)}$
Active Power-Down Current All banks open; $t_{CK} = t_{CK.MIN}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to HIGH (Slow Power-down Exit);	$I_{DD3P(1)}$
Operating Current urst Write: All banks open; Continuous burst writes; BL = 4; AL = 0, CL = CL _{MIN} ; $t_{CK} = t_{CK.MIN}$; $t_{RAS} = t_{RAS.MAX}$, $t_{RP} = t_{RP.MAX}$; CKE is HIGH, \overline{CS} is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING;	I_{DD4W}
Burst Refresh Current $t_{CK} = t_{CK.MIN}$, Refresh command every $t_{RFC} = t_{RFC.MIN}$ interval, CKE is HIGH, \overline{CS} is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD5B}
Distributed Refresh Current $t_{CK} = t_{CK.MIN}$, Refresh command every $t_{RFC} = t_{REFI}$ interval, CKE is LOW and \overline{CS} is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD5D}

Table 20 I_{DD} Measurement Conditions (cont'd)¹⁾²⁾³⁾⁴⁾⁵⁾⁶⁾

Parameter	Symbol
Self-Refresh Current CKE \leq 0.2 V; external clock off, CK and \overline{CK} at 0 V; Other control and address inputs are FLOATING, Data bus inputs are FLOATING. I_{DD6} current values are guaranteed up to T_{CASE} of 85 °C max.	I_{DD6}
All Bank Interleave Read Current All banks are being interleaved at minimum t_{RC} without violating t_{RRD} using a burst length of 4. Control and address bus inputs are STABLE during DESELECTS. $I_{out} = 0$ mA.	I_{DD7}

- 1) $V_{DDQ} = 1.8 \text{ V} \pm 0.1 \text{ V}$; $V_{DD} = 1.8 \text{ V} \pm 0.1 \text{ V}$
- 2) I_{DD} specifications are tested after the device is properly initialized and I_{DD} parameter are specified with ODT disabled.
- 3) Definitions for I_{DD} see [Table 21](#)
- 4) I_{DD1} , I_{DD4R} and I_{DD7} current measurements are defined with the outputs disabled ($I_{OUT} = 0$ mA). To achieve this on module level the output buffers can be disabled using an EMRS(1) (Extended Mode Register Command) by setting A12 bit to HIGH.
- 5) For two rank modules: for all active current measurements the other rank is in Precharge Power-Down Mode I_{DD2P}
- 6) For details and notes see the relevant INFINEON component data sheet

Table 21 Definitions for I_{DD}

Parameter	Description
LOW	$V_{IN} \leq V_{IL(ac),MAX}$, HIGH is defined as $V_{IN} \geq V_{IH(ac),MIN}$
STABLE	inputs are stable at a HIGH or LOW level
FLOATING	inputs are $V_{REF} = V_{DDQ} / 2$
SWITCHING	inputs are changing between HIGH and LOW every other clock (once per 2 cycles) for address and control signals, and inputs changing between HIGH and LOW every other data transfer (once per cycle) for DQ signals not including mask or strobes

Table 22 I_{DD} Specification for HYS72T[64/128/256]xxxHR-3.7-B

Product Type	HYS72T64000HR-3.7-B	HYS72T128000HR-3.7-B	HYS72T128020HR-3.7-B	HYS72T256220HR-3.7-B	Unit	Note ¹⁾
Organization	512 MB	1 GB	1 GB	2 GB		
	1 Rank	1 Rank	2 Ranks	2 Ranks		
	×72	×72	×72	×72		
	-3.7	-3.7	-3.7	-3.7		
Symbol	Max.	Max.	Max.	Max.		
I_{DD0}	920	1670	980	1800	mA	2)
I_{DD1}	1010	1850	1070	1980	mA	2)
I_{DD2P}	390	630	460	750	mA	3)
I_{DD2N}	670	1180	1010	1870	mA	3)
I_{DD2Q}	650	1130	960	1760	mA	3)
$I_{DD3P(MRS = 0)}$	580	1000	830	1510	mA	3)
$I_{DD3P(MRS = 1)}$	410	660	490	820	mA	3)
I_{DD3N}	720	1270	1100	2050	mA	3)
I_{DD4R}	1320	2480	1380	2610	mA	2)
I_{DD4W}	1320	2480	1380	2610	mA	2)
I_{DD5B}	1500	2840	1560	2970	mA	2)
I_{DD5D}	410	660	490	820	mA	3)4)
I_{DD6}	63	126	126	252	mA	3)4)
I_{DD7}	1640	3110	1700	3240	mA	2)

- 1) Module I_{DD} is calculated on the basis of component I_{DD} and includes currents of Registers and PLL. ODT disabled. I_{DD1} , I_{DD4R} , and I_{DD7} are defined with the outputs disabled.
- 2) The other rank is in I_{DD2P} Precharge Power-Down Current mode
- 3) Both ranks are in the same I_{DD} current mode
- 4) I_{DD5D} and I_{DD6} values are for $0\text{ °C} \leq T_{Case} \leq 85\text{ °C}$

Table 23 I_{DD} Specification for HYS72T[64/128/256]xxxHR-5-B

Product Type	HYS72T64000HR-5-B	HYS72T128000HR-5-B	HYS72T128020HR-5-B	HYS72T256220HR-5-B	Unit	Note ¹⁾
Organization	512 MB	1 GB	1GB	2 GB		
	1 Rank	1 Rank	2 Ranks	2 Ranks		
	×72	×72	×72	×72		
	-5	-5	-5	-5		
Symbol	Max.	Max.	Max.	Max.		
I_{DD0}	820	1500	890	1630	mA	2)
I_{DD1}	910	1670	970	1790	mA	2)
I_{DD2P}	340	530	400	660	mA	3)
I_{DD2N}	580	1020	890	1630	mA	3)
I_{DD2Q}	560	980	850	1560	mA	3)
$I_{DD3P(MRS = 0)}$	490	840	710	1270	mA	3)
$I_{DD3P(MRS = 1)}$	360	570	440	730	mA	3)
I_{DD3N}	630	1110	980	1810	mA	3)
I_{DD4R}	1130	2120	1190	2240	mA	2)
I_{DD4W}	1130	2120	1190	2240	mA	2)
I_{DD5B}	1400	2660	1460	2780	mA	2)
I_{DD5D}	360	570	440	730	mA	3)4)
I_{DD6}	63	126	126	252	mA	3)4)
I_{DD7}	1540	2940	1610	3070	mA	2)

1) Module I_{DD} is calculated on the basis of component I_{DD} and includes currents of Registers and PLL. ODT disabled. I_{DD1} , I_{DD4R} , and I_{DD7} , are defined with the outputs disabled.

2) The other rank is in I_{DD2P} Precharge Power-Down Current mode

3) Both ranks are in the same I_{DD} current mode

4) I_{DD5D} and I_{DD6} values are for $0\text{ }^{\circ}\text{C} \leq T_{\text{Case}} \leq 85\text{ }^{\circ}\text{C}$.

3.4.1 I_{DD} Test Conditions

For testing the I_{DD} parameters, the timing parameters as shown in the tables below are used.

- [Table 24 “IDD Measurement Test Condition for DDR2–533C” on Page 34](#)
- [Table 25 “IDD Measurement Test Condition for DDR2–400B” on Page 34](#)

Table 24 I_{DD} Measurement Test Condition for DDR2–533C

Parameter	Symbol	–3.7	Unit	Notes
		DDR2–533C		
CAS Latency	CL_{IDD}	3	t_{CK}	
Clock Cycle Time	$t_{CK,IDD}$	3.75	ns	
Active to Read or Write delay	$t_{RCD,IDD}$	15	ns	
Active to Active / Auto-Refresh command period	$t_{RC,IDD}$	60	ns	
Active bank A to Active bank B command delay	$t_{RRD,IDD}$	7.5	ns	1)
		10	ns	2)
Active to Precharge Command	$t_{RAS,MIN,IDD}$	45	ns	
	$t_{RAS,MAX,IDD}$	7000	ns	
Precharge Command Period	$t_{RP,IDD}$	15	ns	
Auto-Refresh to Active / Auto-Refresh command period	$t_{RFC,IDD}$		ns	
Average periodic Refresh interval	$0^{\circ}\text{C} \leq T_{CASE} \leq 85^{\circ}\text{C}$	t_{REFI}	7.8	μS
	$85^{\circ}\text{C} \leq T_{CASE} \leq 95^{\circ}\text{C}$	t_{REFI}	3.9	μS

1) $\times 4$ & $\times 8$ (1 kB page size)

2) $\times 16$ (2 kB page size)

Table 25 I_{DD} Measurement Test Condition for DDR2–400B

Parameter	Symbol	–5	Unit	Notes
		DDR2–400B		
CAS Latency	CL_{IDD}	3	t_{CK}	
Clock Cycle Time	$t_{CK,IDD}$	5	ns	
Active to Read or Write delay	$t_{RCD,IDD}$	15	ns	
Active to Active / Auto-Refresh command period	$t_{RC,IDD}$	55	ns	
Active bank A to Active bank B command delay	$t_{RRD,IDD}$	7.5	ns	1)
		10	ns	2)
Active to Precharge Command	$t_{RAS,MIN,IDD}$	40	ns	
	$t_{RAS,MAX,IDD}$	7000	ns	
Precharge Command Period	$t_{RP,IDD}$	15	ns	
Auto-Refresh to Active / Auto-Refresh command period	$t_{RFC,IDD}$		ns	
Average periodic Refresh interval	$0^{\circ}\text{C} \leq T_{CASE} \leq 85^{\circ}\text{C}$	t_{REFI}	7.8	μS
	$85^{\circ}\text{C} \leq T_{CASE} \leq 95^{\circ}\text{C}$	t_{REFI}	3.9	μS

1) $\times 4$ & $\times 8$ (1 kB page size)

2) $\times 16$ (2 kB page size)

3.4.2 On Die Termination (ODT) Current

The ODT function adds additional current consumption to the DDR2 SDRAM when enabled by the EMRS(1). Depending on address bits A[6,2] in the EMRS(1) a “weak” or “strong” termination can be selected. The

current consumption for any terminated input pin, depends on the input pin is in tri-state or driving 0 or 1, as long a ODT is enabled during a given period of time.

Table 26 ODT current per terminated pin

Parameter	Symbol	Min.	Typ.	Max.	Unit	EMRS(1) State
Enabled ODT current per DQ ODT is HIGH; Data Bus inputs are FLOATING	I_{ODTO}	5	6	7.5	mA/DQ	A6 = 0, A2 = 1
		2.5	3	3.75	mA/DQ	A6 = 1, A2 = 0
Active ODT current per DQ ODT is HIGH; worst case of Data Bus inputs are STABLE or SWITCHING.	I_{ODTT}	10	12	15	mA/DQ	A6 = 0, A2 = 1
		5	6	7.5	mA/DQ	A6 = 1, A2 = 0

Note: For power consumption calculations the ODT duty cycle has to be taken into account

4 SPD Codes

This chapter lists all hexadecimal byte values stored in the EEPROM of the products described in this data sheet. SPD stands for serial presence detect. All values with XX in the table are module specific bytes which are defined during production.

List of SPD Code Tables

- [Table 27 “HYS72T\[64/128/256\]xxxHR-3.7-B” on Page 36](#)
- [Table 28 “HYS72T\[64/128/256\]xxxHR-5-B” on Page 41](#)

Table 27 HYS72T[64/128/256]xxxHR-3.7-B

Product Type		HYS72T64000HR-3.7-B	HYS72T128000HR-3.7-B	HYS72T128020HR-3.7-B	HYS72T256220HR-3.7-B
Organization		512MB	1 GByte	1 GByte	2 GByte
		×72	×72	×72	×72
		1 Rank (×8)	1 Rank (×4)	2 Ranks (×8)	2 Ranks (×4)
Label Code		PC2-4200R-444	PC2-4200R-444	PC2-4200R-444	PC2-4200R-444
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2	Rev. 1.2	Rev. 1.2
Byte#	Description	HEX	HEX	HEX	HEX
0	Programmed SPD Bytes in EEPROM	80	80	80	80
1	Total number of Bytes in EEPROM	08	08	08	08
2	Memory Type (DDR2)	08	08	08	08
3	Number of Row Addresses	0E	0E	0E	0E
4	Number of Column Addresses	0A	0B	0A	0B
5	DIMM Rank and Stacking Information	60	60	61	61
6	Data Width	48	48	48	48
7	Not used	00	00	00	00
8	Interface Voltage Level	05	05	05	05
9	$t_{CK} @ CL_{MAX}$ (Byte 18) [ns]	3D	3D	3D	3D
10	t_{AC} SDRAM @ CL_{MAX} (Byte 18) [ns]	50	50	50	50
11	Error Correction Support (non-ECC, ECC)	02	02	02	02
12	Refresh Rate and Type	82	82	82	82
13	Primary SDRAM Width	08	04	08	04
14	Error Checking SDRAM Width	08	04	08	04
15	Not used	00	00	00	00
16	Burst Length Supported	0C	0C	0C	0C
17	Number of Banks on SDRAM Device	04	04	04	04

Table 27 HYS72T[64/128/256]xxxHR-3.7-B (cont'd)

Product Type		HYS72T64000HR-3.7-B	HYS72T128000HR-3.7-B	HYS72T128020HR-3.7-B	HYS72T256220HR-3.7-B
Organization		512MB	1 GByte	1 GByte	2 GByte
		×72	×72	×72	×72
		1 Rank (×8)	1 Rank (×4)	2 Ranks (×8)	2 Ranks (×4)
Label Code		PC2-4200R-444	PC2-4200R-444	PC2-4200R-444	PC2-4200R-444
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2	Rev. 1.2	Rev. 1.2
Byte#	Description	HEX	HEX	HEX	HEX
18	Supported CAS Latencies	38	38	38	38
19	DIMM Mechanical Characteristics	01	01	01	01
20	DIMM Type Information	01	01	01	01
21	DIMM Attributes	04	05	05	07
22	Component Attributes	07	07	07	07
23	$t_{CK} @ CL_{MAX} -1$ (Byte 18) [ns]	3D	3D	3D	3D
24	t_{AC} SDRAM @ $CL_{MAX} -1$ [ns]	50	50	50	50
25	$t_{CK} @ CL_{MAX} -2$ (Byte 18) [ns]	50	50	50	50
26	t_{AC} SDRAM @ $CL_{MAX} -2$ [ns]	60	60	60	60
27	$t_{RP.MIN}$ [ns]	3C	3C	3C	3C
28	$t_{RRD.MIN}$ [ns]	1E	1E	1E	1E
29	$t_{RCD.MIN}$ [ns]	3C	3C	3C	3C
30	$t_{RAS.MIN}$ [ns]	2D	2D	2D	2D
31	Module Density per Rank	80	01	80	01
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	25	25	25	25
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	37	37	37	37
34	$t_{DS.MIN}$ [ns]	10	10	10	10
35	$t_{DH.MIN}$ [ns]	22	22	22	22
36	$t_{WR.MIN}$ [ns]	3C	3C	3C	3C
37	$t_{WTR.MIN}$ [ns]	1E	1E	1E	1E
38	$t_{RTP.MIN}$ [ns]	1E	1E	1E	1E
39	Analysis Characteristics	00	00	00	00
40	t_{RC} and t_{RFC} Extension	00	00	00	00
41	$t_{RC.MIN}$ [ns]	3C	3C	3C	3C
42	$t_{RFC.MIN}$ [ns]	69	69	69	69
43	$t_{CK.MAX}$ [ns]	80	80	80	80

Table 27 HYS72T[64/128/256]xxxHR-3.7-B (cont'd)

Product Type		HYS72T64000HR-3.7-B	HYS72T128000HR-3.7-B	HYS72T128020HR-3.7-B	HYS72T256220HR-3.7-B
Organization		512MB	1 GByte	1 GByte	2 GByte
		×72	×72	×72	×72
		1 Rank (×8)	1 Rank (×4)	2 Ranks (×8)	2 Ranks (×4)
Label Code		PC2-4200R-444	PC2-4200R-444	PC2-4200R-444	PC2-4200R-444
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2	Rev. 1.2	Rev. 1.2
Byte#	Description	HEX	HEX	HEX	HEX
44	$t_{DQSQ.MAX}$ [ns]	1E	1E	1E	1E
45	$t_{QHS.MAX}$ [ns]	28	28	28	28
46	PLL Relock Time	0F	0F	0F	0F
47	$T_{CASE.MAX}$ Delta / ΔT_{4R4W} Delta	50	50	50	50
48	Psi(T-A) DRAM	7A	7A	7A	7A
49	ΔT_0 (DT0)	43	43	43	43
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} (DT2Q, RDIMM)	29	29	29	29
51	ΔT_{2P} (DT2P)	36	36	36	36
52	ΔT_{3N} (DT3N)	21	21	21	21
53	$\Delta T_{3P.fast}$ (DT3P fast)	41	41	41	41
54	$\Delta T_{3P.slow}$ (DT3P slow)	2A	2A	2A	2A
55	ΔT_{4R} (DT4R) / ΔT_{4R4W} Sign (DT4R4W)	40	40	40	40
56	ΔT_{5B} (DT5B)	1E	1E	1E	1E
57	ΔT_7 (DT7)	22	22	22	22
58	Psi(ca) PLL	C4	C4	C4	C4
59	Psi(ca) REG	8C	8C	8C	8C
60	ΔT_{PLL} (DTPLL)	61	61	61	61
61	ΔT_{REG} (DTREG) / Toggle Rate	78	78	78	78
62	SPD Revision	12	12	12	12
63	Checksum of Bytes 0-62	7E	F9	80	FC
64	JEDEC ID Code of Infineon (1)	C1	C1	C1	C1
65	JEDEC ID Code of Infineon (2)	00	00	00	00
66	JEDEC ID Code of Infineon (3)	00	00	00	00
67	JEDEC ID Code of Infineon (4)	00	00	00	00
68	JEDEC ID Code of Infineon (5)	00	00	00	00
69	JEDEC ID Code of Infineon (6)	00	00	00	00

Table 27 HYS72T[64/128/256]xxxHR-3.7-B (cont'd)

Product Type		HYS72T64000HR-3.7-B	HYS72T128000HR-3.7-B	HYS72T128020HR-3.7-B	HYS72T256220HR-3.7-B
Organization		512MB	1 GByte	1 GByte	2 GByte
		×72	×72	×72	×72
		1 Rank (×8)	1 Rank (×4)	2 Ranks (×8)	2 Ranks (×4)
Label Code		PC2-4200R-444	PC2-4200R-444	PC2-4200R-444	PC2-4200R-444
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2	Rev. 1.2	Rev. 1.2
Byte#	Description	HEX	HEX	HEX	HEX
70	JEDEC ID Code of Infineon (7)	00	00	00	00
71	JEDEC ID Code of Infineon (8)	00	00	00	00
72	Module Manufacturer Location	xx	xx	xx	xx
73	Product Type, Char 1	37	37	37	37
74	Product Type, Char 2	32	32	32	32
75	Product Type, Char 3	54	54	54	54
76	Product Type, Char 4	36	31	31	32
77	Product Type, Char 5	34	32	32	35
78	Product Type, Char 6	30	38	38	36
79	Product Type, Char 7	30	30	30	32
80	Product Type, Char 8	30	30	32	32
81	Product Type, Char 9	48	30	30	30
82	Product Type, Char 10	52	48	48	48
83	Product Type, Char 11	33	52	52	52
84	Product Type, Char 12	2E	33	33	33
85	Product Type, Char 13	37	2E	2E	2E
86	Product Type, Char 14	42	37	37	37
87	Product Type, Char 15	20	42	42	42
88	Product Type, Char 16	20	20	20	20
89	Product Type, Char 17	20	20	20	20
90	Product Type, Char 18	20	20	20	20
91	Module Revision Code	2x	2x	2x	0x
92	Test Program Revision Code	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx

Table 27 HYS72T[64/128/256]xxxHR-3.7-B (cont'd)

Product Type		HYS72T64000HR-3.7-B	HYS72T128000HR-3.7-B	HYS72T128020HR-3.7-B	HYS72T256220HR-3.7-B
Organization		512MB ×72 1 Rank (×8)	1 GByte ×72 1 Rank (×4)	1 GByte ×72 2 Ranks (×8)	2 GByte ×72 2 Ranks (×4)
Label Code		PC2-4200R-444	PC2-4200R-444	PC2-4200R-444	PC2-4200R-444
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2	Rev. 1.2	Rev. 1.2
Byte#	Description	HEX	HEX	HEX	HEX
95 - 98	Module Serial Number	xx	xx	xx	xx
99 - 127	Not used	00	00	00	00

Table 28 HYS72T[64/128/256]xxxHR-5-B

Product Type		HYS72T64000HR-5-B	HYS72T128000HR-5-B	HYS72T128020HR-5-B	HYS72T256220HR-5-B
Organization		512MB	1 GByte	1 GByte	2 GByte
		×72	×72	×72	×72
		1 Rank (×8)	1 Rank (×4)	2 Ranks (×8)	2 Ranks (×4)
Label Code		PC2-3200R-333	PC2-3200R-333	PC2-3200R-333	PC2-3200R-333
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2	Rev. 1.2	Rev. 1.2
Byte#	Description	HEX	HEX	HEX	HEX
0	Programmed SPD Bytes in EEPROM	80	80	80	80
1	Total number of Bytes in EEPROM	08	08	08	08
2	Memory Type (DDR2)	08	08	08	08
3	Number of Row Addresses	0E	0E	0E	0E
4	Number of Column Addresses	0A	0B	0A	0B
5	DIMM Rank and Stacking Information	60	60	61	61
6	Data Width	48	48	48	48
7	Not used	00	00	00	00
8	Interface Voltage Level	05	05	05	05
9	$t_{CK} @ CL_{MAX}$ (Byte 18) [ns]	50	50	50	50
10	t_{AC} SDRAM @ CL_{MAX} (Byte 18) [ns]	60	60	60	60
11	Error Correction Support (non-ECC, ECC)	02	02	02	02
12	Refresh Rate and Type	82	82	82	82
13	Primary SDRAM Width	08	04	08	04
14	Error Checking SDRAM Width	08	04	08	04
15	Not used	00	00	00	00
16	Burst Length Supported	0C	0C	0C	0C
17	Number of Banks on SDRAM Device	04	04	04	04
18	Supported CAS Latencies	38	38	38	38
19	DIMM Mechanical Characteristics	01	01	01	01
20	DIMM Type Information	01	01	01	01
21	DIMM Attributes	04	05	05	07
22	Component Attributes	07	07	07	07
23	$t_{CK} @ CL_{MAX} -1$ (Byte 18) [ns]	50	50	50	50
24	t_{AC} SDRAM @ $CL_{MAX} -1$ [ns]	60	60	60	60
25	$t_{CK} @ CL_{MAX} -2$ (Byte 18) [ns]	50	50	50	50

Table 28 HYS72T[64/128/256]xxxHR-5-B (cont'd)

Product Type		HYS72T64000HR-5-B	HYS72T128000HR-5-B	HYS72T128020HR-5-B	HYS72T256220HR-5-B
Organization		512MB ×72 1 Rank (×8)	1 GByte ×72 1 Rank (×4)	1 GByte ×72 2 Ranks (×8)	2 GByte ×72 2 Ranks (×4)
Label Code		PC2-3200R-333	PC2-3200R-333	PC2-3200R-333	PC2-3200R-333
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2	Rev. 1.2	Rev. 1.2
Byte#	Description	HEX	HEX	HEX	HEX
26	t_{AC} SDRAM @ $CL_{MAX} - 2$ [ns]	60	60	60	60
27	$t_{RP.MIN}$ [ns]	3C	3C	3C	3C
28	$t_{RRD.MIN}$ [ns]	1E	1E	1E	1E
29	$t_{RCD.MIN}$ [ns]	3C	3C	3C	3C
30	$t_{RAS.MIN}$ [ns]	28	28	28	28
31	Module Density per Rank	80	01	80	01
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	35	35	35	35
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	47	47	47	47
34	$t_{DS.MIN}$ [ns]	15	15	15	15
35	$t_{DH.MIN}$ [ns]	27	27	27	27
36	$t_{WR.MIN}$ [ns]	3C	3C	3C	3C
37	$t_{WTR.MIN}$ [ns]	28	28	28	28
38	$t_{RTP.MIN}$ [ns]	1E	1E	1E	1E
39	Analysis Characteristics	00	00	00	00
40	t_{RC} and t_{RFC} Extension	00	00	00	00
41	$t_{RC.MIN}$ [ns]	37	37	37	37
42	$t_{RFC.MIN}$ [ns]	69	69	69	69
43	$t_{CK.MAX}$ [ns]	80	80	80	80
44	$t_{DQSQ.MAX}$ [ns]	23	23	23	23
45	$t_{QHS.MAX}$ [ns]	2D	2D	2D	2D
46	PLL Relock Time	0F	0F	0F	0F
47	$T_{CASE.MAX}$ Delta / ΔT_{4R4W} Delta	50	50	50	50
48	Psi(T-A) DRAM	7A	7A	7A	7A
49	ΔT_0 (DT0)	3B	3B	3B	3B
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} (DT2Q, RDIMM)	25	25	25	25
51	ΔT_{2P} (DT2P)	36	36	36	36
52	ΔT_{3N} (DT3N)	1E	1E	1E	1E

Table 28 HYS72T[64/128/256]xxxHR-5-B (cont'd)

Product Type		HYS72T64000HR-5-B	HYS72T128000HR-5-B	HYS72T128020HR-5-B	HYS72T256220HR-5-B
Organization		512MB ×72 1 Rank (×8)	1 GByte ×72 1 Rank (×4)	1 GByte ×72 2 Ranks (×8)	2 GByte ×72 2 Ranks (×4)
Label Code		PC2-3200R-333	PC2-3200R-333	PC2-3200R-333	PC2-3200R-333
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2	Rev. 1.2	Rev. 1.2
Byte#	Description	HEX	HEX	HEX	HEX
53	$\Delta T_{3P.fast}$ (DT3P fast)	38	38	38	38
54	$\Delta T_{3P.slow}$ (DT3P slow)	2A	2A	2A	2A
55	ΔT_{4R} (DT4R) / ΔT_{4R4W} Sign (DT4R4W)	38	38	38	38
56	ΔT_{5B} (DT5B)	1D	1D	1D	1D
57	ΔT_7 (DT7)	21	21	21	21
58	Psi(ca) PLL	C4	C4	C4	C4
59	Psi(ca) REG	8C	8C	8C	8C
60	ΔT_{PLL} (DTPLL)	59	59	59	59
61	ΔT_{REG} (DTREG) / Toggle Rate	5C	5C	5C	5C
62	SPD Revision	12	12	12	12
63	Checksum of Bytes 0-62	B2	2D	B4	30
64	JEDEC ID Code of Infineon (1)	C1	C1	C1	C1
65	JEDEC ID Code of Infineon (2)	00	00	00	00
66	JEDEC ID Code of Infineon (3)	00	00	00	00
67	JEDEC ID Code of Infineon (4)	00	00	00	00
68	JEDEC ID Code of Infineon (5)	00	00	00	00
69	JEDEC ID Code of Infineon (6)	00	00	00	00
70	JEDEC ID Code of Infineon (7)	00	00	00	00
71	JEDEC ID Code of Infineon (8)	00	00	00	00
72	Module Manufacturer Location	xx	xx	xx	xx
73	Product Type, Char 1	37	37	37	37
74	Product Type, Char 2	32	32	32	32
75	Product Type, Char 3	54	54	54	54
76	Product Type, Char 4	36	31	31	32
77	Product Type, Char 5	34	32	32	35
78	Product Type, Char 6	30	38	38	36
79	Product Type, Char 7	30	30	30	32

Table 28 HYS72T[64/128/256]xxxHR-5-B (cont'd)

Product Type		HYS72T64000HR-5-B	HYS72T128000HR-5-B	HYS72T128020HR-5-B	HYS72T256220HR-5-B
Organization		512MB ×72 1 Rank (×8)	1 GByte ×72 1 Rank (×4)	1 GByte ×72 2 Ranks (×8)	2 GByte ×72 2 Ranks (×4)
Label Code		PC2-3200R-333	PC2-3200R-333	PC2-3200R-333	PC2-3200R-333
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2	Rev. 1.2	Rev. 1.2
Byte#	Description	HEX	HEX	HEX	HEX
80	Product Type, Char 8	30	30	32	32
81	Product Type, Char 9	48	30	30	30
82	Product Type, Char 10	52	48	48	48
83	Product Type, Char 11	35	52	52	52
84	Product Type, Char 12	42	35	35	35
85	Product Type, Char 13	20	42	42	42
86	Product Type, Char 14	20	20	20	20
87	Product Type, Char 15	20	20	20	20
88	Product Type, Char 16	20	20	20	20
89	Product Type, Char 17	20	20	20	20
90	Product Type, Char 18	20	20	20	20
91	Module Revision Code	2x	2x	2x	0x
92	Test Program Revision Code	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx	xx
99 - 127	Not used	00	00	00	00

5 Package Outlines

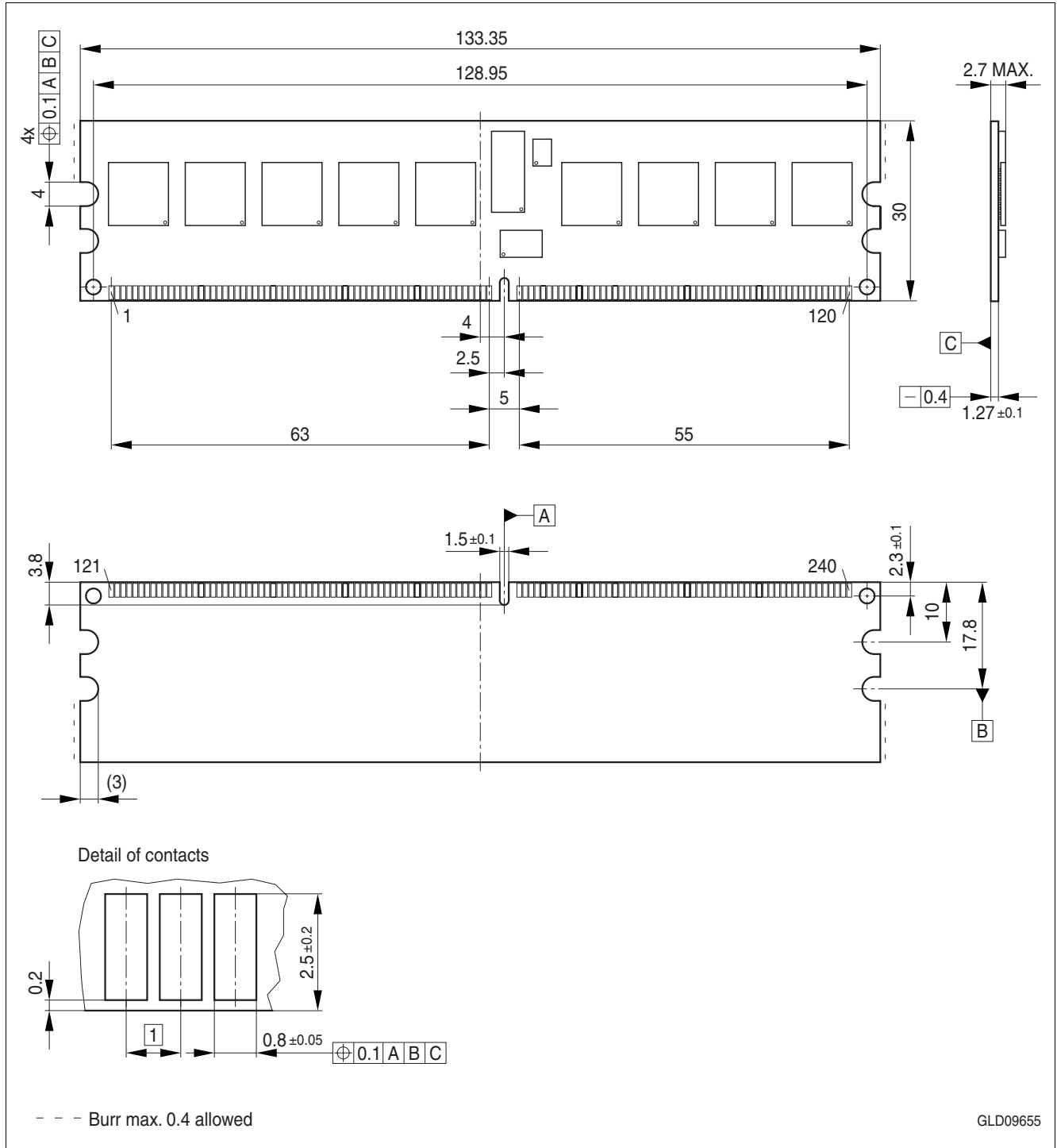


Figure 6 Package Outline Raw Card A L-DIM-240-11

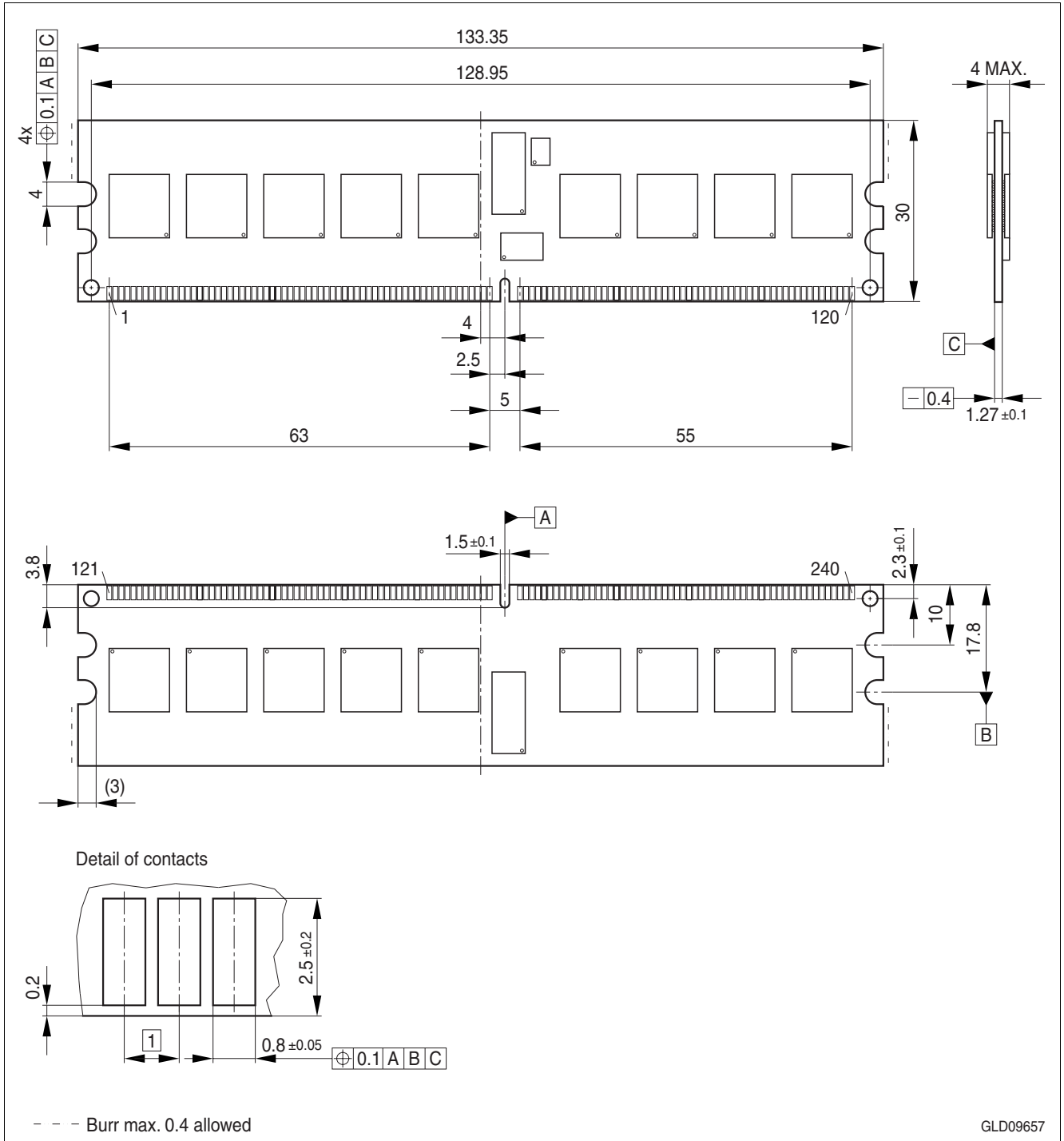


Figure 7 Package Outline Raw Card C L-DIM-240-13

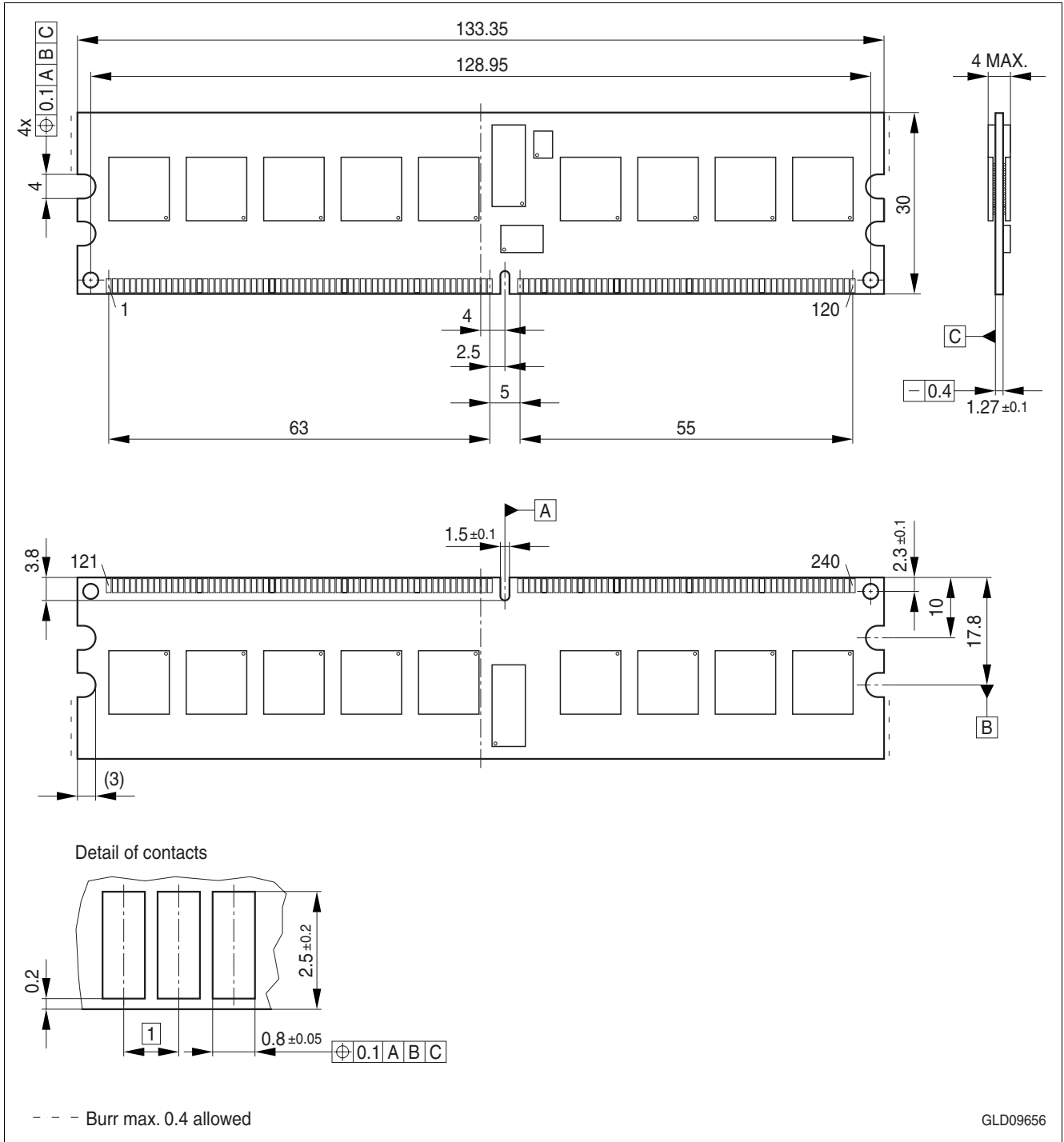
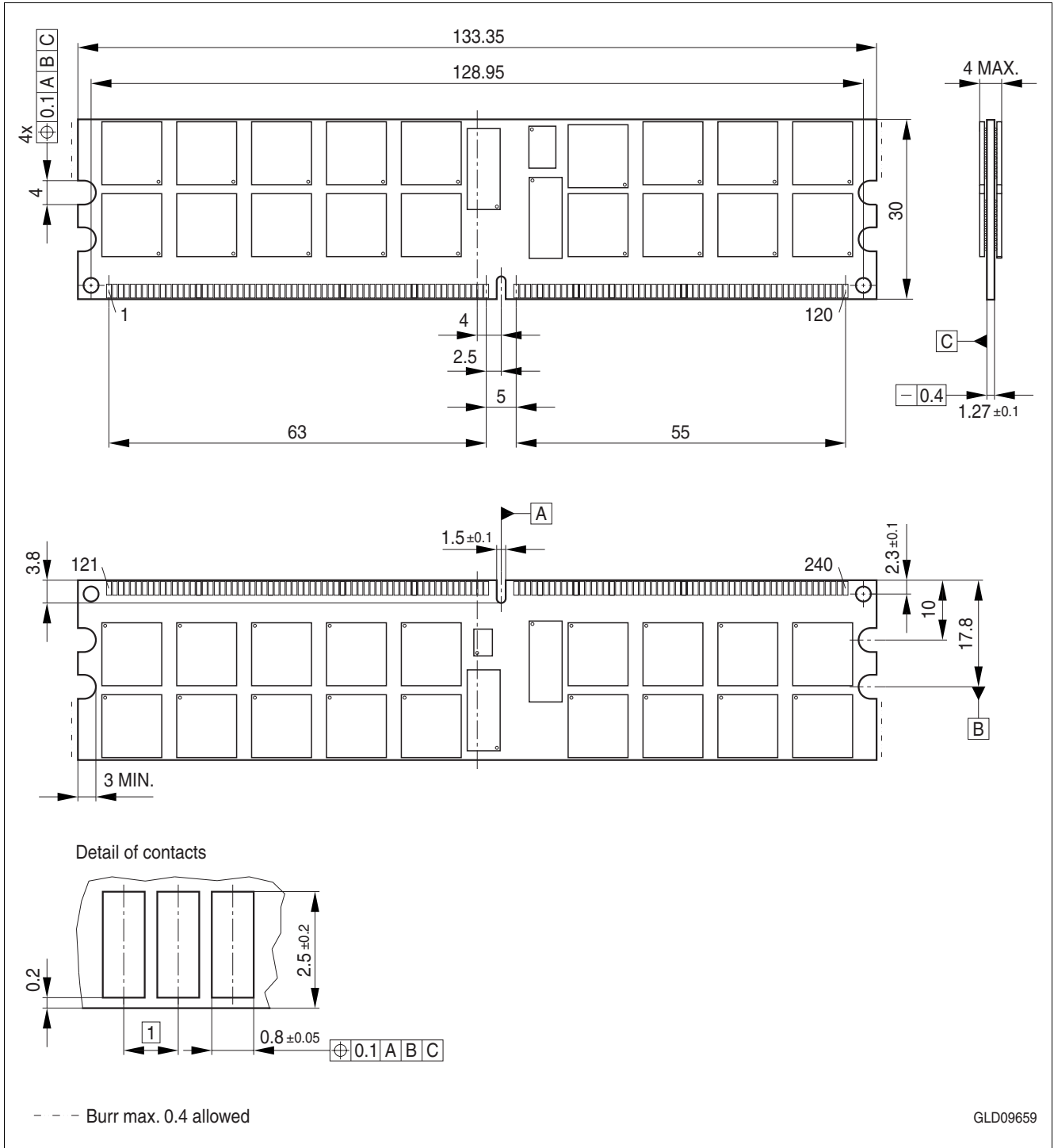


Figure 8 Package Outline Raw Card B L-DIM-240-12



6 Product Type Nomenclature (DDR2 DRAMs and DIMMs)

Infineon's nomenclature uses simple coding combined with some proprietary coding. [Table 29](#) provides examples for module and component product type number as well as the field number. The detailed field

description together with possible values and coding explanation is listed for modules in [Table 30](#) and for components in [Table 31](#).

Table 29 Nomenclature Fields and Examples

Example for	Field Number										
	1	2	3	4	5	6	7	8	9	10	11
Micro-DIMM	HYS	64	T	64	0	2	0	K	M	-5	-A
DDR2 DRAM	HYB	18	T	512	16		0	A	C	-5	

Table 30 DDR2 DIMM Nomenclature

Field	Description	Values	Coding
1	INFINEON Modul Prefix	HYS	Constant
2	Module Data Width [bit]	64	Non-ECC
		72	ECC
3	DRAM Technology	T	DDR2
4	Memory Density per I/O [Mbit]; Module Density ¹⁾	32	256 MByte
		64	512 MByte
		128	1 GByte
		256	2 GByte
		512	4 GByte
5	Raw Card Generation	0 .. 9	Look up table
6	Number of Module Ranks	0, 2, 4	1, 2, 4
7	Product Variations	0 .. 9	Look up table
8	Package, Lead-Free Status	A .. Z	Look up table
9	Module Type	D	SO-DIMM
		M	Micro-DIMM
		R	Registered
		U	Unbuffered
10	Speed Grade	-2.5	PC2-6400 6-6-6
		-3	PC2-5300 4-4-4
		-3S	PC2-5300 5-5-5
		-3.7	PC2-4200 4-4-4
		-3.7F	PC2-4200 CL3
		-5	PC2-3200 3-3-3
11	Die Revision	-A	First
		-B	Second

- 1) Multiplying "Memory Density per I/O" with "Module Data Width" and dividing by 8 for Non-ECC and 9 for ECC modules gives the overall module memory density in MBytes as listed in column "Coding".

Table 31 DDR2 DRAM Nomenclature

Field	Description	Values	Coding
1	INFINEON Component Prefix	HYB	Constant
2	Interface Voltage [V]	18	SSTL1.8
3	DRAM Technology	T	DDR2
4	Component Density [Mbit]	256	256 Mbit
		512	512 Mbit
		1G	1 Gbit
		2G	2 Gbit
5+6	Number of I/Os	40	×4
		80	×8
		16	×16
7	Product Variations	0 .. 9	Look up table
8	Die Revision	A	First
		B	Second
9	Package, Lead-Free Status	C	FBGA, lead-containing
		F	FBGA, lead-free
10	Speed Grade	-2.5	DDR2-800E 6-6-6
		-3	DDR2-667C 4-4-4
		-3S	DDR2-667D 5-5-5
		-3.7	DDR2-533C 4-4-4
		-3.7F	DDR2-533C CL3
		-5	DDR2-400B 3-3-3

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