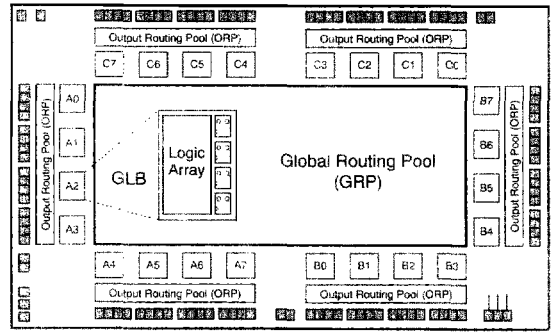
ispLSI® 2096E

In-System Programmable SuperFAST™ High Density PLD

Features

- **SUPERFAST HIGH DENSITY IN-SYSTEM PROGRAMMABLE LOGIC**
  - **4000 PLD Gates**
  - **96 I/O Pins, Six Dedicated Inputs**
  - **96 Registers**
  - **High Speed Global Interconnect**
  - **Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  - **Small Logic Block Size for Random Logic**
  - **100% Functional/JEDEC Upward Compatible with ispLSI 2096 Devices**
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **fmax = 180 MHz Maximum Operating Frequency**
  - **tpd = 5.0 ns Propagation Delay**
  - **TTL Compatible Inputs and Outputs**
  - **5V Programmable Logic Core**
  - **ispJTAG™ In-System Programmable via IEEE 1149.1 (JTAG) Test Access Port**
  - **User-Selectable 3.3V or 5V I/O Supports Mixed-Voltage Systems**
  - **PCI Compatible Outputs**
  - **Open-Drain Output Option**
  - **Electrically Erasable and Reprogrammable**
  - **Non-Volatile**
  - **Unused Product Term Shutdown Saves Power**
- **ispLSI OFFERS THE FOLLOWING ADDED FEATURES**
  - **Increased Manufacturing Yields, Reduced Time-to-Market and Improved Product Quality**
  - **Reprogram Soldered Devices for Faster Prototyping**
- **OFFERS THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - **Complete Programmable Device Can Combine Glue Logic and Structured Designs**
  - **Enhanced Pin Locking Capability**
  - **Three Dedicated Clock Input Pins**
  - **Synchronous and Asynchronous Clocks**
  - **Programmable Output Slew Rate Control to Minimize Switching Noise**
  - **Flexible Pin Placement**
  - **Optimized Global Routing Pool Provides Global Interconnectivity**
- **ispEXPERT™ – LOGIC COMPILER AND COMPLETE ISP DEVICE DESIGN SYSTEMS FROM HDL SYNTHESIS THROUGH IN-SYSTEM PROGRAMMING**
  - **Superior Quality of Results**
  - **Tightly Integrated with Leading CAE Vendor Tools**
  - **Productivity Enhancing Timing Analyzer, Explore Tools, Timing Simulator and ispANALYZER™**
  - **PC and UNIX Platforms**

Functional Block Diagram



Description

The ispLSI 2096E is a High Density Programmable Logic Device. The device contains 96 Registers, 96 Universal I/O pins, six Dedicated Input pins, three Dedicated Clock Input pins, two dedicated Global OE input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 2096E features 5V in-system programmability and in-system diagnostic capabilities. The ispLSI 2096E offers non-volatile reprogrammability of all logic, as well as the interconnect to provide truly reconfigurable systems.

The basic unit of logic on the ispLSI 2096E device is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. C7 (see Figure 1). There are a total of 24 GLBs in the ispLSI 2096E device. Each GLB is made up of four macrocells. Each GLB has 18 inputs, a programmable AND/OR/Exclusive OR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any GLB on the device.

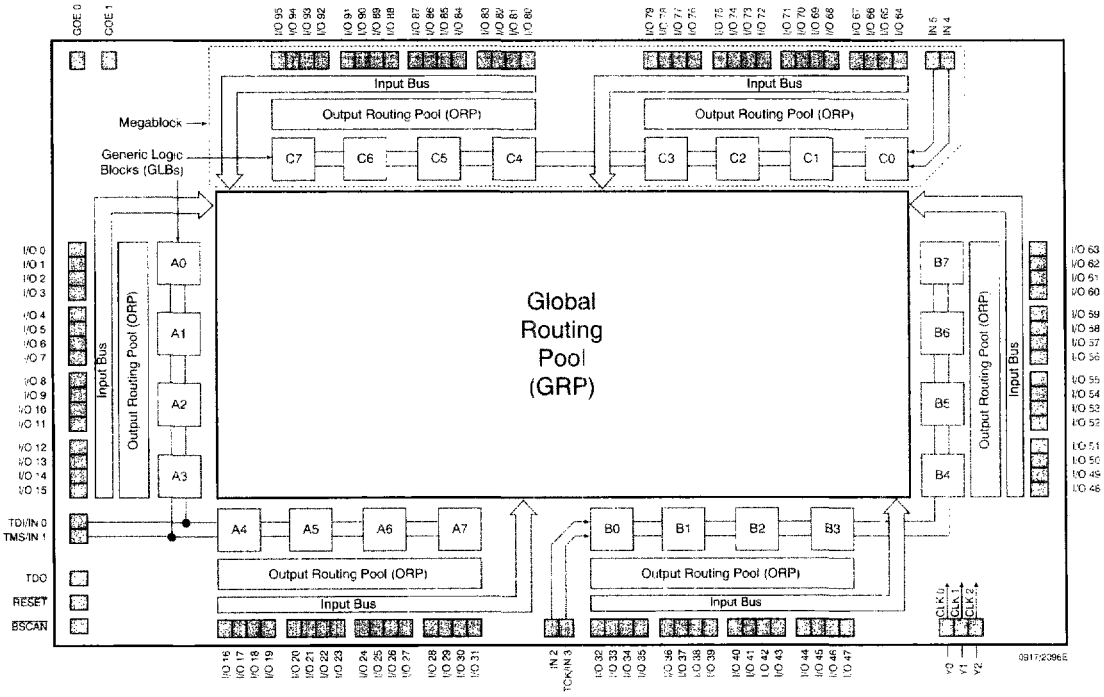
The device also has 96 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, output or bi-directional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise. By connecting

LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-LATTICE; FAX (503) 681-3037; http://www.latticesemi.com

November 1998

Functional Block Diagram

Figure 1. ispLSI 2096E Functional Block Diagram



the VCCIO pins to a common 5V or 3.3V power supply, I/O output levels can be matched to 5V or 3.3V compatible voltages. When connected to a 5V supply, the I/O pins provide PCI-compatible output drive.

Eight GLBs, 32 I/O cells, two dedicated inputs and two ORPs are connected together to make a Megablock (see Figure 1). The outputs of the eight GLBs are connected to a set of 32 universal I/O cells by the two ORPs. Each ispLSI 2096E device contains three Megablocks.

The GRP has as its inputs, the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI 2096E device are selected using the dedicated clock pins. Three dedicated clock pins (Y0, Y1, Y2) or an asynchronous clock can be selected on a GLB basis. The asynchronous or Product Term clock can be generated in any GLB for its own clock.

Programmable Open-Drain Outputs

In addition to the standard output configuration, the outputs of the ispLSI 2096E are individually programmable, either as a standard totem-pole output or an open-drain output. The totem-pole output drives the specified Voh and Vol levels, whereas the open-drain output drives only the specified Vol. The Voh level on the open-drain output depends on the external loading and pull-up. This output configuration is controlled by a programmable fuse. The default configuration when the device is in bulk erased state is totem-pole configuration. The open-drain/totem-pole option is selectable through the ispEXPERT software tools.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST COND.[4]	#[2]	DESCRIPTION[1]	-180		-135		-100		UNITS
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Data Prop Delay, 4PT Bypass, ORP Bypass	–	5.0	–	7.5	–	10.0	ns
t_{pd2}	A	2	Data Prop Delay	–	7.5	–	10.0	–	13.0	ns
f_{max}	A	3	Clk Freq with Internal Feedback[3]	180	–	135	–	100	–	MHz
f_{max} (Ext.)	–	4	Clk Freq with External Feedback $\left(\frac{1}{t_{su2} + t_{co1}}\right)$	125	–	100	–	77	–	MHz
f_{max} (Tog.)	–	5	Clk Frequency, Max. Toggle	200	–	143	–	100	–	MHz
t_{su1}	–	6	GLB Reg Setup Time before Clk, 4 PT Bypass	4.0	–	5.0	–	6.5	–	ns
t_{co1}	A	7	GLB Reg Clk to Output Delay, ORP Bypass	–	3.0	–	4.0	–	5.0	ns
t_{h1}	–	8	GLB Reg Hold Time after Clk, 4 PT Bypass	0.0	–	0.0	–	0.0	–	ns
t_{su2}	–	9	GLB Reg Setup Time before Clk	5.0	–	6.0	–	8.0	–	ns
t_{co2}	–	10	GLB Reg Clk to Output Delay	–	3.5	–	4.5	–	6.0	ns
t_{h2}	–	11	GLB Reg Hold Time after Clk	0.0	–	0.0	–	0.0	–	ns
t_{r1}	A	12	External Reset Pin to Output Delay	–	7.0	–	10.0	–	13.5	ns
t_{rw1}	–	13	External Reset Pulse Duration	4.0	–	5.0	–	6.5	–	ns
t_{ptoeen}	B	14	Input to Output Enable	–	10.0	–	12.0	–	15.0	ns
$t_{ptoedis}$	C	15	Input to Output Disable	–	10.0	–	12.0	–	15.0	ns
t_{goeen}	B	16	Global OE Output Enable	–	5.0	–	7.0	–	9.0	ns
t_{goedis}	C	17	Global OE Output Disable	–	5.0	–	7.0	–	9.0	ns
t_{wh}	–	18	External Synch Clk Pulse Duration, High	2.5	–	3.5	–	5.0	–	ns
t_{wl}	–	19	External Synch Clk Pulse Duration, Low	2.5	–	3.5	–	5.0	–	ns

Table 2-0030A/2096E

1. Unless noted otherwise, all parameters use a GRP load of four GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. Reference Switching Test Conditions section.