

To our customers,

Old Company Name in Catalogs and Other Documents

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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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M5M5256DFP,VP -70G,-70GI,-70XG

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5256DFP,VP is 262,144-bit CMOS static RAMs organized as 32,768-words by 8-bits which is fabricated using high-performance 3 poly silicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery results in a high density and low power static RAM. Stand-by current is small enough for battery back-up application. It is ideal for the memory systems which require simple interface.

Especially the M5M5256DVP are packaged in a 28-pin thin small outline package.

FEATURE

| Type | Access time (max) | Operating Temperature | Power supply current | |
|------------------------|-------------------|-----------------------|---|---|
| | | | Active (max) | Stand-by (max) |
| M5M5256DFP,VP -70G | 70ns | 0~70°C | 45mA (V _{CC} =5.5V) | 20μA (V _{CC} =5.5V) |
| | | | | 12μA (V _{CC} =3.6V) |
| M5M5256DFP,VP -70GI | 70ns | -40~85°C | 25mA (V _{CC} =3.6V) | 40μA (V _{CC} =5.5V) |
| | | | | 24μA (V _{CC} =3.6V) |
| M5M5256DFP,VP -70XG | 70ns | 0~70°C | 0.05μA (V _{CC} =3.0V Typical) | 5μA (V _{CC} =5.5V) |
| | | | | 2.4μA (V _{CC} =3.6V) |
| | | | | 0.05μA (V _{CC} =3.0V Typical) |

- Single 3.0~5.5V power supply
- No clocks, no refresh
- Data-Hold on +2.0V power supply
- Directly TTL compatible : all inputs and outputs
- Three-state outputs : OR-tie capability
- /OE prevents data contention in the I/O bus
- Common Data I/O
- Battery backup capability
- Low stand-by current 0.05μA(typ.)

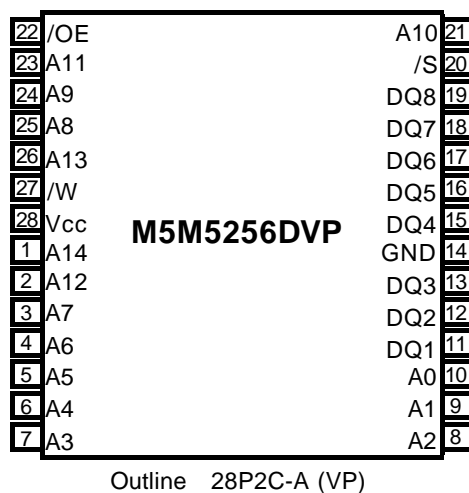
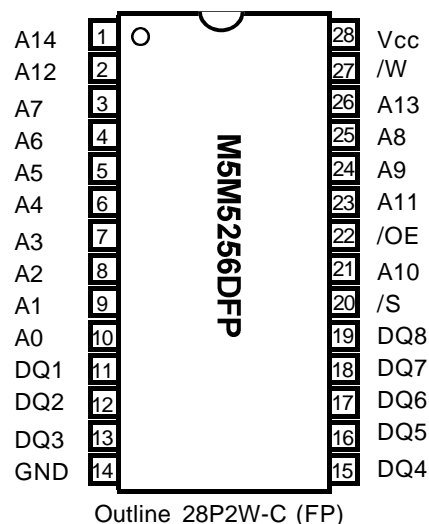
PACKAGE

M5M5256DFP : 28 pin 450 mil SOP
M5M5256DVP : 28pin 8 X 13.4 mm² TSOP

APPLICATION

Small capacity memory units

PIN CONFIGURATION (TOP VIEW)



M5M5256DFP,VP -70G,-70GI,-70XG**262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM****FUNCTION**

The operation mode of the M5M5256DFP,VP is determined by a combination of the device control inputs /S, /W and /OE. Each mode is summarized in the function table.

A write cycle is executed whenever the low level /W overlaps with the low level /S. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of /W, /S, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable /OE directly controls the output stage. Setting the /OE at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is executed by setting /W at a high level and /OE at a low level while /S are in an active state.

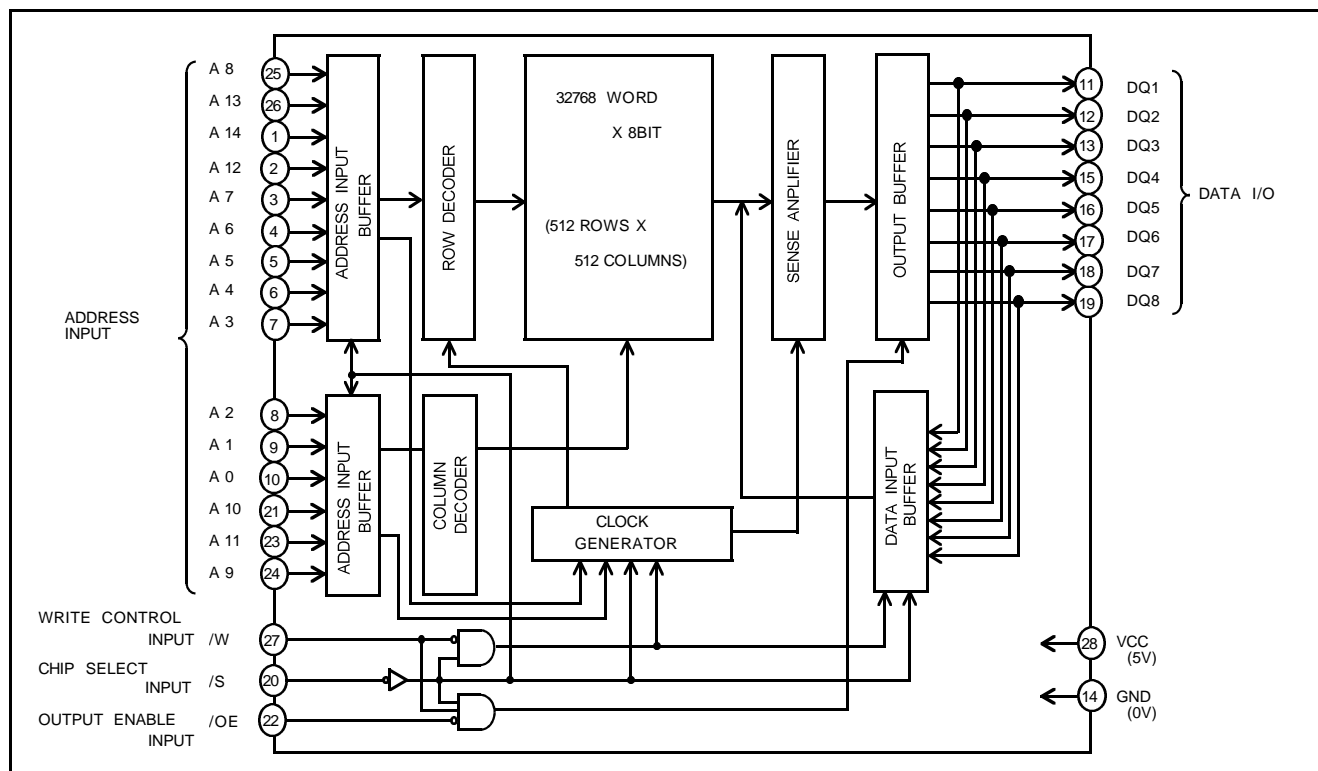
When setting /S at a high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by /S. The power supply current is reduced as low as the stand-by current which is specified as Icc3 or Icc4, and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

| /S | /W | /OE | Mode | DQ | Icc |
|----|----|-----|---------------|------------------|----------|
| H | X | X | Non selection | High-impedance | Stand-by |
| L | L | X | Write | D _{IN} | Active |
| L | H | L | Read | D _{OUT} | Active |
| L | H | H | | High-impedance | Active |

Note • "H" and "L" in this table mean VIH and VIL, respectively.

• "X" in this table should be "H" or "L".

BLOCK DIAGRAM

M5M5256DFP,VP -70G,-70GI,-70XG

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Ratings | Unit |
|------------------|-----------------------|----------------------|---|------|
| V _{CC} | Supply voltage | With respect to GND | -0.3*~7.0 | V |
| V _I | Input voltage | | -0.3*~V _{CC} +0.3 (Max 7.0) | V |
| V _O | Output voltage | | 0~V _{CC} | V |
| P _d | Power dissipation | T _a =25°C | 700 | mW |
| T _{opr} | Operating temperature | -G,-XG | 0~70 | °C |
| T _{stg} | Storage temperature | -GI | -40~85 | |
| | | | -65~150 | °C |

* -3.0V in case of AC (Pulse width ≤ 30ns)

DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test conditions | Limits1 (V _{CC} =3.3±0.3V) | | | Limits2 (V _{CC} =5.0±0.5V) | | | Unit |
|------------------|---|---|--|--------|----------------------|--|-----|----------------------|------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| V _{IH} | High-level input voltage | | 2.0 | | V _{CC} +0.3 | 2.2 | | V _{CC} +0.3 | V |
| V _{IL} | Low-level input voltage | | -0.3* | | 0.6 | -0.3* | | 0.8 | V |
| V _{OH1} | High-level output voltage 1 | I _{OH} =-1mA (V _{CC} =5.0±0.5V) I _{OH} =-0.5mA (V _{CC} =3.3±0.3V) | 2.4 | | | 2.4 | | | V |
| V _{OH2} | High-level output voltage 2 | I _{OH} =-0.1mA (V _{CC} =5.0±0.5V) I _{OH} =-0.05mA (V _{CC} =3.3±0.3V) | V _{CC} -0.5 | | | V _{CC} -0.5 | | | V |
| V _{OL} | Low-level output voltage | I _{OL} =2mA (V _{CC} =5.0±0.5V) I _{OL} =1mA (V _{CC} =3.3±0.3V) | | | 0.4 | | | 0.4 | V |
| I _I | Input current | V _I =0~V _{CC} | | | ±1 | | | ±1 | μA |
| I _O | Output current in off-state | /S=V _{IH} or or /OE=V _{IH} , V _{I/O} =0~V _{CC} | | | ±1 | | | ±1 | μA |
| I _{CC1} | Active supply current (AC, MOS level) | /S<0.2V, Output-open Other inputs<0.2V or >V _{CC} -0.2V | 70ns | 13 | 25 | | 25 | 40 | mA |
| | | | 1MHz | 1.5 | 3 | | 2 | 4 | |
| I _{CC2} | Active supply current (AC, TTL level) | /S=V _{IL} , Output-open other inputs=V _{IH} or V _{IL} | 70ns | 14 | 25 | | 25 | 45 | mA |
| | | | 1MHz | 1.5 | 3 | | 4 | 8 | |
| I _{CC3} | Stand-by current | /S>V _{CC} -0.2V, other inputs =0~V _{CC} | ~25°C | -G,-GI | | 1.2 | | 2 | μA |
| | | | | -XG | 0.05 | 0.3 | 0.1 | 0.4 | |
| | | | ~40°C | -G,-GI | | 3.6 | | 6 | |
| | | | | -XG | | 0.8 | | 1.2 | |
| | | | ~70°C | -G,-GI | | 12 | | 20 | |
| | | | | -XG | | 2.4 | | 5 | |
| | | | ~85°C | -GI | | 24 | | 40 | |
| I _{CC4} | Stand-by current | /S=V _{IH} , other inputs=0~V _{CC} | | | 0.33 | | | 3 | mA |

* -3.0V in case of AC (Pulse width ≤ 30ns)

CAPACITANCE

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|----------------|--------------------|--|--------|-----|-----|------|
| | | | Min | Typ | Max | |
| C _I | Input capacitance | V _I =GND, V _I =25mVrms, f=1MHz | | | 6 | pF |
| C _O | Output capacitance | V _O =GND, V _O =25mVrms, f=1MHz | | | 8 | pF |

Note 0: Direction for current flowing into an IC is positive (no mark).

1: Typical value is one at T_a = 25°C.2: C_I, C_O are periodically sampled and are not 100% tested.

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AC ELECTRICAL CHARACTERISTICS**(1) READ CYCLE**

| Symbol | Parameter | Limits1 V _{CC} =3.3±0.3V | | Limits2 V _{CC} =5.0±0.5V | | Unit |
|-----------------------|------------------------------------|--------------------------------------|-----|--------------------------------------|-----|------|
| | | Min | Max | Min | Max | |
| t _{CR} | Read cycle time | 70 | | 70 | | ns |
| t _a (A) | Address access time | | 70 | | 70 | ns |
| t _a (S) | Chip select access time | | 70 | | 70 | ns |
| t _a (OE) | Output enable access time | | 35 | | 35 | ns |
| t _{dis} (S) | Output disable time after /S high | | 25 | | 25 | ns |
| t _{dis} (OE) | Output disable time after /OE high | | 25 | | 25 | ns |
| t _{en} (S) | Output enable time after /S low | 5 | | 5 | | ns |
| t _{en} (OE) | Output enable time after /OE low | 5 | | 5 | | ns |
| t _v (A) | Data valid time after address | 10 | | 10 | | ns |

(2) WRITE CYCLE

| Symbol | Parameter | Limits1 V _{CC} =3.3±0.3V | | Limits2 V _{CC} =5.0±0.5V | | Unit |
|------------------------|--|--------------------------------------|-----|--------------------------------------|-----|------|
| | | Min | Max | Min | Max | |
| t _{CW} | Write cycle time | 70 | | 70 | | ns |
| t _w (W) | Write pulse width | 55 | | 50 | | ns |
| t _{su} (A) | Address setup time | 0 | | 0 | | ns |
| t _{su} (A-WH) | Address setup time with respect to /W high | 65 | | 65 | | ns |
| t _{su} (S) | Chip select setup time | 65 | | 65 | | ns |
| t _{su} (D) | Data setup time | 30 | | 30 | | ns |
| t _h (D) | Data hold time | 0 | | 0 | | ns |
| t _{rec} (W) | Write recovery time | 0 | | 0 | | ns |
| t _{dis} (W) | Output disable time from /W low | | 25 | | 25 | ns |
| t _{dis} (OE) | Output disable time from /OE high | | 25 | | 25 | ns |
| t _{en} (W) | Output enable time from /W high | 5 | | 5 | | ns |
| t _{en} (OE) | Output enable time from /OE low | 5 | | 5 | | ns |

The diagram illustrates the timing relationships for a read cycle. The signals shown are A_{0-14} , $/S$, $/OE$, and DQ_{1-8} . The $/W = "H"$ level is indicated at the bottom. Key timing parameters are labeled: t_{CR} (Read cycle time), $t_a(A)$ (Address setup time), $t_v(A)$ (Address hold time), $t_a(S)$ (Select setup time), $t_a(OE)$ (Output Enable setup time), $t_{dis}(S)$ (Select delay time), $t_{dis}(OE)$ (Output Enable delay time), $t_{en}(S)$ (Select enable time), $t_{en}(OE)$ (Output Enable enable time), and $t_{en}(S)$ (Select enable time). The DQ_{1-8} signal is shown as a bus with a **DATA VALID** period indicated by a double-headed arrow.

Write cycle (/W control mode)

The diagram illustrates the timing relationships for a write cycle in /W control mode. The signals shown are A_{0-14} , $/S$, $/OE$, $/W$, and DQ_{1-8} .

Key timing parameters and their definitions:

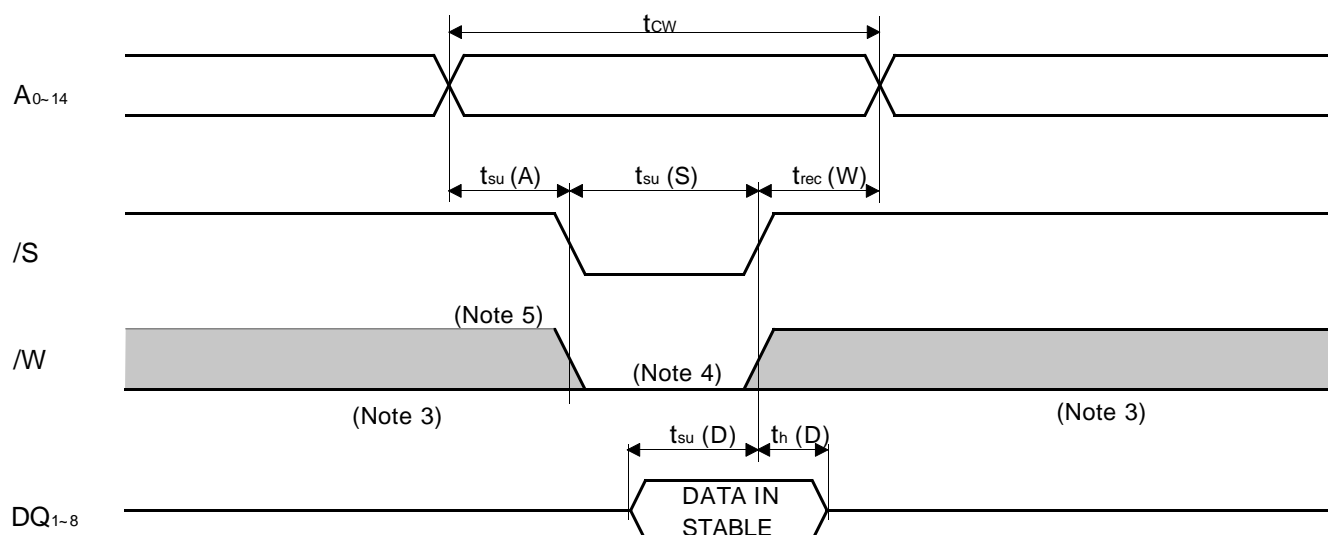
- t_{CW} : Write cycle time (from $/S$ setup to $/S$ hold).
- $t_{SU}(S)$: Setup time for $/S$ relative to $/W$.
- $t_{SU}(A-WH)$: Setup time for A_{0-14} relative to $/W$ hold.
- $t_{SU}(A)$: Setup time for A_{0-14} relative to $/W$ setup.
- $t_W(W)$: Write pulse width for $/W$.
- $t_{REC}(W)$: Recovery time for $/W$ after the write pulse.
- $t_{DIS}(W)$: Delay from $/W$ setup to data output disable.
- $t_{EN}(W)$: Delay from $/W$ hold to data output enable.
- $t_{EN}(OE)$: Delay from $/OE$ setup to data output enable.
- $t_{DIS}(OE)$: Delay from $/OE$ hold to data output disable.
- $t_{SU}(D)$: Setup time for DQ_{1-8} relative to $/W$ hold.
- $t_H(D)$: Hold time for DQ_{1-8} relative to $/W$ hold.

Notes:

- (Note 3) indicates that $/S$ and DQ_{1-8} are in a high-impedance state during the write cycle.
- The data bus DQ_{1-8} is labeled "DATA IN STABLE" during the write cycle.

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262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

Write cycle (/S control mode)**(4) MEASUREMENT CONDITIONS**

Limits1:Vcc=3.3±0.3V

Input pulse level $V_{IH}=2.4V, V_{IL}=0.4V$

Input rise and fall time 5ns

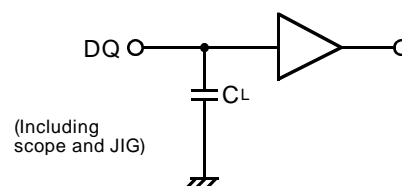
Reference level $V_{OH}=V_{OL}=1.5V$ Output load Fig.1, $CL=30pF$ $CL=5pF$ (for t_{en}, t_{dis})Transition is measured ±500mV from steady state voltage. (for t_{en}, t_{dis})

Fig.1 Output load

Limits2:Vcc=5.0±0.5V

Input pulse level $V_{IH}=2.4V, V_{IL}=0.6V$

Input rise and fall time 5ns

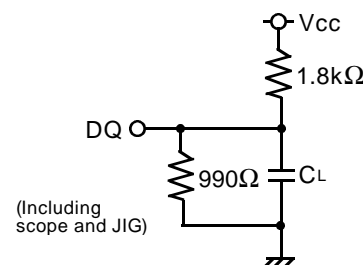
Reference level $V_{OH}=V_{OL}=1.5V$ Output load Fig.2, $CL=100pF$ $CL=5pF$ (for t_{en}, t_{dis})Transition is measured ±500mV from steady state voltage. (for t_{en}, t_{dis})

Fig.2 Output load

Note 3 : Hatching indicates the state is "don't care".

4 : Writing is executed in overlap of /S and /W low.

5 : If /W goes low simultaneously with or prior to /S, the outputs remain in the high impedance state.

6 : Don't apply inverted phase signal externally when DQ pin is output mode.

7 : t_{en}, t_{dis} are periodically sampled and are not 100% tested.

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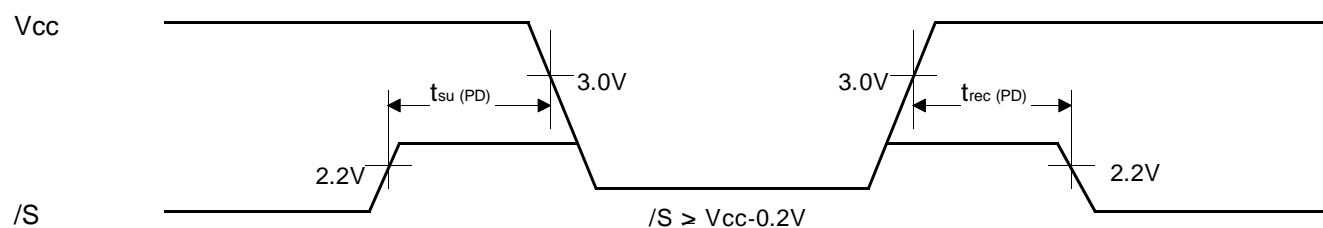
262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

POWER DOWN CHARACTERISTICS**(1) ELECTRICAL CHARACTERISTICS**

| Symbol | Parameter | Test conditions | | Limits | | | Unit | |
|----------------------|---------------------------|--|-------|--------|----------------------|------|------|----|
| | | | | Min | Typ | Max | | |
| V _{CC} (PD) | Power down supply voltage | | | 2 | | | V | |
| V _I (/S) | Chip select input /S | 2.2V ≤ V _{CC} (PD) | | 2.2 | | | V | |
| | | 2V≤ V _{CC} (PD) ≤ 2.2V | | | V _{CC} (PD) | | V | |
| I _{CC} (PD) | Power down supply current | V _{CC} = 3V,/S ≥ V _{CC} -0.2V, Other inputs=0~V _{CC} | ~25°C | -G,-GI | | | 1 | μA |
| | | | | -XG | | 0.05 | 0.2 | |
| | | | ~40°C | -G,-GI | | | 3 | |
| | | | | -XG | | | 0.6 | |
| | | | ~70°C | -G,-GI | | | 10 | |
| | | | | -XG | | | 2 | |
| ~85°C | -GI | | | 20 | | | | |

(2) TIMING REQUIREMENTS

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---------------|--------------------------|-----------------|--------|-----|-----|------|
| | | | Min | Typ | Max | |
| $t_{su(PD)}$ | Power down set up time | | 0 | | | ns |
| $t_{rec(PD)}$ | Power down recovery time | | tCR | | | ns |

(3) POWER DOWN CHARACTERISTICS**/S control mode**

M5M5256DFP,VP -70G,-70GI,-70XG

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

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