

M5M5258BP, J-15, -17, -20, -25, -35, -20L, -25L, -35L,

262144-BIT (65536-WORD BY 4-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5258B is a family of 65536 word by 4-bit static RAMs, fabricated with the high-performance CMOS silicongate MOS process and designed for high-speed application. These devices operate on a single 5V supply, and are directly TTL compatible. They include a power-down feature as well.

FEATURES

- Fast access time
 - M5M5258BP, J-15..... 15ns(max)
 - M5M5258BP, J-17..... 17ns(max)
 - M5M5258BP, J-20, 20L..... 20ns(max)
 - M5M5258BP, J-25, 25L..... 25ns(max)
 - M5M5258BP, J-35, 35L..... 35ns(max)
- Low power dissipation
 - Active..... 300mW(typ)
 - Stand by(-15, -17, -20, -25, -35)..... 5mW(typ)
 - Stand by(-20L, -25L, -35L)..... 50μW(typ)
- Power down by \bar{S}
- Single 5V power supply
- Fully static operation
- Requires neither external clock nor refreshing
- All inputs and outputs are directly TTL compatible
- Easy memory expansion by chip-select (\bar{S}) input
- All address inputs are changeable with each other

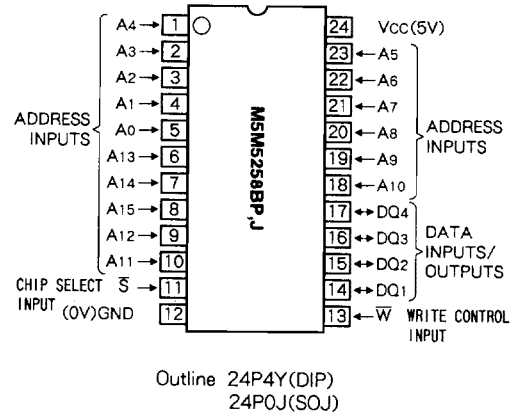
APPLICATION

High-speed memory systems

FUNCTION

A write operation is executed during the \bar{S} low and \bar{W} low overlap time. In this period, address signals must be stable. When \bar{W} is low, the DQ terminal is maintained in the high impedance state.

PIN CONFIGURATION (TOP VIEW)

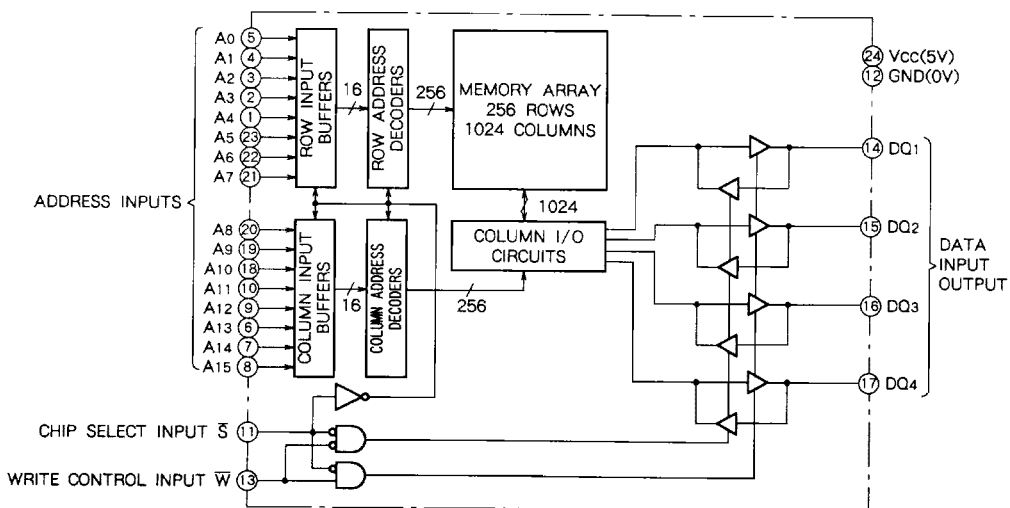


In a read operation, after setting \bar{W} to high, and \bar{S} to low if the address signals are stable, the data is available at the DQ terminal.

When \bar{S} is high, the chip is in the non-selectable state, disabling both reading and writing. In this case the output is in the floating (high-impedance) state, useful for OR-ties with other devices.

Signal \bar{S} controls the power-down feature. When \bar{S} goes high, power dissipation is reduced extremely. The access time from \bar{S} is equivalent to the address access time.

BLOCK DIAGRAM



M5M5258BP,J-15,-17,-20,-25,-35,-20L,-25L,-35L

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MODE SELECTION

\bar{S}	\bar{W}	Mode	Data I/O	I _{cc}
H	X	Non selection	High - impedance	Stand by
L	L	Write	D _{in}	Active
L	H	Read	D _{out}	Active

H : V_{IH} L : V_{IL} X : V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{cc}	Supply voltage	With respect to GND	- 3.5* ~ 7	V
V _I	Input voltage		- 3.5* ~ 7	V
V _O	Output voltage		- 3.5* ~ 7	V
P _d	Maximum power dissipation		1	W
T _{opr}	Operating temperature		0~70	°C
T _{stg(bias)}	Storage temperature(bias)		- 10~85	°C
T _{stg}	Storage temperature		- 65~150	°C

* Pulse width ≤ 20ns, In case of DC : - 0.5V

DC ELECTRICAL CHARACTERISTICS (Ta = 0~70 °C, V_{cc} = 5V ± 10 %, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V _{IH}	High-level input voltage		2.2		V _{cc} +0.3	V
V _{IL}	Low-level input voltage		- 0.5*		0.8	V
V _{OH}	High-level output voltage	I _{OH} = - 4mA	2.4			V
V _{OL}	Low-level output voltage	I _{OL} = 8mA			0.4	V
I _I	Input current	V _I = 0~V _{cc}			2	μA
I _{oz}	Off-state output current	V _{I(S)} = V _{IH} , V _O = 0~V _{cc}			10	μA
I _{cc1}	Supply current from V _{cc}	V _{I(S)} = V _{IL} Output open	AC(15, 17ns cycle)		130	mA
			AC(20,25,35ns cycle)		120	
			DC	70	85	
I _{cc2}	Stand by current	V _{I(S)} = V _{IH}	AC(15, 17ns cycle)		50	mA
			AC(20,25,35ns cycle)		40	
			Other V _I ≥ V _{IH} or ≤ V _{IL}		30	
I _{cc3}	Stand by current	V _{I(S)} = V _{cc} -0.2V Other V _I ≤ 0.2V or V _I ≥ V _{cc} -0.2V	-15,-17,-20,-25,-35	1	10	mA
			-20L, -25L, -35L	10	100	

Note 1. Current flow into an IC is positive, out is negative.

* - 3.0V in case of AC(Pulse width ≤ 20ns)

CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C _I	Input capacitance	V _I = GND, V _I = 25mVrms, f = 1MHz			5	pF
C _O	Output capacitance	V _O = GND, V _O = 25mVrms, f = 1MHz			7	pF

AC ELECTRICAL CHARACTERISTICS (Ta = 0~70 °C, V_{cc} = 5V ± 10 %, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse levels V_{IH} = 3V, V_{IL} = 0V

Input rise and fall time 3ns

Input timing reference levels V_{IH} = 2.4V, V_{IL} = 0.6V

Output timing reference levels ... V_{OH} = 2.0V, V_{OL} = 0.8V

Output loads Fig.1, Fig.2

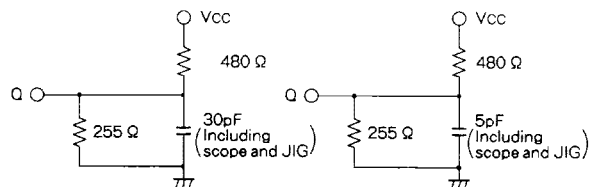


Fig.1 Output load

Fig. 2 Output load for t_{en}, t_{dis}

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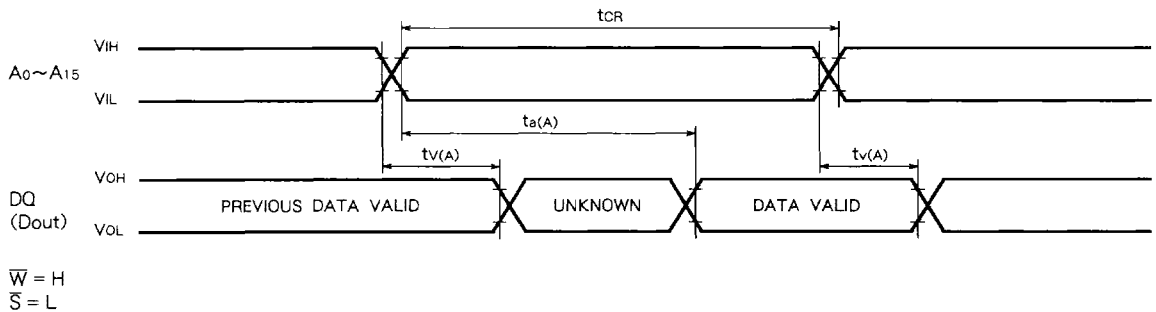
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(2) READ CYCLE

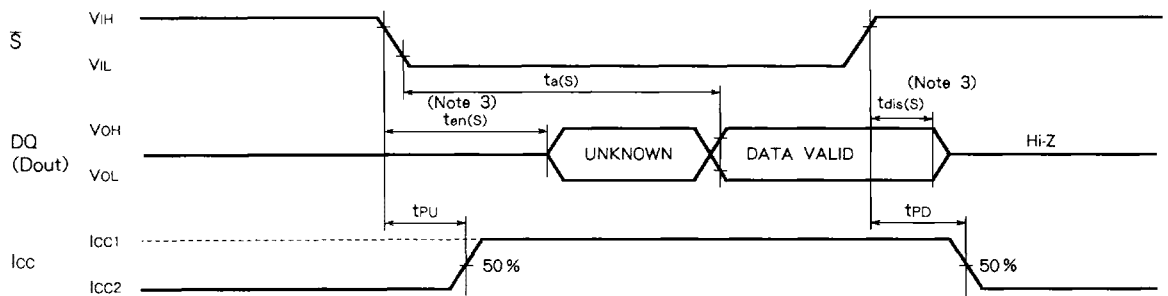
Symbol	Parameter	Limits										Unit
		M5M5258B-15		M5M5258B-17		M5M5258B-20, -20L		M5M5258B-25, -25L		M5M5258B-35, -35L		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t _{CR}	Read cycle time	15		17		20		25		35		ns
t _{a(A)}	Address access time		15		17		20		25		35	ns
t _{a(S)}	Chip select access time		15		17		20		25		35	ns
t _{v(A)}	Data valid time after address	3		3		3		5		5		ns
t _{en(S)}	Output enable time after chip selection	3		3		3		5		5		ns
t _{dis(S)}	Output disable time after chip deselection	0	7	0	7	0	8	0	10	0	10	ns
t _{PU}	Power-up time after chip selection	0		0		0		0		0		ns
t _{PD}	Power-down time after chip deselection		15		17		20		25		35	ns

(3) TIMING DIAGRAMS FOR READ CYCLE

Read cycle 1



Read cycle 2 (Note 2)



Note 2. Addresses valid prior to or coincident with \bar{S} transition low.

3. Transition is measured $\pm 500\text{mV}$ from steady state voltage with specified loading in Figure 2.

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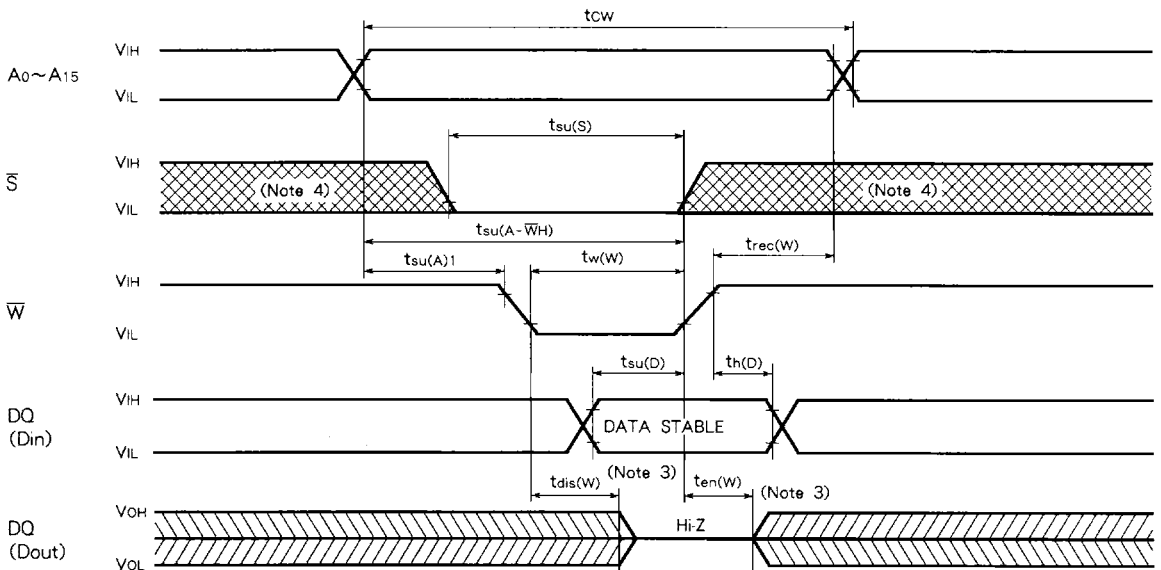
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(4) WRITE CYCLE

Symbol	Parameter	Limits										Unit
		M5M5258B-15		M5M5258B-17		M5M5258B-20, -20L		M5M5258B-25, -25L		M5M5258B-35, -35L		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t _{cw}	Write cycle time	15		17		20		25		35		ns
t _{su(S)}	Chip select setup time	12		13		15		20		30		ns
t _{su(A)1}	Address setup time(\overline{W})	0		0		0		0		0		ns
t _{su(A)2}	Address setup time(\overline{S})	0		0		0		0		0		ns
t _{w(W)}	Write pulse width	12		13		15		20		25		ns
t _{rec(W)}	Write recovery time	0		0		0		0		0		ns
t _{su(D)}	Data setup time	7		7		8		10		15		ns
t _{h(D)}	Data hold time	0		0		0		0		0		ns
t _{dis(W)}	Output disable time after \overline{W} low	0	7	0	7	0	8	0	10	0	10	ns
t _{en(W)}	Output enable time after \overline{W} high	0		0		0		0		0		ns
t _{su(A-\overline{W}H)}	Address to \overline{W} high	12		13		15		20		30		ns

(5) TIMING DIAGRAMS FOR WRITE CYCLE

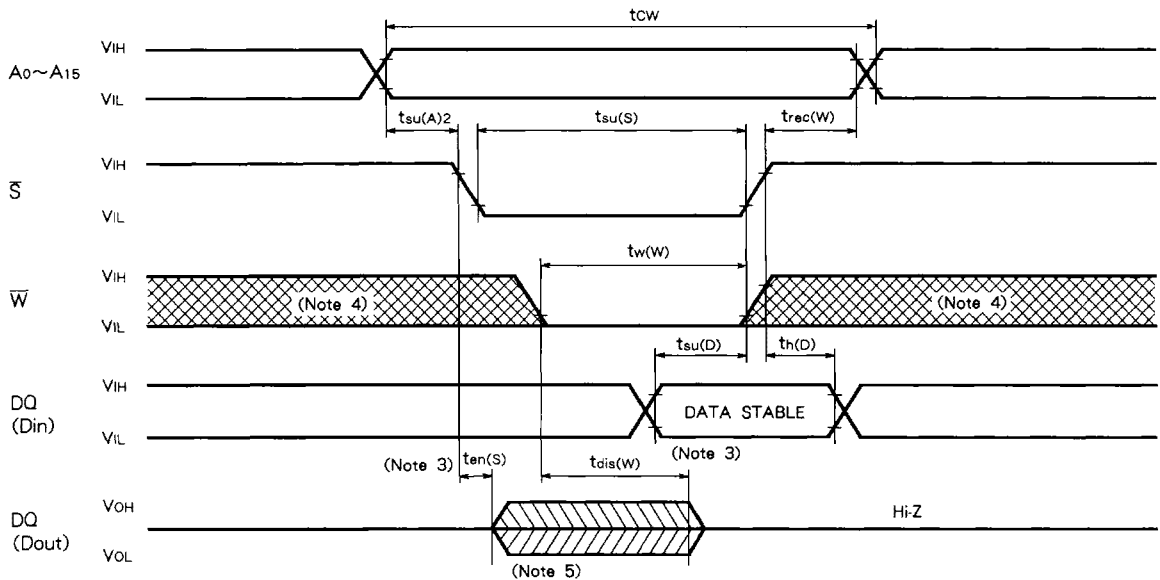
Write cycle 1 (\overline{W} control mode)



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Write cycle 2 (\bar{S} control mode)



Note 4. Hatching indicates the state is don't care.

5. When the falling edge of \bar{W} is simultaneous or prior to the falling edge of \bar{S} , the output is maintained in the high impedance.

POWER DOWN CHARACTERISTICS (Ta = 0~70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V _{CC(PD)}	Power down supply voltage		2			V
V _{I(S)}	Chip select input voltage		V _{CC} -0.2			V
t _{SU(PD)}	Power down setup time	V _{I(S)} ≥ V _{CC} - 0.2V V _I ≥ V _{CC} - 0.2V or 0V ≤ V _I ≤ 0.2V	0			ns
t _{REC(PD)}	Power down recovery time		-20L	20		ns
			-25L	25		
			-35L	35		
I _{CC(PD)}	Power down supply current	V _{CC} = 3.0V			50	μA
		V _{CC} = 5.5V			100	

Note 6. This is only M5M5258BP, J-20L, -25L, -35L.

TIMING WAVEFORM FOR POWER DOWN

