FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-11239-1E

MEMORY

4 M × 36 BIT HYPER PAGE MODE DRAM MODULE

MB8504E036AA-60/-70

4M × 36 BIT Hyper Page Mode DRAM Module, 5 V, 1-Bank

■ DESCRIPTION

The Fujitsu MB8504E036AA is a fully decoded, CMOS Dynamic Random Access Memory (DRAM) module consisting of eight MB8117405A and four MB814105C devices. The MB8504E036AA is optimized for those applications requiring high speed, high performance and large memory storage. The operation and electrical characteristics of the MB8504E036AA are the same as the MB8117405A which features hyper page mode operation providing extended valid time for data output and higher speed random access of upto 2,048-bit of data within the same row than the fast page mode. For ease of memory expansion, the MB8504E036AA is offered in a 72-pad Single In-line Memory Module package (SIMM).

■ PRODUCT LINE & FEATURES

Parameter		MB8504E036AA-60	MB8504E036AA-70
$\overline{RAS}$ Access Time		60 ns max.	70 ns max.
Random Cycle Time		104 ns min.	124 ns min.
Address Access Time		30 ns max.	35 ns max.
$\overline{CAS}$ Access Time		15 ns max.	20 ns max.
Hyper Page Mode Cycle Time		25 ns min.	30 ns min.
Power Dissipation	Operating Mode	5962 mW max.	5148 mW max.
	Standby Mode	66 mW (CMOS) / 132 mW (TTL)	

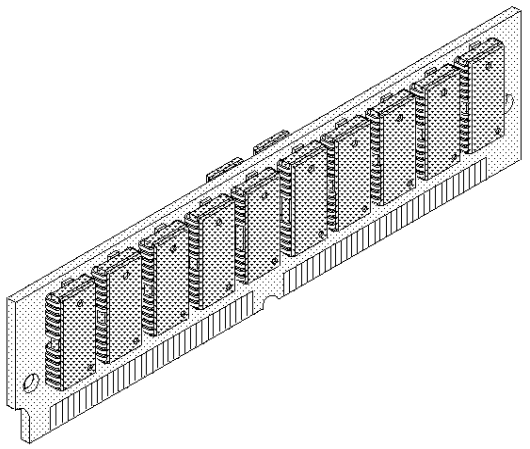
- Organization : 4,194,304 words × 36 bits
- Memory : MB8117405A, 8 pcs
  MB814105C, 4 pcs
- 5.0 V ± 10% Supply Voltage
- 2,048 Refresh Cycles / 32.8 ms
- Hyper page mode operation (EDO)
- Package and Ordering Information:
  72-pin SIMM, order as
  MB8504E036AA-xxSG
  (SG = Gold Pad)
  MB8504E036AA-xxSS
  (SS = Solder Pad)

■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{IN}	−0.5 to +7.0	V
Output Voltage	V_{OUT}	−0.5 to +7.0	V
Short Circuit Output Current	I_{OUT}	±50	mA
Power Dissipation	P_D	12	W
Storage Temperature	T_{STG}	−55 to +125	°C

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ PACKAGE

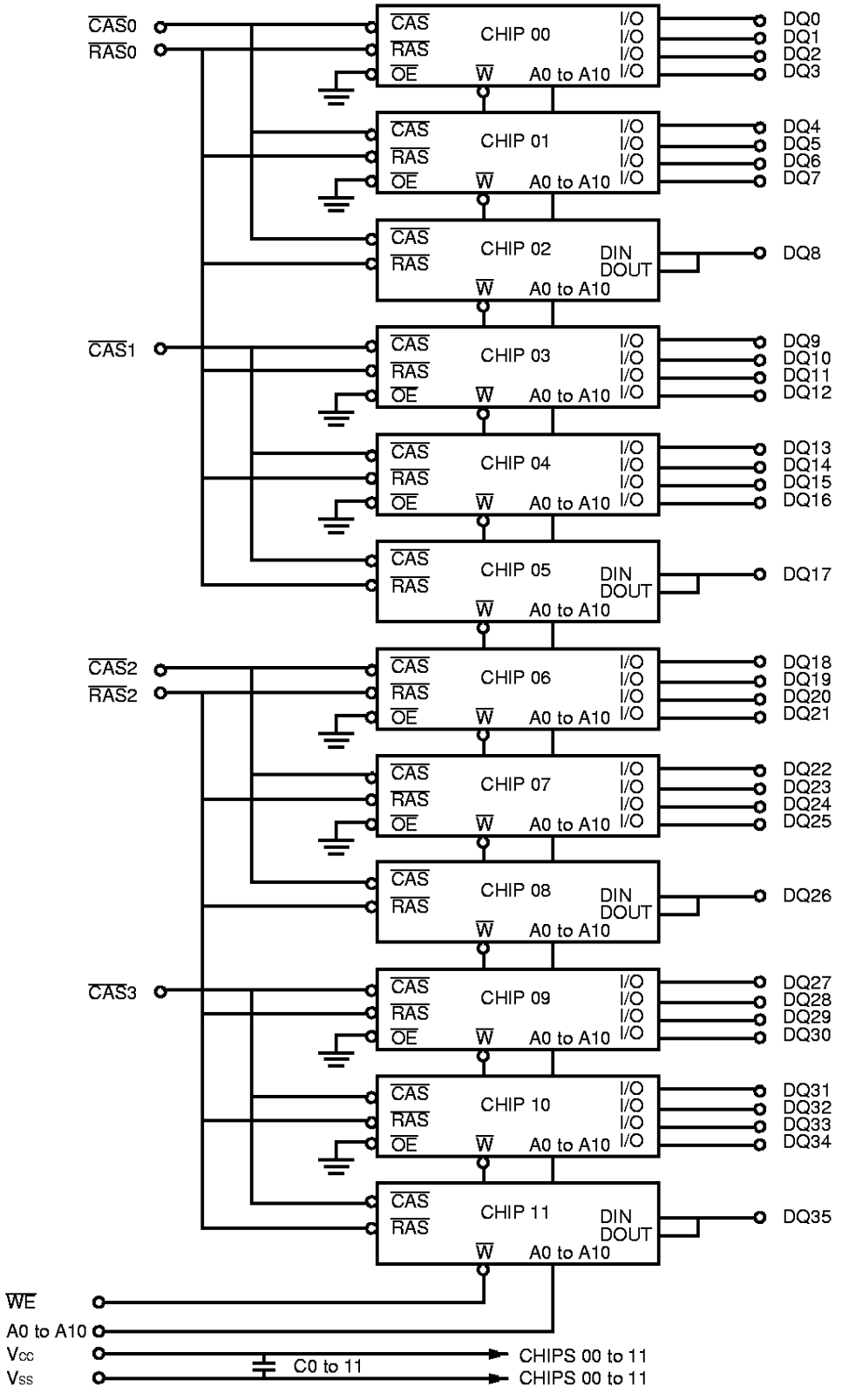


Plastic SIMM Package
(MSS-72P-P81)

		1	V_{SS}
DQ0	2	3	DQ18
DQ1	4	5	DQ19
DQ2	6	7	DQ20
DQ3	8	9	DQ21
V_{CC}	10	11	N.C.
A0	12	13	A1
A2	14	15	A3
A4	16	17	A5
A6	18	19	A10
DQ4	20	21	DQ22
DQ5	22	23	DQ23
DQ6	24	25	DQ24
DQ7	26	27	DQ25
A7	28	29	N.C.
V_{CC}	30	31	A8
A9	32	33	N.C.
$\overline{RAS2}$	34	35	DQ26
DQ8	36		
		37	DQ17
$\overline{DQ35}$	38	39	V_{SS}
$\overline{CAS0}$	40	41	$\overline{CAS2}$
$\overline{CAS3}$	42	43	$\overline{CAS1}$
$\overline{RAS0}$	44	45	N.C.
N.C.	46	47	$\overline{WE}$
N.C.	48	49	DQ9
DQ27	50	51	DQ10
DQ28	52	53	DQ11
DQ29	54	55	DQ12
DQ30	56	57	DQ13
DQ31	58	59	V_{CC}
DQ32	60	61	DQ14
DQ33	62	63	DQ15
DQ34	64	65	DQ16
N.C.	66	67	PD1
PD2	68	69	PD3
PD4	70	71	N.C.
V_{SS}	72		

Pin #	Symbol	-60	-70
67	PD1	V_{SS}	V_{SS}
68	PD2	N.C.	N.C.
69	PD3	N.C.	V_{SS}
70	PD4	N.C.	N.C.

FUNCTIONAL BLOCK DIAGRAM



■ RECOMMENDED OPERATING CONDITION

(Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	—	0	—	V
Input High Voltage, all inputs	V_{IH}	2.4	—	6.5	V
Input Low Voltage, all inputs*	V_{IL}	–0.3	—	0.8	V
Ambient Temperature	T_A	0	—	70	°C

* : Undershoots of up to –2.0 volts with a pulse width not exceeding 10 ns are acceptable

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

■ DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Notes		Symbol	Condition	Value		Unit
					Min.	Max.	
Output High Voltage	*1		V_{OH}	I_{OH} = –5.0 mA	2.4	—	V
Output Low Voltage	*1		V_{OL}	I_{OL} = 4.2 mA	—	0.4	V
Input Leakage Current		$\overline{RAS}$	$I_{I(L)}$	0 V ≤ V_{IN} ≤ V_{CC}, 4.5 V ≤ V_{CC} ≤ 5.5 V, V_{SS} = 0 V, All other pins not under test = 0 V	–40	40	µA
		$\overline{CAS}$			–30	30	
		Address, $\overline{WE}$			–80	80	
Output Leakage Current			$I_{O(L)}$	0 V ≤ V_{OUT} ≤ 5.5 V, Data out disabled	–20	20	µA
Operating Current (Average power supply current)	*2	MB8504E036AA-60	I_{CC1}	$\overline{RAS}$ & $\overline{CAS}$ cycling, t_{RC} = min	—	1084	mA
		MB8504E036AA-70			—	936	
Standby Current (Power supply current)		TTL Level	I_{CC2}	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH} $\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} –0.2 V	—	24	mA
		CMOS Level			—	12	
Refresh Current#1 (Average power supply current)	*2	MB8504E036AA-60	I_{CC3}	$\overline{CAS}$ = V_{IH}, $\overline{RAS}$ = cycling, t_{RC} = min	—	1084	mA
		MB8504E036AA-70			—	936	
Hyper Page Mode Current	*2	MB8504E036AA-60	I_{CC4}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = cycling, t_{HPC} = min	—	984	mA
		MB8504E036AA-70			—	860	
Refresh Current#2 (Average power supply current)	*2	MB8504E036AA-60	I_{CC5}	$\overline{RAS}$ cycling, $\overline{CAS}$-before-$\overline{RAS}$, t_{RC} = min	—	1036	mA
		MB8504E036AA-70			—	896	

Notes: *1. Referenced to V_{SS}.

*2. I_{CC} depends on the output load conditions and cycle rate. The specific values are obtained with the output open.
I_{CC} depends on the number of address change as $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}, V_{IL} > –0.3 V.
I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} are specified at one time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
I_{CC2} is specified during $\overline{RAS}$ = V_{IH} and V_{IL} > –0.3 V.

■ CAPACITANCE (T_A = 25°C, f = 1 MHz, V_{CC} = 5.0 V)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance, A0 to A10	C_{IN1}	—	85	pF
Input Capacitance, $\overline{RAS}$0 and $\overline{RAS}$2	C_{IN2}	—	46	pF
Input Capacitance, $\overline{CAS}$0 to $\overline{CAS}$3	C_{IN3}	—	27	pF
Input Capacitance, $\overline{WE}$	C_{IN4}	—	83	pF
I/O Capacitance, (DQ0-7, DQ9-16, DQ18-25, DQ27-34)	C_{DQ1}	—	12	pF
I/O Capacitance, (DQ8, DQ17, DQ26, DQ35)	C_{DQ2}	—	13	pF

■ AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

No.	Parameter	Notes	Symbol	MB8504E036EAA-60		MB8504E036EAA-70		Unit
				Min.	Max.	Min.	Max.	
1	Time Between Refresh		t_{REF}	—	32.8	—	32.8	ms
2	Random Read/Write Cycle Time		t_{RC}	104	—	124	—	ns
3	Access Time from $\overline{RAS}$	*4,7	t_{RAC}	—	60	—	70	ns
4	Access Time from $\overline{CAS}$	*5,7	t_{CAC}	—	15	—	20	ns
5	Column Address Access Time	*6,7	t_{AA}	—	30	—	35	ns
6	Output Hold Time		t_{OH}	5	—	5	—	ns
7	Output Hold Time from $\overline{CAS}$		t_{CHC}	5	—	5	—	ns
8	Output Buffer Turn On Delay Time		t_{ON}	0	—	0	—	ns
9	Output Buffer Turn Off Delay Time	*8	t_{OFF}	—	15	—	17	ns
10	Output Buffer Turn Off Delay Time from $\overline{RAS}$	*8	t_{OFR}	—	15	—	17	ns
11	Output Buffer Turn Off Delay Time from $\overline{WE}$	*8	t_{WEZ}	—	15	—	17	ns
12	Transition Time		t_T	1	50	1	50	ns
13	$\overline{RAS}$ Precharge Time		t_{RP}	40	—	50	—	ns
14	$\overline{RAS}$ Pulse Width		t_{RAS}	60	100000	70	100000	ns
15	$\overline{RAS}$ Hold Time		t_{RSH}	15	—	20	—	ns
16	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	5	—	5	—	ns
17	$\overline{CAS}$ to $\overline{RAS}$ Delay Time	*9,10	t_{RCD}	14	45	14	53	ns
18	$\overline{CAS}$ Pulse Width		t_{CAS}	10	—	13	—	ns
19	$\overline{CAS}$ Hold Time		t_{CSH}	40	—	50	—	ns
20	$\overline{CAS}$ Precharge Time (Normal)	*15	t_{CPN}	10	—	10	—	ns
21	Row Address Set Up Time		t_{RSR}	0	—	0	—	ns
22	Row Address Hold Time		t_{RAH}	10	—	10	—	ns
23	Column Address Set Up Time		t_{ASC}	0	—	0	—	ns
24	Column Address Hold Time		t_{CAH}	10	—	10	—	ns
25	Column Address Hold Time from $\overline{RAS}$		t_{AR}	24	—	24	—	ns
26	$\overline{RAS}$ to Column Address Delay Time	*11	t_{RAD}	12	30	12	35	ns
27	Column Address to $\overline{RAS}$ Lead Time		t_{PAL}	30	—	35	—	ns
28	Column Address to $\overline{CAS}$ Lead Time		t_{CAL}	23	—	28	—	ns
29	Read Command Set Up Time		t_{RCS}	0	—	0	—	ns
30	Read Command Hold Time Referenced to $\overline{RAS}$	*12	t_{RRH}	0	—	0	—	ns
31	Read Command Hold Time Referenced to $\overline{CAS}$	*12	t_{RCH}	0		0	—	ns

(Continued)

(Continued)

No.	Parameter	Notes	Symbol	MB8504E036EAA-60		MB8504E036EAA-70		Unit
				Min.	Max.	Min.	Max.	
32	Write Command Set Up Time	*13	t_{WCS}	0	—	0	—	ns
33	Write Command Hold Time		t_{WCH}	10	—	10	—	ns
34	Write Command Hold Time from $\overline{RAS}$		t_{WCR}	24	—	24	—	ns
35	$\overline{WE}$ Pulse Width		t_{WP}	10	—	10	—	ns
36	Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	15	—	18	—	ns
37	Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	10	—	13	—	ns
38	DIN Set Up Time		t_{DS}	0	—	0	—	ns
39	DIN Hold Time		t_{DH}	10	—	10	—	ns
40	Date Hold Time from $\overline{RAS}$		t_{DHR}	24	—	24	—	ns
41	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh Cycles)		t_{RPC}	5		5	—	ns
42	$\overline{CAS}$ Set Up Time (C-B-R Refresh)		t_{CSR}	0	—	0	—	ns
43	$\overline{CAS}$ Hold Time (C-B-R Refresh)		t_{CHR}	10	—	12	—	ns
44	$\overline{WE}$ Set Up Time from $\overline{RAS}$	*16	t_{WSR}	0	—	0	—	ns
45	$\overline{WE}$ Hold Time from $\overline{RAS}$	*16	t_{WHR}	10	—	10	—	ns
46	$\overline{RAS}$ to Data In Delay Time		t_{RDD}	15	—	17	—	ns
47	$\overline{CAS}$ to Data In Delay Time		t_{CDD}	15	—	17	—	ns
48	DIN to $\overline{CAS}$ Delay Time		t_{DZC}	0	—	0	—	ns
49	$\overline{WE}$ Precharge Time		t_{WPZ}	8	—	8	—	ns
50	$\overline{WE}$ to Data In Delay Time		t_{WED}	15	—	17	—	ns
51	Hyper Page Mode $\overline{RAS}$ Pulse Width		t_{RASP}	—	100000	—	100000	ns
52	Hyper Page Mode Read/Write Cycle Time		t_{HPC}	25	—	30	—	ns
53	Access Time from $\overline{CAS}$ Precharge	*7,14	t_{CPA}	—	35	—	40	ns
54	Hyper Page Mode $\overline{CAS}$ Precharge Time		t_{CP}	10	—	10	—	ns
55	Hyper Page Mode $\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge		t_{RHCP}	35	—	40	—	ns

Notes: *1. An initial pause ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH}) of 200 µs is required after power-up followed by any eight $\overline{RAS}$ -only cycles before proper device operation is achieved. If an internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles are required instead of eight $\overline{RAS}$ cycles.

*2. AC characteristics assume t_T = 5 ns.

*3. V_{IH} (min) and V_{IL} (max) are reference levels for measureing the timing of input signals. Transition times are measured between V_{IH} (min) and V_{IL} (max).

*4. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown.

*5. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.

*6. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.

*7. Measured with a load equivalent to two TTL loads and 100 pF.

*8. t_{OFF}, t_{OFR} and t_{WEZ} are specified that output buffer change to high impedance state.

*9. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.

*10. t_{RCD} (min) = t_{RAH} (min)+ 2 t_T + t_{ASC} (min).

*11. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.

*12. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

*13. t_{WCS} is specified as a reference point only. If $t_{WCS} \geq t_{WCS}$ (min) the data output pin will remain High-Z state through entire cycle.

*14. t_{CPA} is access time from the selection of a new column address (caused by changing $\overline{CAS}$ from "L" to "H"). Therefore, if t_{CP} become long, t_{CPA} also become longer than t_{CPA} (max).

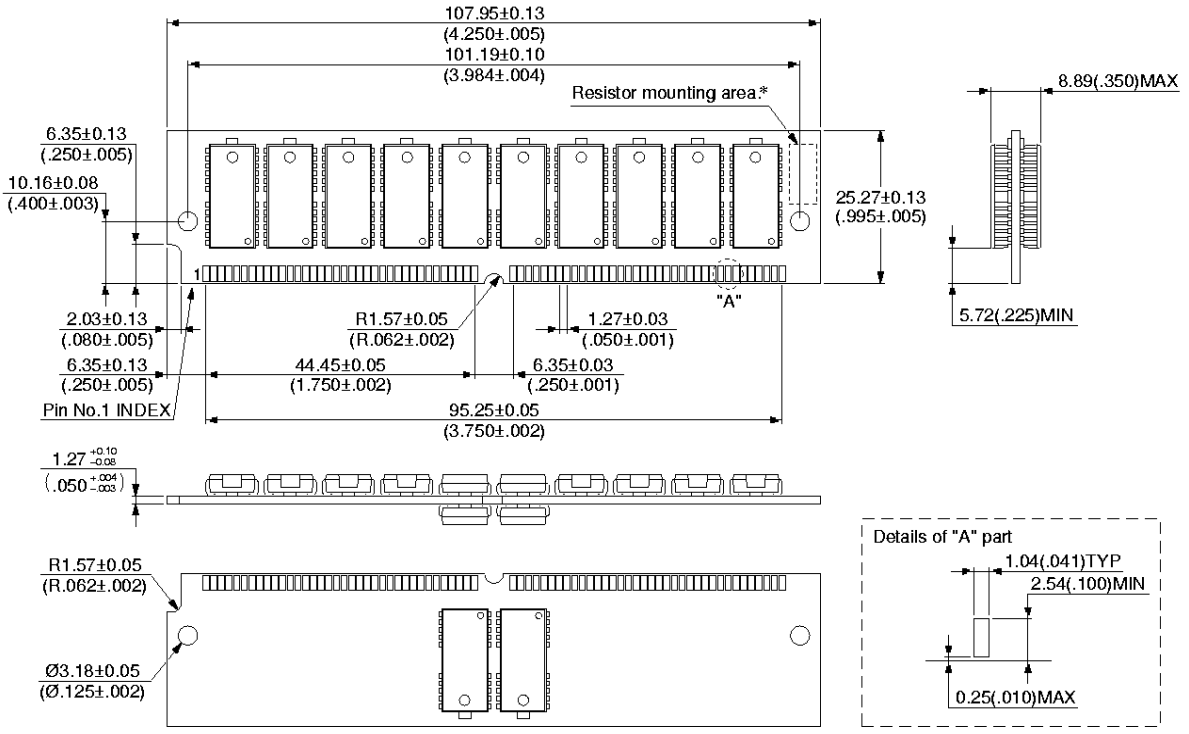
*15. Assumes that $\overline{CAS}$-before-$\overline{RAS}$ refresh.

*16. Assumes that test mode function.

*Source: See MB8117405A Data Sheet for details on the electricals.

■ PACKAGE DIMENSIONS

72-PAD PLASTIC SINGLE IN-LINE TYPE MODULE
(CASE No.: MSS-72P-P81)



Dimension in mm (inches)

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