# SPT5450

## 14-BIT, 160 MWPS D/A CONVERTER

## ADVANCE INFORMATION

### FEATURES

- 14-bit, 160 MWPS digital-to-analog converter
- +2.7 V to +5.5 V operation for digital supplies
- High wideband spurious free dynamic range
- Low glitch impulse 5 pV-s
- Low power: 100 mW @ +3.0 V digital supply
- Internal voltage reference
- Powerdown mode

### APPLICATIONS

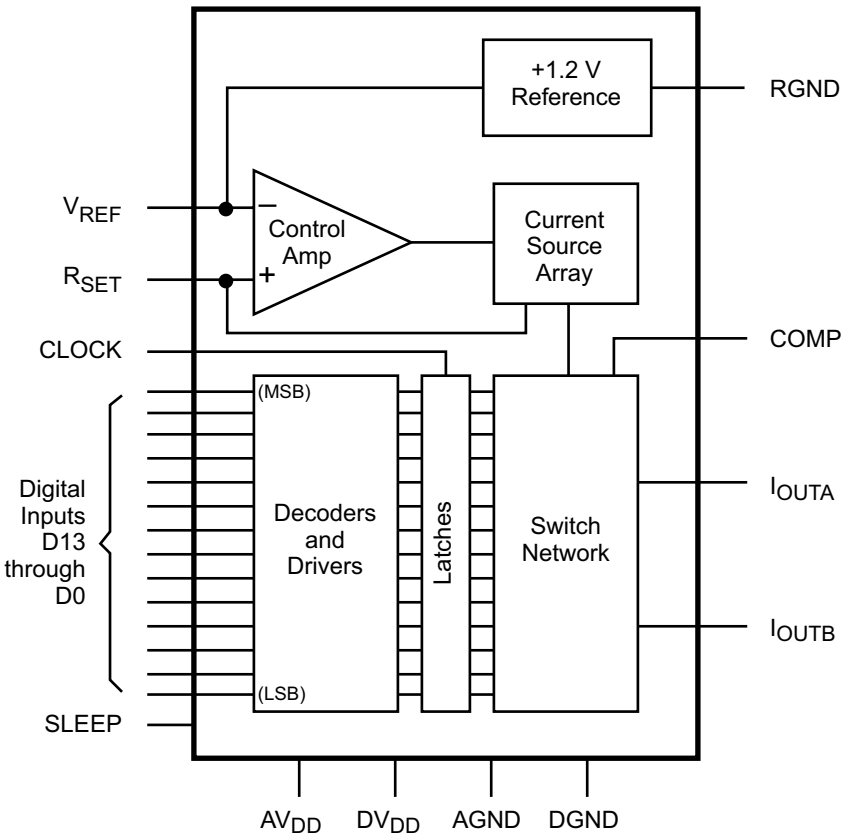
- Broadband modems
- Wireless local loops
- Cellular and PCS basestations
- Head-end broadcast video transmission systems
- Professional broadcast video equipment
- Communications test equipment
- Direct digital synthesis

### DESCRIPTION

The SPT5450 is a 14-bit, 160 MWPS digital-to-analog converter designed primarily for RF communications and instrumentation applications. It provides excellent spurious performance operation at the lowest possible cost. The digital power supply can range from +2.7 V to +5.5 V.

The SPT5450 operates at an industrial temperature range of –40 °C to +85 °C and is available in 28-lead SOIC or SSOP-equivalent packages.

### BLOCK DIAGRAM





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## ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

**Supply Voltages**

$AV_{DD}$ ..... –0.3 V to +6.5 V
$DV_{DD}$ ..... –0.3 V to +6.5 V
AGND, DGND, RGND ..... –0.3 V to +0.3 V
AGND – DGND ..... ±300 mV

**Input Voltages**

Digital Inputs ..... –0.3 V to $DV_{DD}$ + 0.3 V
$V_{REF}$, $R_{SET}$ ..... –0.3 V to $AV_{DD}$ + 0.3 V
COMP ..... –0.3 V to $AV_{DD}$ + 0.3 V

**Output**

$I_{OUTA}$, $I_{OUTB}$ Current ..... 15 mA
$I_{OUTA}$, $I_{OUTB}$ Voltage ..... –1.0 to $AV_{DD}$ + 0.3 V

**Temperature**

Operating Temperature ..... –40 to +85 °C
Junction Temperature ..... +175 °C
Lead Temperature, (soldering 10 seconds) ..... +300 °C
Storage Temperature ..... –65 to +150 °C

Note 1: Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

## ELECTRICAL SPECIFICATIONS

$T_A$=$T_{MIN}$ to $T_{MAX}$, $AV_{DD}$=$DV_{DD}$=+5.0 V, unless otherwise specified.

| PARAMETERS | TEST CONDITIONS | TEST LEVEL | SPT5450 MIN | SPT5450 TYP | SPT5450 MAX | UNITS |
|---|---|---|---|---|---|---|
| **DC Performance** | | | | | | |
| Resolution | | | | 14 | | Bits |
| Differential Linearity | 25 °C | | | ±2.0 | | LSB |
| Differential Linearity | Full Temp. | | | ±4.0 | | LSB |
| Integral Linearity | 25 °C | | | ±2.0 | | LSB |
| Integral Linearity | Full Temp. | | | ±4.0 | | LSB |
| Offset Error | | | | | ±0.025 | % FS |
| Gain Error (without internal reference) | | | | ±2 | ±10 | % FS |
| Gain Error (with internal reference) | | | | ±1 | ±10 | % FS |
| Full-Scale Output Current | | | | 20.48 | | mA |
| Output Compliance Voltage | | | –1.0 | | +1.25 | V |
| Equivalent Output Resistance | | | | >100 | | kΩ |
| Gain Error Tempco | | | | tbd | | PPM/°C |
| Zero-Scale Offset Error | | | | | ±0.025 | % FS |
| Output Capacitance | | | | 5 | | pF |
| Offset Drift | | | | tbd | | ppm FS/°C |
| Gain Drift (without internal reference) | | | | ±50 | | ppm FS/°C |
| Gain Drift (with internal reference) | | | | ±100 | | ppm FS/°C |
| **Dynamic Performance** | | | | | | |
| Maximum Output Update Rate | | | | 160 | | MWPS |
| Output Settling Time (to 0.1%) | | | | 25 | 35 | ns |
| Output Propagation Delay | | | | tbd | | ns |
| Glitch Impulse | | | | 5 | | pV-s |
| Output Rise Time (10% to 90%) | | | | tbd | | ns |
| Output Fall Time (10% to 90%) | | | | tbd | | ns |
| Output Noise ($I_{OUTFS}$ = 10 mA) | | | | 25 | 50 | pA/√Hz |
| Spurious Free Dynamic Range to Nyquist | | | | | | |
| $f_{CLK}$ = 50 MHz; $f_{OUT}$ = 20 MHz | | | | 67 | | dBc |
| $f_{CLK}$ = 100 MHz; $f_{OUT}$ = 20 MHz | | | | 67 | | dBc |
| $f_{CLK}$ = 160 MHz; $f_{OUT}$ = 20 MHz | | | | 63 | | dBc |
| Spurious Free Dynamic Range within a Window | | | | | | |
| $f_{CLK}$ = 50 MHz; $f_{OUT}$ = 5 MHz; 2 MHz Span | | | | 86 | | dBc |
| $f_{CLK}$ = 100 MHz; $f_{OUT}$ = 5 MHz; 4 MHz Span | | | | 86 | | dBc |
| Multitone Power Ratio (8 Tones at 110 kHz Spacing) | | | | | | |
| $f_{CLK}$ = 20 MHz; $f_{OUT}$ = 2.00 to 2.99 MHz | | | | 75 | | dBc |

## ELECTRICAL SPECIFICATIONS

$T_A$=$T_{MIN}$ to $T_{MAX}$, $AV_{DD}$=$DV_{DD}$=+5.0 V, unless otherwise specified.

| PARAMETERS | TEST CONDITIONS | TEST LEVEL | SPT5450 MIN | SPT5450 TYP | SPT5450 MAX | UNITS |
|---|---|---|---|---|---|---|
| **Power Supply Requirements** | | | | | | |
| Analog Supply Voltage $AV_{DD}$ | | | 4.5 | | 5.5 | V |
| Digital Supply Voltage $DV_{DD}$ | | | 2.7 | | 5.5 | V |
| Analog Supply Current | | | | tbd | tbd | mA |
| Digital Supply Current | | | | tbd | tbd | mA |
| Supply Current Sleep Mode | | | | tbd | 5 | mA |
| Power Dissipation | | | | | | |
| At +3 V Supplies and 10 mA Current Output | | | | 100 | | mW |
| At +5 V Supplies and 10 mA Current Output | | | | 300 | | mW |
| Power Supply Rejection Ratio ($AV_{DD}$) | | | | ±0.02 | ±0.2 | %FS/V |
| Power Supply Rejection Ratio ($DV_{DD}$) | | | | ±0.002 | ±0.025 | %FS/V |
| **Reference** | | | | | | |
| Reference Voltage | | | | 1.20 | | V |
| Reference Output Current | | | | tbd | | |
| Reference Input Compliance Range | | | 0.1 | | 1.25 | V |
| Small Signal Bandwidth | | | | tbd | | MHz |
| Reference Voltage Drift | | | | ±50 | | ppm/°C |
| **Digital Inputs** | | | | | | |
| Logic “1” Voltage ($DV_{DD}$ = +3 V) | | | 2.1 | | | V |
| Logic “0” Voltage ($DV_{DD}$ = +3 V) | | | | | 0.9 | V |
| Logic “1” Voltage ($DV_{DD}$ = +5 V) | | | 3.5 | | | V |
| Logic “0” Voltage ($DV_{DD}$ = +5 V) | | | | | 1.3 | V |
| Logic “1” Current | | | –10 | | +10 | µA |
| Logic “0” Current | | | –10 | | +10 | µA |
| Input Capacitance | | | | 3 | 5 | pF |
| Input Setup Time – $t_S$ | | | 2 | <1 | | ns |
| Input Hold Time – $t_H$ | | | 2 | <1 | | ns |
| Latch Pulse Width – $t_{LPW}$ | | | tbd | | | ns |

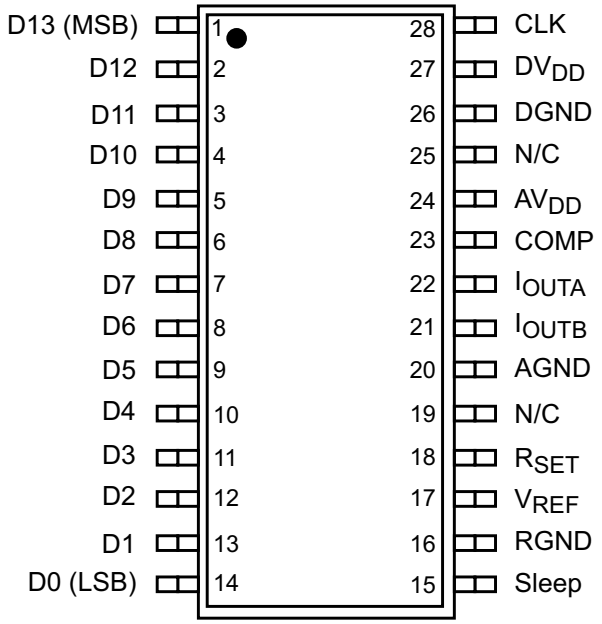
### TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

| TEST LEVEL | TEST PROCEDURE |
|---|---|
| I | 100% production tested at the specified temperature. |
| II | 100% production tested at $T_A$ = +25 °C, and sample tested at the specified temperatures. |
| III | QA sample tested only at the specified temperatures. |
| IV | Parameter is guaranteed (but not tested) by design and characterization data. |
| V | Parameter is a typical value for information purposes only. |
| VI | 100% production tested at $T_A$ = +25 °C. Parameter is guaranteed over specified temperature range. |

## PIN ASSIGNMENTS




## PIN FUNCTIONS

| Name | Function |
|---|---|
| **ANALOG OUTPUTS** | |
| $I_{OUTA}$ | DAC current output. |
| $I_{OUTB}$ | Complementary current output. |
| **DIGITAL INPUTS** | |
| D0–D13 | Digital Inputs (D0 is the LSB) |
| Sleep | Sleep mode pin. Active high. Contains active pull-down resistor. |
| CLK | Clock input pin. Data is latched on the rising edge. |
| **REFERENCE & COMPENSATION** | |
| RGND | Reference ground when using internal 1.2 V reference. Connect to $AV_{DD}$ to disable internal reference. |
| $V_{REF}$ | Reference input/output. Serves as an input when internal reference is disabled. Serves as a 1.2 V reference output when internal reference is enabled. Requires a 0.1 µF capacitor tied to AGND when internal reference is enabled. |
| $R_{SET}$ | Full-scale current output adjustment. |
| COMP | Internal bias node for switch driver circuitry. Use 0.1 µF capacitor tied to AGND. |
| **POWER** | |
| AGND | Analog Supply Return. |
| DGND | Digital Supply Return. |
| $AV_{DD}$ | Analog +4.5 to +5.5 V supply. |
| $DV_{DD}$ | Digital +2.7 to +5.5 V supply. |
| N/C | No connect. |

## ORDERING INFORMATION

| PART NUMBER | TEMPERATURE RANGE | PACKAGE |
|---|---|---|
| SPT5450SIS | –40 °C to +85 °C | 28L SOIC |
| SPT5450SIR | –40 °C to +85 °C | 28L SSOP Equivalent |