V59C1512(404/804/164)QC
HIGH PERFORMANCE 512 Mbit DDR2 SDRAM
4 BANKS X 32Mbit X 4 (404)
4 BANKS X 16Mbit X 8 (804)
4 BANKS X 8Mbit X 16 (164)

	5	37	3	25A	25	19
	DDR2-400	DDR2-533	DDR2-667	DDR2-800	DDR2-800	DDR2-1066
Clock Cycle Time (t_{CK3})	5ns	5ns	5ns	5ns	5ns	5ns
Clock Cycle Time (t_{CK4})	5ns	3.75ns	3.75ns	3.75ns	3.75ns	3.75ns
Clock Cycle Time (t_{CK5})	5ns	3.75ns	3ns	3ns	2.5ns	2.5ns
Clock Cycle Time (t_{CK6})	5ns	3.75ns	3ns	2.5ns	2.5ns	1.87ns
System Frequency ($f_{CK\ max}$)	200 MHz	266 MHz	333 MHz	400 MHz	400 MHz	533 MHz

Features

- High speed data transfer rates with system frequency up to 533MHz
- Posted CAS
- Programmable $\overline{\text{CAS}}$ Latency: 3, 4, 5 and 6
- Programmable Additive Latency:0, 1, 2, 3, 4 and 5
- Write Latency=Read Latency-1
- Programmable Wrap Sequence: Sequential or Interleave
- Programmable Burst Length: 4 and 8
  Automatic and Controlled Precharge Command
- Power Down Mode
- Auto Refresh and Self Refresh
- Refresh Interval: 7.8 us (8192 cycles/64 ms)
- OCD (Off-Chip Driver Impendance Adjustment)
- ODT (On-Die Termination)
- Weak Strength Data-Output Driver Option
- Bidirectional differential Data Strobe (Single-ended data-strobe is an optional feature)
- On-Chip DLL aligns DQ and DQs transitions with CK transitions
- Differential clock inputs CK and $\overline{\text{CK}}$
- JEDEC Power Supply 1.8V ± 0.1V
- VDDQ=1.8V ± 0.1V
- Available in 60-ball FBGA for x4 and x8 component or 84 ball FBGA for x16 component
- PASR Partial Array Self Refresh
- All inputs & outputs are compatible with SSTL_18 interface
- tRAS lockout supported
- Read Data Strobe supported (x8 only)
- Internal four bank operations with single pulsed RAS

Description

The V59C1512(404/804/164)QC is a four bank DDR DRAM organized as 4 banks x 32Mbit x 4 (404), 4 banks x 16Mbit x 8 (804), or 4 banks x 8Mbit x 16 (164). The V59C1512(404/804/164)QC achieves high speed data transfer rates by employing a chip architecture that prefetches multiple bits and then synchronizes the output data to a system clock.

The chip is designed to comply with the following key DDR2 SDRAM features:(1) posted CAS with additive latency, (2)write latency=read latency-1, (3)Off-chip Driver(OCD) impedance adjustment, (4) On Die Termination.

All of the control, address, circuits are synchronized with the positive edge of an externally supplied clock. I/O s are synchronized with a pair of bidirectional strobes (DQS, $\overline{\text{DQS}}$) in a source synchronous fashion.

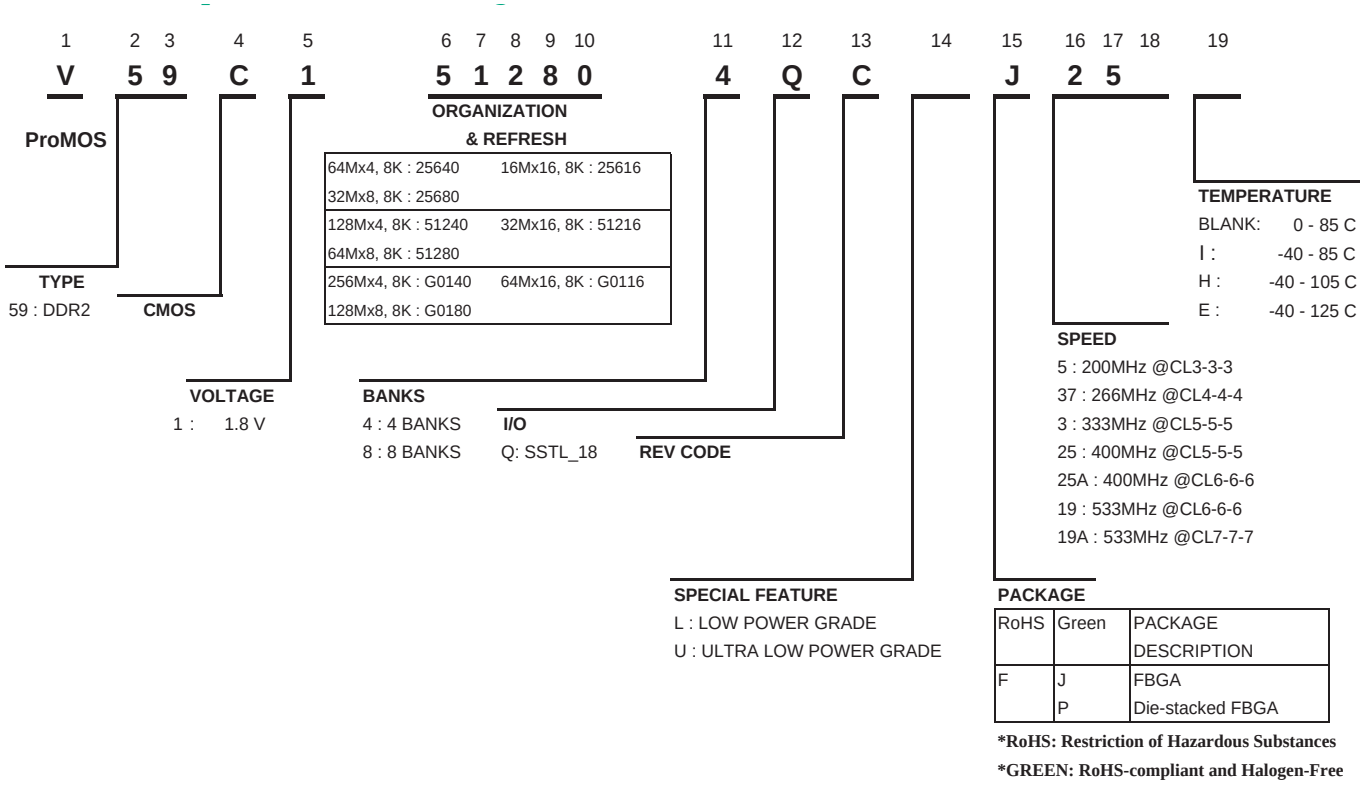
Operating the four memory banks in an interleaved fashion allows random access operation to occur at a higher rate than is possible with standard DRAMs. A sequential and gapless data rate is possible depending on burst length, CAS latency and speed grade of the device.

Available Speed Grade:
-5 (DDR2-400) @ CL 3-3-3
-37 (DDR2-533) @ CL 4-4-4
-3 (DDR2-667) @ CL 5-5-5
-25A (DDR2-800) @ CL 6-6-6
-25 (DDR2-800) @ CL 5-5-5
-19(DDR2-1066)@CL 6-6-6

Device Usage Chart

Operating Temperature Range	Package Outline	CK Cycle Time (ns)						Power		Temperature Mark
	60 ball FBGA 84 ball FBGA	-5	-37	-3	-25A	-25	-19	Std.	L	
0°C to 85°C	•	•	•	•	•	•	•	•	•	Blank

DDR Part Number



***RoHS: Restriction of Hazardous Substances**

***GREEN: RoHS-compliant and Halogen-Free**

512Mb Addressing

Configuration	128Mb x4	64Mb x 8	32Mb x16
# of Bank	4	4	4
Bank Address	BA0,BA1	BA0,BA1	BA0,BA1
Auto precharge	A_{10}/AP	A_{10}/AP	A_{10}/AP
Row Address	A_0 ~ A_{13}	A_0 ~ A_{13}	A_0 ~ A_{12}
Column Address	A_0 ~ A_9,A_{11}	A_0 ~ A_9	A_0 ~ A_9

x4 package pinout (Top View) : 60ball FBGA Package

1	2	3		7	8	9
VDD	NC	VSS	A	VSSQ	$\overline{DQS}$	VDDQ
NC	VSSQ	DM	B	DQS	VSSQ	NC
VDDQ	DQ1	VDDQ	C	VDDQ	DQ0	VDDQ
NC	VSSQ	DQ3	D	DQ2	VSSQ	NC
VDDL	VREF	VSS	E	VSSDL	CK	VDD
	CKE	$\overline{WE}$	F	$\overline{RAS}$	$\overline{CK}$	ODT
NC	BA0	BA1	G	$\overline{CAS}$	$\overline{CS}$	
	A10	A1	H	A2	A0	VDD
VSS	A3	A5	J	A6	A4	
	A7	A9	K	A11	A8	VSS
VDD	A12	NC	L	NC	A13	

Notes:
B1, B9, D1, D9 = NC for x4 organization.
Pins B3 has identical capacitance as pins B7.
VDDL and VSSDL are power and ground for the DLL. It is recommended that they are isolated on the device from VDD, VDDQ, VSS, and VSSQ.

Ball Locations (x4)

● : Populated Ball
+ : Depopulated Ball

Top View (See the balls through the Package)

	1	2	3	4	5	6	7	8	9
A	●	●	●	+	+	+	●	●	●
B	●	●	●	+	+	+	●	●	●
C	●	●	●	+	+	+	●	●	●
D	●	●	●	+	+	+	●	●	●
E	●	●	●	+	+	+	●	●	●
F	+	●	●	+	+	+	●	●	●
G	●	●	●	+	+	+	●	●	+
H	+	●	●	+	+	+	●	●	●
J	●	●	●	+	+	+	●	●	+
K	+	●	●	+	+	+	●	●	●
L	●	●	●	+	+	+	●	●	+

x8 package pinout (Top View) : 60ball FBGA Package

1	2	3		7	8	9
VDD	NU/ RDQS	VSS	A	VSSQ	DQS	VDDQ
DQ6	VSSQ	DM/ RDQS	B	DQS	VSSQ	DQ7
VDDQ	DQ1	VDDQ	C	VDDQ	DQ0	VDDQ
DQ4	VSSQ	DQ3	D	DQ2	VSSQ	DQ5
VDDL	VREF	VSS	E	VSSDL	CK	VDD
	CKE	WE	F	RAS	CK	ODT
NC	BA0	BA1	G	CAS	CS	
	A10	A1	H	A2	A0	VDD
VSS	A3	A5	J	A6	A4	
	A7	A9	K	A11	A8	VSS
VDD	A12	NC	L	NC	A13	

Notes:
1. Pins B3 and A2 have identical capacitance as pins B7 and A8.
2. For a read, when enabled, strobe pair RDQS & RDQS are identical in function and timing to strobe pair DQS & DQS and input masking function is disabled.
3. The function of DM or RDQS/RDQS are enabled by EMRS command.
4. VDDL and VSSDL are power and ground for the DLL. It is recommended that they are isolated on the device from VDD, VDDQ, VSS, and VSSQ.

Ball Locations (x8)

● : Populated Ball
✚ : Depopulated Ball

Top View (See the balls through the Package)

	1	2	3	4	5	6	7	8	9
A	●	●	●	✚	✚	✚	●	●	●
B	●	●	●	✚	✚	✚	●	●	●
C	●	●	●	✚	✚	✚	●	●	●
D	●	●	●	✚	✚	✚	●	●	●
E	●	●	●	✚	✚	✚	●	●	●
F	✚	●	●	✚	✚	✚	●	●	●
G	●	●	●	✚	✚	✚	●	●	✚
H	✚	●	●	✚	✚	✚	●	●	●
J	●	●	●	✚	✚	✚	●	●	✚
K	✚	●	●	✚	✚	✚	●	●	●
L	●	●	●	✚	✚	✚	●	●	✚

x16 package pinout (Top View) : 84 ball FBGA Package

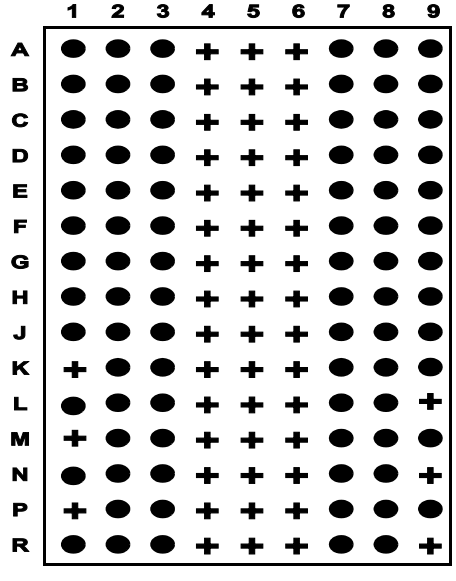
1	2	3		7	8	9
VDD	NC	VSS	A	VSSQ	$\overline{\text{UDQS}}$	VDDQ
UDQ6	VSSQ	UDM	B	UDQS	VSSQ	UDQ7
VDDQ	UDQ1	VDDQ	C	VDDQ	UDQ0	VDDQ
UDQ4	VSSQ	UDQ3	D	UDQ2	VSSQ	UDQ5
VDD	NC	VSS	E	VSSQ	$\overline{\text{LDQS}}$	VDDQ
LDQ6	VSSQ	LDM	F	LDQS	VSSQ	LDQ7
VDDQ	LDQ1	VDDQ	G	VDDQ	LDQ0	VDDQ
LDQ4	VSSQ	LDQ3	H	LDQ2	VSSQ	LDQ5
VDDL	VREF	VSS	J	VSSDL	CK	VDD
	CKE	$\overline{\text{WE}}$	K	$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT
NC	BA0	BA1	L	$\overline{\text{CAS}}$	$\overline{\text{CS}}$	
	A10	A1	M	A2	A0	VDD
VSS	A3	A5	N	A6	A4	
	A7	A9	P	A11	A8	VSS
VDD	A12	NC	R	NC	NC	

Notes:
VDDL and VSSDL are power and ground for the DLL. It is recommended that they are isolated on the device from VDD, VDDQ, VSS, and VSSQ.

Ball Locations (x16)

● : Populated Ball
✚ : Depopulated Ball

Top View
(See the balls through the Package)

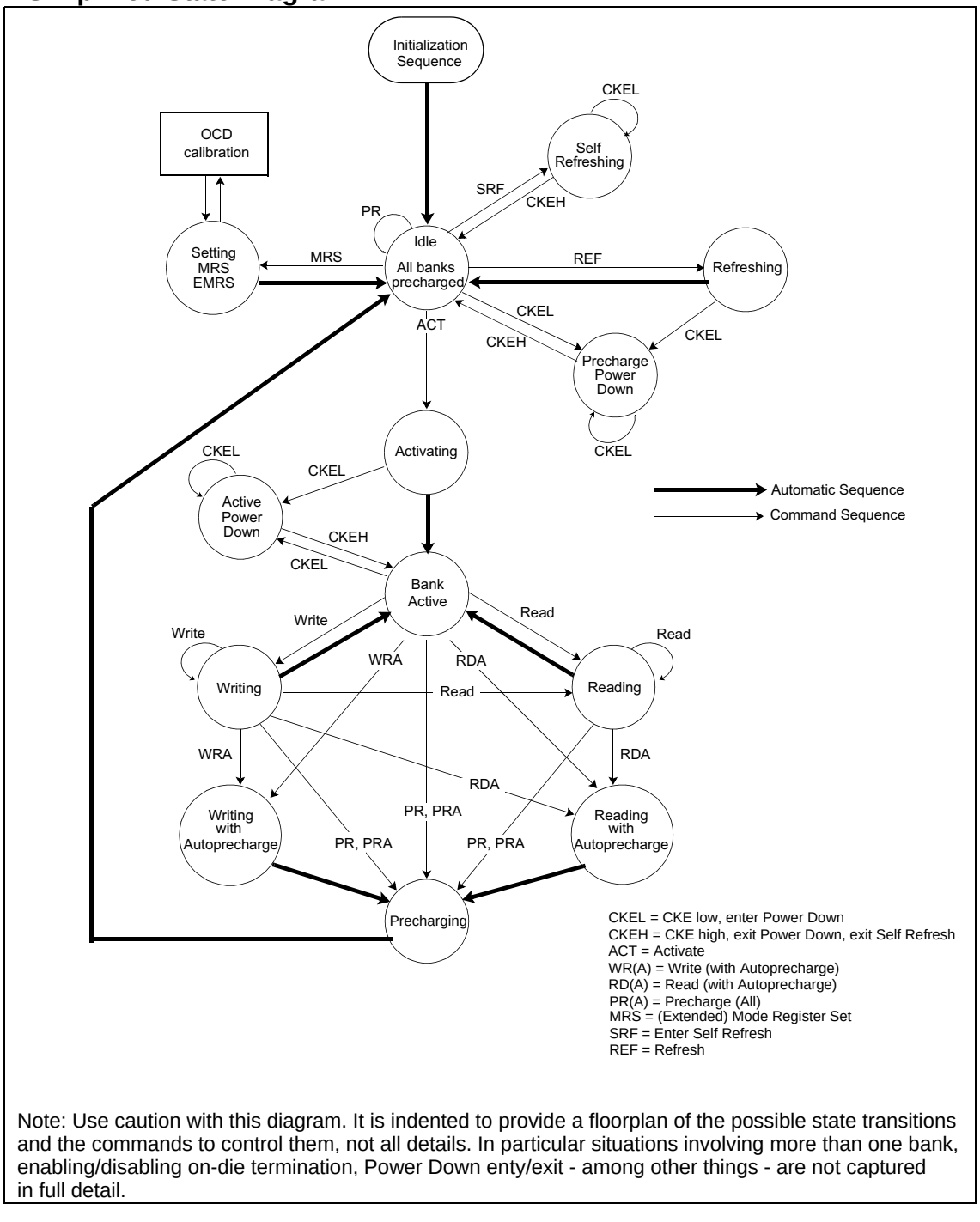


Signal Pin Description

Pin	Type	Function
CK $\overline{CK}$	Input	The system clock input. All inputs except DQs and DMs are sampled on the rising edge of CK.
CKE	Input	Activates the CK signal when high and deactivates the CK signal when low, thereby initiates either the Power Down mode, or the Self Refresh mode.
$\overline{CS}$	Input	$\overline{CS}$ enables the command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$, $\overline{CAS}$ $\overline{WE}$	Input	When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the command to be executed by the SDRAM.
A0 - A13	Input	During a Bank Activate command cycle, A0-A13 defines the row address (RA0-RA13) when sampled at the rising clock edge for x4 and x8 and A0-A12 row address for x16 device. During a Read or Write command cycle, A0-An defines the column address (CA0-CAn) when sampled at the rising clock edge.CAn depends on the SDRAM organization: 128M x 4 DDR CAn = CA9, A11 64M x 8 DDR CAn = CA9 32M x 16 DDR CAn = CA9 In addition to the column address, A10(=AP) is used to invoke autoprecharge operation at the end of the burst read or write cycle. If A10 is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If A10 is low, autoprecharge is disabled. During a Precharge command cycle, A10(=AP) is used in conjunction with BA0 and BA1 to control which bank(s) to precharge. If A10 is high, all four banks will be precharged simultaneously regardless of state of BA0 and BA1.
BA0, BA1	Input	Selects which bank is to be active.
DQx LDQx,UDQx	Input/ Output	Data Input/Output pins operate in the same manner as on conventional DRAMs. DQ0-DQ3 for x4 component, DQ0-DQ7 for x8 component and LDQ0-LDQ7 , UDQ0-UDQ7 for x16 component.
DQS,($\overline{DQS}$) LDQS,($\overline{LDQS}$) UDQS,($\overline{UDQS}$) RDQS,($\overline{RDQS}$)	Input/ Output	Data Strobe, output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16 component, LDQS corresponds to the data on LDQ0-LDQ7; UDQS coresponds to the data on UDQ0-UDQ7. For the x8, an RDQS option using DM pin can be enabled via the EMRS(1) to simplify read timing. The data strobes DQS, LDQS, UDQS, and RDQS may be used in single ended mode or paired with optional complimentary signals $\overline{DQS}$, $\overline{LDQS}$, $\overline{UDQS}$, and $\overline{RDQS}$ to provide differential pair signaling to the system during both reads and writes. AN EMRS(1) control bit enables or disables all complementary data strobe signals. In this data sheet, “differential DQS signals” refers to any of the following with A10 = 0 of EMRS(1) x4 DQS/$\overline{DQS}$ x8 DQS/$\overline{DQS}$ if EMRS(1)[A11] = 0 x8 DQS/$\overline{DQS}$, RDQS/$\overline{RDQS}$ if EMRS(1)[A11] = 1 x16 LDQS/$\overline{LDQS}$ and UDQS/$\overline{UDQS}$ “single-ended DQS signals” refers to any of the following with A10 = 1 of EMRS(1) x4 DQS x8 DQS if EMRS(1)[A11] = 0 x8 DQS, RDQS, if EMRS(1)[A11] = 1 x16LDQS and UDQS

DM, LDM,UDM	Input	In Write mode, DM has a latency of zero and operates as a word mask by allowing input data to be written if it is low but blocks the write operation if is high for x 16 LDM corresponds to data on LDQ0-LDQ7, UDM corresponds to data on UDQ0-UDQ7.
VDD,VSS	Supply	Power and ground for the input buffers and the core logic.
VDDQ VSSQ	Supply	Isolated power supply and ground for the output buffers to provide improved noise immunity. 1.8V +/- 0.1V
VREF	Input	SSTL Reference Voltage for Inputs
VDDLQ VSSDL	Supply	Isolated power supply and ground for the DLL to provide improved noise immunity. 1.8V +/- 0.1V
ODT	Input	On Die Termination Enable. It enables termination resistance internal to the DRAM. ODT is applied to each DQ, DQS, $\overline{\text{DQS}}$ and DM signals for x4 component and DQ, DQS, $\overline{\text{DQS}}$, RDQS, $\overline{\text{RDQS}}$ and DM for the x8 component. For x16 configuration ODT is applied to each DQ, UDQS/$\overline{\text{UDQS}}$, LDQS/$\overline{\text{LDQS}}$, UDM and LDM signal. ODT will be ignored if EMRS disable the function.
RFU		Reserved for future use

Simplified State Diagram



Note: Use caution with this diagram. It is indented to provide a floorplan of the possible state transitions and the commands to control them, not all details. In particular situations involving more than one bank, enabling/disabling on-die termination, Power Down enty/exit - among other things - are not captured in full detail.

Basic Functionality

Read and write accesses to the DDR2 SDRAM are burst oriented; accesses start at a selected location and continue for a burst length of four or eight in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the active command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A13 select the row). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst access and to determine if the auto precharge command is to be issued.

Prior to normal operation, the DDR2 SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

Power up and Initialization

DDR2 SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

Power-up and Initialization Sequence

The following sequence is required for POWER UP and Initialization.

1. Apply power and attempt to maintain CKE below 0.2*VDDQ and ODT[*1] at a low state (all other inputs may be undefined.)

   - VDD, VDDL and VDDQ are driven from a single power converter output, AND
   - VTT is limited to 0.95 V max, AND
   - Vref tracks VDDQ/2.

   or

   - Apply VDD before or at the same time as VDDL.
   - Apply VDDL before or at the same time as VDDQ.
   - Apply VDDQ before or at the same time as VTT & Vref.

   at least one of these two sets of conditions must be met.

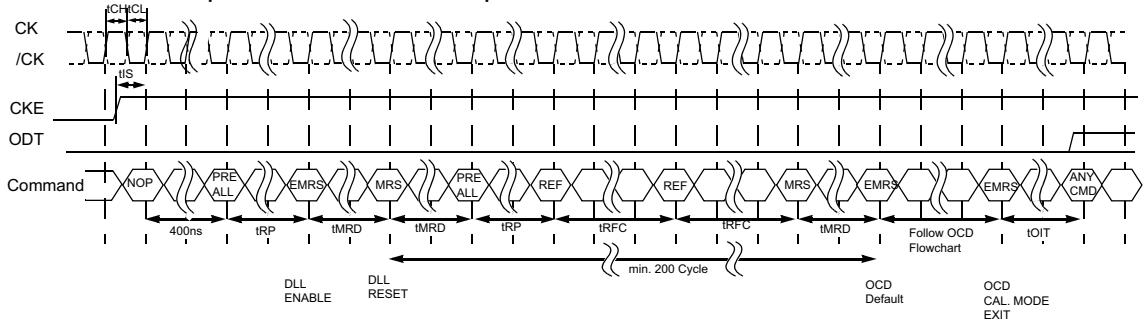
2. Start clock and maintain stable condition.
3. For the minimum of 200us after stable power and clock(CK, $\overline{CK}$), then apply NOP or deselect & take CKE high.
4. Wait minimum of 400ns then issue precharge all command. NOP or deselect applied during 400ns period.
5. Issue EMRS(2) command. (To issue EMRS(2) command, provide “Low” to BA0, “High” to BA1.)
6. Issue EMRS(3) command. (To issue EMRS(3) command, provide “High” to BA0 and BA1.)
7. Issue EMRS to enable DLL. (To issue "DLL Enable" command, provide "Low" to A0, "High" to BA0 and "Low" to BA1 and A12.)
8. Issue a Mode Register Set command for “DLL reset”.
   (To issue DLL reset command, provide "High" to A8 and "Low" to BA0-1)
9. Issue precharge all command.
10. Issue 2 or more auto-refresh commands.
11. Issue a mode register set command with low to A8 to initialize device operation. (i.e. to program operating parameters without resetting the DLL.
12. At least 200 clocks after step 8, execute OCD Calibration (Off Chip Driver impedance adjustment).
    If OCD calibration is not used, EMRS OCD Default command (A9=A8= A7=1) followed by EMRS OCD

Calibration Mode Exit command (A9=A8=A7=0) must be issued with other operating parameters of EMRS.

13. The DDR2 SDRAM is now ready for normal operation.

*1) To guarantee ODT off, VREF must be valid and a low level must be applied to the ODT pin.

Initialization Sequence after Power Up



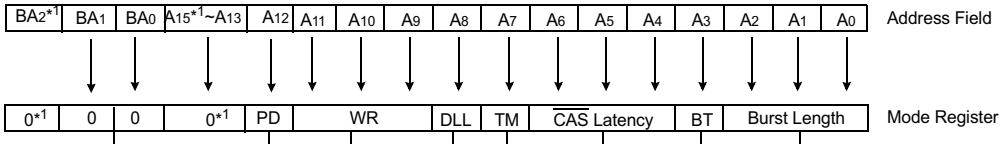
Programming the Mode Register

For application flexibility, burst length, burst type, $\overline{\text{CAS}}$ latency, DLL reset function, write recovery time(tWR) are user defined variables and must be programmed with a Mode Register Set (MRS) command. Additionally, DLL disable function, driver impedance, additive CAS latency, ODT(On Die Termination), single-ended strobe, and OCD(off chip driver impedance adjustment) are also user defined variables and must be programmed with an Extended Mode Register Set (EMRS) command. Contents of the Mode Register(MR) or Extended Mode Registers(EMR(#)) can be altered by re-executing the MRS and EMRS Commands. If the user chooses to modify only a subset of the MRS or EMRS variables, all variables must be redefined when the MRS or EMRS commands are issued.

MRS, EMRS and Reset DLL do not affect array contents, which means reinitialization including those can be executed any time after power-up without affecting array contents.

DDR2 SDRAM Mode Register Set (MRS)

The mode register stores the data for controlling the various operating modes of DDR2 SDRAM. It controls CAS latency, burst length, burst sequence, test mode, DLL reset, tWR and various vendor specific options to make DDR2 SDRAM useful for various applications. The default value of the mode register is not defined, therefore the mode register must be written after power-up for proper operation. The mode register is written by asserting low on CS, RAS, CAS, WE, BA0 and BA1, while controlling the state of address pins A0 ~ A15. The DDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the mode register. The mode register set command cycle time (tMRD) is required to complete the write operation to the mode register. The mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. The mode register is divided into various fields depending on functionality. Burst length is defined by A0 ~ A2 with options of 4 and 8 bit burst lengths. The burst length decodes are compatible with DDR SDRAM. Burst address sequence type is defined by A3, CAS latency is defined by A4 ~ A6. The DDR2 doesn't support half clock latency mode. A7 is used for test mode. A8 is used for DLL reset. A7 must be set to low for normal MRS operation. Write recovery time tWR is defined by A9 ~ A11. Refer to the table for specific codes.



A8	DLL Reset
0	No
1	Yes

A7	mode
0	Normal
1	Test

A3	Burst Type
0	Sequential
1	Interleave

Burst Length

A2	A1	A0	BL
0	1	0	4
0	1	1	8

A12	Active power down exit time
0	Fast exit(use tXARD)
1	Slow exit(use tXARDS)

BA1	BA0	MRS mode
0	0	MRS
0	1	EMRS(1)
1	0	EMRS(2): Reserved
1	1	EMRS(3): Reserved

Write recovery for autoprecharge

A11	A10	A9	WR(cycles)
0	0	0	Reserved
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	Reserved
1	1	1	Reserved

*2

CAS Latency

A6	A5	A4	Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	Reserved

*1 : A13 is reserved for future use and must be programmed to 0 when setting the mode register.
BA2 and A14 are not used for 512Mb, but used for 1Gb and 2Gb DDR2 SDRAMs. A15 is reserved for future usage.

*2 : WR(write recovery for autoprecharge) min is determined by tCK max and WR max is determined by tCK min. WR in clock cycles is calculated by dividing tWR (in ns) by tCK (in ns) and rounding up a non-integer value to the next integer (WR[cycles] = tWR(ns)/tCK(ns)). The mode register must be programmed to this value. This is also used with tRP to determine tDAL.

DDR2 SDRAM Extended Mode Register Set

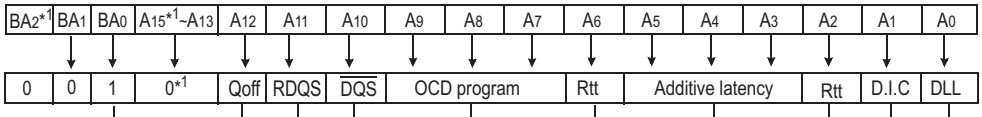
EMRS(1)

The extended mode register(1) stores the data for enabling or disabling the DLL, output driver strength, ODT value selection and additive latency. The default value of the extended mode register is not defined, therefore the extended mode register must be written after power-up for proper operation. The extended mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and high on BA0, while controlling the states of address pins A0 ~ A13. The DDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register. The mode register set command cycle time (tMRD) must be satisfied to complete the write operation to the extended mode register. Mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. A0 is used for DLL enable or disable. A1 is used for enabling a half strength data-output driver. A3~A5 determines the additive latency, A2 and A6 are used for ODT value selection, A7~A9 are used for OCD control, A10 is used for DQS# disable and A11 is used for RDQS enable.

DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. The DLL is automatically disabled when entering self refresh operation and is automatically re-enabled upon exit of self refresh operation. Any time the DLL is enabled (and subsequently reset), 200 clock cycles must occur before a Read command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tAC or tDQSCK parameters.

EMRS(1) Programming



BA1	BA0	MRS mode
0	0	MRS
0	1	EMRS(1)
1	0	EMRS(2)
1	1	EMRS(3): Reserved

A6	A2	Rtt (NOMINAL)
0	0	ODT Disable
0	1	75 ohm
1	0	150 ohm
1	1	50 ohm (*2)

A0	DLL Enable
0	Enable
1	Disable

A9	A8	A7	OCD Calibration Program
0	0	0	OCD Calibration mode exit; maintain setting
0	0	1	Drive(1)
0	1	0	Drive(0)
1	0	0	Adjust mode[a]
1	1	1	OCD Calibration default [b]

a: When Adjust mode is issued, AL from previously set value must be applied.
b: After setting to default, OCD mode needs to be exited by setting A9-A7 to 000. Refer to the following 3.2.2.3 section for detailed information

A5	A4	A3	Additive Latency
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	Reserved
1	1	1	Reserved

A12	Qoff (Optional) [a]
0	Output buffer enabled
1	Output buffer disabled

a. Outputs disabled - DQs, DQSs, $\overline{DQS}$s, RDQS, $\overline{RDQS}$. This feature is used in conjunction with dimm IDD meaurements when IDDQ is not desired to be included.

A1	Output Driver Impedence Control	Driver Size
0	Normal	100%
1	Weak	60%

A10	$\overline{DQS}$
0	Enable
1	Disable

A11	RDQS Enable
0	Disable
1	Enable

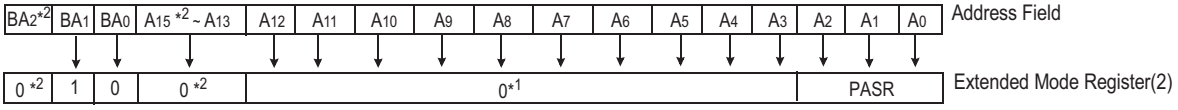
* If RDQS is enabled, the DM function is disabled. RDQS is active for reads and don't care for writes.

A11 (RDQS Enable)	A10 ($\overline{DQS}$ Enable)	Strobe Function Matrix			
		RDQS/DM	$\overline{RDQS}$	DQS	$\overline{DQS}$
0 (Disable)	0 (Enable)	DM	Hi-z	DQS	$\overline{DQS}$
0 (Disable)	1 (Disable)	DM	Hi-z	DQS	Hi-z
1 (Enable)	0 (Enable)	RDQS	$\overline{RDQS}$	DQS	$\overline{DQS}$
1 (Enable)	1 (Disable)	RDQS	Hi-z	DQS	Hi-z

*1 : A13 is reserved for future use and must be programmed to 0 when setting the mode register.
BA2 and A14 are not used for 512Mb, but used for 1Gb and 2Gb DDR2 SDRAMs. A15 is reserved for future use.

*2 : Optional for DDR2-400/533/667/800

EMRS(2) Programming: *1 PASR



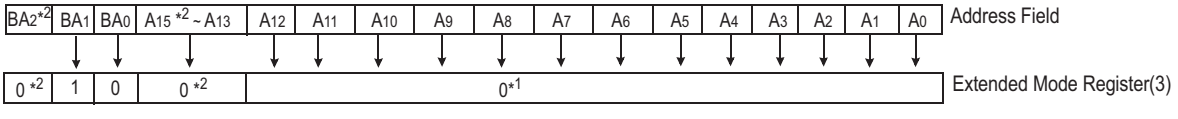
*1 BA0 and BA1 must be programmed to 0 when setting the mode register during initialization.

*2 : BA2 and A14 are not used for 512Mb, but used for 1Gb and 2Gb DDR2 SDRAMs. A15 is reserved for future usage.

The PASR bits allows the user to dynamically customize the memory array size to the actual needs. This feature allows the device to reduce standby current by refreshing only the memory arrays that contain essential data.The refresh options are full array, one-half array, one-quarter array, three-fourth array, or none of the array. The mapping of these partitions can start at either the beginning or the end of the address map. Please see the following table.

PASR[2]	PASR[1]	PASR[0]	ACTIVE SECTION
0	0	0	Full array
0	0	1	1/2 array (Banks 0,1)
0	1	0	1/4 array (Bank 0)
0	1	1	Not defined
1	0	0	3/4 array (Banks 1, 2, 3)
1	0	1	1/2 array (Banks 2, 3)
1	1	0	1/4 array (Bank 3)
1	1	1	Not defined

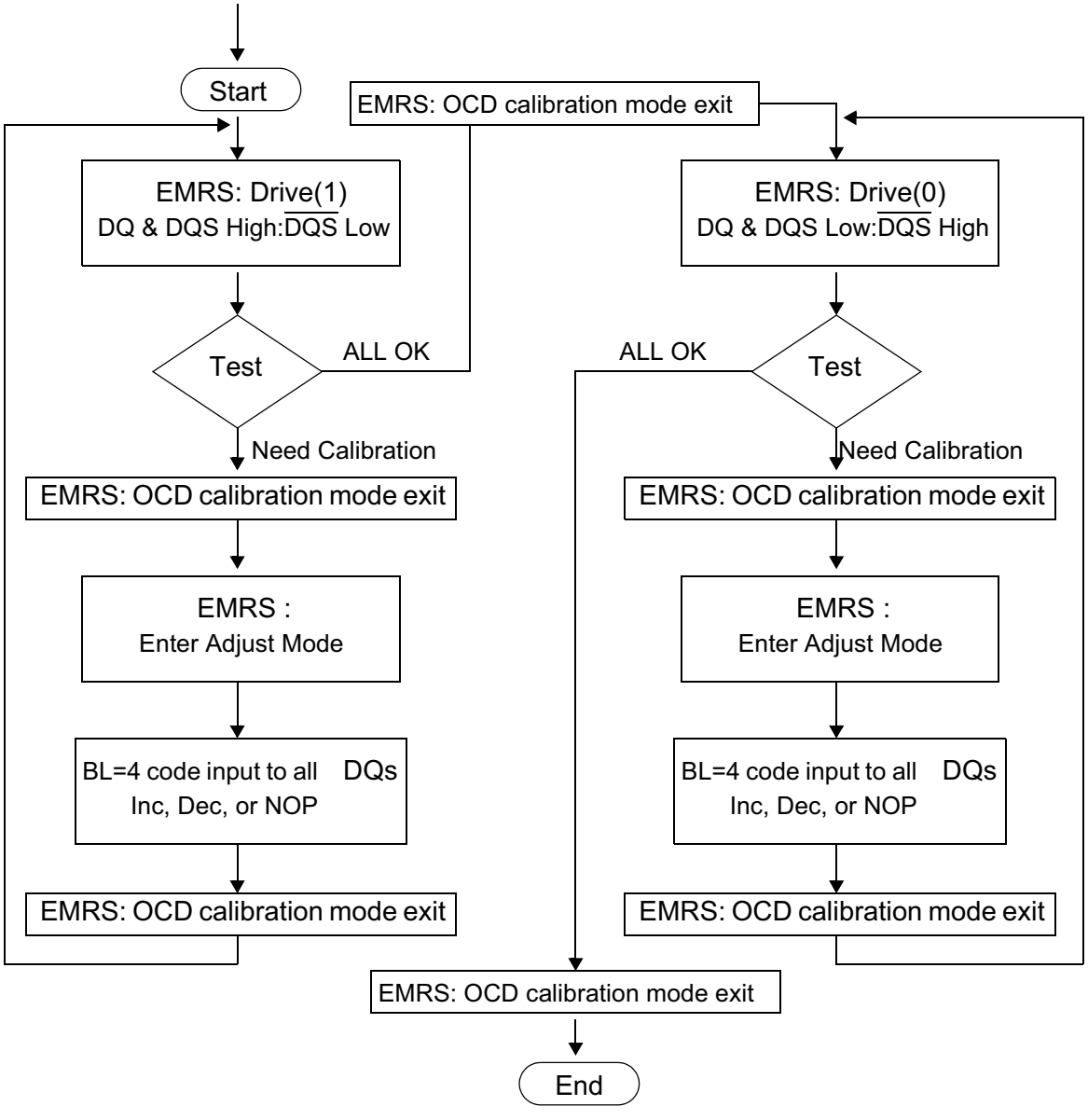
EMRS(3) Programming: Reserved *1



*1 : EMRS(3) is reserved for future use and all bits except BA0 and BA1 must be programmed to 0 when setting the mode register during initialization.
*2 : BA2 and A14 are not used for 512Mb, but used for 1Gb and 2Gb DDR2 SDRAMs. A15 is reserved for future usage.

Off-Chip Driver (OCD) Impedance Adjustment

DDR2 SDRAM supports driver calibration feature and the flow chart below is an example of the sequence. Every calibration mode command should be followed by "OCD calibration mode exit" before any other command being issued. MRS should be set before entering OCD impedance adjustment and ODT (On Die Termination) should be carefully controlled depending on system environment.



Extended Mode Register Set for OCD impedance adjustment

OCD impedance adjustment can be done using the following EMRS mode. In drive mode all outputs are driven out by DDR2 SDRAM and drive of RDQS is dependent on EMRS bit enabling RDQS operation. In Drive(1) mode, all DQ, DQS (and RDQS) signals are driven high and all $\overline{DQS}$ (and $\overline{RDQS}$) signals are driven low. In Drive(0) mode, all DQ, DQS (and RDQS) signals are driven low and all $\overline{DQS}$ (and $\overline{RDQS}$) signals are driven high. In adjust mode, BL = 4 of operation code data must be used. In case of OCD calibration default, output driver characteristics have a nominal impedance value of 18 Ohms during nominal temperature and voltage conditions. Output driver characteristics for OCD calibration default are specified in the following table. OCD applies only to normal full strength output drive setting defined by EMRS and if half strength is set, OCD default driver characteristics are not applicable. When OCD calibration adjust mode is used, OCD default output driver characteristics are not applicable. After OCD calibration is completed or driver strength is set to default, subsequent EMRS commands not intended to adjust OCD characteristics must specify A7~A9 as '000' in order to maintain the default or calibrated value.

OCD impedance adjust

To adjust output driver impedance, controllers must issue the ADJUST EMRS command along with a 4 bit burst code to DDR2 SDRAM as in the following table. For this operation, Burst Length has to be set to BL = 4 via MRS command before activating OCD and controllers must drive the burst code to all DQs at the same time. DT0 is the table means all DQ bits at bit time 0, DT1 at bit time 1, and so forth. The driver output impedance is adjusted for all DDR2 SDRAM DQs simultaneously and after OCD calibration, all DQs of a given DDR2 SDRAM will be adjusted to the same driver strength setting. The maximum step count for adjustment is 8 and when the limit is reached, further increment or decrement code has no effect. The default setting may be any step within the 8 step range.

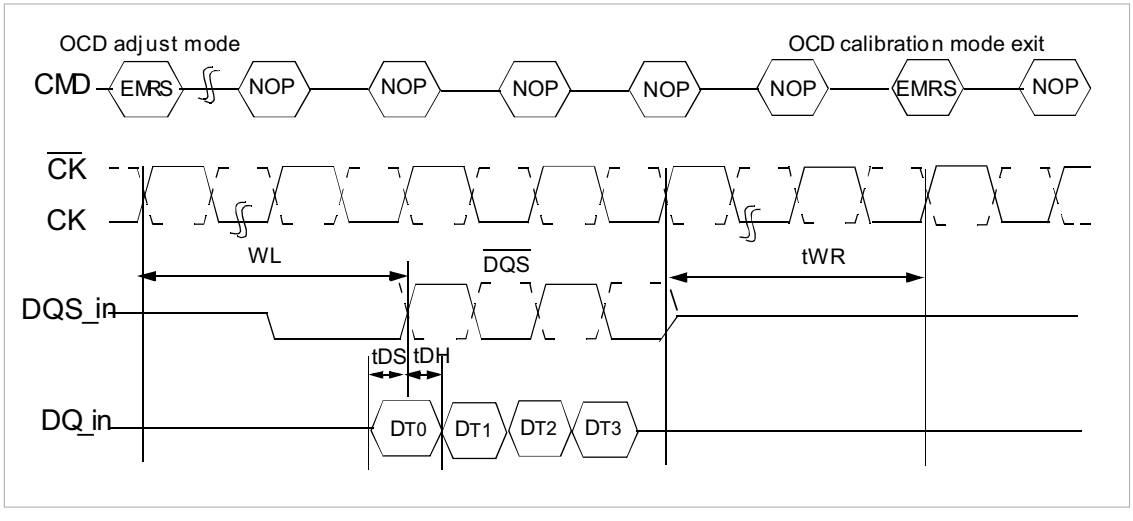
Off- Chip-Driver program

A9	A8	A7	Operation
0	0	0	OCD calibration mode exit
0	0	1	Drive(1) DQ, DQS, (RDQS) high and $\overline{DQS}$, ($\overline{RDQS}$) low
0	1	0	Drive(0) DQ, DQS, (RDQS) low and $\overline{DQS}$, ($\overline{RDQS}$) high
1	0	0	Adjust mode
1	1	1	OCD calibration default

Off- Chip-Driver Adjust Program

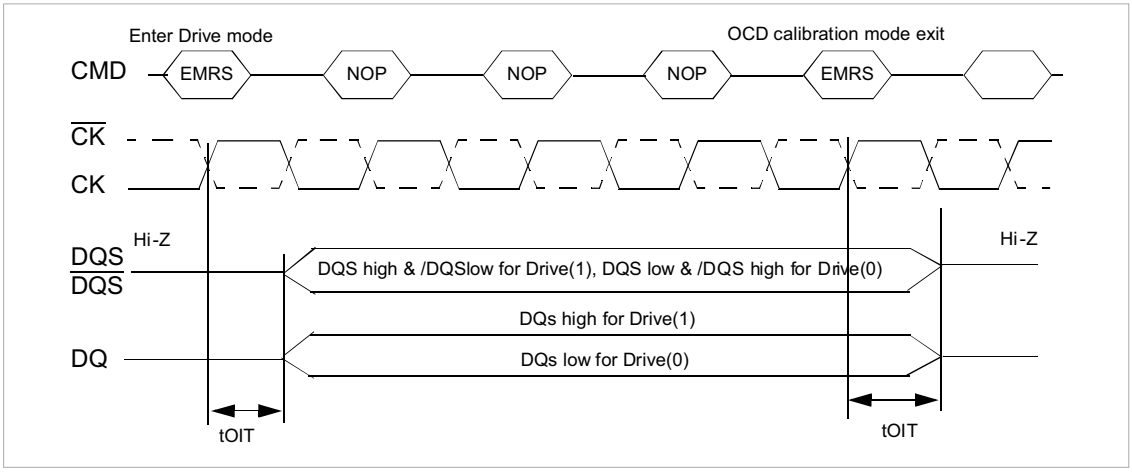
4 bit burst code inputs to all DQs				Operation	
D_{T0}	D_{T1}	D_{T2}	D_{T3}	Pull-up driver strength	Pull-down driver strength
0	0	0	0	NOP (no operation)	NOP (no operation)
0	0	0	1	Increase by 1 step	NOP
0	0	1	0	Decrease by 1 step	NOP
0	1	0	0	NOP	Increase by 1 step
1	0	0	0	NOP	Decrease by 1 step
0	1	0	1	Increase by 1 step	Increase by 1 step
0	1	1	0	Decrease by 1 step	Increase by 1 step
1	0	0	1	Increase by 1 step	Decrease by 1 step
1	0	1	0	Decrease by 1 step	Decrease by 1 step
Other Combinations				Reserved	Reserved

For proper operation of adjust mode, WL = RL - 1 = AL + CL -1 clocks and tDS / tDH should be met as the following timing diagram. Input data pattern for adjustment, DT0 - DT3 is fixed and not affected by MRS addressing mode (i.e. sequential or interleave). Burst length of 4 have to be programmed in the MRS for OCD impedance adjustment.



Drive Mode

Drive mode, both Drive(1) and Drive(0), is used for controllers to measure DDR2 SDRAM Driver impedance before OCD impedance adjustment. In this mode, all outputs are driven out tOIT after “enter drive mode” command and all output drivers are turned-off tOIT after “OCD calibration mode exit” command as the following timing diagram.



On-Die Termination (ODT)

ODT (On-Die Termination) is a new feature on DDR2 components that allows a DRAM to turn on/off termination resistance for each DQ, DQS, $\overline{DQS}$ and DM for x4 and DQ, DQS, $\overline{DQS}$, DM, RDQS (DM and RDQS share the same pin), and $\overline{RDQS}$ for x8 configuration via the ODT control pin, where $\overline{DQS}$ is terminated only when enabled in the EMRS by address bit A10 = 0. For x8 configuration $\overline{RDQS}$ is only terminated, when enabled in the EMRS by address bits A10 = 0 and A11 = 1.

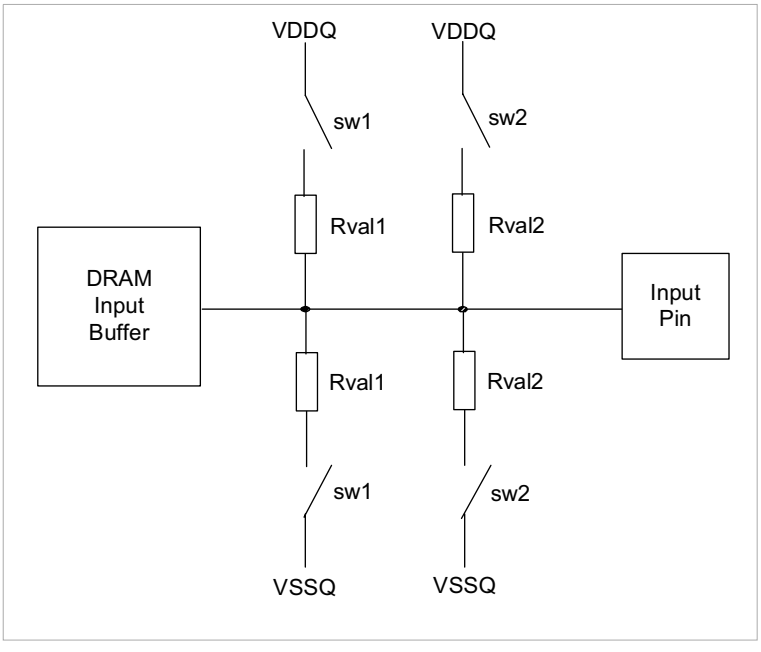
For x16 configuration ODT is applied to each UDQ, LDQ, UDQS, $\overline{UDQS}$, LDQS, $\overline{LDQS}$, UDM and LDM signal via the ODT control pin, where $\overline{UDQS}$ and $\overline{LDQS}$ are terminated only when enabled in the EMRS by address bit A10 = 0.

The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.

The ODT function can be used for all active and standby modes. ODT is turned off and not supported in Self-Refresh mode.

Funtional Prepresentation of ODT

.



Switch sw1 or sw2 is enabled by the ODT pin. Selection between sw1 or sw2 is determined by “Rtt (nominal)” in EMRS address bits A6 & A2. Target Rtt = 0.5 * Rval1 or 0.5 * Rval2.

The ODT pin will be ignored if the Extended Mode Register (EMRS) is programmed to disable ODT.

ODT Truth Tables

The ODT Truth Table shows which of the input pins are terminated depending on the state of address bit A10 and A11 in the EMRS for all three device organisations (x4, x8 and x16). To activate termination of any of these pins, the ODT function has to be enabled in the EMRS by address bits A6 and A2.

Input Pin	EMRS Adress Bit A10	EMRS Adress Bit A11
x4 components:		
DQ0~DQ3	X	X
DQS	X	X
$\overline{\text{DQS}}$	0	X
DM	X	X
x8 components:		
DQ0~DQ7	X	X
DQS	X	X
$\overline{\text{DQS}}$	0	X
RDQS	X	1
$\overline{\text{RDQS}}$	0	1
DM	X	0
x16 components:		
LDQ0~LDQ7	X	X
UDQ0~UDQ7	X	X
LDQS	X	X
$\overline{\text{LDQS}}$	0	X
UDQS	X	X
$\overline{\text{UDQS}}$	0	X
LDM	X	X
UDM	X	X

DC Electrical Characteristics and Operation Conditions:

Parameter / Condition	Symbol	min.	nom.	max.	Units	Notes
Rtt eff. impedance value for EMRS(A6,A2)=0,1; 75 ohm	Rtt1(eff)	60	75	90	ohm	1
Rtt eff. impedance value for EMRS(A6,A2)=0,1; 150 ohm	Rtt2(eff)	120	150	180	ohm	1
Rtt eff. impedance value for EMRS(A6,A2)=1,1; 50 ohm	Rtt3(eff)	40	50	60	ohm	1,3
Deviation of VM with respect to VDDQ/2	delta VM	- 6		+ 6	%	2

1) Measurement Definition for Rtt(eff):
Apply VIHac and VILac to test pin seperately, then measure current I(VIHac) and I(VILac) respectively

$$Rtt(eff) = (VIHac - VILac) / (I(VIHac) - I(VILac))$$

2) Measurement Defintion for VM:
Measure voltage (VM) at test pin (midpoint) with no load:

$$\text{delta VM} = ((2 * VM / VDDQ) - 1) \times 100\%$$

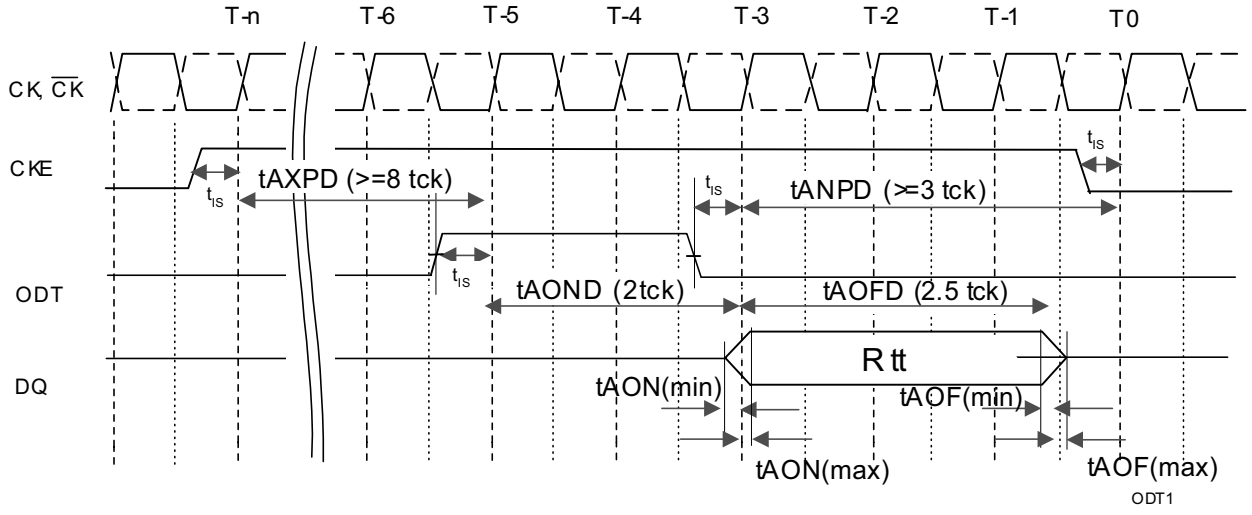
3) Optional for DDR2-400/533/667/800

AC Electrical Characteristics and Operation Conditions:

Symbol	Parameter / Condition	min.	max.	Units	Notes
t_{AOND}	ODT turn-on delay	2	2	t_{CK}	
t_{AON}	ODT turn-on	tAC(min)	tAC(max) + 1ns	ns	1
t_{AONPD}	ODT turn-on (Power-Down Modes)	tAC(min) + 2ns	$2t_{CK}$ + tAC(max) + 1ns	ns	3
t_{AOFD}	ODT turn-off delay	2.5	2.5	t_{CK}	
t_{AOF}	ODT turn-off	tAC (min)	tAC (max) + 0.6ns	ns	2
t_{AOFPD}	ODT turn-off (Power-Down Modes)	tAC(min) + 2ns	$2.5t_{CK}$ + tAC(max) + 1ns	ns	3
t_{ANPD}	ODT to Power Down Mode Entry Latency	3		t_{CK}	4
t_{AXPD}	ODT Power Down Exit Latency	8		t_{CK}	4

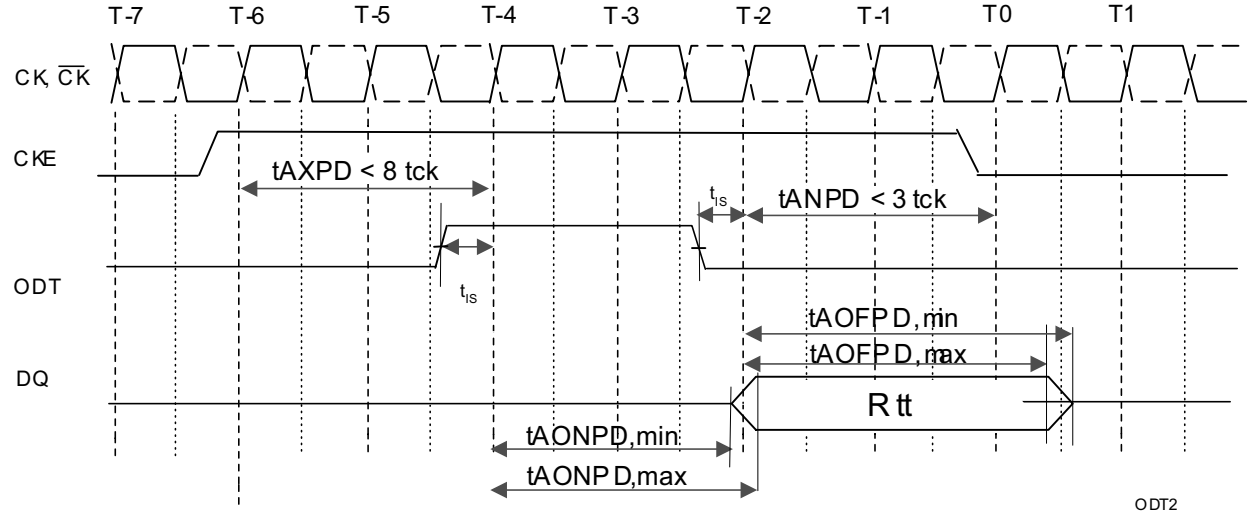
1) ODT turn on time min. is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max. is when the ODT resistance is fully on. Both are measured from t_{AOND}.
2) ODT turn off time min. is when the device starts to turn-off ODT resistance.. ODT turn off time max. is when the bus is in high impedance. Both are measured from t_{AOFD}.
3) For Standard Active Power-down - with MRS A12 = "0" - the non power-down timings (tAOND, tAON, tAOFD and tAOF) apply
4) tANPD and tAXPD define the timing limit when either Power Down Mode Timings (tAONPD, tAOFPD) or Non-Power Down Mode timings (tAOND, tAOFD) have to be applied

ODT Timing for Active / Standby (Idle) Mode and Standard Active Power-Down Mode



1) Both ODT to Power Down Entry and Exit Latency timing parameter tANPD and tAXPD are met, therefore Non-Power Down Mode timings have to be applied.
2) ODT turn-on time ($t_{AON,min}$) is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max. ($t_{AON,max}$) is when the ODT resistance is fully on. Both are measured from t_{AOND}.
3) ODT turn off time min. ($t_{AOF,min}$) is when the device starts to turn off the ODT resistance. ODT turn off time max. ($t_{AOF,max}$) is when the bus is in high impedance. Both are measured from t_{AOFD}.

ODT Timing for Precharge Power-Down and Low Power Power-Down Mode

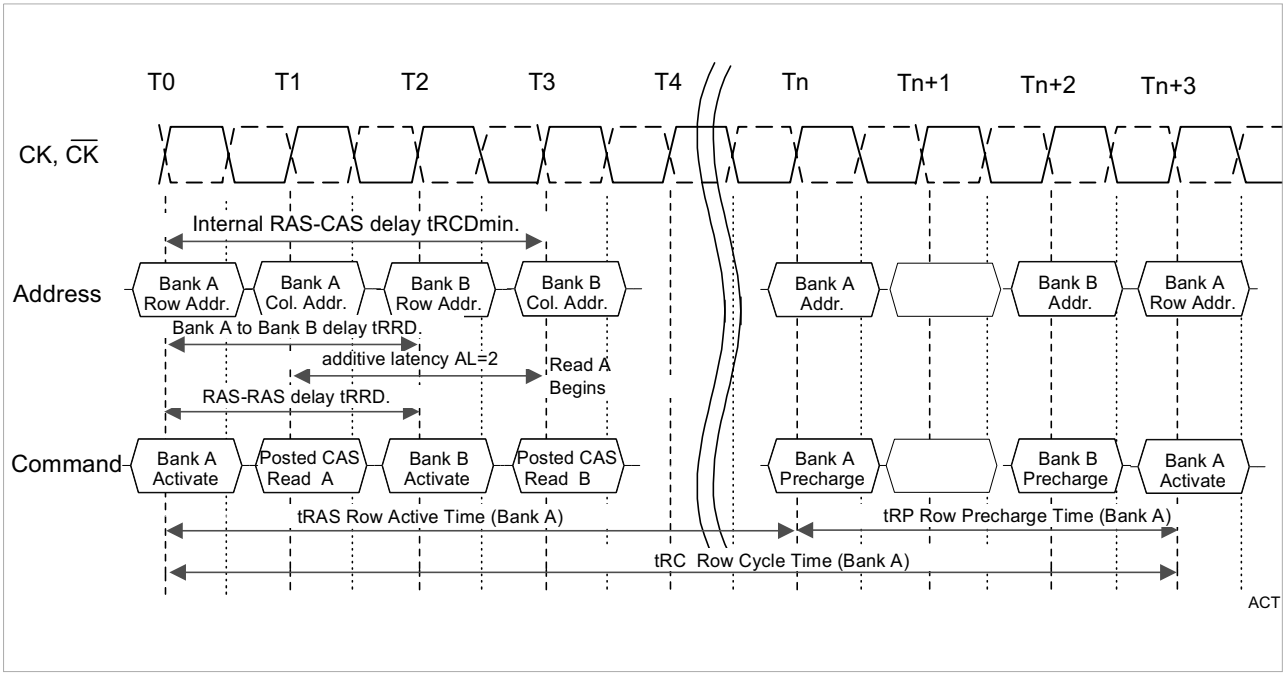


1) Both ODT to Power Down Entry and Exit Latencies tANPD and tAXPD are not met, therefore Power-Down Mode timings have to be applied.

Bank Activate Command

The Bank Activate command is issued by holding $\overline{CAS}$ and $\overline{WE}$ high with $\overline{CS}$ and $\overline{RAS}$ low at the rising edge of the clock. The bank addresses BA0 and BA1 are used to select the desired bank. The row addresses A0 through A12 are used to determine which row to activate in the selected bank for x4 and x8 organised components. For x16 components row addresses A0 through A12 have to be applied. The Bank Activate command must be applied before any Read or Write operation can be executed. Immediately after the bank active command, the DDR2 SDRAM can accept a read or write command (with or without Auto-Precharge) on the following clock cycle. If a R/W command is issued to a bank that has not satisfied the tRCDmin specification, then additive latency must be programmed into the device to delay the R/W command which is internally issued to the device. The additive latency value must be chosen to assure tRCDmin is satisfied. Additive latencies of 0, 1, 2, 3 and 4 are supported. Once a bank has been activated it must be precharged before another Bank Activate command can be applied to the same bank. The bank active and precharge times are defined as tRAS and tRP, respectively. The minimum time interval between successive Bank Activate commands to the same bank is determined (tRC). The minimum time interval between Bank Active commands, to any other bank, is the Bank A to Bank B delay time (tRRD).

Bank Activate Command Cycle: tRCD = 3, AL = 2, tRP = 3, tRRD = 2



Read and Write Commands and Access Modes

After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting $\overline{RAS}$ high, $\overline{CS}$ and $\overline{CAS}$ low at the clock's rising edge. $\overline{WE}$ must also be defined at this time to determine whether the access cycle is a read operation ($\overline{WE}$ high) or a write operation ($\overline{WE}$ low). The DDR2 SDRAM provides a wide variety of fast access modes. A single Read or Write Command will initiate a serial read or write operation on successive clock cycles at data rates of up to 667Mb/sec/pin for main memory. The boundary of the burst cycle is restricted to specific segments of the page length.

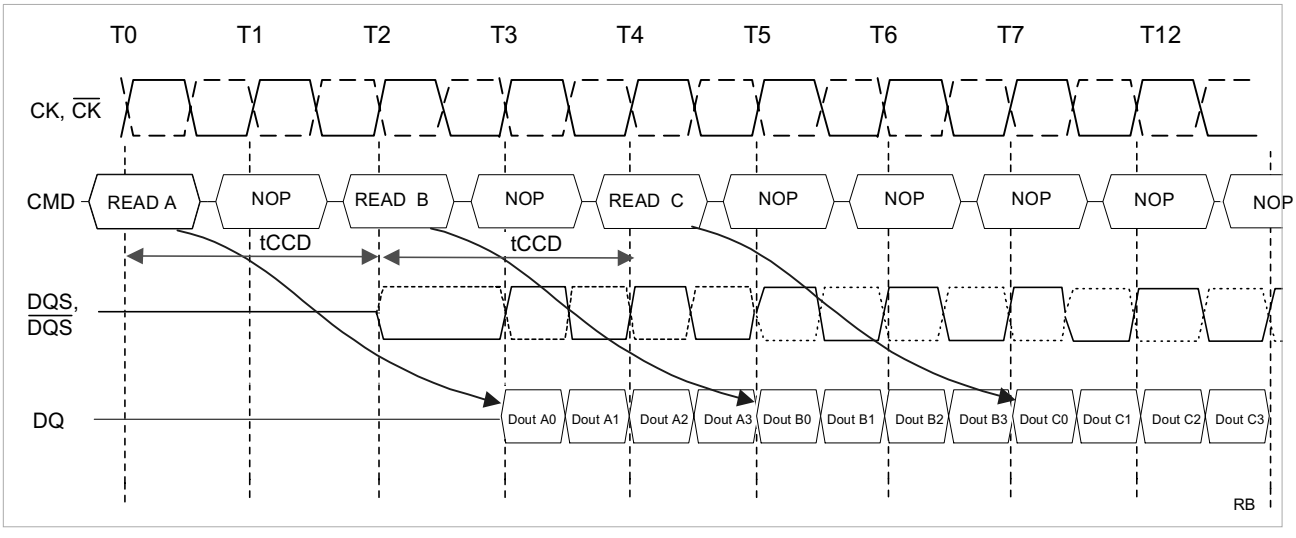
For example, the 32Mbit x 4 I/O x 4 Bank chip has a page length of 1 kByte (defined by CA0-CA9 & CA11). In case of a 4-bit burst operation (burst length = 4) the page length of 1 kByte is divided into 512 uniquely addressable segments (4-bits x 4 I/O each). The 4-bit burst operation will occur entirely within one of the 512 segments (defined by CA0-CA8) beginning with the column address supplied to the device during the Read or Write Command (CA0-CA9 & A11). The second, third and fourth access will also occur within this segment, however, the burst order is a function of the starting address, and the burst sequence.

In case of a 8-bit burst operation (burst length = 8) the page length of 1 kByte is divided into 256 uniquely addressable double segments (8-bits x 4 I/O each). The 8-bit burst operation will occur entirely within one of the 256 double segments (defined by CA0-CA7) beginning with the column address supplied to the deivce during the Read or Write Command (CA0-CA9 & CA11).

A new burst access must not interrupt the previous 4 bit burst operation in case of BL = 4 setting. Therefore the minimum $\overline{CAS}$ to $\overline{CAS}$ delay (tCCD) is a minimum of 2 clocks for read or write cycles.

For 8 bit burst operation (BL = 8) the minimum $\overline{CAS}$ to $\overline{CAS}$ delay (tCCD) is 4 clocks for read or write cycles. Burst interruption is allowed with 8 bit burst operation. For details see the "Burst Interrupt" - Section of this datasheet.

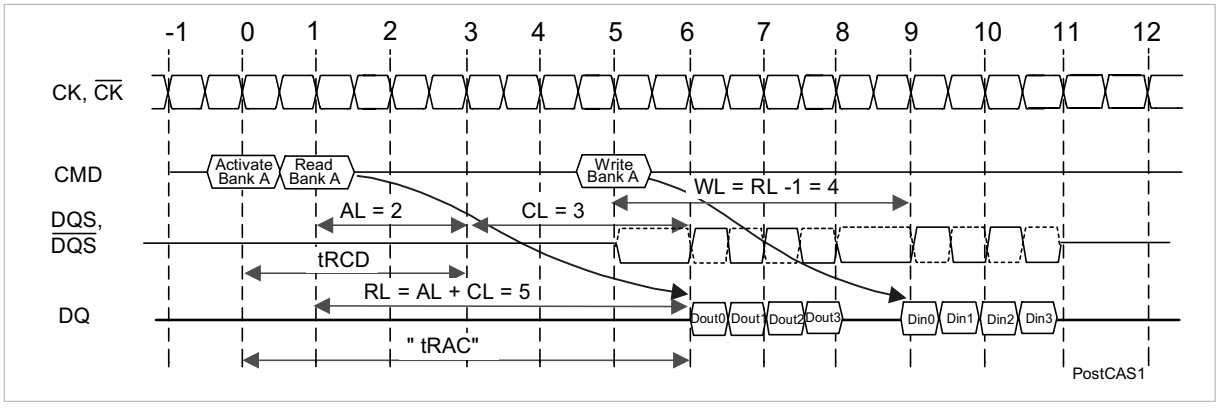
Read Burst Timing Example : (CL = 3, AL = 0, RL = 3, BL = 4)



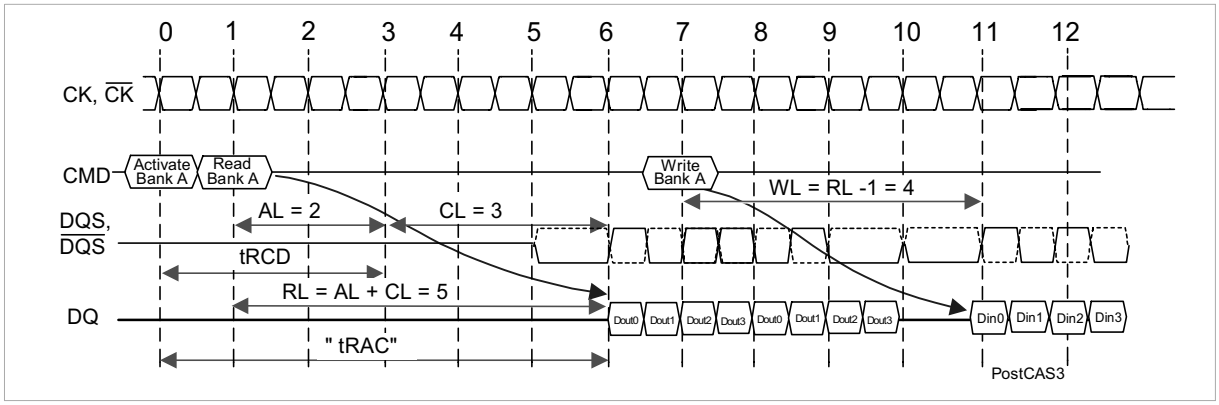
Posted CAS

Posted CAS operation is supported to make command and data bus efficient for sustainable bandwidths in DDR2 SDRAM. In this operation, the DDR2 SDRAM allows a Read or Write command to be issued immediately after the RAS bank activate command (or any time during the RAS to CAS delay time, tRCD, period). The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is the sum of AL and the CAS latency (CL). Therefore if a user chooses to issue a Read/Write command before the tRCDmin, then AL greater than 0 must be written into the EMRS. The Write Latency (WL) is always defined as RL - 1 (Read Latency -1) where Read Latency is defined as the sum of Additive Latency plus CAS latency (RL=AL+CL). If a user chooses to issue a Read command after the tRCDmin period, the Read Latency is also defined as RL = AL + CL.

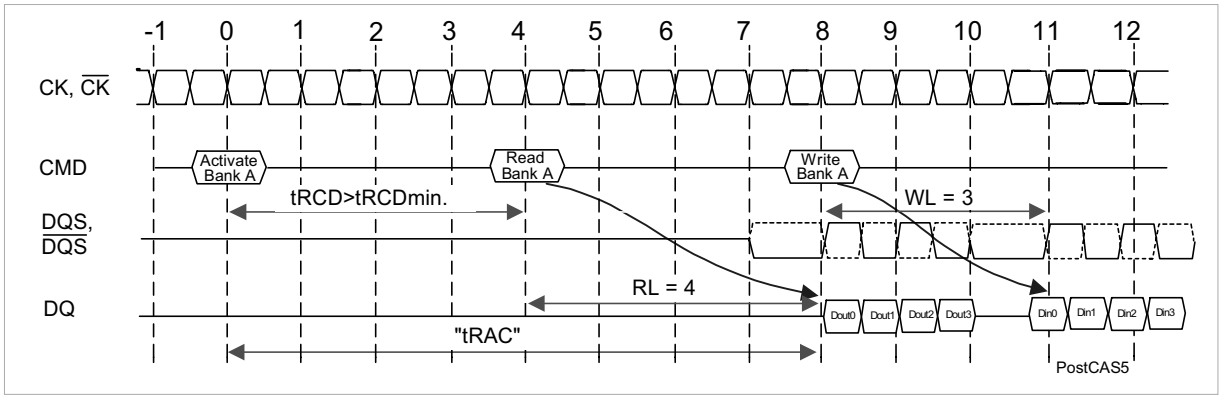
Read followed by a write to the same bank, Activate to Read delay < tRCDmin:
AL = 2 and CL = 3, RL = (AL + CL) = 5, WL = (RL -1) = 4, BL = 4



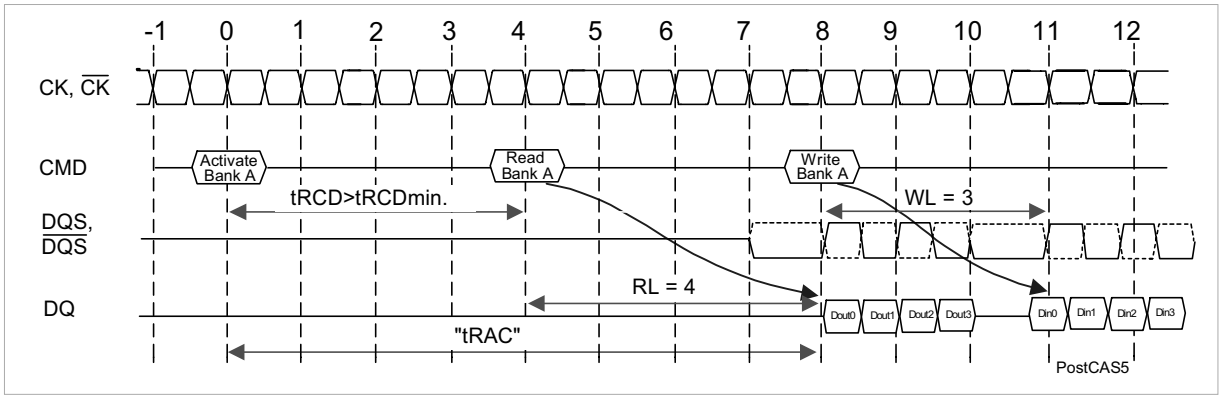
Read followed by a write to the same bank, Activate to Read delay < tRCDmin:
AL = 2 and CL = 3, RL = (AL + CL) = 5, WL = (RL -1) = 4, BL = 8



Read followed by a write to the same bank, Activate to Read delay = tRCDmin:
AL = 0, CL = 3, RL = (AL + CL) = 3, WL = (RL -1) = 2, BL = 4



Read followed by a write to the same bank, Activate to Read delay > tRCDmin:
AL = 1, CL = 3, RL = 4, WL = 3, BL = 4



Burst Mode Operation

Burst mode operation is used to provide a constant flow of data to memory locations (write cycle), or from memory locations (read cycle). The parameters that define how the burst mode will operate are burst sequence and burst length. The DDR2 SDRAM supports 4 bit and 8 bit burst modes only. For 8 bit burst mode, full interleave address ordering is supported, however, sequential address ordering is nibble based for ease of implementation. The burst length is programmable and defined by the addresses A0 ~ A2 of the MRS. The burst type, either sequential or interleaved, is programmable and defined by the address bit 3 (A3) of the MRS. Seamless burst read or write operations are supported. Interruption of a burst read or write operation is prohibited, when burst length = 4 is programmed. For burst interruption of a read or write burst when burst length = 8 is used, see the "Burst Interruption " section of this datasheet. A Burst Stop command is not supported on DDR2 SDRAM devices.

Burst Length and Sequence

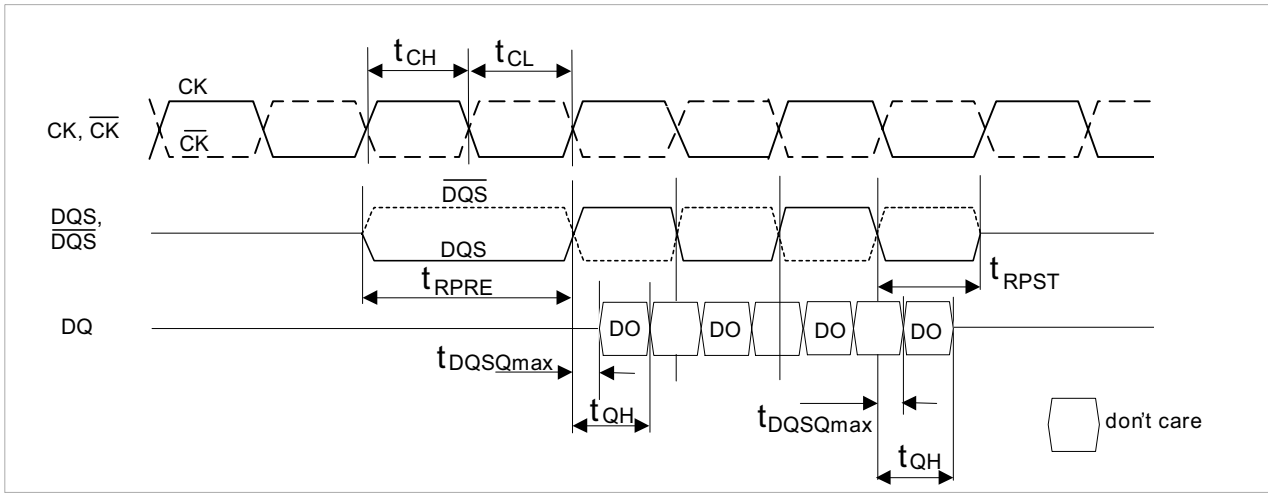
Burst Length	Starting Address (A2 A1 A0)	Sequential Addressing (decimal)	Interleave Addressing (decimal)
4	x 0 0	0, 1, 2, 3	0, 1, 2, 3
	x 0 1	1, 2, 3, 0	1, 0, 3, 2
	x 1 0	2, 3, 0, 1	2, 3, 0, 1
	x 1 1	3, 0, 1, 2	3, 2, 1, 0
8	0 0 0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	0 0 1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6
	0 1 0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5
	0 1 1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4
	1 0 0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	1 0 1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2
	1 1 0	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1
	1 1 1	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0

Note: 1) Page length is a function of I/O organization
128Mb X 4 organization (CA0-CA9, CA11); Page Length = 1 kByte
64Mb X 8 organization (CA0-CA9); Page Length = 1 kByte
32Mb X 16 organization (CA0-CA9); Page Length = 2 kByte
2) Order of burst access for sequential addressing is "nibble-based" and therefore different from SDR or DDR components

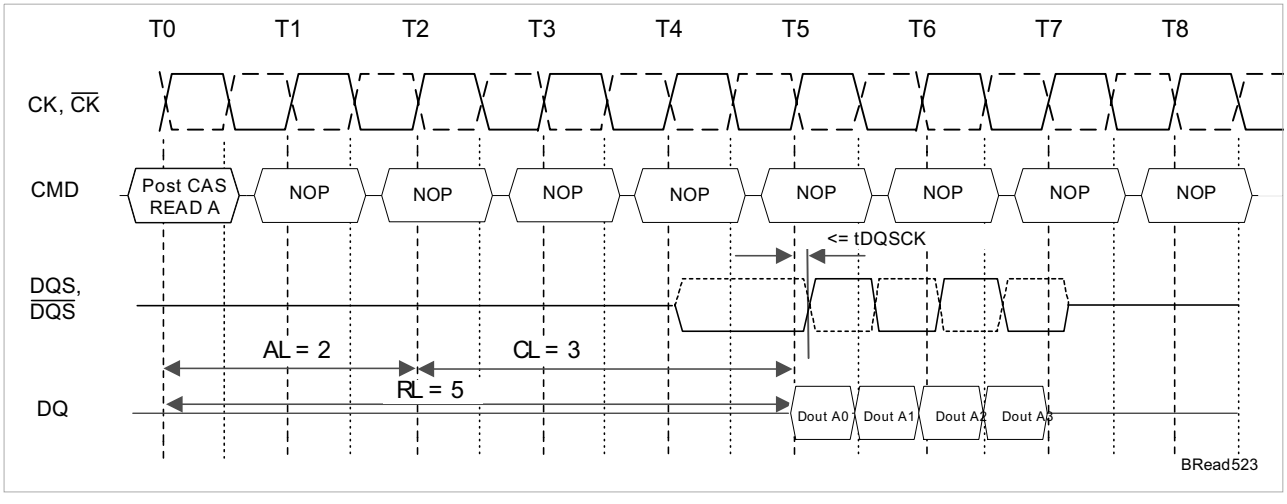
Burst Read Command

The Burst Read command is initiated by having $\overline{CS}$ and $\overline{CAS}$ low while holding $\overline{RAS}$ and $\overline{WE}$ high at the rising edge of the clock. The address inputs determine the starting column address for the burst. The delay from the start of the command until the data from the first cell appears on the outputs is equal to the value of the read latency (RL). The data strobe output (DQS) is driven low one clock cycle before valid data (DQ) is driven onto the data bus. The first bit of the burst is synchronized with the rising edge of the data strobe (DQS). Each subsequent data-out appears on the DQ pin in phase with the DQS signal in a source synchronous manner. The RL is equal to an additive latency (AL) plus $\overline{CAS}$ latency (CL). The CL is defined by the Mode Register Set (MRS). The AL is defined by the Extended Mode Register Set (EMRS).

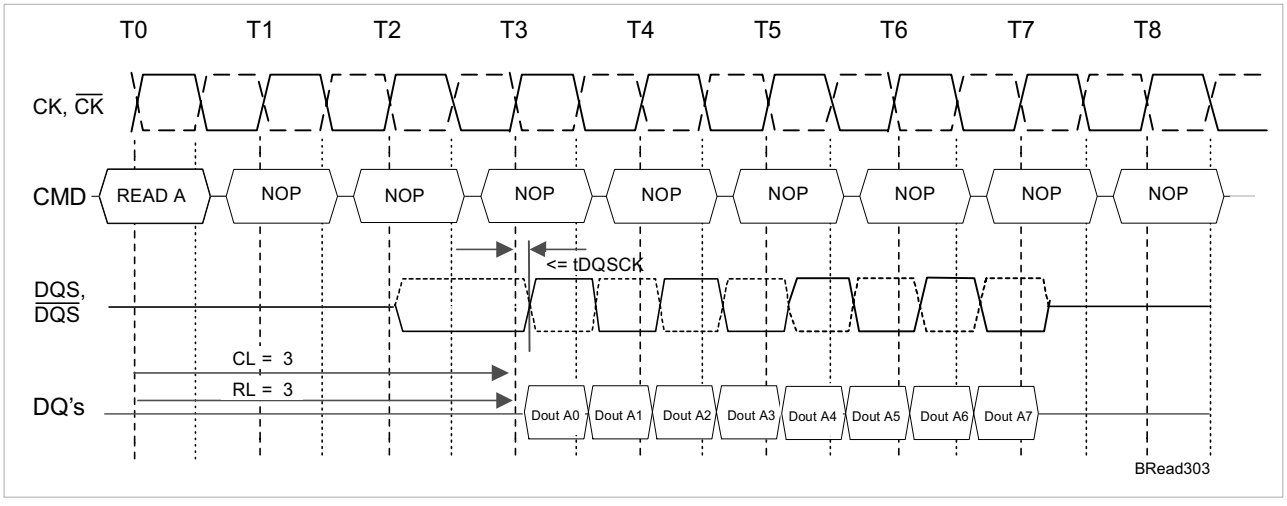
Basic Burst Read Timing



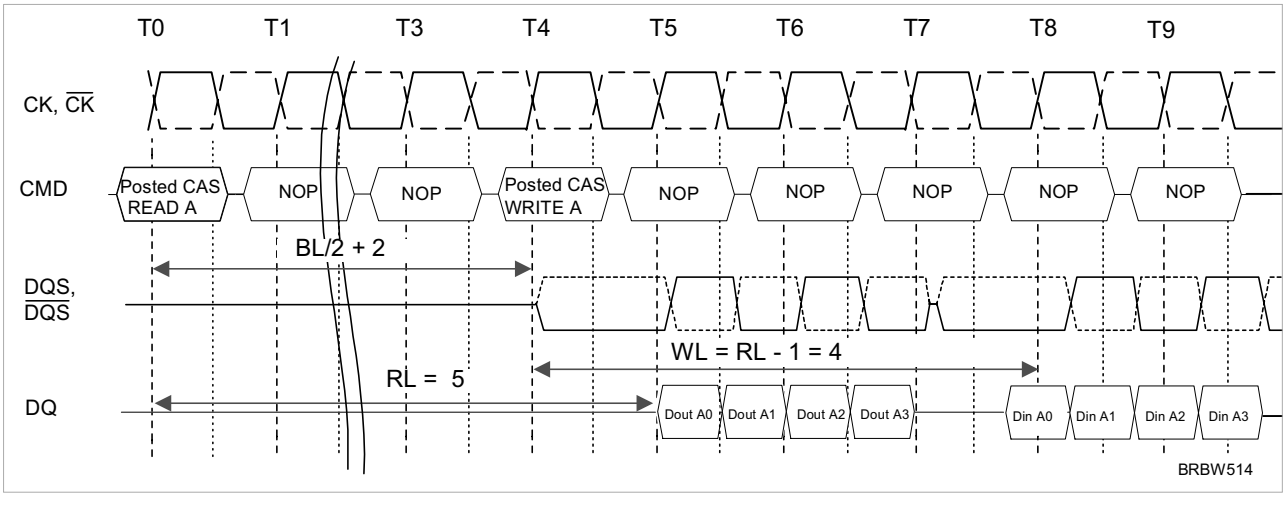
Burst Read Operation: RL = 5 (AL = 2, CL = 3, BL = 4)



Burst Read Operation: RL = 3 (AL = 0, CL = 3, BL = 8)

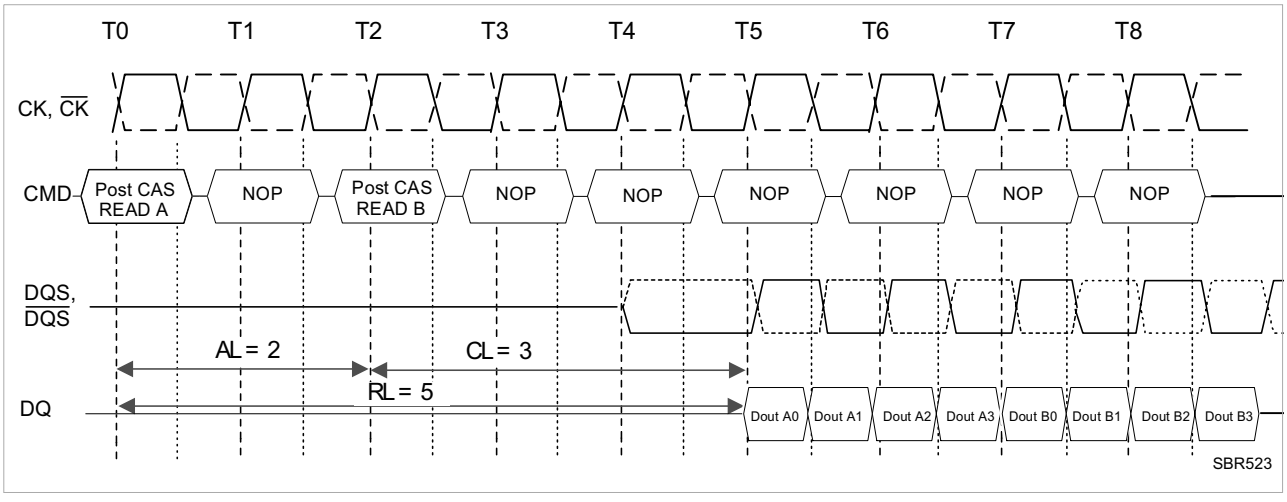


Burst Read followed by Burst Write : RL = 5, WL = (RL-1) = 4, BL = 4



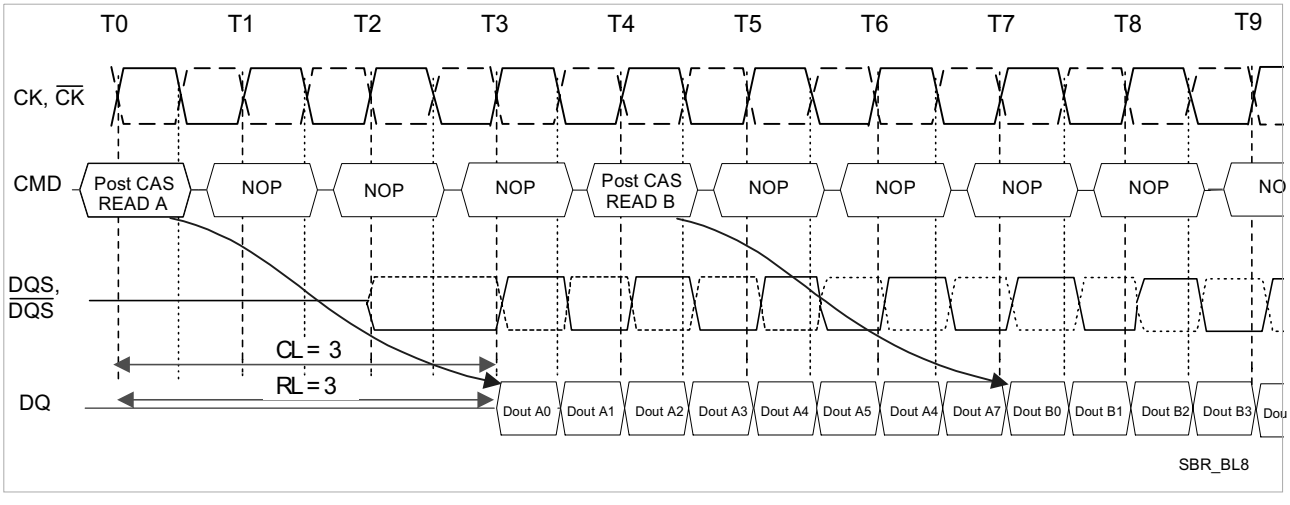
The minimum time from the burst read command to the burst write command is defined by a read-to-write turn-around time, which is BL/2 + 2 clocks.

Seamless Burst Read Operation : RL = 5, AL = 2, CL = 3, BL = 4



The seamless burst read operation is supported by enabling a read command at every BL / 2 number of clocks. This operation is allowed regardless of same or different banks as long as the banks are activated.

Seamless Burst Read Operation : RL = 3, AL = 0, CL = 3, BL = 8 (non interrupting)

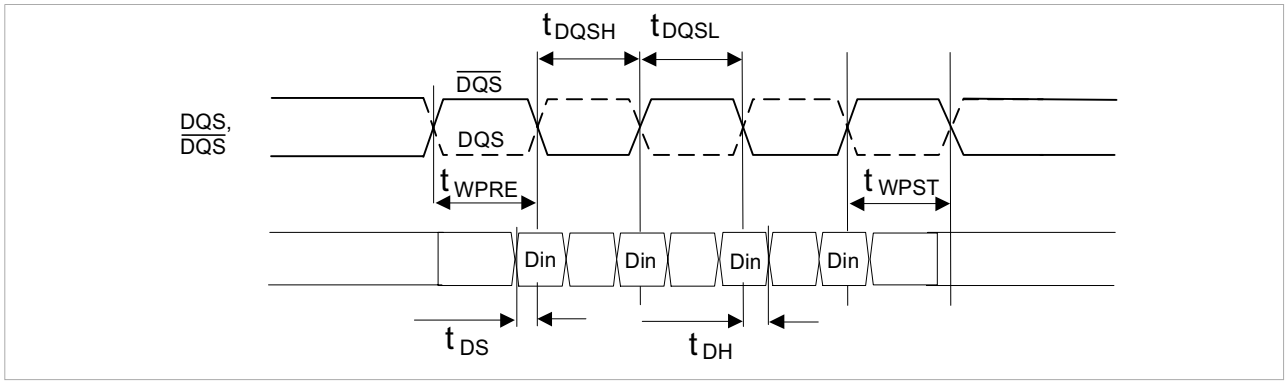


The seamless, non interrupting 8-bit burst read operation is supported by enabling a read command at every BL / 2 number of clocks. This operation is allowed regardless of same or different banks as long as the banks are activated.

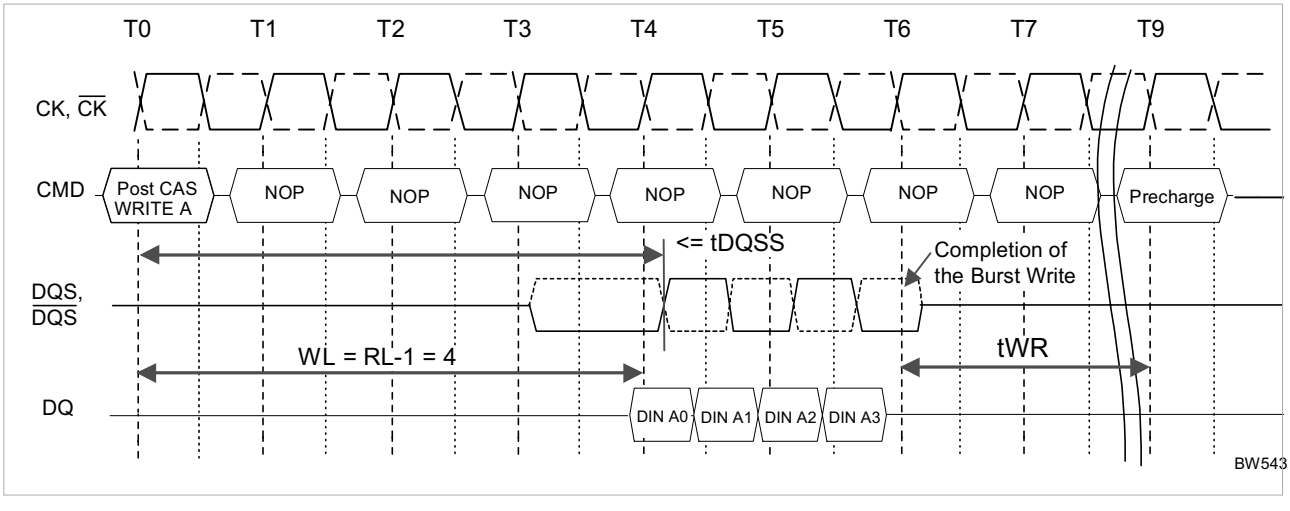
Burst Write Command

The Burst Write command is initiated by having $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ low while holding $\overline{RAS}$ high at the rising edge of the clock. The address inputs determine the starting column address. Write latency (WL) is defined by a read latency (RL) minus one and is equal to (AL + CL -1). A data strobe signal (DQS) should be driven low (preamble) one clock prior to the WL. The first data bit of the burst cycle must be applied to the DQ pins at the first rising edge of the DQS following the preamble. The tDQSS specification must be satisfied for write cycles. The subsequent burst bit data are issued on successive edges of the DQS until the burst length is completed. When the burst has finished, any additional data supplied to the DQ pins will be ignored. The DQ signal is ignored after the burst write operation is complete. The time from the completion of the burst write to bank precharge is named “write recovery time” (tWR) and is the time needed to store the write data into the memory array. tWR is an analog timing parameter (see the AC table in this specification) and is not the programmed value for WR in the MRS.

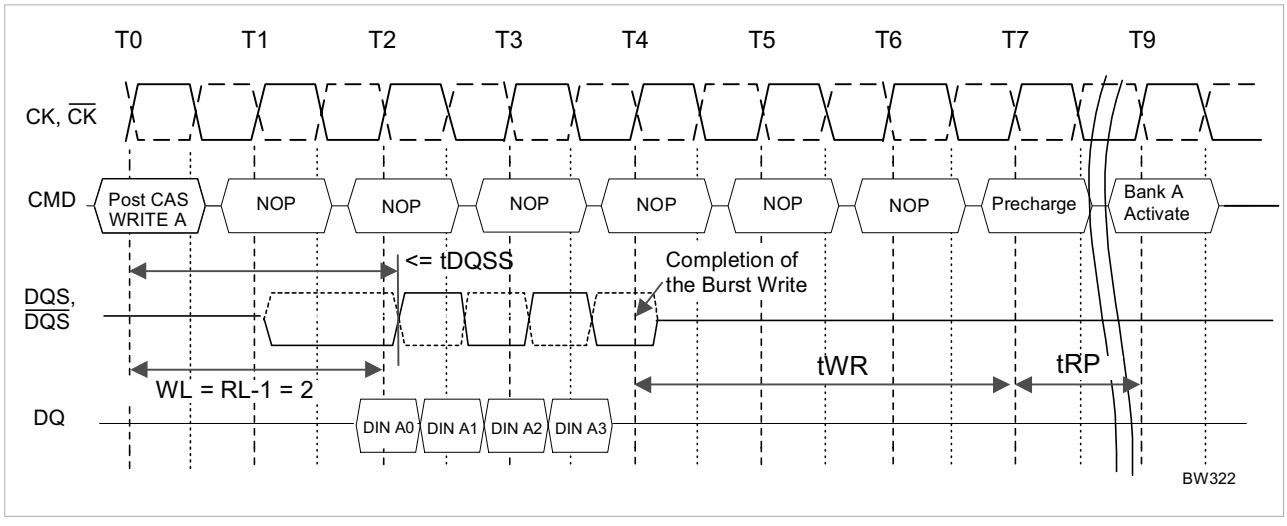
Basic Burst Write Timing



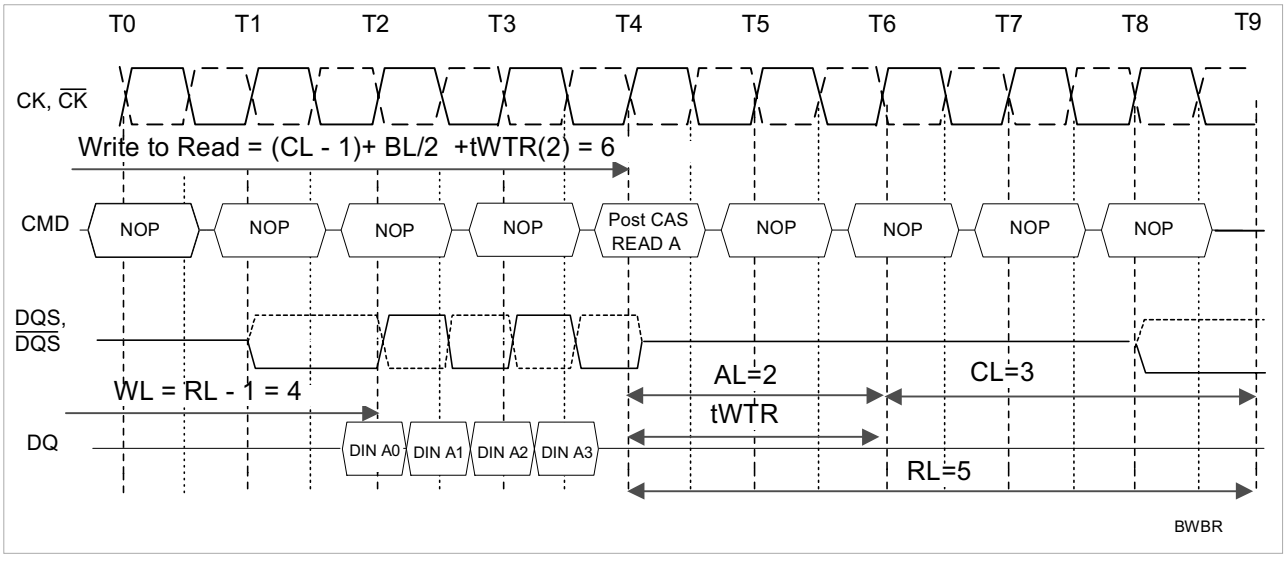
Burst Write Operation : RL = 5 (AL = 2, CL = 3), WL = 4, BL = 4



Burst Write Operation : RL = 3 (AL = 0, CL = 3), WL = 2, BL = 4



Burst Write followed by Burst Read : RL = 5 (AL = 2, CL = 3), WL = 4, tWTR = 2, BL = 4

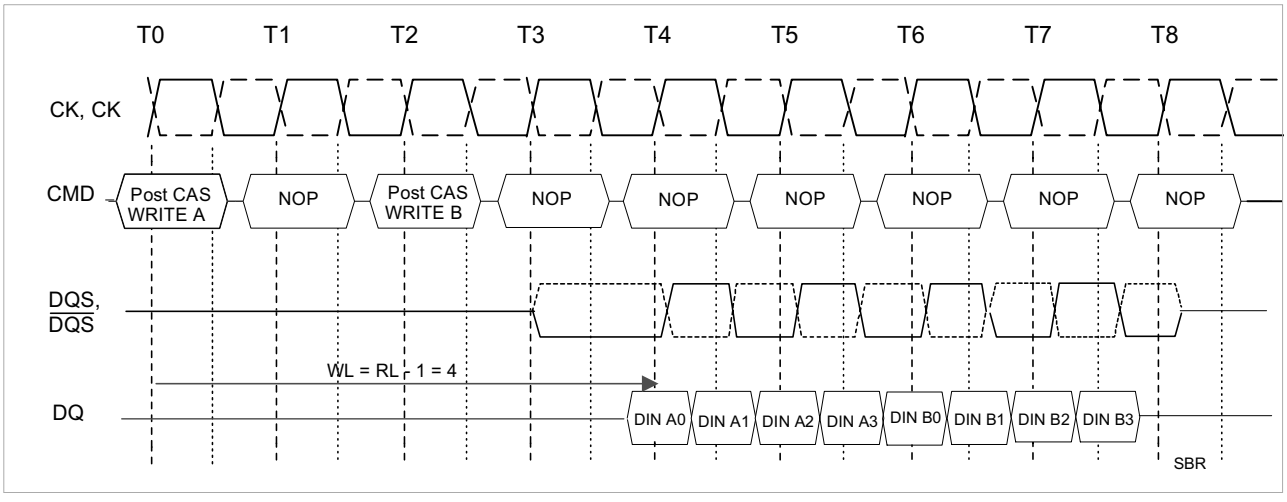


The minimum number of clocks from the burst write command to the burst read command is

(CL - 1) +BL/2 + tWTR

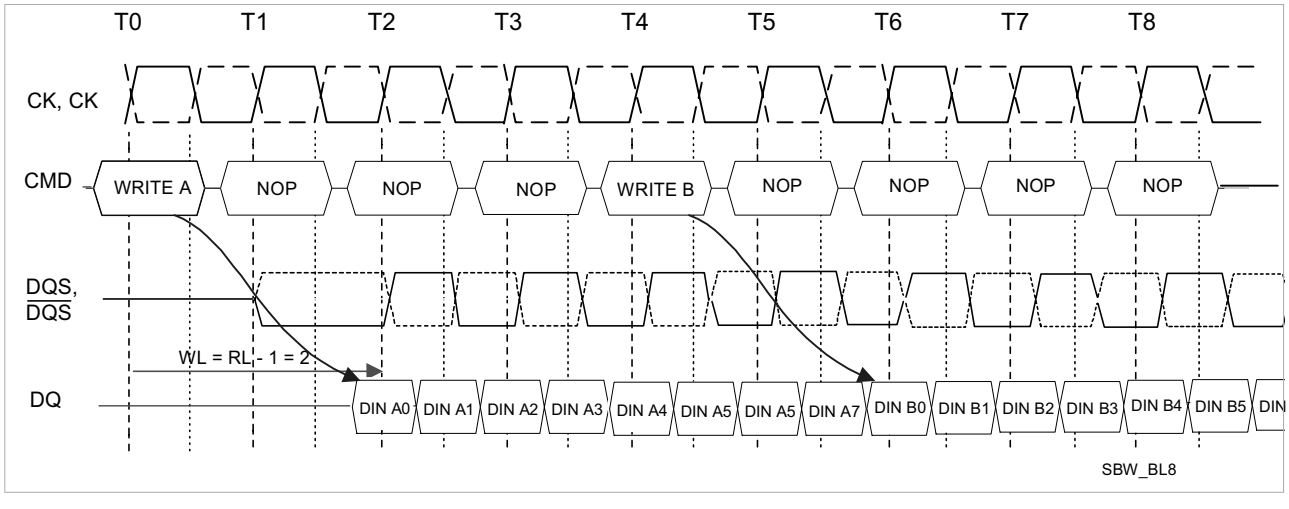
where tWTR is the write-to-read turn-around time tWTR expressed in clock cycles. The tWTR is not a write recovery time (tWR) but the time required to transfer 4 bit write data from the input buffer into sense amplifiers in the array.

Seamless Burst Write Operation: RL=5, WL=4, BL=4



The seamless burst write operation is supported by enabling a write command every BL / 2 number of clocks. This operation is allowed regardless of same or different banks as long as the banks are activated.

Seamless Burst Write Operation: RL=3, WL=2, BL=8, noninterrupting

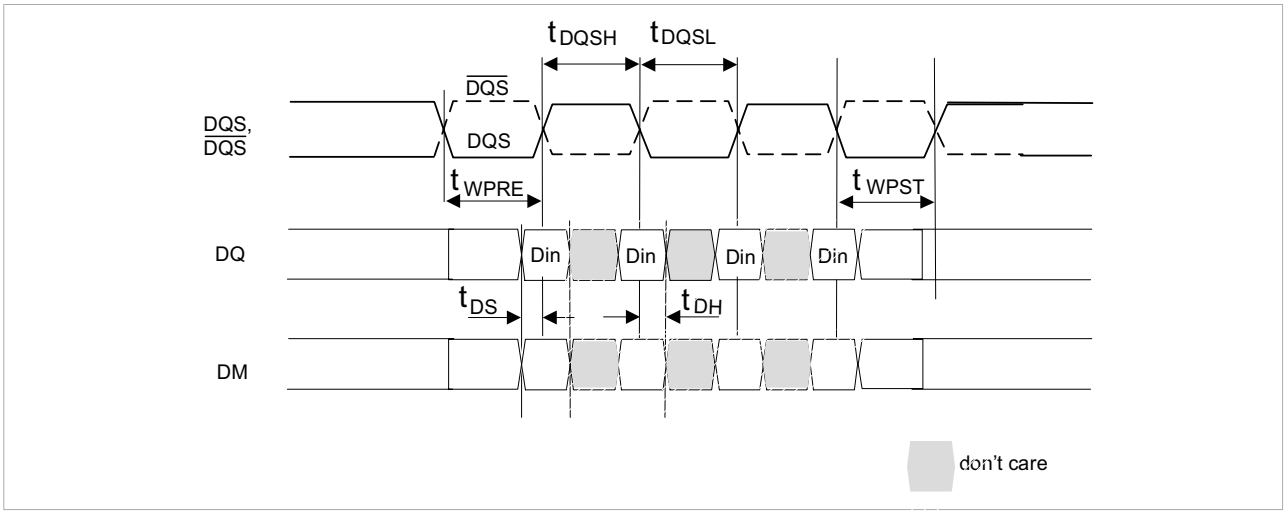


The seamless, non interrupting 8-bit burst write operation is supported by enabling a write command at every BL / 2 number of clocks. This operation is allowed regardless of same or different banks as long as the banks are activated.

Write Data Mask

One write data mask input (DM) for x4 and x8 components and two write data mask inputs (LDM, UDM) for x16 components are supported on DDR2 SDRAMs, consistent with the implementation on DDR SDRAMs. It has identical timings on write operations as the data bits, and though used in a uni-directional manner, is internally loaded identically to data bits to insure matched system timing. Data mask is not used during read cycles. If DM is high during a write burst coincident with the write data, the write data bit is not written to the memory. For x8 components the DM function is disabled, when RDQS / $\overline{RDQS}$ are enabled by EMRS.

Write Data Mask Timing



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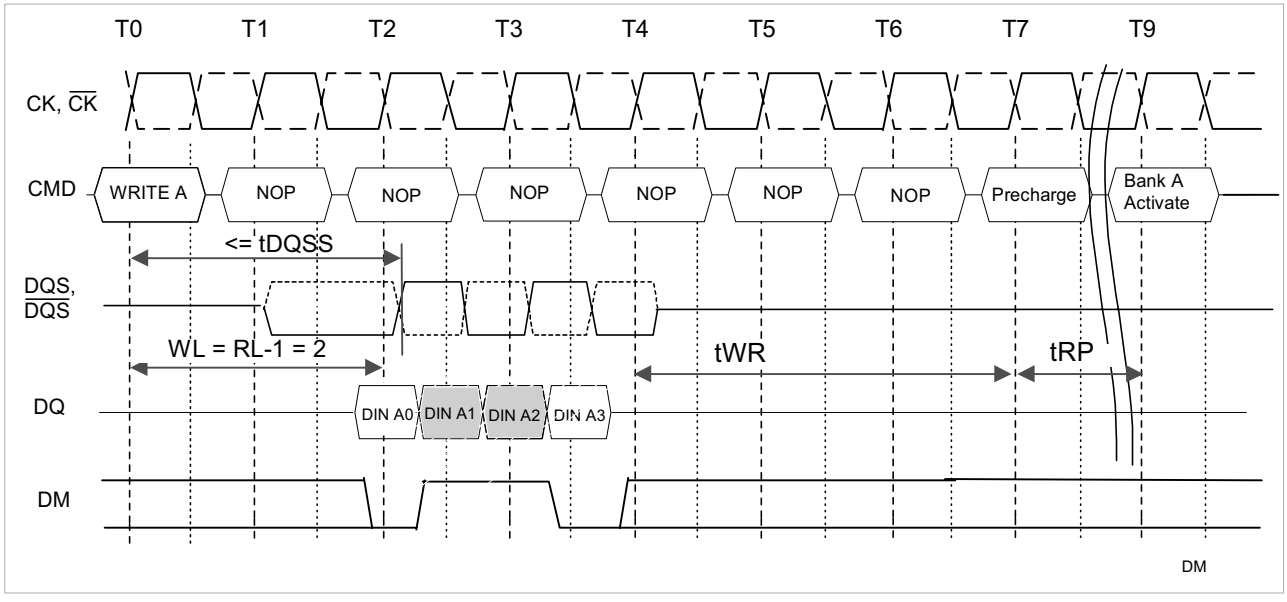
Burst Write Operation with Data Mask : RL = 3 (AL = 0, CL = 3), WL = 2, tWR = 3 , BL = 4

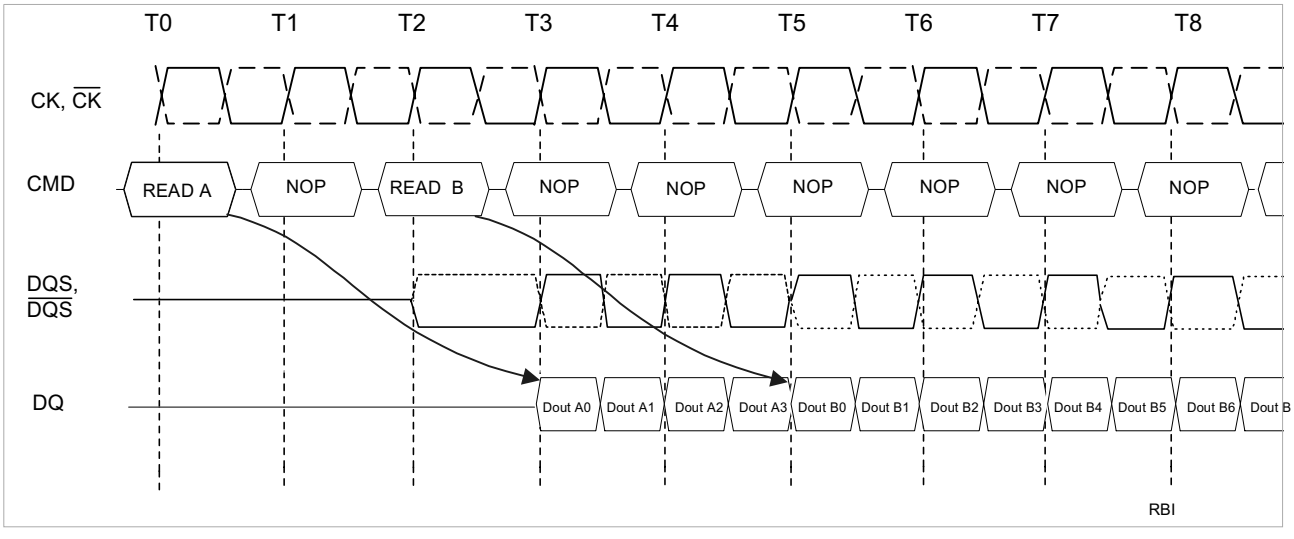


Burst Interruption

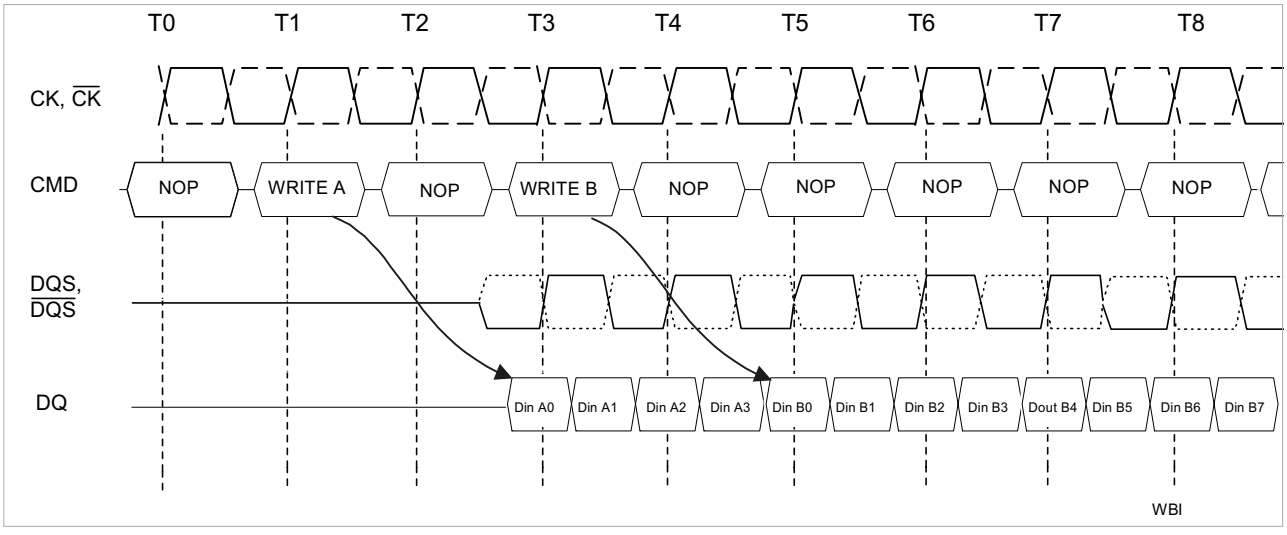
Interruption of a read or write burst is prohibited for burst length of 4 and only allowed for burst length of 8 under the following conditions:

1. A Read Burst of 8 can only be interrupted by another Read command. Read burst interruption by a Write or Precharge Command is prohibited.
2. A Write Burst of 8 can only be interrupted by another Write command. Write burst interruption by a Read or Precharge Command is prohibited.
3. Read burst interrupt must occur exactly two clocks after the previous Read command. Any other Read burst interrupt timings are prohibited.
4. Write burst interrupt must occur exactly two clocks after the previous Write command. Any other Read burst interrupt timings are prohibited.
5. Read or Write burst interruption is allowed to any bank inside the DDR2 SDRAM.
6. Read or Write burst with Auto-Precharge enabled is not allowed to be interrupted.
7. Read burst interruption is allowed by a Read with Auto-Precharge command.
8. Write burst interruption is allowed by a Write with Auto-Precharge command.
9. All command timings are referenced to burst length set in the mode register. They are not referenced to the actual burst. For example, Minimum Read to Precharge timing is AL + BL/2 where BL is the burst length set in the mode register and not the actual burst (which is shorter because of interrupt). Minimum Write to Precharge timing is WL + BL/ 2 + tWR, where tWR starts with the rising clock after the un-interrupted burst end and not form the end of the actual burst end.

Read Burst Interrupt Timing Example : (CL = 3, AL = 0, RL = 3, BL = 8)



Write Burst Interrupt Timing Example : (CL = 3, AL = 0, WL = 2, BL = 8)



Precharge Command

The Precharge Command is used to precharge or close a bank that has been activated. The Precharge Command is triggered when $\overline{CS}$, $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at the rising edge of the clock. The Precharge Command can be used to precharge each bank independently or all banks simultaneously. Three address bits A10, BA1 and BA0 are used to define which bank to precharge when the command is issued.

Bank Selection for Precharge by Address Bits

A10	BA1	BA0	Precharge Bank(s)
LOW	LOW	LOW	Bank 0 only
LOW	LOW	HIGH	Bank 1 only
LOW	HIGH	LOW	Bank 2 only
LOW	HIGH	HIGH	Bank 3 only
HIGH	Don't Care	Don't Care	all banks

Burst Read Operation Followed by a Precharge

The following rules apply as long as the tRTP timing parameter - Internal Read to Precharge Command delay time - is less or equal two clocks, which is the case for operating frequencies less or equal 266 Mhz (DDR2 400 and 533 speed sorts):

Minimum Read to Precharge command spacing to the same bank = AL + BL/2 clocks. For the earliest possible precharge, the precharge command may be issued on the rising edge which is "Additive Latency (AL) + BL/2 clocks" after a Read Command, as long as the minimum tRAS timing is satisfied.

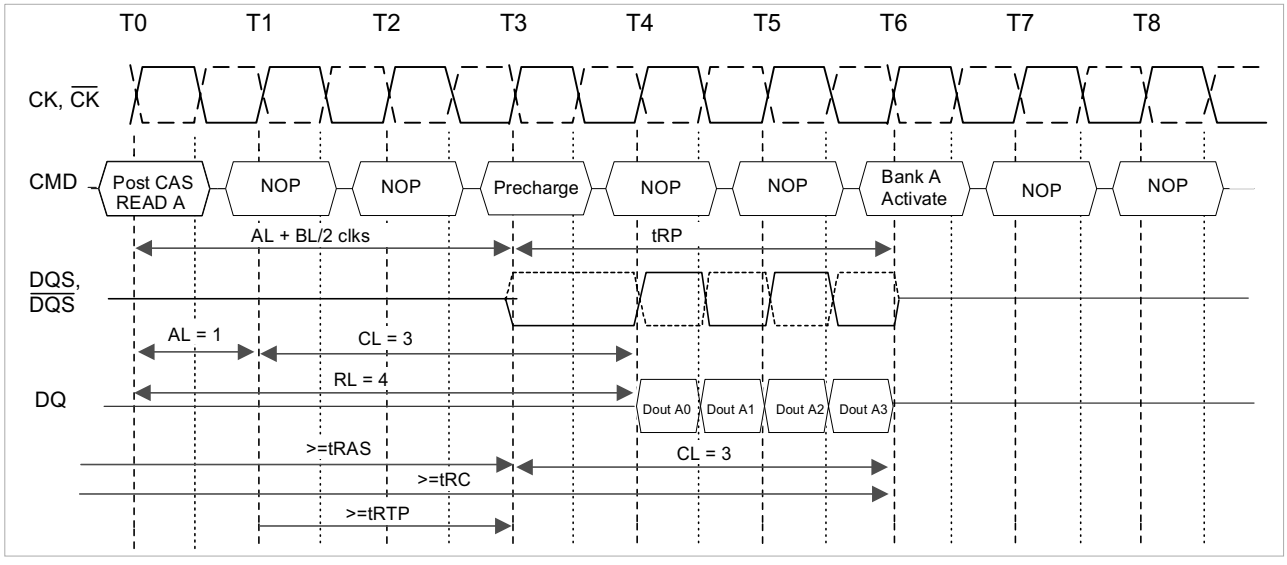
A new bank active command may be issued to the same bank if the following two conditions are satisfied simultaneously:

(1) The RAS precharge time (tRP) has been satisfied from the clock at which the precharge begins.

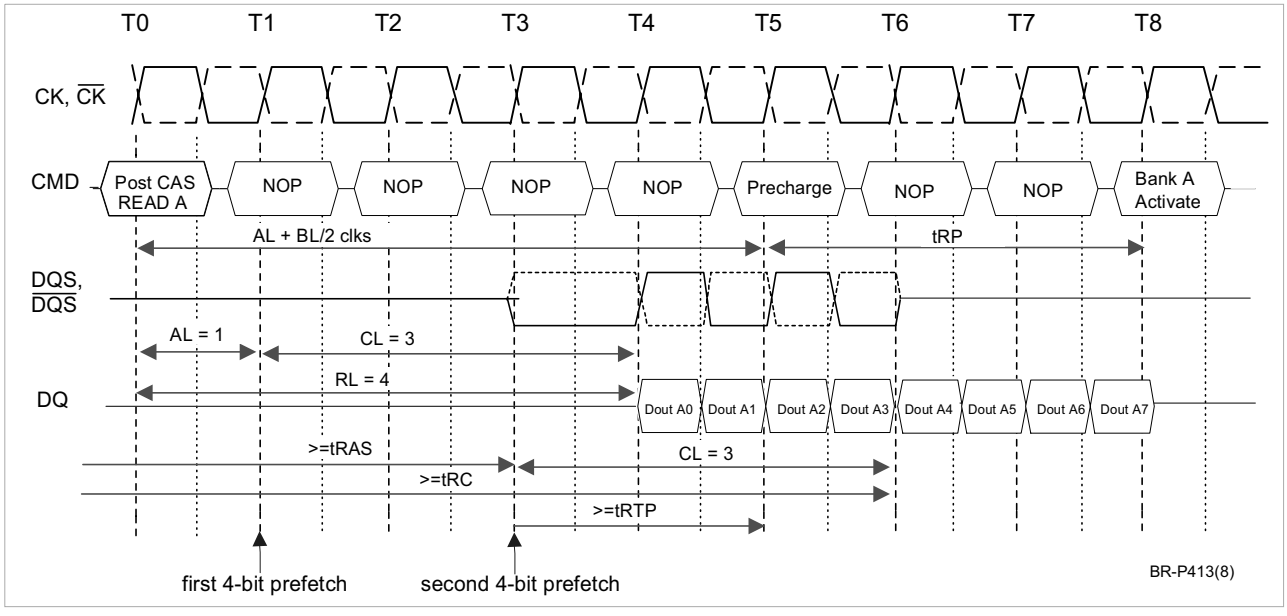
(2) The RAS cycle time (tRCmin) from the previous bank activation has been satisfied.

For operating frequencies higher than 266 MHz, tRTP becomes > 2 clocks and one additional clock cycle has to be added for the minimum Read to Precharge command spacing, which now becomes AL + BL/2 + 1 clocks.

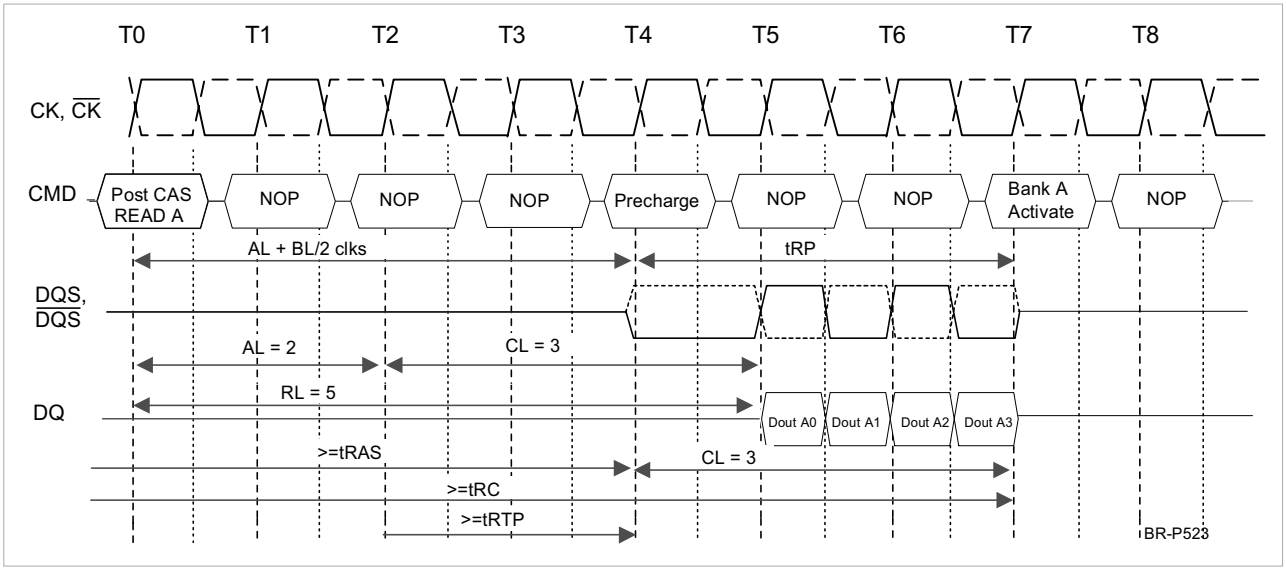
Burst Read Operation Followed by Precharge: RL = 4 (AL = 1, CL = 3), BL = 4, tRTP <= 2 clocks



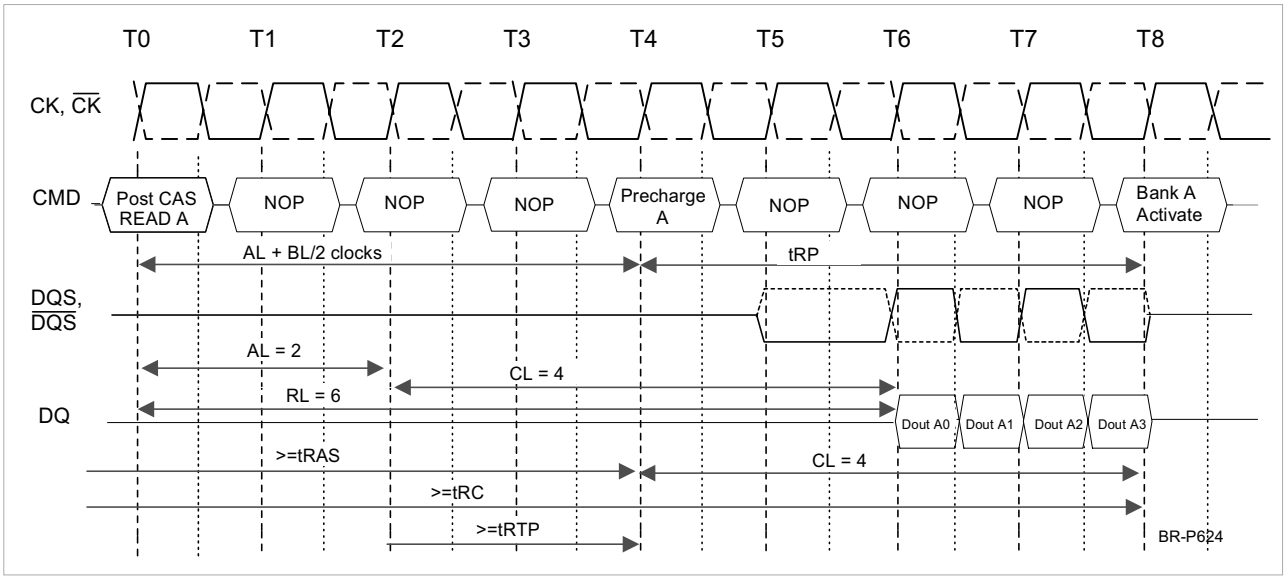
Burst Read Operation Followed by Precharge: RL = 4 (AL = 1, CL = 3), BL = 8, tRTP <= 2 clocks



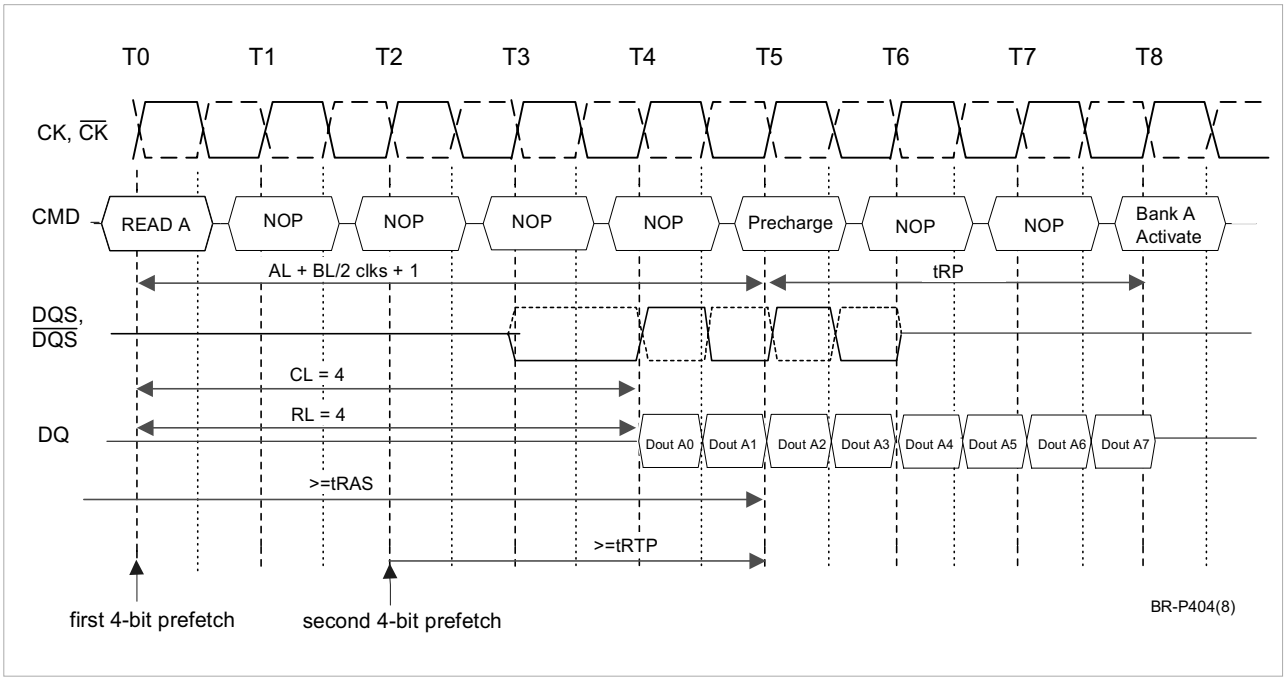
Burst Read operation Followed by Precharge: RL=5(AL=2, CL=3), BL=4, tRTP<=2 clocks



Burst Read operation Followed by Precharge: RL=6(AL=2, CL=4), BL=4, tRTP<=2 clocks



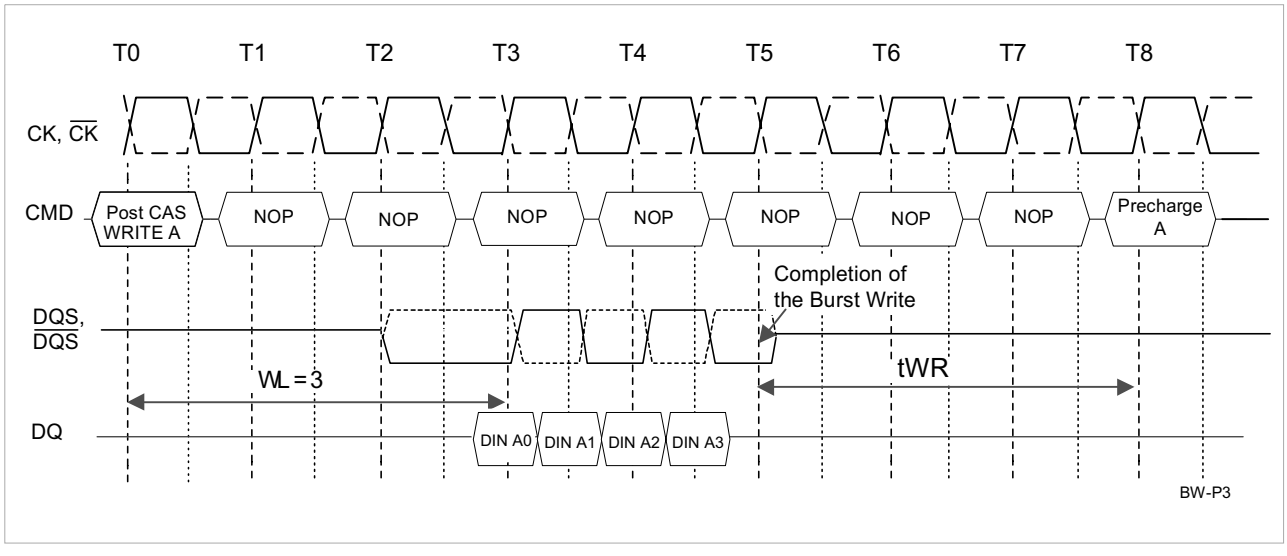
Burst Read Operation Followed by Precharge: RL=4, (AL=0, CL=4), BL=8, tRTP>2 clocks



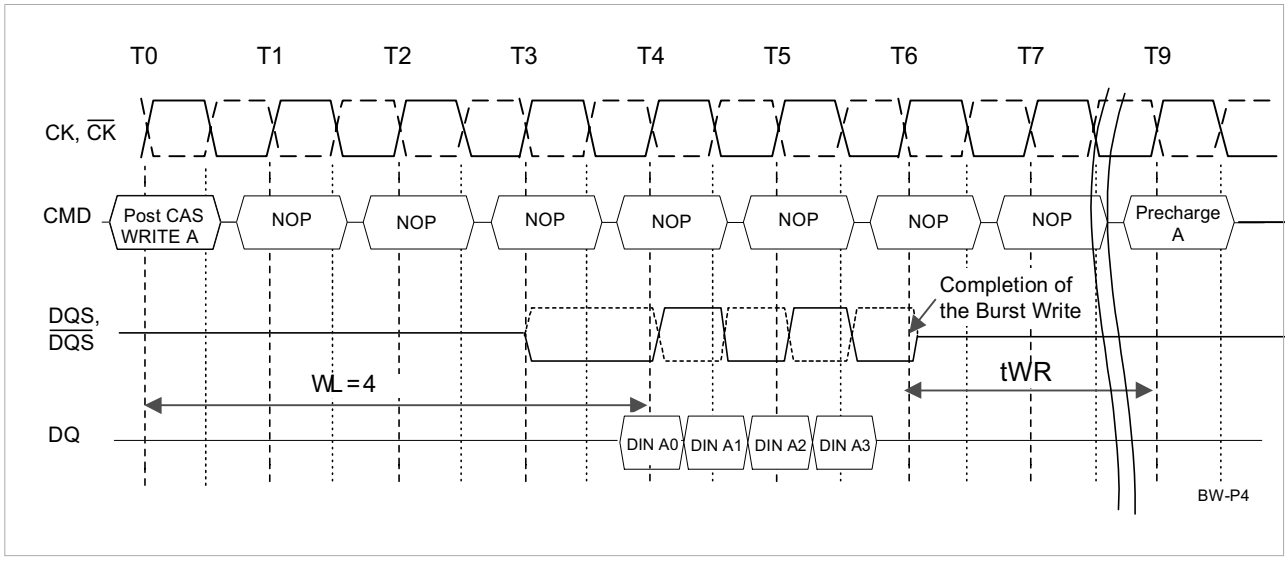
Burst Write followed by Precharge

Minimum Write to Precharge command spacing to the same bank = **WL + BL/2 + tWR**. For write cycles, a delay must be satisfied from the completion of the last burst write cycle until the Precharge command can be issued. This delay is known as a write recovery time (t WR) referenced from the completion of the burst write to the Precharge command. No Precharge command should be issued prior to the tWR delay, as DDR2 SDRAM does not support any burst interrupt by a Precharge command. tWR is an analog timing parameter (see the AC table in this datasheet) and is not the programmed value for tWR in the MRS.

Burst Write followed by Precharge : WL = (RL - 1) = 3, BL = 4, tWR = 3



Burst Write followed by Precharge : WL = (RL - 1) = 4, BL = 4, tWR = 3



Auto-Precharge Operation

Before a new row in an active bank can be opened, the active bank must be precharged using either the Precharge Command or the Auto-Precharge function. When a Read or a Write Command is given to the DDR2 SDRAM, the $\overline{CAS}$ timing accepts one extra address, column address A10, to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle. If A10 is low when the Read or Write Command is issued, then normal Read or Write burst operation is executed and the bank remains active at the completion of the burst sequence. If A10 is high when the Read or Write Command is issued, then the Auto-Precharge function is enabled. During Auto-Precharge, a Read Command will execute as normal with the exception that the active bank will begin to precharge internally on the rising edge which is CAS Latency (CL) clock cycles before the end of the read burst. Auto-Precharge is also implemented for Write Commands.The precharge operation engaged by the Auto-Precharge command will not begin until the last datga of the write burst sequence is properly stored in the memory array. This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon CAS Latency) thus improving system performance for random data access. The RAS lockout circuit internally delays the Precharge operation until the array restore operation has been completed so that the Auto-Precharge command may be issied with any read or write command.

Burst Read with Auto-Precharge

If A10 is high when a Read Command is issued, the Read with Auto-Precharge function is engaged. The DDR2 SDRAM starts an Auto-Precharge operation on the rising edge which is (AL + BL/2) cycles later from the Read with AP command if tRAS(min) and tRTP are satisfied. If tRAS(min) is not satisfied at the edge, the start point of Auto-Precharge operation will be delayed until tRAS(min) is satisfied. If tRTP(min) is not satisfied at the edge, the start point of Auto-precharge operation will be delayed until tRTP(min) is satisfied.
In case the internal precharge is pushed out by tRTP, tRP starts at the point where the internal precharge happens (not at the next rising clock edge after this event). So for BL = 4 the minimum time from Read with Auto-Precharge to the next Activate command becomes AL + tRTP + tRP. For BL = 8 the time from Read with Auto-Precharge to the next Activate command is AL + 2 + tRTP + tRP. Note that both parameters tRTP and tRP have to be rounded up to the next integer value. In any event internal precharge does not start earlier than two clocks after the last 4-bit prefetch.

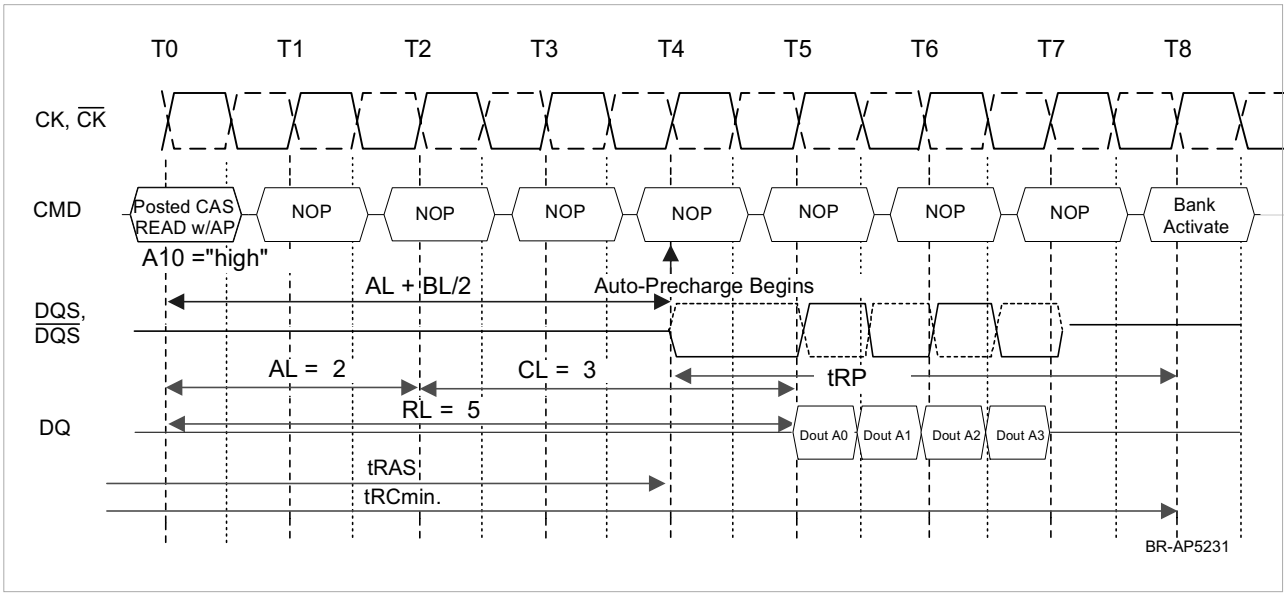
A new bank active (command) may be issued to the same bank if the following two conditions are satisfied simultaneously:

(1) The $\overline{RAS}$ precharge time (tRP) has been satisfied from the clock at which the Auto-Precharge begins.

(2) The $\overline{RAS}$ cycle time (tRC) from the previous bank activation has been satisfied.

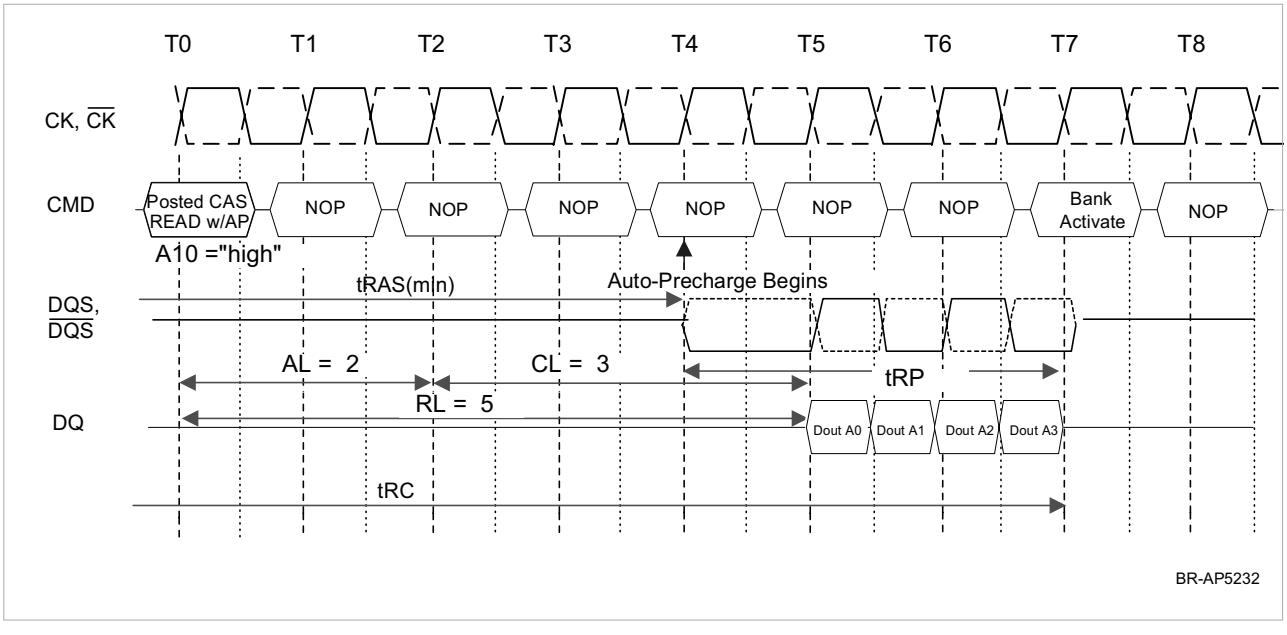
Burst Read with Auto-Precharge followed by an activation to the Same Bank (tRC Limit)

RL = 5 (AL = 2, CL = 3), BL = 4, tRTP <= 2 clocks



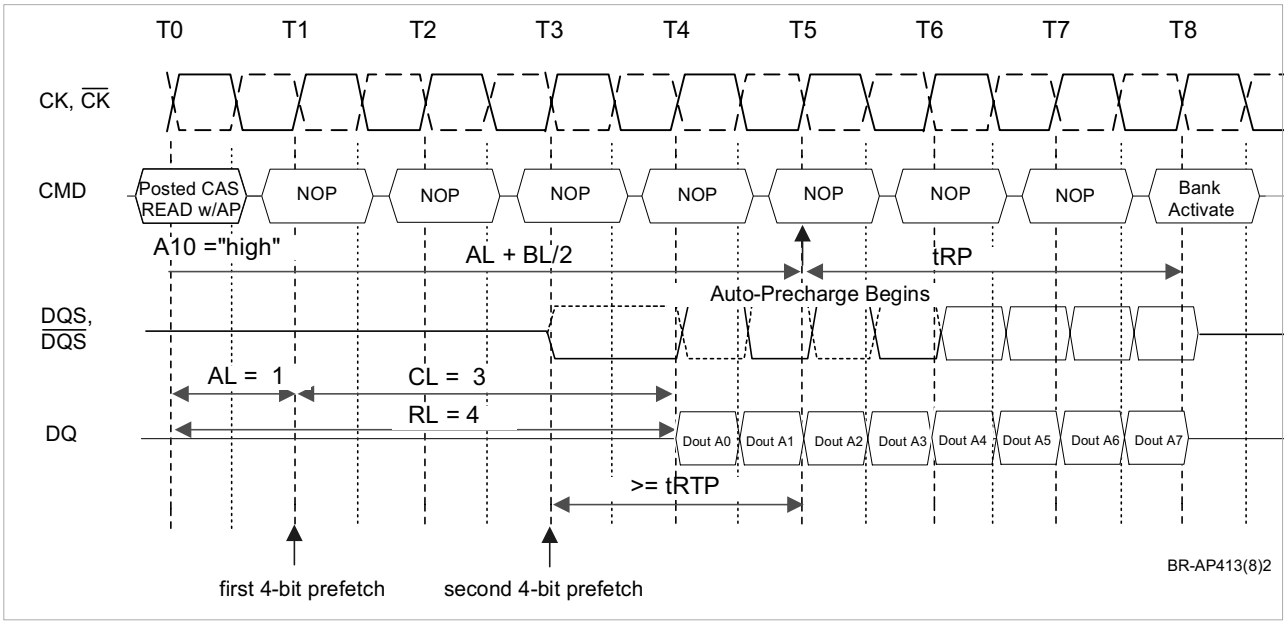
Burst Read with Auto-Precharge followed by an Activation to the Same Bank (tRAS Limit):

RL = 5 (AL = 2, CL = 3), BL = 4, tRTP <= 2 clocks



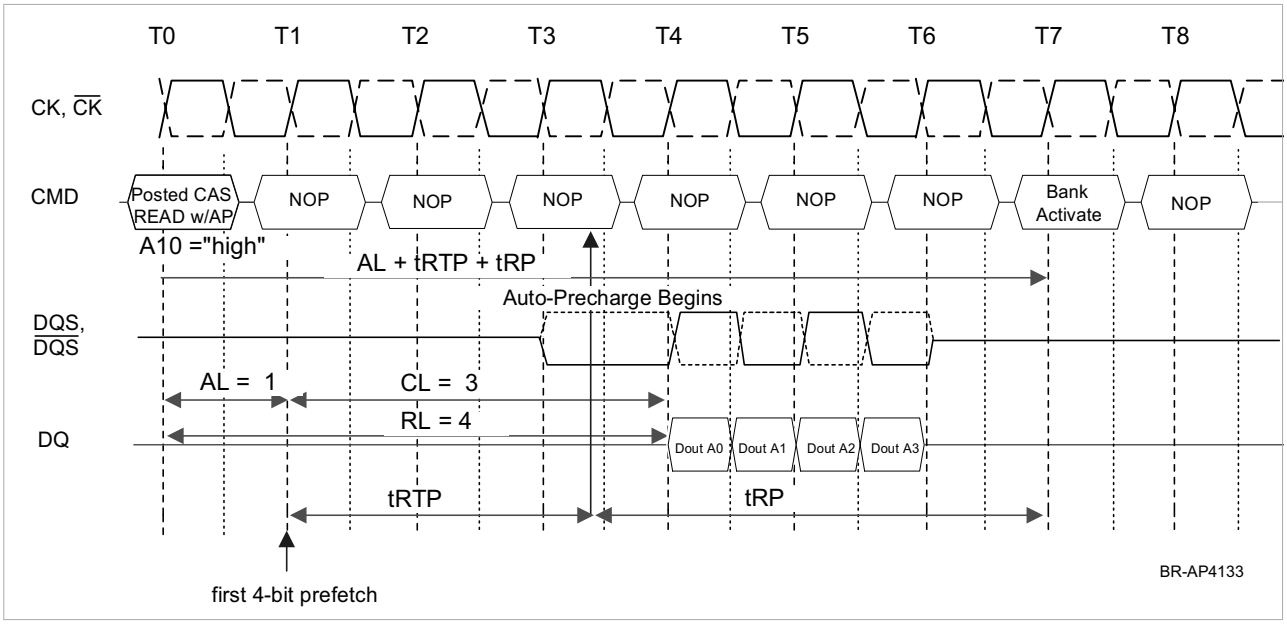
Burst Read with Auto-Precharge followed by an Activation to the Same Bank:

RL=4(AL=1, CL=3), BL=8, tRTP<=2 clocks



Burst Read with Auto-Precharge followed by an Activation to the Same Bank:

RL=4(AL=1, CL=3), BL=8, tRTP>2 clocks



Burst Write with Auto-Precharge

If A10 is high when a Write Command is issued, the Write with Auto-Precharge function is engaged. The DDR2 SDRAM automatically begins precharge operation after the completion of the write burst plus the write recovery time delay (WR), programmed in the MRS register, as long as tRAS is satisfied. The bank undergoing Auto-Precharge from the completion of the write burst may be reactivated if the following two conditions are satisfied.

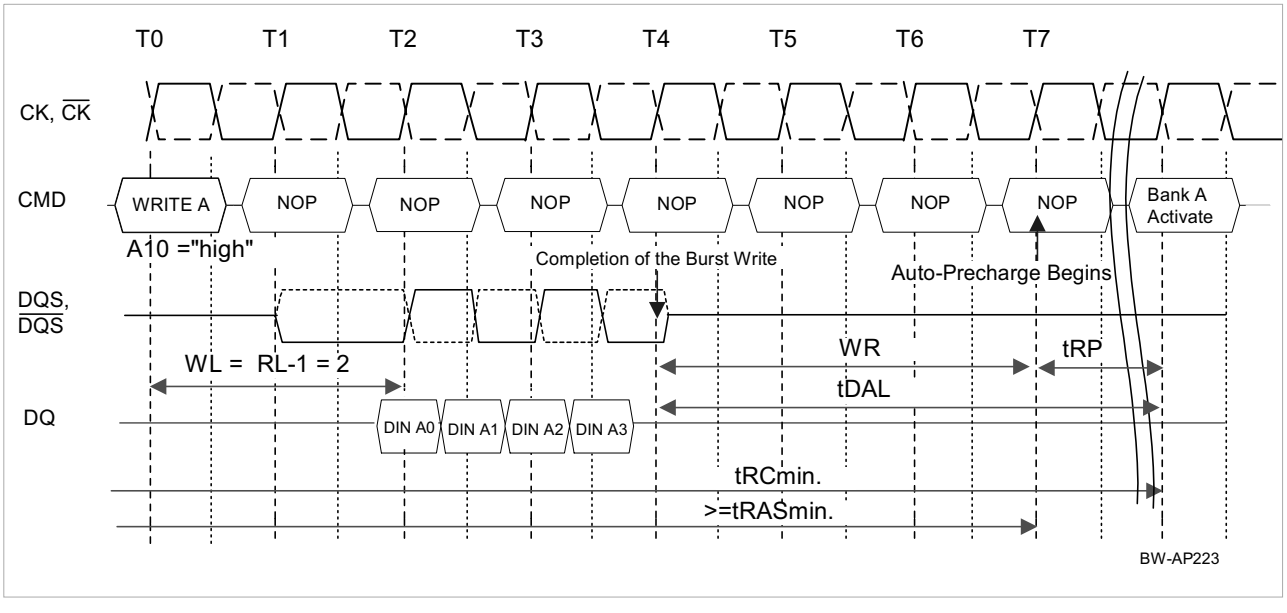
(1) The last data-in to bank activate delay time (tDAL = WR + tRP) has been satisfied.

(2) The RAS cycle time (tRC) from the previous bank activation has been satisfied.

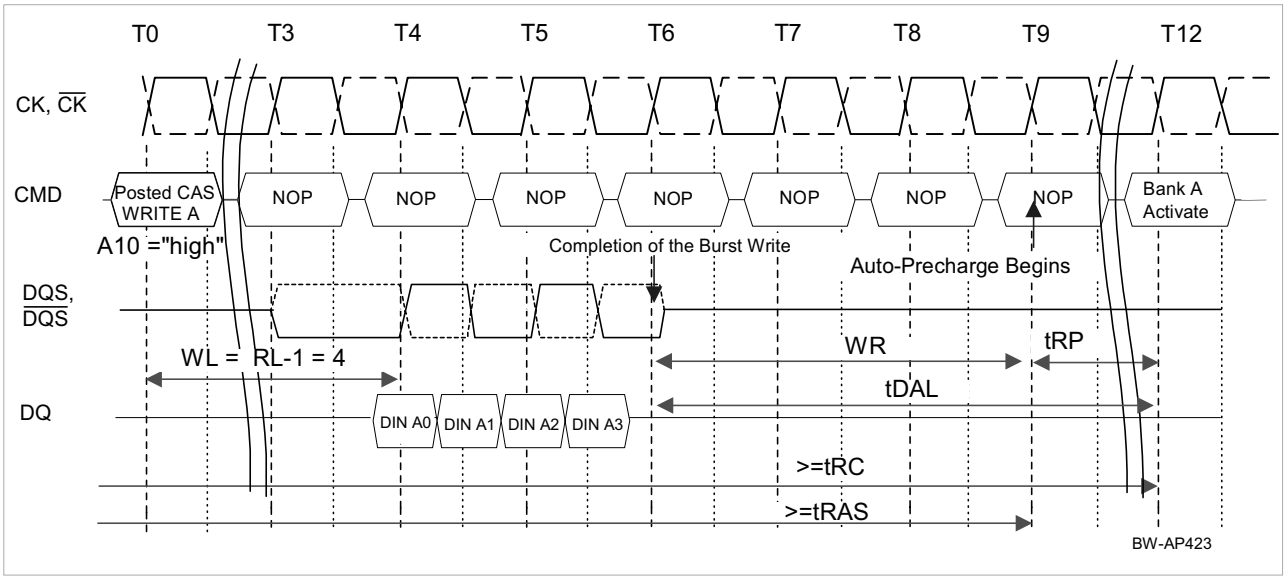
In DDR2 SDRAMs the write recovery time delay (WR) has to be programmed into the MRS mode register. As long as the analog twr timing parameter is not violated, WR can be programmed between 2 and 6 clock cycles. Minimum Write to Activate command spacing to the same bank = **WL + BL/2 + tDAL.**

Examples:

Burst Write with Auto-Precharge (tRC Limit) : WL = 2, tDAL = 6 (WR = 3, tRP = 3) , BL = 4



Burst Write with Auto-Precharge (WR+tRP Limit): WL=4, tDAL=6(WR=3, tRP=3), BL=4



Concurrent Auto-Precharge

DDR2 devices support the “concurrent Auto-Precharge” feature. A read with Auto-Precharge enabled, or a write with Auto-Precharge enabled, may be followed by any command to the other bank, as long as that command does not interrupt the read or write data transfer, and all other related limitations (e.g. contention between Read data and Write data must be avoided externally and on the internal data bus.

The minimum delay from a read or write command with Auto-Precharge enabled, to a command to a different bank, is summarized in the table below. As defined, the WL = RL - 1 for DDR2 devices which allows the command gap and corresponding data gaps to be minimized.

From Command	To Command (different bank, non-interrupting command)	Minimum Delay with Concurrent Auto-Precharge Support	Units
WRITE w/AP	Read or Read w/AP	(CL -1) + (BL/2) + tWTR	tCK
	Write ot Write w/AP	BL/2	tCK
	Precharge or Activate	1	tCK
Read w/AP	Read or Read w/AP	BL/2	tCK
	Write or Write w/AP	BL/2 + 2	tCK
	Precharge or Activate	1	tCK

Refresh

SDRAMs require a refresh of all rows in any rolling 64 ms interval. Each refresh is generated in one of two ways : by an explicit Auto-Refresh command, or by an internally timed event in Self-Refresh mode. Dividing the number of device rows into the rolling 64 ms interval defined the average refresh interval tREFI, which is a guideline to controlles for distributed refresh timing. For example, a 512Mbit DDR2 SDRAM has 8192 rows resulting in a tREFI of 7,8 µs.

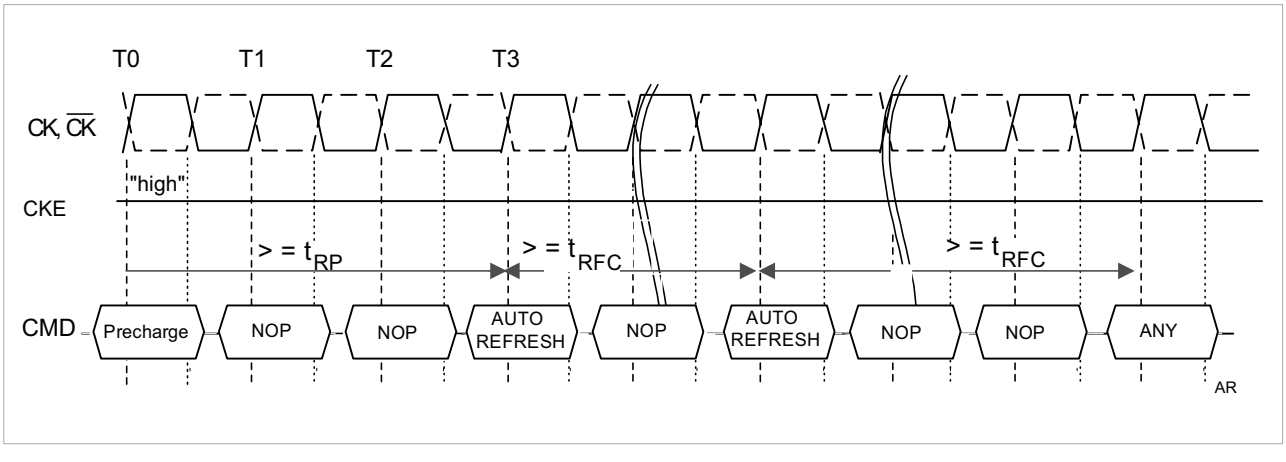
Auto-Refresh Command

Auto-Refresh is used during normal operation of the DDR2 SDRAMs. This command is nonpersistent, so it must be issued each time a refresh is required. The refresh addressing is generated by the internal refresh controller. This makes the address bits ”Don’t Care” during an Auto-Refresh command. The DDR2 SDRAM requires Auto-Refresh cycles at an average periodic interval of tREFI (maximum).

When $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ are held low and $\overline{WE}$ high at the rising edge of the clock, the chip enters the Auto-Refresh mode. All banks of the SDRAM must be precharged and idle for a minimum of the Precharge time (t_{RP}) before the Auto-Refresh Command can be applied. An internal address counter supplies the addresses during the refresh cycle. No control of the external address bus is required once this cycle has started.

When the refresh cycle has completed, all banks of the SDRAM will be in the precharged (idle) state. A delay between the Auto-Refresh Command and the next Activate Command or subsequent Auto-Refresh Command must be greater than or equal to the Auto-Refresh cycle time (t_{RFC}).

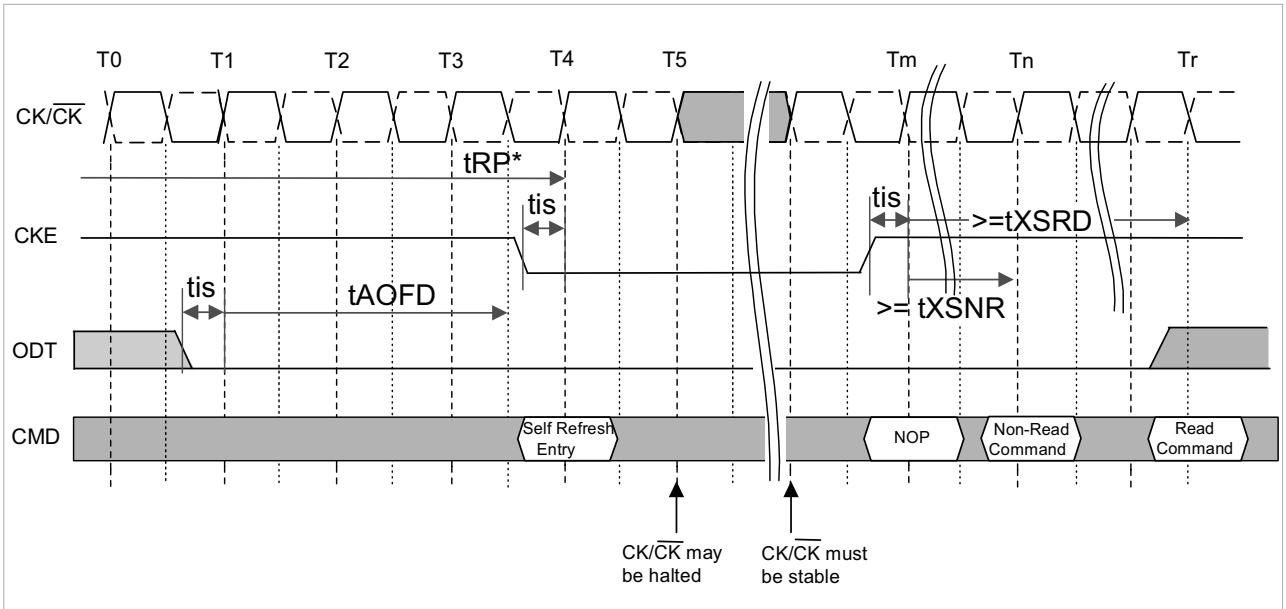
To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight Auto-Refresh commands can be posted to any given DDR2 SDRAM, meaning that the maximum absolute interval between any Auto-Refresh command and the next Auto-Refresh command is 9 * tREFI.



Self-Refresh Command

The Self-Refresh command can be used to retain data, even if the rest of the system is powered down. When in the Self-Refresh mode, the DDR2 SDRAM retains data without external clocking.

The DDR2 SDRAM device has a built-in timer to accommodate Self-Refresh operation. The Self-Refresh Command is defined by having $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE held low with $\overline{WE}$ high at the rising edge of the clock. ODT must be turned off before issuing Self Refresh command, by either driving ODT pin low or using EMRS command. Once the command is registered, CKE must be held low to keep the device in Self-Refresh mode. When the DDR2 SDRAM has entered Self-Refresh mode all of the external control signals, except CKE, are disabled. The clock is internally disabled during Self-Refresh Operation to save power. The user may change the external clock frequency or halt the external clock one clock after Self-Refresh entry is registered, however, the clock must be restarted and stable before the device can exit Self-Refresh operation. Once Self-Refresh Exit command is registered, a delay equal or longer than the tXSNR or tXSRD must be satisfied before a valid command can be issued to the device. CKE must remain high for the entire Self-Refresh exit period (tXSNR or tXSRD) for proper operation. NOP or DESELECT commands must be registered on each positive clock edge during the Self-Refresh exit interval. Since the ODT function is not supported during Self-Refresh operation, ODT has to be turned off tAOFD before entering Self-Refresh Mode and can be turned on again when the tXSRD timing is satisfied.



* = Device must be in the "All banks idle" state to entering Self Refresh mode.
ODT must be turned off prior to entering Self Refresh mode.
tXSRD has to be satisfied for a Read or a Read with Auto-Precharge command.
tXSNR has to be satisfied for any command except a Read or a Read with Auto-Precharge command.

Power-Down

Power-down is synchronously entered when CKE is registered low along with NOP or Deselect command. No read or write operation may be in progress when CKE goes low. These operations are any of the following: read burst or write burst and recovery. CKE is allowed to go low while any of other operations such as row activation, precharge or autoprecharge, mode register or extended mode register command time, or autorefresh is in progress. The DLL should be in a locked state when power-down is entered. Otherwise DLL should be reset after exiting power-down mode for proper read operation.

If power-down occurs when all banks are precharged, this mode is referred to as *Precharge Power-down*; if power-down occurs when there is a row active in any bank, this mode is referred to as *Active Power-down*. For *Active Power-down* two different power saving modes can be selected within the MRS register, address bit A12. When A12 is set to "low" this mode is referred as "standard active power-down mode" and a fast power-down exit timing defined by the tXARD timing parameter can be used. When A12 is set to "high" this mode is referred as a power saving "low power active power-down mode". This mode takes longer to exit from the power-down mode and the tXARDS timing parameter has to be satisfied.
Entering power-down deactivates the input and output buffers, excluding CK, $\overline{CK}$, ODT and CKE. Also the DLL is disabled upon entering precharge power-down or slow exit active power-down, but the DLL is kept enabled during fast exit active power-down. In power-down mode, CKE low and a stable clock signal must be maintained at the inputs of the DDR2 SDRAM, and all other input signals are "Don't Care". Power-down duration is limited by 9 times tREFI of the device.

The power-down state is synchronously exited when CKE is registered high (along with a NOP or Deselect command). A valid, executable command can be applied with power-down exit latency, tXP, tXARD or tXARDS, after CKE goes high. Power-down exit latencies are defined in the AC spec table of this data sheet.

Power-Down Entry

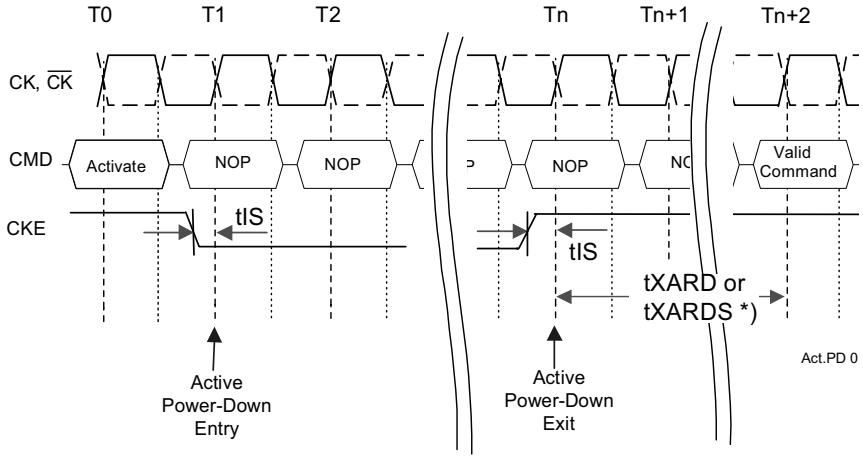
Active Power-down mode can be entered after an activate command. *Precharge Power-down* mode can be entered after a precharge, precharge-all or internal precharge command. It is also allowed to enter power-mode after an Auto-Refresh command or MRS / EMRS command when tMRD is satisfied.

Active Power-down mode entry is prohibited as long as a Read Burst is in progress, meaning CKE should be kept high until the burst operation is finished. Therefore Active Power-Down mode entry after a Read or Read with Auto-Precharge command is allowed after RL + BL/2 is satisfied.

Active Power-down mode entry is prohibited as long as a Write Burst and the internal write recovery is in progress. In case of a write command, active power-down mode entry is allowed when WL + BL/2 + tWTR is satisfied.

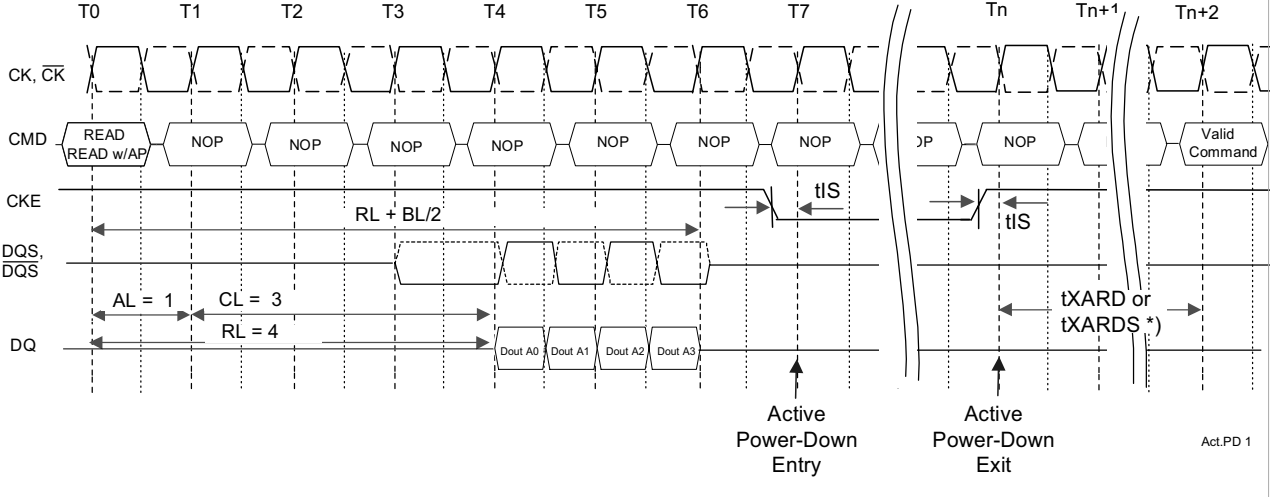
In case of a write command with auto-precharge, power-down mode entry is allowed after the internal precharge command has been executed, which is WL + BL/2 + WR starting from the write with auto-precharge command. In case the DDR2 SDRAM enters the *Precharge Power-down* mode.

Active Power-Down Mode Entry and Exit after an Activate Command



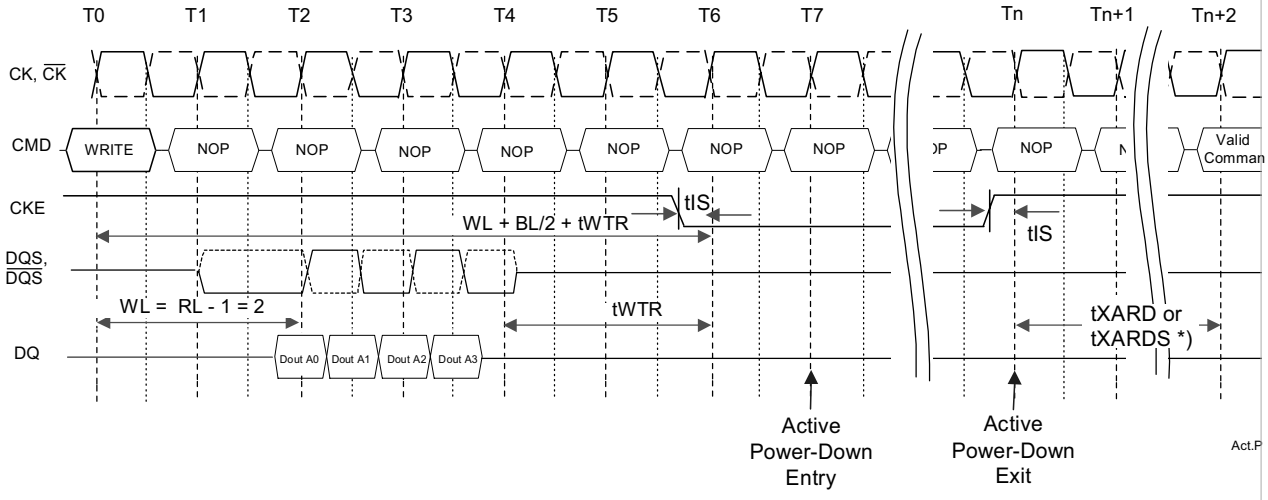
note: Active Power-Down mode exit timing tXARD (“fast exit”) or tXARDS (“slow exit”) depends on the programmed state in the MRS, address bit A12.

Active Power-Down Mode Entry and Exit after a Read Burst: RL = 4 (AL = 1, CL =3), BL = 4



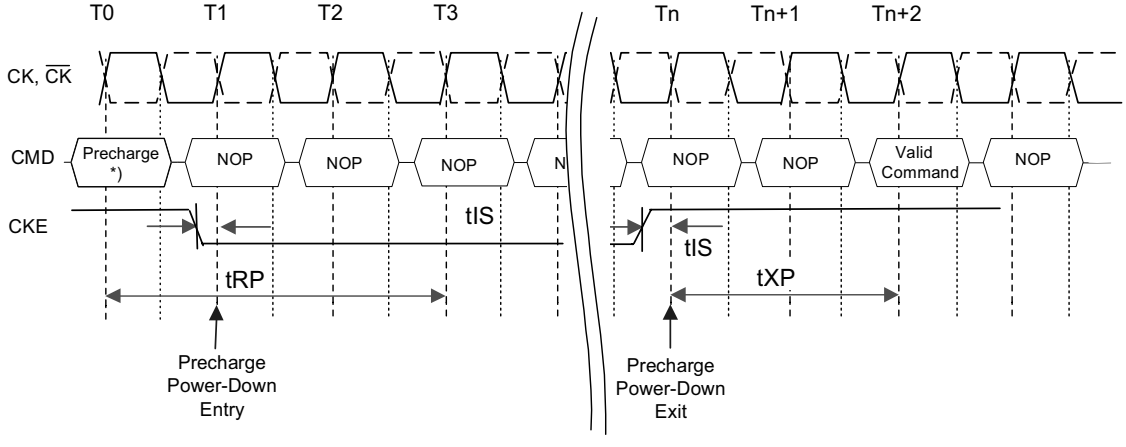
note: Active Power-Down mode exit timing tXARD (“fast exit”) or tXARDS (“slow exit”) depends on the programmed state in the MRS, address bit A12.

Active Power-Down Mode Entry and Exit after a Write Burst: WL = 2, tWTR = 2, BL = 4



note: Active Power-Down mode exit timing tXARD ("fast exit") or tXARDS ("slow exit") depends on the programmed state in the MRS, address bit A12.

Precharge Power Down Mode Entry and Exit



*) "Precharge" may be an external command or an internal precharge following Write with AP.

No Operation Command

The No Operation Command should be used in cases when the SDRAM is in a idle or a wait state. The purpose of the No Operation Command is to prevent the SDRAM from registering any unwanted commands between operations. A No Operation Command is registered when $\overline{CS}$ is low with $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ held high at the rising edge of the clock. A No Operation Command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

Deselect Command

The Deselect Command performs the same function as a No Operation Command. Deselect Command occurs when $\overline{CS}$ is brought high, the $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ signals become don't care.

Input Clock Frequency Change

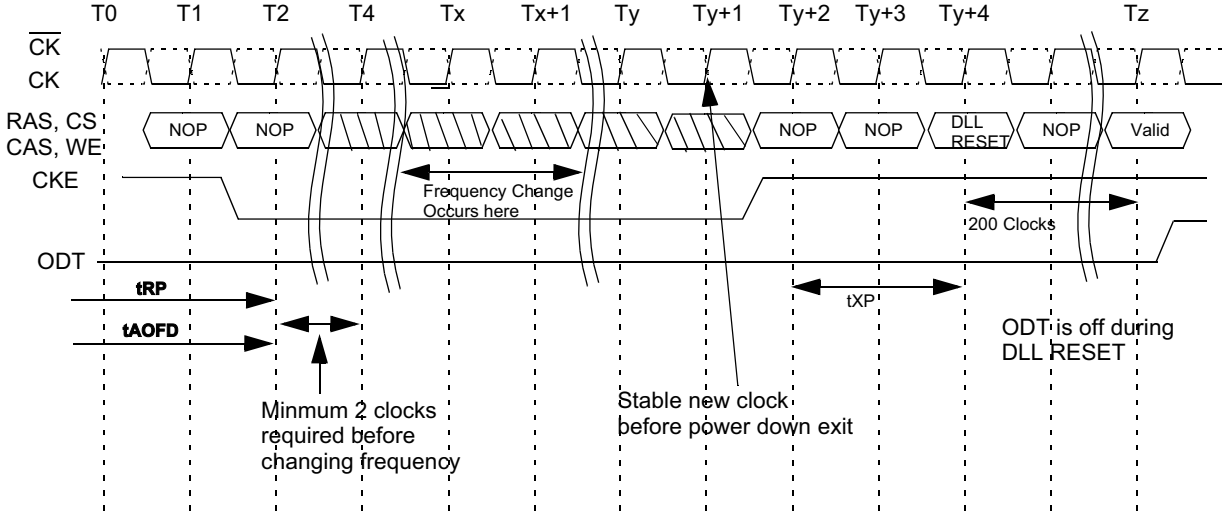
During operation the DRAM input clock frequency can be changed under the following conditions:

a) During Self-Refresh operation

b) DRAM is in precharged power-down mode and ODT is completely turned off.

The DDR2-SDRAM has to be in precharged power-down mode and idle. ODT must be allready turned off and CKE must be at a logic "low" state. After a minimum of two clock cycles after tRP and tAOFD have been satisfied the input clock frequency can be changed. A stable new clock frequency has to be provided, before CKE can be changed to a "high" logic level again. After tXP has been satisfied a DLL RESET command via EMRS has to be issued. During the following DLL re-lock period of 200 clock cycles, ODT must remain off. After the DLL-re-lock period the DRAM is ready to operate with the new clock frequency.

Clock Frequency Change in Precharge Power Down Mode

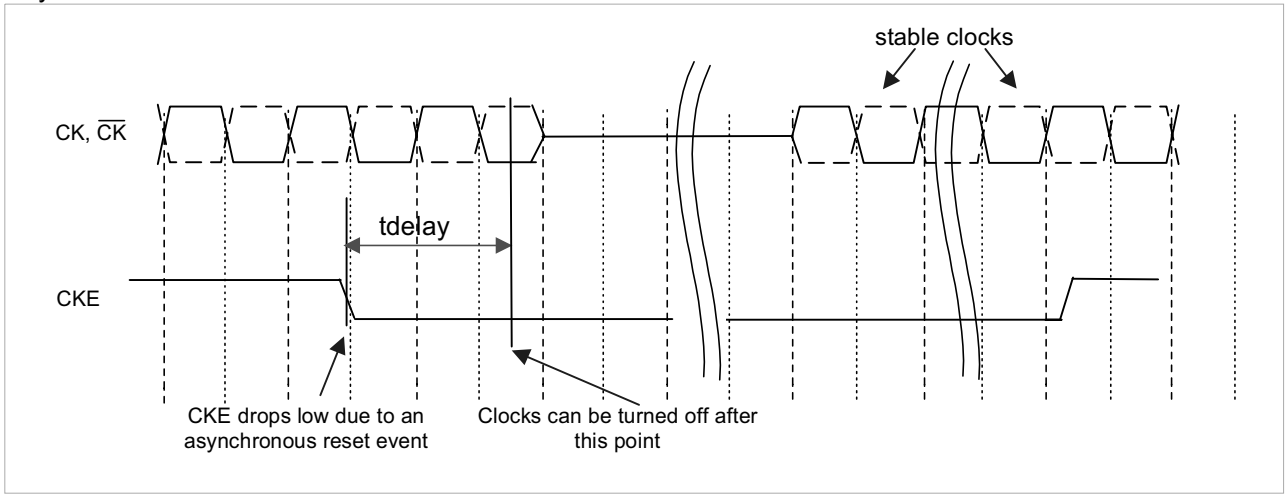


Asynchronous CKE Low Event

DRAM requires CKE to be maintained “high” for all valid operations as defined in this data sheet. If CKE asynchronously drops “low” during any valid operation DRAM is not guaranteed to preserve the contents of the memory array. If this event occurs, the memory controller must satisfy a time delay (t_{delay}) before turning off the clocks. Stable clocks must exist at the input of DRAM before CKE is raised “high” again. The DRAM must be fully re-initialized as described the the initialization sequence starting with step 4.

The DRAM is ready for normal operation after the initialization sequence. The minimum time clocks needs to be ON after CKE asynchronously drops low (the t_{delay} timing parameter) is equal to tIS + tCK + tIH.

Asynchronous CKE Low Event



Truth Tables

Command Truth Table

Function	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0 BA1	A12-A11	A10	A9 - A0	Notes
	Previous Cycle	Current Cycle									
(Extended) Mode Register Set	H	H	L	L	L	L	BA	OP Code			1, 2
Auto-Refresh	H	H	L	L	L	H	X	X	X	X	1
Self-Refresh Entry	H	L	L	L	L	H	X	X	X	X	1
Self-Refresh Exit	L	H	H	X	X	X	X	X	X	X	1
			L	H	H	H	X	X	X	X	1
Precharge all Banks	H	H	L	L	H	L	X	X	H	X	1
Bank Activate	H	H	L	L	H	H	BA	Row Address			1, 2
Write	H	H	L	H	L	L	BA	Column	L	Column	1,2,3
Write with Auto-Precharge	H	H	L	H	L	L	BA	Column	H	Column	1,2,3
Read	H	H	L	H	L	H	BA	Column	L	Column	1,2,3
Read with Auto-Precharge	H	H	L	H	L	H	BA	Column	H	Column	1,2,3
No Operation	H	X	L	H	H	H	X	X	X	X	1
Device Deselect	H	X	H	X	X	X	X	X	X	X	1
Power Down Entry	H	L	H	X	X	X	X	X	X	X	1,4
			L	H	H	H					
Power Down Exit	L	H	H	X	X	X	X	X	X	X	1,4
			L	H	H	H					
Single Bank Precharge	H	H	L	L	H	L	BA	X	L	X	1, 2

1. All DDR2 SDRAM commands are defined by states of $\overline{CS}$, $\overline{WE}$, $\overline{RAS}$, $\overline{CAS}$, and CKE at the rising edge of the clock.
2. Bank addresses (BA0, BA1) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.
3. Burst reads or writes at BL = 4 cannot be terminated. See sections “Reads interrupted by a Read” and “Writes interrupted by a Write”.
4. The Power Down Mode does not perform any refresh operations. The duration of Power Down is therefore limited by the refresh requirements.
5. The state of ODT does not affect the states decribed in this table. The ODT function is not available during Self Refresh.
6. “X” means “H or L (but a defined logic level)”.
7. Operation that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restartet through the specified initialization sequence before normal operation can continue.

Clock Enable (CKE) Truth Table for Synchronous Transistions

Current State[2]	CKE		Command (N) [3,12]	Action (N) [3]	Notes
	Previous Cycle [1] (N-1)	Current Cycle [1] (N)	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$		
Power-Down	L	L	X	Maintain Power-Down	13, 15
	L	H	DESELECT or NOP	Power-Down Exit	4, 8, 11
Self Refresh	L	L	X	Maintain Self Refresh	15
	L	H	DESELECT or NOP	Self Refresh Exit	4, 5, 9
Bank(s) Active	H	L	DESELECT or NOP	Active Power-Down Entry	4,8,10,11
All Banks Idle	H	L	DESELECT or NOP	Precharge Power-Down Entry	4,8,10,11
	H	L	AUTOREFRESH	Self Refresh Entry	6, 11
Any State other than listed above	H	H	Refer to the Command Truth Table		7

1. CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.
2. Current state is the state of the DDR2 SDRAM immediately prior to clock edge N.
3. Command (N) is the command registered at clock edge N, and Action (N) is a result of Command (N).
4. All states and sequences not shown are illegal or reserved unless explicitely described elsewhere in this document.
5. On Self Refresh Exit DESELECT or NOP commands must be issued on every clock edge occuring during the tXSNR period. Read commands may be issued only after tXSRD (200 clocks) is satisfied.
6. Self Refresh mode can only be entered from the All Banks Idle state.
7. Must be a legal command as defined in the Command Truth Table.
8. Valid commands for Power-Down Entry and Exit are NOP and DESELECT only.
9. Valid commands for Self Refresh Exit are NOP and DESELCT only.
10. Power-Down and Self Refresh can not be entered while Read or Write operations, (Extended) mode Register operations, Pre-charge or Refresh operations are in progress.
11. Minimum CKE high time is 3 clocks, minimum CKE low time is 3 clocks.
12. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
13. The Power-Down Mode does not perform any refresh operations. The duration of Power-Down Mode is therefor limited by the refresh requirements.
14. CKE must be maintained high while the device is in OCD calibration mode, f.e. if any of the bits A7, A8, A9 in EMRS are set to “1”.
15. “X” means “don’t care (including floating around VREF)” in Self Refresh and Power Down. However ODT must be driven high or low in Power Down if the ODT function is enabled (Bit A2 or A6 set to “1” in EMRS).
16. Operation that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restartet through the specified initialization sequence before normal operation can continue.

Data Mask (DM) Truth Table

Name (Function)	DM	DQs	Notes
Write Enable	L	Valid	1
Write Inhibit	H	X	1

1. Used to mask write data; provided coincident with the corresponding data.

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
VDD	Voltage on VDD pin relative to Vss	- 1.0 V ~ 2.3 V	V	1
VDDQ	Voltage on VDDQ pin relative to Vss	- 0.5 V ~ 2.3 V	V	1
VDDL	Voltage on VDDL pin relative to Vss	- 0.5 V ~ 2.3 V	V	1
V_{IN}, V_{OUT}	Voltage on any pin relative to Vss	- 0.5 V ~ 2.3 V	V	1
T_{STG}	Storage Temperature	-55 to +100	C	1

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

AC & DC Operating Conditions

Recommended DC Operating Conditions (SSTL - 1.8)

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.7	1.8	1.9	V	
VDDL	Supply Voltage for DLL	1.7	1.8	1.9	V	4
VDDQ	Supply Voltage for Output	1.7	1.8	1.9	V	4
VREF	Input Reference Voltage	0.49*VDDQ	0.50*VDDQ	0.51*VDDQ	V	1.2
VTT	Termination Voltage	VREF-0.04	VREF	VREF+0.04	V	3

There is no specific device VDD supply voltage requirement for SSTL-1.8 compliance. However under all conditions VDDQ must be less than or equal to VDD.

1. The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.5 x VDDQ of the transmitting device and VREF is expected to track variations in VDDQ.
2. Peak to peak ac noise on VREF may not exceed +/-2% VREF (dc).
3. VTT of transmitting device must track VREF of receiving device.
4. VDDQ tracks with VDD, VDDL tracks with VDD. AC parameters are measured with VDD, VDDQ and VDDDL tied together.

DC & AC Logic Input Levels

DDR2 SDRAM pin timing are specified for either single ended or differential mode depending on the setting of the EMRS "Enable $\overline{DQS}$" mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timing are measured is mode dependent. In single ended mode, timing relationships are measured relative to the rising or falling edges of DQS crossing at VREF. In differential mode, these timing relationships are measured relative to the crosspoint of DQS and its complement, $\overline{DQS}$. This distinction in timing methods is guaranteed by design and characterisation. In single ended mode, the $\overline{DQS}$ (and $\overline{RDQS}$) signals are internally disabled and don't care.

Single-ended DC Input Levels

Symbol	Parameter	Min.	Max.	Units
VIH (dc)	DC input logic high	VREF + 0.125	VDDQ + 0.3	V
VIL (dc)	DC input low	- 0.3	VREF - 0.125	V

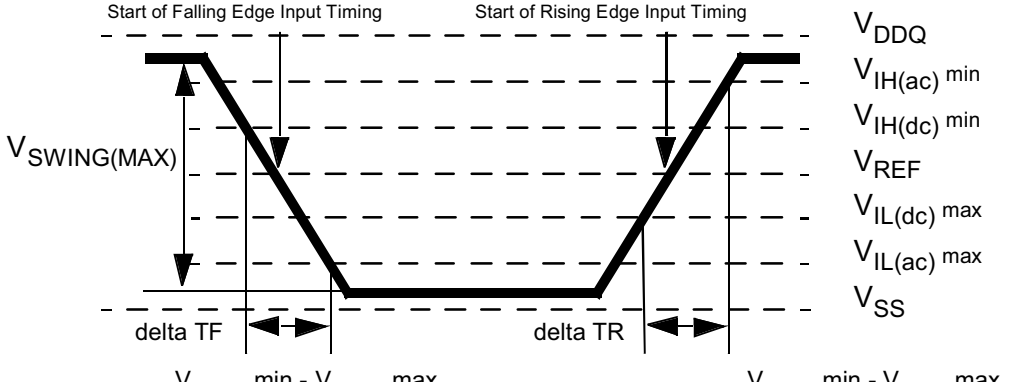
Single-ended AC Input Levels

Symbol	Parameter	DDR2 400,533		DDR2 667,800		Units
		Min	Max	Min	Max	
V_{IH}(ac)	ac input logic high	VREF+0.250	-	VREF+0.200	-	V
V_{IL}(ac)	ac input logic low	-	VREF-0.250	-	VREF-0.200	V

Single-ended AC Input Test Conditions

Symbol	Condition	Value	Units	Notes
VREF	Input reference voltage	0.5 * VDDQ	V	1
VSWING(max)	Input signal maximum peak to peak swing	1.0	V	1
SLEW	Input signal minimum slew rate	1.0	V / ns	2, 3

1. Input waveform timing is referenced to the input signal crossing through the VREF level applied to the device under test.
2. The input signal minimum slew rate is to be maintained over the range from VIL(dc)max to VIH(ac)min for rising edges and the range from VIH(dc)min to VIL(ac)max for falling edges as shown in the below figure.
3. AC timings are referenced with input waveforms switching from VIL(ac) to VIH(ac) on the positive transitions and VIH(ac) to VIL(ac) on the negative transitions.



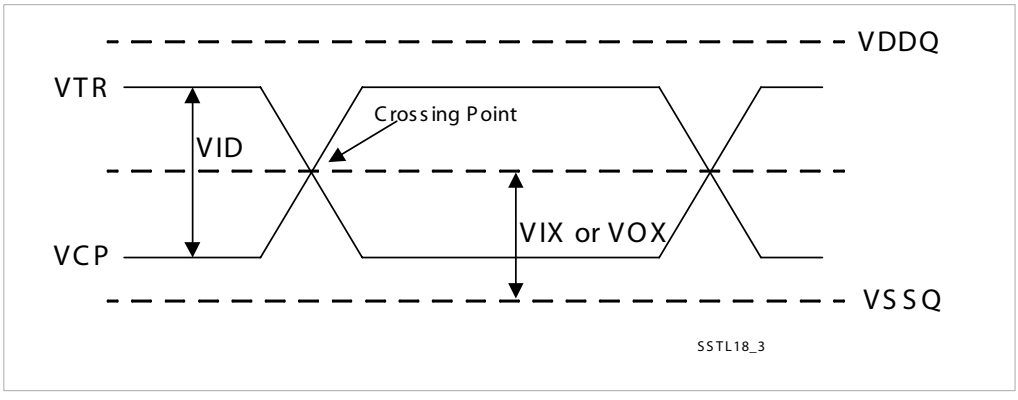
$$\text{Falling Slew} = \frac{V_{IH(dc)}\ \text{min} - V_{IL(ac)}\ \text{max}}{\text{delta TF}}$$

$$\text{Rising Slew} = \frac{V_{IH(ac)}\ \text{min} - V_{IL(dc)}\ \text{max}}{\text{delta TR}}$$

Differential DC and AC Input and Output Logic Levels

Symbol	Parameter	min.	max.	Units	Notes
VIN(dc)	DC input signal voltage	-0.3	VDDQ + 0.3		1
VID(dc)	DC differential input voltage	0.25	VDDQ + 0.6		2
VID(ac)	AC differential input voltage	0.5	VDDQ + 0.6	V	3
VIX(ac)	AC differential cross point input voltage	0.5 * VDDQ - 0.175	0.5 * VDDQ + 0.175	V	4
VOX(ac)	AC differential cross point output voltage	0.5 * VDDQ - 0.125	0.5 * VDDQ + 0.125	V	5

notes:
1) VIN(dc) specifies the allowable DC execution of each input of differential pair such as CK, $\overline{CK}$, DQS, $\overline{DQS}$,etc.
2) VID(dc) specifies the input differential voltage VTR - VCP required for switching. The minimum value is equal to VIH(dc) - VIL(dc).
3) VID(ac) specifies the input differential voltage VTR - VCP required for switching. The minimum value is equal to VIH(ac) - VIL(ac).
4) The value of VIX(ac) is expected to equal 0.5 x VDDQ of the transmitting device and VIX(ac) is expected to track variations in VDDQ. VIX(ac) indicates the voltage at which differential input signals must cross.
5) The value of VOX(ac) is expected to equal 0.5 x VDDQ of the transmitting device and VOX(ac) is expected to track variations in VDDQ. VOX(ac) indicates the voltage at which differential input signals must cross.



Capacitance Values

Parameter	Symbol	DDR2-400 DDR2-533		DDR2-667		DDR2-800		Units
		Min	Max	Min	Max	Min	Max	
Input capacitance, CK and $\overline{CK}$	CCK	1.0	2.0	1.0	2.0	1.0	2.0	pF
Input capacitance delta, CK and $\overline{CK}$	CDCK	x	0.25	x	0.25	x	0.25	pF
Input capacitance, all other input-only pins	CI	1.0	2.0	1.0	2.0	1.0	1.75	pF
Input capacitance delta, all other input-only pins	CDI	x	0.25	x	0.25	x	0.25	pF
Input/output capacitance, DQ, DM, DQS, $\overline{DQS}$	CIO	2.5	4.0	2.5	3.5	2.5	3.5	pF
Input/output capacitance delta, DQ, DM, DQS, $\overline{DQS}$	CDIO	x	0.5	x	0.5	x	0.5	pF

Power and ground clamps are implemented on the following input only pins:

1. BA0-BA2
2. A0-A15
3. $\overline{RAS}$
4. $\overline{CAS}$
5. $\overline{WE}$
6. $\overline{CS}$
7. ODT
8. CKE

V-I Characteristics for input only pins with clamps

Voltage across clamp(V)	Minimum Power Clamp Current (mA)	Minimum Ground Clamp Current (mA)
0.0	0	0
0.1	0	0
0.2	0	0
0.3	0	0
0.4	0	0
0.5	0	0
0.6	0	0
0.7	0	0
0.8	0.1	0.1
0.9	1.0	1.0
1.0	2.5	2.5
1.1	4.7	4.7
1.2	6.8	6.8
1.3	9.1	9.1
1.4	11.0	11.0
1.5	13.5	13.5
1.6	16.0	16.0
1.7	18.2	18.2
1.8	21.0	21.0

Output AC Test Conditions

Symbol	Parameter	SSTL_18 Class II	Units	Notes
V_{OH}	Minimum Required Output Pull-up under AC Test Load	V_{TT} + 0.603	V	
V_{OL}	Maximum Required Output Pull-down under AC Test Load	V_{TT} - 0.603	V	
V_{OTR}	Output Timing Measurement Reference Level	0.5 * V_{DDQ}	V	1

1. The VDDQ of the device under test is referenced.

Output DC Current Drive

Symbol	Parameter	SSTI_18 Class II	Units	Notes
$I_{OH(dc)}$	Output Minimum Source DC Current	- 13.4	mA	1, 3, 4
$I_{OL(dc)}$	Output Minimum Sink DC Current	13.4	mA	2, 3, 4

1. V_{DDQ} = 1.7 V; V_{OUT} = 1420 mV. (V_{OUT} - V_{DDQ})/I_{OH} must be less than 21 ohm for values of V_{OUT} between V_{DDQ} and V_{DDQ} - 280 mV.
2. V_{DDQ} = 1.7 V; V_{OUT} = 280 mV. V_{OUT}/I_{OL} must be less than 21 ohm for values of V_{OUT} between 0 V and 280 mV.
3. The dc value of V_{REF} applied to the receiving device is set to V_{TT}
4. The values of $I_{OH(dc)}$ and $I_{OL(dc)}$ are based on the conditions given in Notes 1 and 2. They are used to test device drive current capability to ensure V_{IH} min plus a noise margin and V_{IL} max minus a noise margin are delivered to an SSTL_18 receiver. The actual current values are derived by shifting the desired driver operating point (see Section 3.3) along a 21 ohm load line to define a convenient driver current for measurement.

OCD default characteristics

Description	Parameter	Min	Nom	Max	Unit	Notes
Output impedance		-	-	-	ohms	1
Output impedance step size for OCD calibration		0		1.5	ohms	6
Pull-up and pull-down mismatch		0		4	ohms	1,2,3
Output slew rate	Sout	1.5	-	5	V/ns	1,4,5,6,7,8

Notes:
1. Absolute Specifications (Toper; VDD = +1.8V +/-0.1V, VDDQ = +1.8V +/-0.1V)
2. Impedance measurement condition for output source dc current: VDDQ=1.7V; VOUT=1420mV; (VOUT-VDDQ)/Ioh must be less than 23.4 ohms for values of VOUT between VDDQ and VDDQ-280mV. Impedance measurement condition for output sink dc current: VDDQ = 1.7V; VOUT = 280mV; VOUT/Iol must be less than 23.4 ohms for values of VOUT between 0V and 280mV.
3. Mismatch is absolute value between pull-up and pull-dn, both are measured at same temperature and voltage.
4. Slew rate measured from vil(ac) to vih(ac).
5. The absolute value of the slew rate as measured from DC to DC is equal to or greater than the slew rate as measured from AC to AC. This is guaranteed by design and characterization.
6. This represents the step size when the OCD is near 18 ohms at nominal conditions across all process corners/variations and represents only the DRAM uncertainty. A 0 ohm value (no calibration) can only be achieved if the OCD impedance is 18 ohms +/- 0.75 ohms under nominal conditions.

Table 1. **Full Strength Default Pulldown Driver Characteristics**

	Pulldown Current (mA)			
Voltage (V)	Minimum (23.4 Ohms)	Nominal Default Low (18 ohms)	Nominal Default High (18 ohms)	Maximum (12.6 Ohms)
0.2	8.5	11.3	11.8	15.9
0.3	12.1	16.5	16.8	23.8
0.4	14.7	21.2	22.1	31.8
0.5	16.4	25.0	27.6	39.7
0.6	17.8	28.3	32.4	47.7
0.7	18.6	30.9	36.9	55.0
0.8	19.0	33.0	40.9	62.3
0.9	19.3	34.5	44.6	69.4
1.0	19.7	35.5	47.7	75.3
1.1	19.9	36.1	50.4	80.5
1.2	20.0	36.6	52.6	84.6
1.3	20.1	36.9	54.2	87.7
1.4	20.2	37.1	55.9	90.8
1.5	20.3	37.4	57.1	92.9
1.6	20.4	37.6	58.4	94.9
1.7	20.6	37.7	59.6	97.0
1.8		37.9	60.9	99.1
1.9				101.1

Figure 1. **DDR2 Default Pulldown Characteristics for Full Strength Driver**

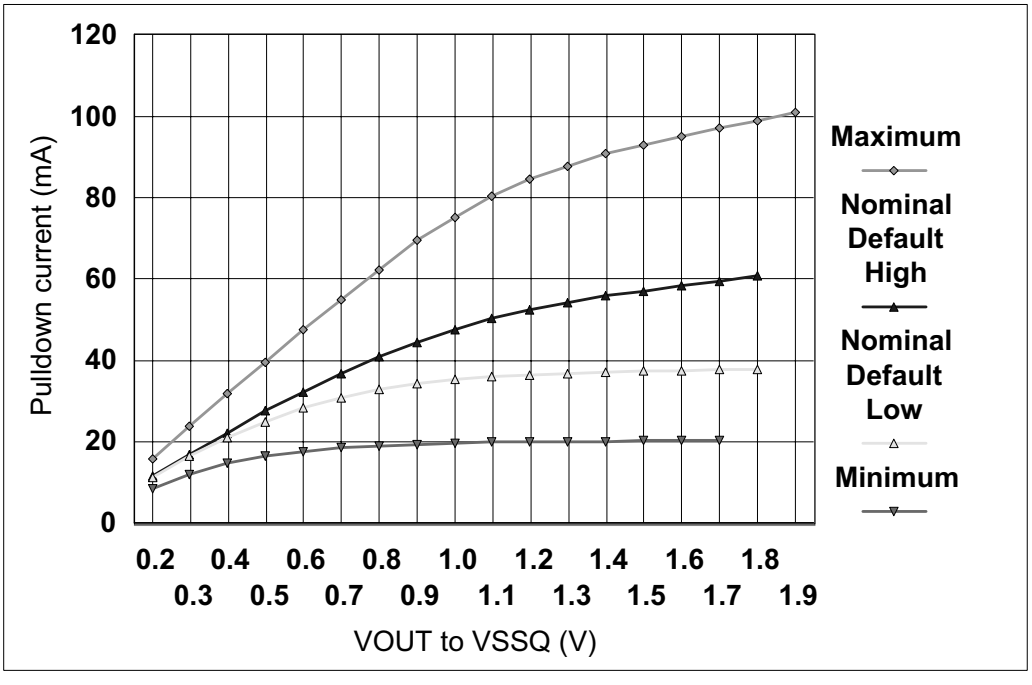
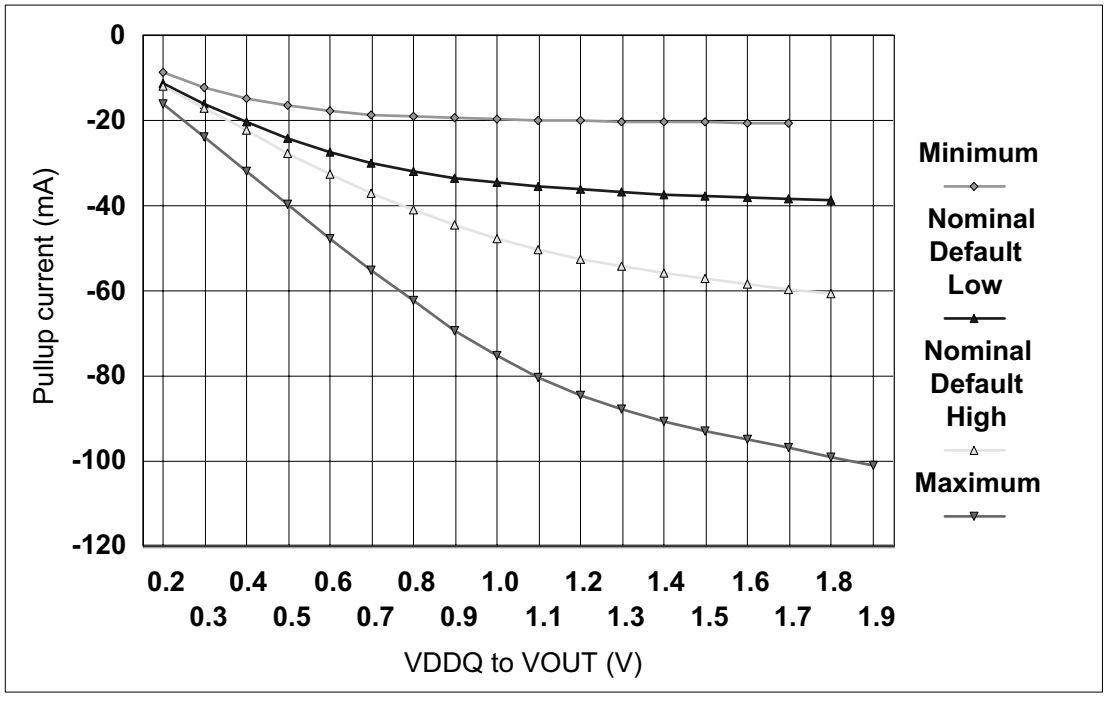


Table 2. **Full Strength Default Pullup Driver Characteristics**

	Pullup Current (mA)			
Voltage (V)	Minimum (23.4 Ohms)	Nominal Default Low (18 ohms)	Nominal Default High (18 ohms)	Maximum (12.6 Ohms)
0.2	-8.5	-11.1	-11.8	-15.9
0.3	-12.1	-16.0	-17.0	-23.8
0.4	-14.7	-20.3	-22.2	-31.8
0.5	-16.4	-24.0	-27.5	-39.7
0.6	-17.8	-27.2	-32.4	-47.7
0.7	-18.6	-29.8	-36.9	-55.0
0.8	-19.0	-31.9	-40.8	-62.3
0.9	-19.3	-33.4	-44.5	-69.4
1.0	-19.7	-34.6	-47.7	-75.3
1.1	-19.9	-35.5	-50.4	-80.5
1.2	-20.0	-36.2	-52.5	-84.6
1.3	-20.1	-36.8	-54.2	-87.7
1.4	-20.2	-37.2	-55.9	-90.8
1.5	-20.3	-37.7	-57.1	-92.9
1.6	-20.4	-38.0	-58.4	-94.9
1.7	-20.6	-38.4	-59.6	-97.0
1.8		-38.6	-60.8	-99.1
1.9				-101.1

Figure 2. **DDR2 Default Pullup Characteristics for Full Strength Output Driver**



DDR2 SDRAM Default Output Driver V–I Characteristics

DDR2 SDRAM output driver characteristics are defined for full strength default operation as selected by the EMRS1 bits A7-A9 = '111'. Figures 1 and 2 show the driver characteristics graphically, and tables 1 and 2 show the same data in tabular format suitable for input into simulation tools. The driver characteristics evaluation conditions are:

Nominal Default 25 °C (T case), VDDQ = 1.8 V, typical process

Minimum TBD °C (T case), VDDQ = 1.7 V, slow–slow process

Maximum 0 °C (T case), VDDQ = 1.9 V, fast–fast process

Default Output Driver Characteristic Curves Notes:

1) The full variation in driver current from minimum to maximum process, temperature, and voltage will lie within the outer bounding lines of the V–I curve of figures 1 and 2.

2) It is recommended that the "typical" IBIS V–I curve lie within the inner bounding lines of the V–I curves of figures 1 and 2.

Table 3. **Full Strength Calibrated Pulldown Driver Characteristics**

	Calibrated Pulldown Current (mA)				
Voltage (V)	Nominal Minimum (21 ohms)	Nominal Low (18.75 ohms)	Nominal (18 ohms)	Nominal High (17.2 ohms)	Nominal Maximum (15 ohms)
0.2	9.5	10.7	11.5	11.8	13.3
0.3	14.3	16.0	16.6	17.4	20.0
0.4	18.7	21.0	21.6	23.0	27.0

Table 4. **Full Strength Calibrated Pullup Driver Characteristics**

	Calibrated Pullup Current (mA)				
Voltage (V)	Nominal Minimum (21 ohms)	Nominal Low (18.75 ohms)	Nominal (18 ohms)	Nominal High (17.2 ohms)	Nominal Maximum (15 ohms)
0.2	-9.5	-10.7	-11.4	-11.8	-13.3
0.3	-14.3	-16.0	-16.5	-17.4	-20.0
0.4	-18.7	-21.0	-21.2	-23.0	-27.0

DDR2 SDRAM Calibrated Output Driver V–I Characteristics

DDR2 SDRAM output driver characteristics are defined for full strength calibrated operation as selected by the procedure outlined in the section of Off-Chip Driver (OCD) Impedance Adjustment. Tables 3 and 4 show the data in tabular format suitable for input into simulation tools. The nominal points represent a device at exactly 18 ohms. The nominal low and nominal high values represent the range that can be achieved with a maximum 1.5 ohm step size with no calibration error at the exact nominal conditions only (i.e. perfect calibration procedure, 1.5 ohm maximum step size guaranteed by specification). Real system calibration error needs to be added to these values. It must be understood that these V-I curves as represented here or in supplier IBIS models need to be adjusted to a wider range as a result of any system calibration error. Since this is a system specific phenomena, it cannot be quantified here. The values in the calibrated tables represent just the DRAM portion of uncertainty while looking at one DQ only. If the cali-

bration procedure is used, it is possible to cause the device to operate outside the bounds of the default device characteristics tables and figures. In such a situation, the timing parameters in the specification cannot be guaranteed. It is solely up to the system application to ensure that the device is calibrated between the minimum and maximum default values at all times. If this can't be guaranteed by the system calibration procedure, re-calibration policy, and uncertainty with DQ to DQ variation, then it is recommended that only the default values be used. The nominal maximum and minimum values represent the change in impedance from nominal low and high as a result of voltage and temperature change from the nominal condition to the maximum and minimum conditions. If calibrated at an extreme condition, the amount of variation could be as much as from the nominal minimum to the nominal maximum or vice versa. The driver characteristics evaluation conditions are:

Nominal 25 ºC (T case), VDDQ = 1.8 V, typical process

Nominal Low and Nominal High 25 ºC (T case), VDDQ = 1.8 V, any process

Nominal Minimum TBD ºC (T case), VDDQ = 1.7 V, any process

Nominal Maximum 0 ºC (T case), VDDQ = 1.9 V, any process

IDD Specifications and Conditions
DDR2-400/533/-667/-800

(0 deg C < Tcase < 85 deg C; VDDQ=1.8V±0.1V; VDD=1.8V±0.1V)

Symbol	Parameter/Condition	I/O	-5 DDR2-400	-3.7 DDR2-533	-3 DDR2-667	-25A/25 DDR2-800	-19 DDR2-1066	Unit	Notes
I_{DD0}	Operating Current	x4/x8/ x16	80 100	80 100	90 110	100 120	110 130	mA	1,2
I_{DD1}	Operating Current	x4/x8/ x16	90 110	90 110	90 120	100 130	110 140	mA	1,2
I_{DD2P}	Precharge Power-Down Current	x4/x8/ x16	8 8	8 8	8 8	8 8	8 8	mA	1,2
I_{DD2N}	Precharge Standby Current	x4/x8/ x16	30 30	40 40	40 40	50 50	60 60	mA	1,2
I_{DD2Q}	Precharge Quiet Standby Current	x4/x8/ x16	30 30	30 30	40 40	40 40	50 50	mA	1,2
	Active Power Down Standby Current MRS(12)=0	all	30	30	30	35	40	mA	1,2
I_{DD3P}	Active Power Down Standby Current MRS(12)=0	all	12	12	12	12	12	mA	1,2
I_{DD3N}	Active Standby Current	x4/x8/ x16	40 40	50 50	50 50	60 60	70 70	mA	1,2
I_{DD4R}	Operating Current Burst Read	x4/x8/ x16	80 110	100 150	120 170	140 200	150 210	mA	1,2
I_{DD4W}	Operating Current Burst Read	x4/x8/ x16	90 130	120 170	140 200	160 240	170 250	mA	1,2
I_{DD5B}	Burst Auto-Refresh Current (tRFC=tRFC-min)	x4/x8/ x16	150 150	150 150	160 160	160 165	170 175	mA	1,2
I_{DD6}	Self-Refresh Current for Standard products	all	8	8	8	8	8	mA	1,2
I_{DD6}	Self-Refresh Current for low power products	all	4	4	4	4	4	mA	1,2
I_{DD7}	Operating Current	x4/x8/ x16	210 320	210 320	220 320	230 340	240 350	mA	1,2

IDD Measurement Conditions

(0 °C ≤ T_{CASE} ≤ 85 °C (tbd); VDDQ = 1.8V ± 0.1V; VDD = 1.8V ± 0.1V)

Symbol	Parameter/Condition
I_{DD0}	Operating Current - One bank Active - Precharge tRC = tRCmin; tCK =tCKmin. ; Databus inputs are SWITCHING; Address and control inputs are SWITCHING, $\overline{CS}$ = HIGH between valid commands.
I_{DD1}	Operating Current - One bank Active - Read - Precharge One bank is accessed with tRCmin , BL = 4, tCK = tCKmin, AL = 0, CL = CLmin.; Address and control inputs are SWITCHING,$\overline{CS}$ = HIGH between valid commands; I_{out} = 0 mA.
I_{DD2P}	Precharge Power-Down Current: all banks idle; power-down mode; CKE is LOW; tCK = tCKmin.; Data Bus inputs are FLOATING.
I_{DD2N}	Precharge Standby Current: all banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; tCK = tCKmin.; Address and control inputs are SWITCHING; Data Bus inputs are SWITCHING.
I_{DD2Q}	Precharge Quiet Standby Current: all banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; tCK = tCKmin.; Address and control inputs are STABLE; Data Bus inputs are FLOATING.
I_{DD3P}	Active Power-Down Current: all banks open; CKE is LOW; Address and control inputs are STABLE; Data Bus inputs are FLOATING. MRS A12 bit is set to "0"(Fast Power-down Exit);
I_{DD3P}	Active Power-Down Current: all banks open; CKE is LOW; Address and control inputs are STABLE; Data Bus inputs are FLOATING. MRS A12 bit is set to "1"(Slow Power-down Exit);
I_{DD3N}	Active Standby Current: all banks open; $\overline{CS}$ is HIGH; CKE is HIGH; tRC = tRASmax; tCK = tCKmin.; Address and control inputs are SWITCHING; Data Bus inputs are SWITCHING.
I_{DD4R}	Operating Current - Burst Read: all banks active; continuous burst reads; BL = 4;AL = 0, CL = CLmin.; tCK = tCKmin.; Address and control inputs are SWITCHING; Data Bus inputs are SWITCHING; IOUT = 0mA.
I_{DD4W}	Operating Current - Burst Write: all banks active; continuous burst writes; BL = 4;AL = 0, CL = CLmin.; tCK = tCKmin.; Address and control inputs are SWITCHING; Data Bus inputs are SWITCHING; IOUT = 0mA.
I_{DD5B}	Burst Auto-Refresh Current: Refresh command at tRFC = tRFCmin, tCK = tCKmin, $\overline{CS}$ is HIGH between valid commands
I_{DD5D}	Distributed Auto-Refresh Current: Refresh command at tREFI; tCK = tCKmin, $\overline{CS}$ is HIGH between valid commands; CKE is LOW except during tRFCmin.
I_{DD6}	Self-Refresh Current: CKE 0.2V; external clock off, CK and $\overline{CK}$ at 0V; tCK = tCKmin; Address and control inputs are FLOATING; Data Bus inputs are FLOATING.
I_{DD7}	Operating Bank Interleave Read Current: 1. All bank interleaving with BL = 4; BL = 4, CL = CLmin.;tRCD = tRCDmin.; tRRD = tRRDmin.;AL = tRCD - 1, Iout = 0 mA. Address and control inputs are stable during DESELECT; Data Bus inputs are SWITCHING. 2. Timing pattern: - DDR2 -400 (200Mhz, CL=3) : tck = 5 ns, BL = 4, tRCD = 3 * tck, AL = 2 * tck, tRC = 12 * tck Read : A0 RA0 A1 RA1 A2 RA2 A3 RA3 D D D D - DDR2 -533 (266Mhz, CL=4) : tck = 3.7 ns, BL = 4, tRCD = 4 * tck, AL = 3 * tck, tRC = 16 * tck Read : A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D D D - DDR2 -667 (333Mhz, CL=5) : tck = 3 ns, BL = 4, tRCD = 5 * tck, AL = 4* tck, tRC = 20 * tck Read : A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D - DDR2 -800 (400Mhz, CL=5) : tck=2.5 ns, BL = 4, tRCD = 5 * tck, AL = 4* tck, tRC = 23 * tck Read : A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D D D D

1. Data Bus consists of DQ, DM, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$, LDQS, $\overline{LDQS}$, UDQS and $\overline{UDQS}$.
2. Definitions for IDD :
   LOW is defined as VIN <= VILAC(max.); HIGH is defined as VIN >= VIHAC(min.);
   STABLE is defined as inputs are stable at a HIGH or LOW level
   FLOATING is defined as inputs are VREF
   SWITCHING is defined as inputs are changing between HIGH and LOW every other clock for adress and control signals, and inputs changing 50% of each data trasnfer for DQ signals.
3. Legend : A=Activate, RA=Read with Auto-Precharge, D=DESELECT

AC Characteristics (AC operating conditions unless otherwise noted)

Parameter		Symbol	(DDR2-400) -5		(DDR2-533) -37		(DDR2-667) -3		(DDR2-800) -25A		(DDR2-800) -25		(DDR2-1066) -19		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Row Cycle Time		t_{RC}	60	-	60	-	60	-	60	-	57.25	-	54	-	ns	
Auto Refresh Row Cycle Time		t_{RFC}	105	-	105	-	105	-	105	-	105	-	105	-	ns	11
Row Active Time		t_{RAS}	40	70K	45	70K	45	70K	45	70K	45	70K	40	70K	ns	21
Row Address to Column Address Delay		t_{RCD}	15	-	15	-	15	-	15	-	12.5	-	11.2	-	ns	20
Row Active to Row Active Delay (x4 & x8)		t_{RRD}	7.5	-	7.5	-	7.5	-	7.5	-	7.5	-	7.5	-	ns	
Row Active to Row Active Delay (x16)		t_{RRD}	10	-	10	-	10	-	10	-	10	-	10	-	ns	
Column Address to Column Address Delay		t_{CCD}	2	-	2	-	2	-	2	-	2	-	2	-	CLK	
Row Precharge Time		t_{RP}	15	-	15	-	15	-	15	-	12.5	-	11.2	-	ns	
Write Recovery Time		t_{WR}	15	-	15	-	15	-	15	-	15	-	15	-	ns	
Auto Precharge Write Recovery + Precharge Time		t_{DAL}	$t_{WR}+t_{RP}$	-	$t_{WR}+t_{RP}$	-	$t_{WR}+t_{RP}$	-	$t_{WR}+t_{RP}$	-	$t_{WR}+t_{RP}$	-	$t_{WR}+t_{RP}$	-	ns	12
System Clock Cycle Time	$\overline{CAS}$ Latency = 3	t_{CK}	5	8	5	8	5	8	5	8	5	8	5	8	ns	2
	$\overline{CAS}$ Latency = 4		5	8	3.75	8	3.75	8	3.75	8	3.75	8	3.75	8	ns	2
	$\overline{CAS}$ Latency = 5		5	8	3.75	8	3	8	3	8	2.5	8	3	8	ns	2
	$\overline{CAS}$ Latency = 6		5	8	3.75	8	3	8	2.5	8	2.5	8	1.87	8	ns	
Clock High Level Width		t_{CH}	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.48	0.52	CLK	
Clock Low Level Width		t_{CL}	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.48	0.52	CLK	
Data-Out edge to Clock edge Skew		t_{AC}	-0.60	0.60	-0.50	0.50	-0.45	0.45	-0.40	0.40	-0.40	0.40	-0.35	0.35	ns	
DQS-Out edge to Clock edge Skew		t_{DQSCK}	-0.50	0.50	-0.45	0.45	-0.40	0.40	-0.35	0.35	-0.35	0.35	-0.325	0.325	ns	
DQS-Out edge to Data-Out edge Skew		t_{DQSQ}	-	0.35	-	0.30	-	0.24	-	0.20	-	0.20	-	0.175	ns	
Data-Out hold time from DQS		t_{QH}	t_{HPmin} -t_{QHS}	-	t_{HPmin} -t_{QHS}	-	t_{HPmin} -t_{QHS}	-	t_{HPmin} -t_{QHS}	-	t_{HPmin} -t_{QHS}	-	t_{HPmin} -t_{QHS}	-	ns	
Data hold skew factor		t_{QHS}	-	450	-	400	-	340	-	300	-	300	-	300	ps	
Clock Half Period		t_{HP}	$t_{CH/L}$ min	-	$t_{CH/L}$ min	-	$t_{CH/L}$ min	-	$t_{CH/L}$ min	-	$t_{CH/L}$ min	-	$t_{CH/L}$ min	-	ns	5
Input Setup Time (fast slew rate)		t_{IS}	350	-	250	-	200	-	175	-	175	-	175	-	ps	15,17

Parameter	Symbol	(DDR2-400) -5		(DDR2-533) -37		(DDR2-667) -3		(DDR2-800) -25A		(DDR2-800) -25		(DDR2-1066) -19		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Input Hold Time (fast slew rate)	t_{IH}	475	-	375	-	275	-	250	-	250	-	250	-	ps	15,17
Input Pulse Width	t_{IPW}	0.6	-	0.6	-	0.6	-	0.6	-	0.6	-	0.6	-	CLK	
Write DQS High Level Width	t_{DQSH}	0.35		0.35		0.35		0.35		0.35		0.35		CLK	
Write DQS Low Level Width	t_{DQSL}	0.35		0.35		0.35		0.35		0.35		0.35		CLK	
CLK to First Rising edge of DQS-In	t_{DQSS}	WL-0.25t_{CK}	WL+0.25t_{CK}	WL-0.25t_{CK}	WL+0.25t_{CK}	WL-0.25t_{CK}	WL+0.25t_{CK}	WL-0.25t_{CK}	WL+0.25t_{CK}	WL-0.25t_{CK}	WL+0.25t_{CK}	WL-0.25t_{CK}	WL+0.25t_{CK}	CLK	
Data-In Setup Time to DQS-In (DQ & DM)	t_{DS}	150	-	100	-	50	-	50	-	50	-	50	-	ps	16,17,18
Data-in Hold Time to DQS-In (DQ & DM)	t_{DH}	275	-	225	-	175	-	125	-	125	-	125	-	ps	16,17,18
DQS falling edge to CLK rising Setup Time	t_{DSS}	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	CLK	
DQS falling edge from CLK rising Hold Time	t_{DSH}	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	CLK	
DQ & DM Input Pulse Width	t_{DIPW}	0.35	-	0.35	-	0.35	-	0.35	-	0.35	-	0.35	-	CLK	
Read DQS Preamble Time	t_{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	CLK	
Read DQS Postamble Time	t_{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	CLK	
Write DQS Preamble Setup Time	t_{WPRES}	0	-	0	-	0	-	0	-	0	-	0	-	CLK	
Write DQS Preamble Hold Time	t_{WPREH}	0.25	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	-	CLK	
Write DQS Postamble Time	t_{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	CLK	10
Internal read to precharge command delay	t_{RTP}	7.5	-	7.5	-	7.5	-	7.5	-	7.5	-	7.5	-	ns	
Internal write to read command delay	t_{WTR}	10	-	7.5	-	7.5	-	7.5	-	7.5	-	7.5	-	ns	13
Data out high impedance time from CLK/$\overline{CLK}$	t_{HZ}	$t_{AC(min)}$	$t_{AC(max)}$	$t_{AC(min)}$	$t_{AC(max)}$	$t_{AC(min)}$	$t_{AC(max)}$	$t_{AC(min)}$	$t_{AC(max)}$	$t_{AC(min)}$	$t_{AC(max)}$	$t_{AC(min)}$	$t_{AC(max)}$	ns	7
Data out low impedance time from CLK/$\overline{CLK}$	t_{LZ}	$t_{AC(min)}$	$t_{AC(max)}$	$t_{AC(min)}$	$t_{AC(max)}$	$t_{AC(min)}$	$t_{AC(max)}$	$t_{AC(min)}$	$t_{AC(max)}$	$t_{AC(min)}$	$t_{AC(max)}$	$t_{AC(min)}$	$t_{AC(max)}$	ns	7
Mode Register Set Delay	t_{MRD}	2	-	2	-	2	-	2	-	2	-	2	-	CLK	9
Exit Self Refresh to Non-Read Command	t_{XSNR}	t_{RFC}+10	-	t_{RFC}+10	-	t_{RFC}+10	-	t_{RFC}+10	-	t_{RFC}+10	-	t_{RFC}+10	-	ns	19
Exit Self Refresh to Read Command	t_{XSRD}	200	-	200	-	200	-	200	-	200	-	200	-	CLK	
Exit Precharge Power Down to any non-Read Command	t_{XP}	2	-	2	-	2	-	2	-	2	-	2	-	CLK	14
Exit Active Power Down to Read Command	t_{XARD}	2	-	2	-	2	-	2	-	2	-	2	-	CLK	

Parameter	Symbol	(DDR2-400) -5		(DDR2-533) -37		(DDR2-667) -3		(DDR2-800) -25A		(DDR2-800) -25		(DDR2-1066) -19		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Exit Active Power Down to Read Command (Slow exit, Lower Power)	t_{XARDS}	6-AL	-	6-AL	-	6-AL	-	6-AL	-	6-AL	-	6-AL	-	CLK	
ODT drive mode output delay	t_{OIT}	0	12	0	12	0	12	0	12	0	12	0	12	ns	
Minimum time clocks remains ON after CKE asynchronously drops LOW	t_{Delay}	tIS+tCK +tIH		tIS+tCK +tIH		tIS+tCK +tIH		tIS+tCK +tIH		tIS+tCK +tIH		tIS+tCK +tIH		ns	
CKE minimum high and low pulse width	t_{CKE}	3	-	3	-	3	-	3	-	3	-	3	-	CLK	
Average Periodic Refresh Interval 0C ≤ T ≤ 85C	t_{REFI}	-	7.8	-	7.8	-	7.8	-	7.8	-	7.8	-	7.8	us	18
Period jitter	t_{JITPER}	-125	125	-125	125	-125	125	-100	100	-100	100	-90	90	ps	22
Half period	t_{JITDTY}	-150	150	-125	125	-125	125	-100	100	-100	100	-75	75	ps	22
Cycle to Cycle	t_{JITCC}	250		250		250		200		200		180		ps	22
Cumulative error, 2 cycles	$t_{ERR(2PER)}$	-175	175	-175	175	-175	175	-150	150	-150	150	-132	132	ps	22
Cumulative error, 3 cycles	$t_{ERR(3PER)}$	-225	225	-225	225	-225	225	-175	175	-175	175	-157	157	ps	22
Cumulative error, 4 cycles	$t_{ERR(4PER)}$	-250	250	-250	250	-250	250	-200	200	-200	200	-175	175	ps	22
Cumulative error, 5 cycles	$t_{ERR(5PER)}$	-250	250	-250	250	-250	250	-200	200	-200	200	-188	188	ps	22
Cumulative error, 6-10 cycles	$t_{ERR(6-10PER)}$	-350	350	-350	350	-350	350	-300	300	-300	300	-250	250	ps	22
Cumulative error, 11-50 cycles	$t_{ERR(11-50PER)}$	-450	450	-450	450	-450	450	-450	450	-450	450	-425	425	ps	22

Notes for Electrical Characteristics & AC Timing

1. Input slew rate is 1 V/ns and AC timings are guarantedd for linear signal transitions. For other slew rates see the derating tables on the next pages.
2. The CK / $\overline{CK}$ input reference level (for timing reference to CK / $\overline{CK}$) is the point at which CK and $\overline{CK}$ cross:the DQS / $\overline{DQS}$ input reference level is the crosspoint when in differential strobe mode; the input reference level for signals other than CK/$\overline{CK}$, or DQS / $\overline{DQS}$ is VREF.
3. Inputs are not recognized as valid until VREF stabilizes. During the period before VREF stabilizes, CKE = 0.2 x VDDQ is recognized as LOW.
4. The output timing reference voltage level is VTT.
5. Min (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH.
6. For input frequency change during DRAM operation.
7. t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).
8. These parameters guarantee device timing, but they are not necessarily tested on each device.
9. The specific requirement is that DQS and $\overline{DQS}$ be valid (HIGH, LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on t_{DQSS}. When programmed in differential strobe mode, DQS is always the logic complement of DQS except when both are in high-Z.
10. The maximum limit for this parameter is not a device limit. The device operate with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
11. A maximum of eight Auto-Refresh commands can be posted to any given DDR2 SDRAM device. (Note : tRFC depends on DRAM density)
12. For each of the terms, if not allready an integer, round to the next highest integer. tCK refers to the application clock period. WR refers to the WR parameter stored in the MRS.
13. tWTR is at least two clocks independent of operation frequency.
14. User can choose two different active power-down modes for additional power saving via MRS address bit A12. In “standard active power-down mode” (MRS, A12 = “0”) a fast power-down exit timing tXARD can be used. In “low active power-down mode” (MRS, A12 =”1”) a slow power-down exit timing tXARDS has to be satisfied.
15. Timings are guaranteed with command / address input slew rate of 1.0 V/ns.
16. Timings are guaranteed with data / mask input slew rate of 1.0 V/ns.
17. Timings are guaranteed with CK /$\overline{CK}$ differential slew rate 2.0 V/ns, and DQS/$\overline{DQS}$ (and RDQS/$\overline{RDQS}$) differential slew rate 2.0 V/ns in differential strobe mode.
18. If refresh timing or tDS / tDH is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.
19. In all circumstances, tXSNR can be satisfied using tXSNR = tRFC + 10 ns.
20. The tRCD timing parameter is valid for both activate command to read or write command with and without Auto-Precharge. Therefore a separate parameter tRAP for activate command to read or write command with Auto-Precharge is not neccessary anymore.
21. tRAS(max) is calculated from the maximum amount of time a DDR2 device can operate without a Refresh command which is equal to 9 * tREFI.

22. Definitions:

- tCK(avg)

  tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window.

$$tCK(avg) = \left(\sum_{j=1}^{N} tCK_j \right) / N$$

$$where \qquad N = 200$$

- tCH(avg) and tCL(avg)

  tCH(avg) is defined as the average HIGH pulse width, as calculated across any consecutive 200 HIGH pulses.

$$tCH(avg) = \left(\sum_{j=1}^{N} tCH_j \right) / (N \times tCK(avg))$$

$$where \qquad N = 200$$

tCL(avg) is defined as the average LOW pulse width, as calculated across any consecutive 200 LOW pulses.

$$tCL(avg) = \left(\sum_{j=1}^{N} tCL_j \right) / (N \times tCK(avg))$$

$$where \qquad N = 200$$

- tJIT(duty)

  tJIT(duty) is defined as the cumulative set of tCH jitter and tCL jitter. tCH jitter is the largest deviation of any single tCH from tCH(avg). tCL jitter is the largest deviation of any single tCL from tCL(avg).

  tJIT(duty) = Min/max of {tJIT(CH), tJIT(CL)}

  where,

  tJIT(CH) = {tCH_i- tCH(avg) where i=1 to 200}

  tJIT(CL) = {tCL_i- tCL(avg) where i=1 to 200}

- tJIT(per), tJIT(per,lck)

  tJIT(per) is defined as the largest deviation of any single tCK from tCK(avg).

tJIT(per) = Min/max of {tCK_i- tCK(avg) where i=1 to 200}

tJIT(per) defines the single period jitter when the DLL is already locked.
tJIT(per,lck) uses the same definition for single period jitter, during the DLL locking period only.
tJIT(per) and tJIT(per,lck) are not guaranteed through final production testing.

- tJIT(cc), tJIT(cc,lck)
  tJIT(cc) is defined as the difference in clock period between two consecutive clock cycles:

  tJIT(cc) = Max of $|tCK_{i+1} - tCK_i|$

  tJIT(cc) defines the cycle to cycle jitter when the DLL is already locked.
  tJIT(cc,lck) uses the same definition for cycle to cycle jitter, during the DLL locking period only.
  tJIT(cc) and tJIT(cc,lck) are not guaranteed through final production testing.

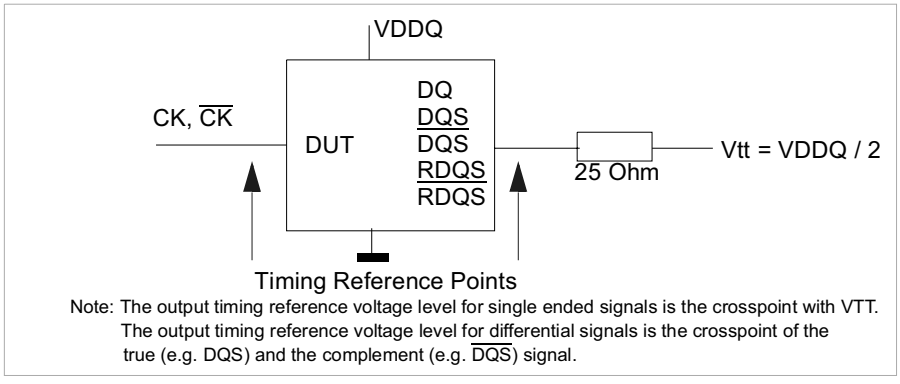
$$tERR(nper) = \left(\sum_{j=1}^{i+n-1} tCK_j \right) - n \times tCK(avg)$$

$$where \begin{cases} n = 2 & for \quad tERR(2per) \\ n = 3 & for \quad tERR(3per) \\ n = 4 & for \quad tERR(4per) \\ n = 5 & for \quad tERR(5per) \\ 6 \le n \le 10 & for \quad tERR(6-10per) \\ 11 \le n \le 50 & for \quad tERR(11-50per) \end{cases}$$

Reference Loads, Slew Rates and Slew Rate Derating

Reference Load for Timing Measurements

The figure represents the timing reference load used in defining the relevant timing parameters of the device. It is not intended to either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to a system environment. This load circuit is also used for output slew rate measurements.

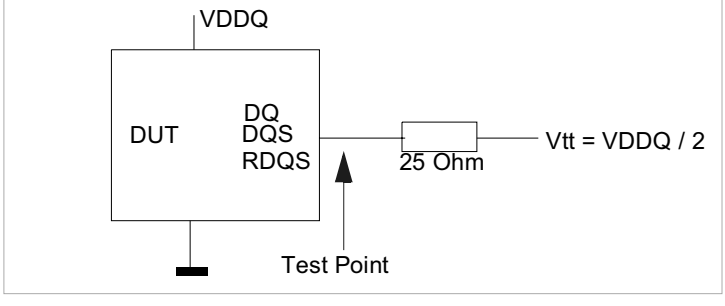


Note: The output timing reference voltage level for single ended signals is the crosspoint with VTT. The output timing reference voltage level for differential signals is the crosspoint of the true (e.g. DQS) and the complement (e.g. DQS) signal.

Slew Rate Measurements

Output Slew Rate

Output slew rate is characterized under the test conditions as shown in the figure below



Output slew rate for falling and rising edges is measured between VTT - 250 mV and VTT + 250 mV for single ended signals.For differential signals (e.g. DQS - DQS) output slew rate is measured between DQS - DQS = - 500 mV and DQS - DQS = + 500 mV.Output slew rate is guaranteed by design, but is not necessarilty tested on each device.

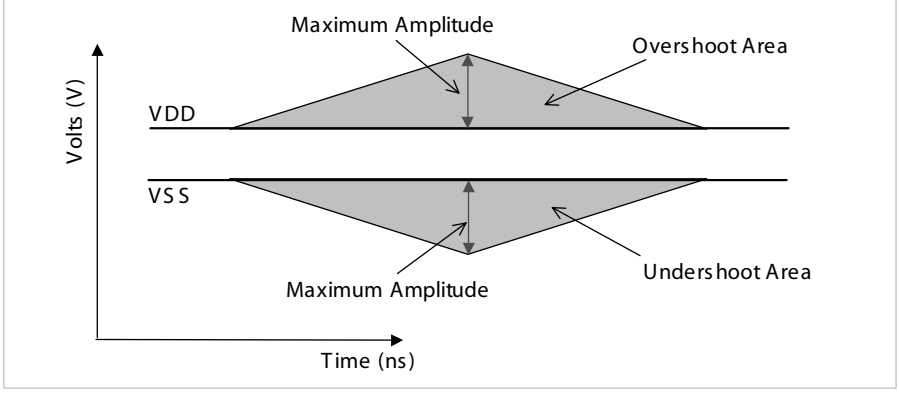
Input Slew Rate

Input slew for single ended signals is measured from dc-level to ac-level from VREF - 125 mV to VERF + 250 mV for rising edges and from VREF + 125 mV to VREF - 250 mV for falling edges.
For differential signals (e.g. CK - CK) slew rate for rising edges is measured from CK - CK = -250 mV to CK -CK = +500 mV (250 mV to -500 mV for falling edges). Test conditions are the same as for timing measurements.

Overshoot and Undershoot Specification

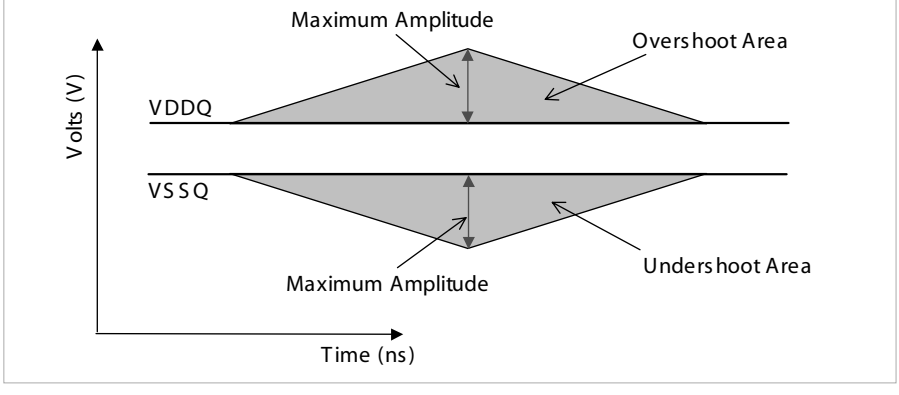
AC Overshoot / Undershoot Specification for Address and Control Pins

Parameter	DDR2 -400	DDR2 -533	DDR2 -667	DDR2 -800	Units
Maximum peak amplitude allowed for overshoot area	0.9	0.9	0.9	0.9	V
Maximum peak amplitude allowed for undershoot area	0.9	0.9	0.9	0.9	V
Maximum overshoot area above VDD	1.33	1.00	0.80	0.66	V.ns
Maximum undershoot area below VSS	1.33	1.00	0.80	0.66	V.ns

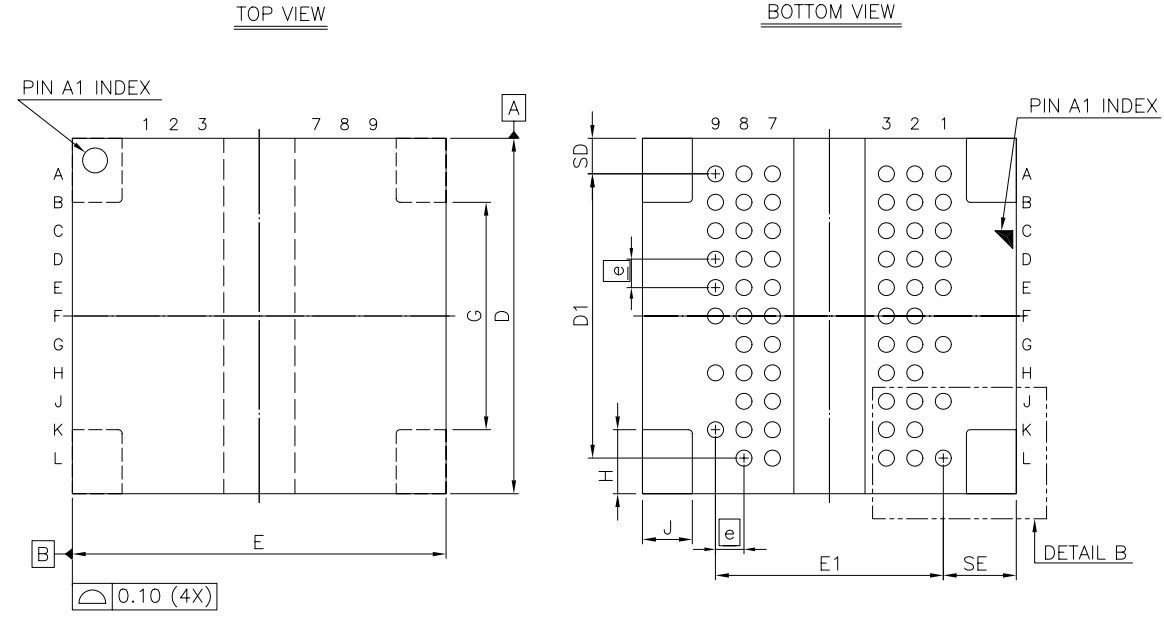


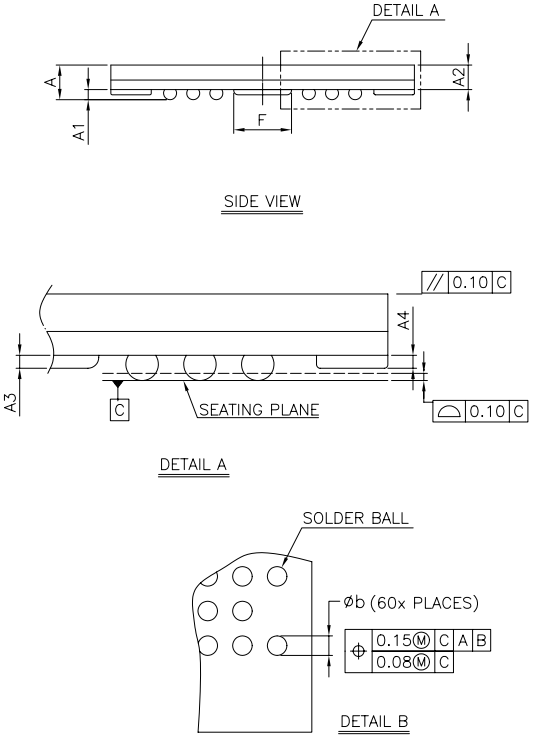
AC Overshoot / Undershoot Specification for Clock, Data, Strobe and Mask Pins

Parameter	DDR2 -400	DDR2 -533	DDR2 -667	DDR2 -800	Units
Maximum peak amplitude allowed for overshoot area	0.9	0.9	0.9	0.9	V
Maximum peak amplitude allowed for undershoot area	0.9	0.9	0.9	0.9	V
Maximum overshoot area above VDDQ	0.38	0.28	0.23	0.18	V.ns
Maximum undershoot area below VSSQ	0.38	0.28	0.23	0.18	V.ns



Package Dimension (x4/x8)
60Ball Fine Pitch Ball Grid Array Outline

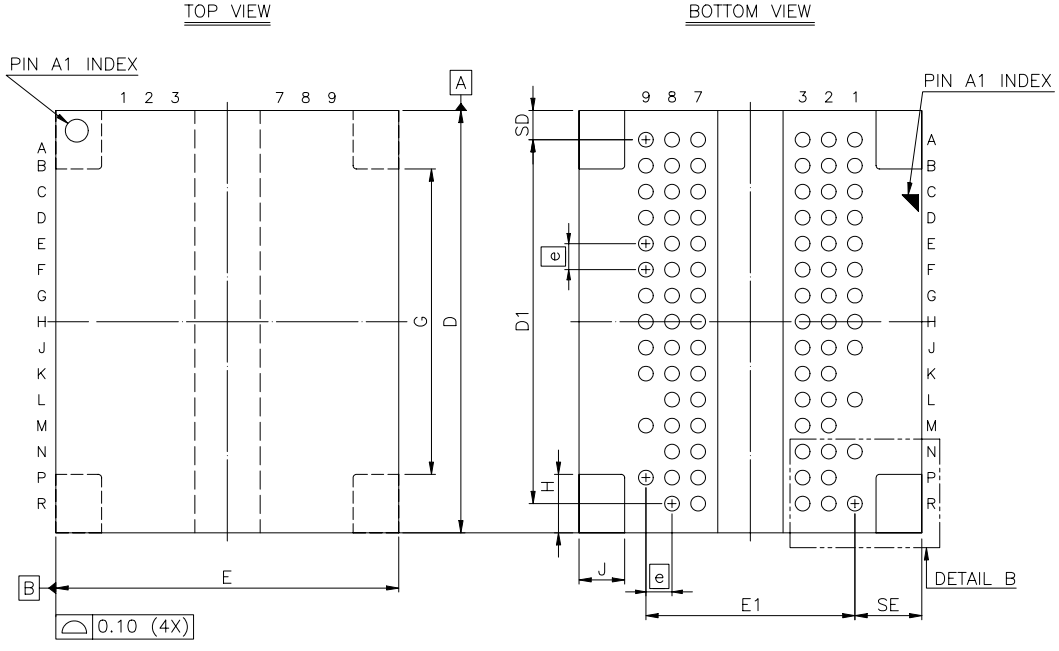


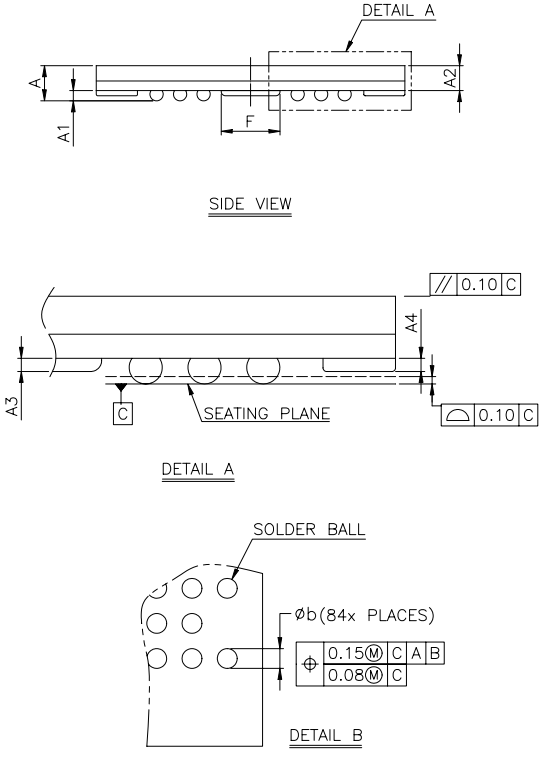


SYM.	DIMENSION (mm)			DIMENSION (inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.30	0.35	0.40	0.012	0.014	0.016
A2	—	—	0.84	—	—	0.033
A3	0.10	0.15	0.20	0.004	0.006	0.008
A4	0.18	0.20	0.22	0.007	0.008	0.009
b	0.40	0.45	0.50	0.016	0.018	0.020
D	9.90	10.00	10.10	0.390	0.394	0.398
D1	8.00 BSC			0.315 BSC		
E	10.40	10.50	10.60	0.409	0.413	0.417
E1	6.40 BSC			0.252 BSC		
F	2.00 BSC			0.079 BSC		
G	6.40 BSC			0.252 BSC		
H	1.80 BSC			0.071 BSC		
J	1.40 BSC			0.055 BSC		
SD	1.00 BSC			0.039 BSC		
SE	2.05 BSC			0.081 BSC		
e	0.80 BSC			0.031 BSC		

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER.
2. REFERENCE DOCUMENT : JEDEC MO−207.

Package Dimension (x16)
84Ball Fine Pitch Ball Grid Array Outline





SYM.	DIMENSION (mm)			DIMENSION (inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.30	0.35	0.40	0.012	0.014	0.016
A2	—	—	0.84	—	—	0.033
A3	0.10	0.15	0.20	0.004	0.006	0.008
A4	0.18	0.20	0.22	0.007	0.008	0.009
b	0.40	0.45	0.50	0.016	0.018	0.020
D	12.90	13.00	13.10	0.508	0.512	0.516
D1	11.20 BSC			0.441 BSC		
E	10.40	10.50	10.60	0.409	0.413	0.417
E1	6.40 BSC			0.252 BSC		
F	2.00 BSC			0.079 BSC		
G	9.40 BSC			0.370 BSC		
H	1.80 BSC			0.071 BSC		
J	1.40 BSC			0.055 BSC		
SD	0.90 BSC			0.035 BSC		
SE	2.05 BSC			0.081 BSC		
e	0.80 BSC			0.031 BSC		

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER.
2. REFERENCE DOCUMENT : JEDEC MO-207.

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