



# VNN7NV04P-E, VNS7NV04P-E

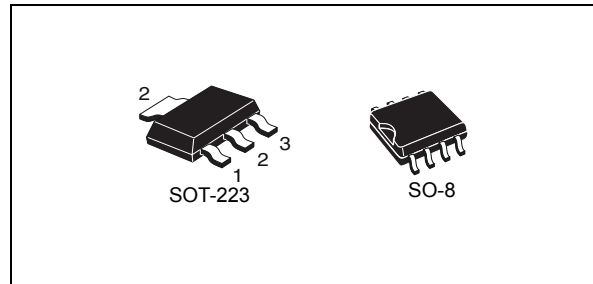
## OMNIFET II

### fully autoprotected Power MOSFET

## Features

Type	$R_{DS(on)}$	$I_{lim}$	$V_{clamp}$
VNN7NV04P-E VNS7NV04P-E	60 m $\Omega$	6 A	40 V

- Linear current limitation
- Thermal shutdown
- Short circuit protection
- Integrated clamp
- Low current drawn from input pin
- Diagnostic feedback through input pin
- ESD protection
- Direct access to the gate of the Power MOSFET (analog driving)
- Compatible with standard Power MOSFET in compliance with the 2002/95/EC European Directive



## Description

The VNN7NV04P-E, VNS7NV04P-E, are monolithic devices designed in STMicroelectronics VIPower™ M0-3 Technology, intended for replacement of standard Power MOSFETs from DC up to 50 kHz applications. Built in thermal shutdown, linear current limitation and overvoltage clamp protect the chip in harsh environments.

Fault feedback can be detected by monitoring the voltage at the input pin.

**Table 1. Device summary**

Package	Order codes	
	Tube	Tape and reel
SOT-223	-	VNN7NV04PTR-E
SO-8	VNS7NV04P-E	VNS7NV04PTR-E

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# 1 Block diagram and pin description

Figure 1. Block diagram

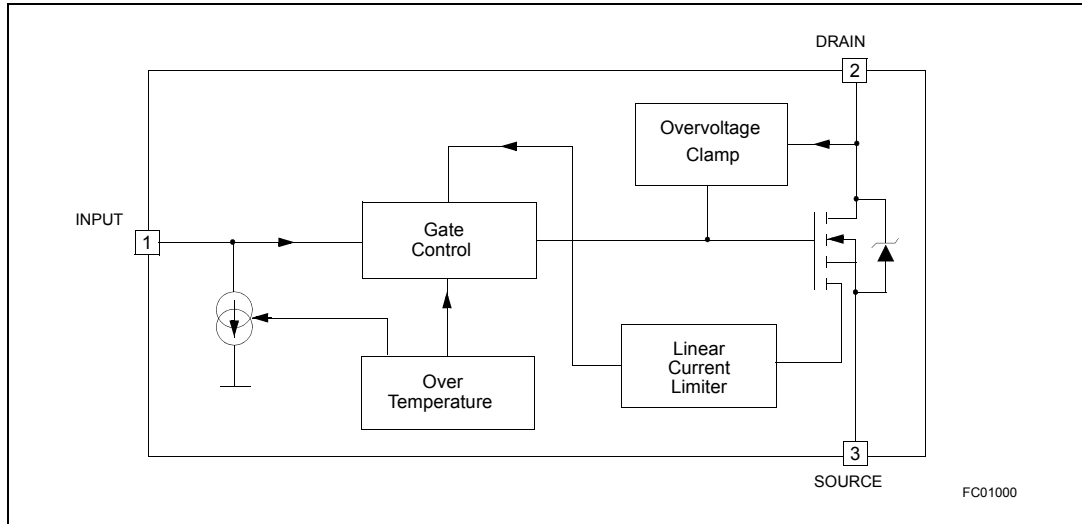
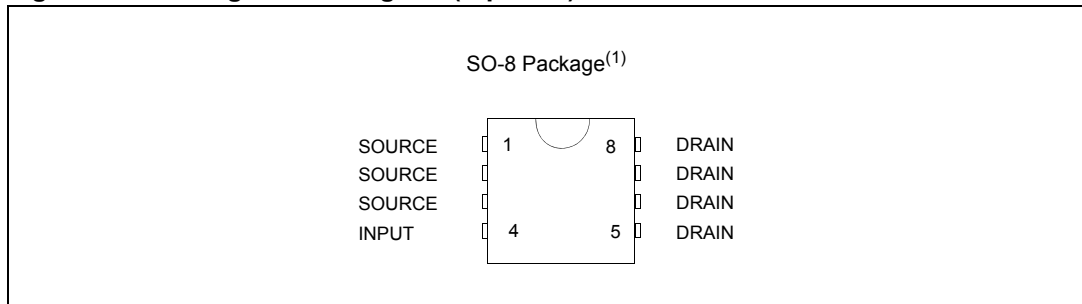


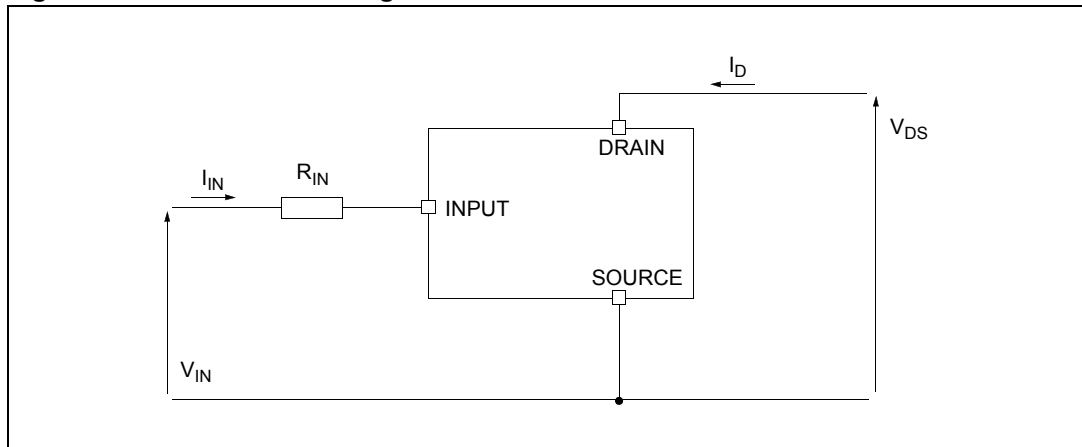
Figure 2. Configuration diagram (top view)



1. For the pins configuration related to SOT-223 see outlines at page 1.

## 2 Electrical specifications

Figure 3. Current and voltage conventions



### 2.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		SOT-223	SO-8	
$V_{DS}$	Drain-source voltage ( $V_{IN}=0$ V)	Internally clamped		V
$V_{IN}$	Input voltage	Internally clamped		V
$I_{IN}$	Input current	+/-20		mA
$R_{IN\ MIN}$	Minimum input series impedance	150		$\Omega$
$I_D$	Drain current	Internally limited		A
$I_R$	Reverse DC output current	-10.5		A
$V_{ESD1}$	Electrostatic discharge ( $R=1.5$ K $\Omega$ , $C=100$ pF)	4000		V
$V_{ESD2}$	Electrostatic discharge on output pin only ( $R=330$ $\Omega$ , $C=150$ pF)	16500		V
$P_{tot}$	Total dissipation at $T_c=25$ $^{\circ}C$	7	4.6	W
$E_{MAX}$	Maximum switching energy ( $L=0.7$ mH; $R_L=0$ $\Omega$ ; $V_{bat}=13.5$ V; $T_{jstart}=150$ $^{\circ}C$ ; $I_L=9$ A)	40		mJ
$E_{MAX}$	Maximum switching energy ( $L=0.6$ mH; $R_L=0$ $\Omega$ ; $V_{bat}=13.5$ V; $T_{jstart}=150$ $^{\circ}C$ ; $I_L=9$ A)		37	mJ
$T_j$	Operating junction temperature	Internally limited		$^{\circ}C$
$T_c$	Case operating temperature	Internally limited		$^{\circ}C$
$T_{stg}$	Storage temperature	-55 to 150		$^{\circ}C$

## 2.2 Thermal data

**Table 3. Thermal data**

Symbol	Parameter	Value		Unit
		SOT-223	SO-8	
$R_{thj-case}$	Thermal resistance junction-case max	18		°C/W
$R_{thj-lead}$	Thermal resistance junction-lead max		27	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max	96 <sup>(1)</sup>	90 <sup>(1)</sup>	°C/W

1. When mounted on a standard single-sided FR4 board with 0.5 mm<sup>2</sup> of Cu (at least 35 µm thick) connected to all DRAIN pins.

## 2.3 Electrical characteristics

-40 °C < T<sub>j</sub> < 150 °C, unless otherwise specified.

**Table 4. Electrical characteristics**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
<b>Off</b>						
V <sub>CLAMP</sub>	Drain-source clamp voltage	V <sub>IN</sub> =0 V; I <sub>D</sub> =3.5 A	40	45	55	V
V <sub>CLTH</sub>	Drain-source clamp threshold voltage	V <sub>IN</sub> =0 V; I <sub>D</sub> =2 mA	36			V
V <sub>INTH</sub>	Input threshold voltage	V <sub>DS</sub> =V <sub>IN</sub> ; I <sub>D</sub> =1 mA	0.5		2.5	V
I <sub>ISS</sub>	Supply current from input pin	V <sub>DS</sub> =0 V; V <sub>IN</sub> =5 V		100	150	µA
V <sub>INCL</sub>	Input-source clamp voltage	I <sub>IN</sub> =1 mA I <sub>IN</sub> =-1 mA	6 -1.0	6.8	8 -0.3	V
I <sub>DSS</sub>	Zero input voltage drain current (V <sub>IN</sub> =0 V)	V <sub>DS</sub> =13 V; V <sub>IN</sub> =0 V; T <sub>j</sub> =25 °C V <sub>DS</sub> =25 V; V <sub>IN</sub> =0 V			30 75	µA
<b>On</b>						
R <sub>DS(on)</sub>	Static drain-source on resistance	V <sub>IN</sub> =5 V; I <sub>D</sub> =3.5 A; T <sub>j</sub> =25 °C V <sub>IN</sub> =5 V; I <sub>D</sub> =3.5 A			60 120	mΩ
<b>Dynamic (T<sub>j</sub>=25 °C, unless otherwise specified)</b>						
g <sub>fs</sub> <sup>(1)</sup>	Forward transconductance	V <sub>DD</sub> =13 V; I <sub>D</sub> =3.5 A		9		S
C <sub>OSS</sub>	Output capacitance	V <sub>DS</sub> =13 V; f=1 MHz; V <sub>IN</sub> =0 V		220		pF
<b>Switching (T<sub>j</sub>=25 °C, unless otherwise specified)</b>						

## Electrical specifications

## VNN7NV04P-E, VNS7NV04P-E

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=15\text{ V}; I_D=3.5\text{ A}$ $V_{gen}=5\text{ V}; R_{gen}=R_{IN\text{ MIN}}=150\ \Omega$ (see figure <a href="#">Figure 4</a> )	100	300	100	ns
$t_r$	Rise time		470	1500	470	ns
$t_{d(off)}$	Turn-off delay time		500	1500	500	ns
$t_f$	Fall time		350	1000	350	ns
$t_{d(on)}$	Turn-on delay time	$V_{DD}=15\text{ V}; I_D=3.5\text{ A}$ $V_{gen}=5\text{ V}; R_{gen}=2.2\text{ K}\Omega$ (see figure <a href="#">Figure 4</a> )	0.75	2.3	0.75	$\mu\text{s}$
$t_r$	Rise time		4.6	14.0	4.6	$\mu\text{s}$
$t_{d(off)}$	Turn-off delay time		5.4	16.0	5.4	$\mu\text{s}$
$t_f$	Fall time		3.6	11.0	3.6	$\mu\text{s}$
$(di/dt)_{on}$	Turn-on current slope	$V_{DD}=15\text{ V}; I_D=3.5\text{ A}$ $V_{gen}=5\text{ V}; R_{gen}=R_{IN\text{ MIN}}=150\ \Omega$	6.5		6.5	$\text{A}/\mu\text{s}$
$Q_i$	Total input charge	$V_{DD}=12\text{ V}; I_D=3.5\text{ A}; V_{IN}=5\text{ V}$ $I_{gen}=2.13\text{ mA}$ (see figure <a href="#">Figure 7</a> )		18		nC
<b>Source drain diode (<math>T_j=25\text{ }^\circ\text{C}</math>, unless otherwise specified)</b>						
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD}=3.5\text{ A}; V_{IN}=0\text{ V}$		0.8		V
$t_{rr}$	Reverse recovery time	$I_{SD}=3.5\text{ A}; di/dt=20\text{ A}/\mu\text{s}$		220		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD}=30\text{ V}; L=200\ \mu\text{H}$		0.28		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see test circuit, figure <a href="#">Figure 5</a> )		2.5		A
<b>Protections (<math>-40\text{ }^\circ\text{C} &lt; T_j &lt; 150\text{ }^\circ\text{C}</math>, unless otherwise specified)</b>						
$I_{lim}$	Drain current limit	$V_{IN}=5\text{ V}; V_{DS}=13\text{ V}$	6	9	12	A
$t_{dlim}$	Step response current limit	$V_{IN}=5\text{ V}; V_{DS}=13\text{ V}$		4.0		$\mu\text{s}$
$T_{jsh}$	Overtemperature shutdown		150	175	200	$^\circ\text{C}$
$T_{jrs}$	Overtemperature reset		135			$^\circ\text{C}$
$I_{gf}$	Fault sink current	$V_{IN}=5\text{ V}; V_{DS}=13\text{ V}; T_j=T_{jsh}$		15		mA
$E_{as}$	Single pulse avalanche energy	starting $T_j=25\text{ }^\circ\text{C}; V_{DD}=24\text{ V}$ $V_{IN}=5\text{ V}; R_{gen}=R_{IN\text{ MIN}}=150\ \Omega; L=24\text{ mH}$ (see figures <a href="#">Figure 6</a> & <a href="#">Figure 8</a> )	200			mJ

1. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %



### 3 Protection features

During normal operation, the input pin is electrically connected to the gate of the internal Power MOSFET through a low impedance path.

The device then behaves like a standard Power MOSFET and can be used as a switch from DC up to 50 kHz. The only difference from the user's standpoint is that a small DC current  $I_{ISS}$  (typ. 100 $\mu$ A) flows into the input pin in order to supply the internal circuitry.

The device integrates:

- Overvoltage clamp protection: internally set at 45 V, along with the rugged avalanche characteristics of the Power MOSFET stage give this device unrivalled ruggedness and energy handling capability. This feature is mainly important when driving inductive loads.
- Linear current limiter circuit: limits the drain current  $I_D$  to  $I_{lim}$  whatever the input pin voltages. When the current limiter is active, the device operates in the linear region, so power dissipation may exceed the capability of the heatsink. Both case and junction temperatures increase, and if this phase lasts long enough, junction temperature may reach the overtemperature threshold  $T_{jsh}$ .
- Overtemperature and short circuit protection: these are based on sensing the chip temperature and are not dependent on the input voltage. The location of the sensing element on the chip in the power stage area ensures fast, accurate detection of the junction temperature. Overtemperature cutout occurs in the range 150 to 190 °C, a typical value being 170 °C. The device is automatically restarted when the chip temperature falls of about 15 °C below shutdown temperature.
- Status feedback: in the case of an overtemperature fault condition ( $T_j > T_{jsh}$ ), the device tries to sink a diagnostic current  $I_{gf}$  through the input pin in order to indicate fault condition. If driven from a low impedance source, this current may be used in order to warn the control circuit of a device shutdown. If the drive impedance is high enough so that the input pin driver is not able to supply the current  $I_{gf}$ , the input pin falls to 0 V. This however not affects the device operation: no requirement is put on the current capability of the input pin driver except to be able to supply the normal operation drive current  $I_{ISS}$ .

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Additional features of this device are ESD protection according to the Human Body model and the ability to be driven from a TTL logic circuit.

Figure 4. Switching time test circuit for resistive load

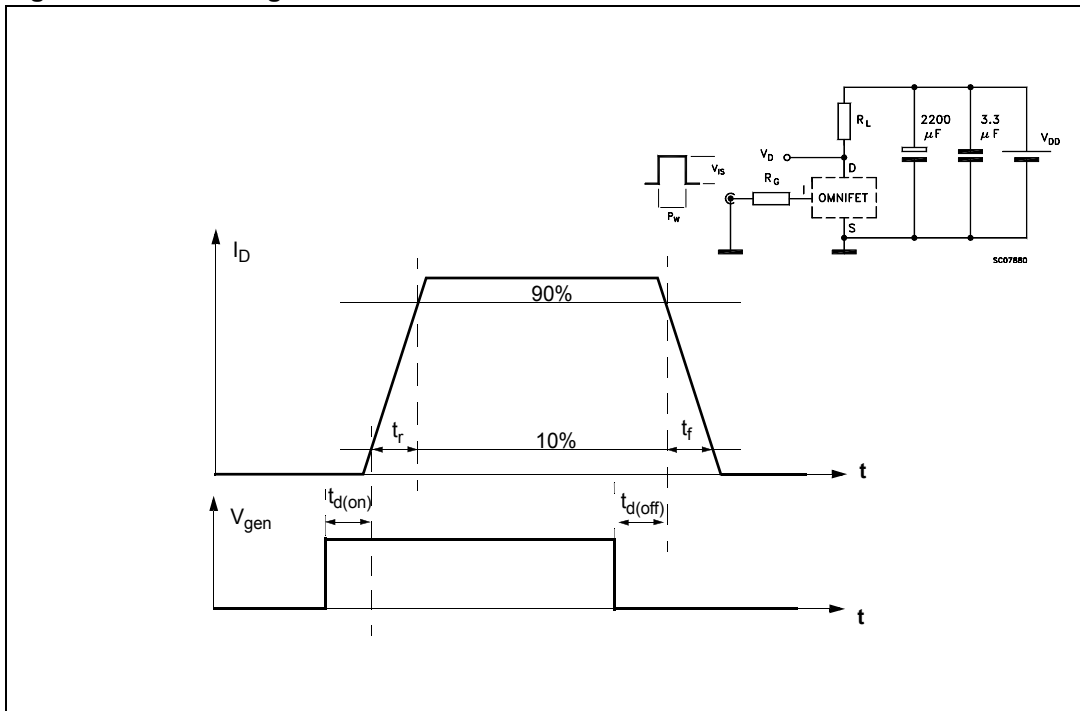
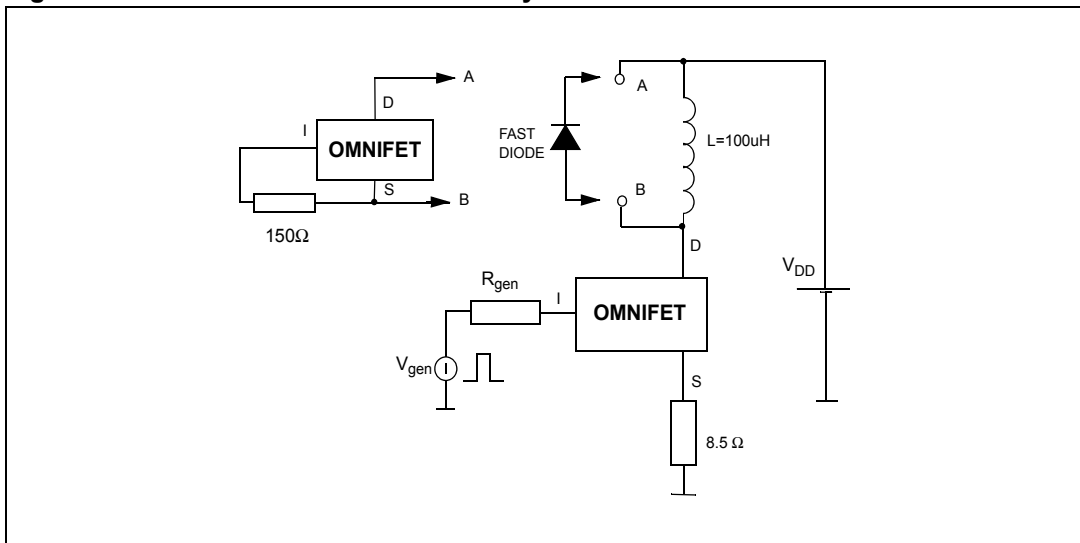


Figure 5. Test circuit for diode recovery times



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Figure 6. Unclamped inductive load test circuits

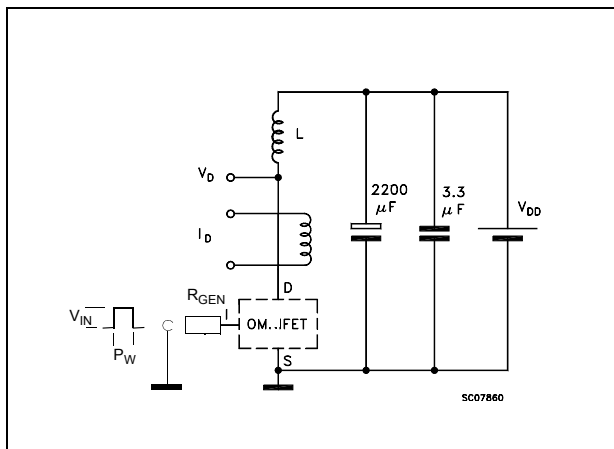


Figure 7. Input charge test circuit

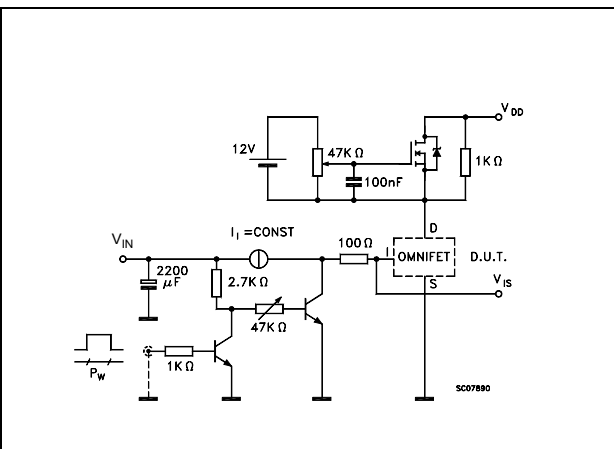
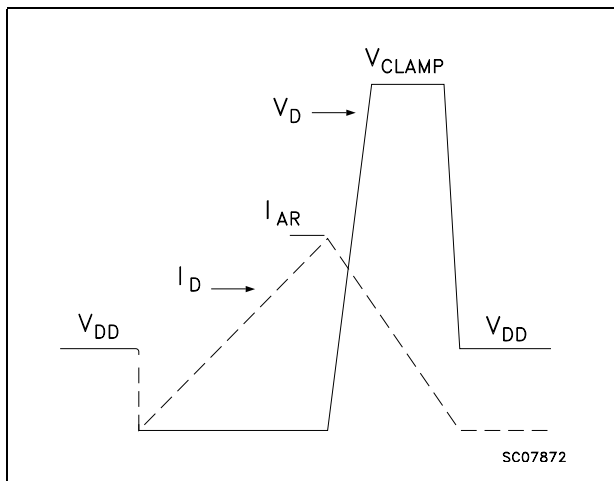


Figure 8. Unclamped inductive waveforms



### 3.1 Electrical characteristics curves

Figure 9. Derating curve

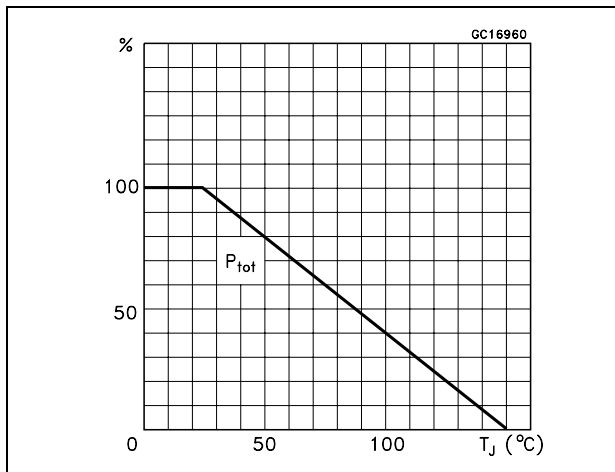


Figure 10. Transconductance

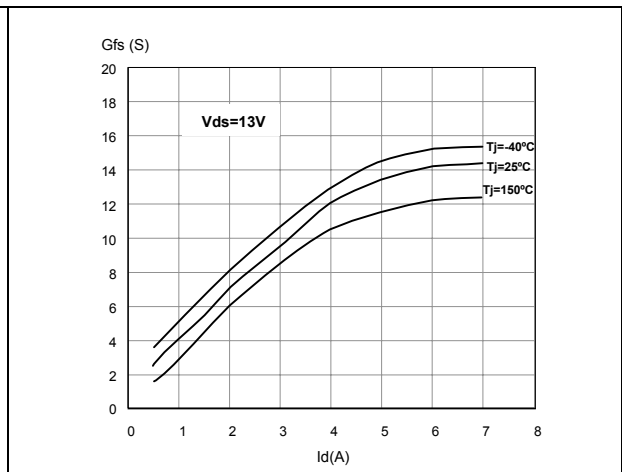


Figure 11. Static drain-source on resistance vs input voltage (part 1/2)

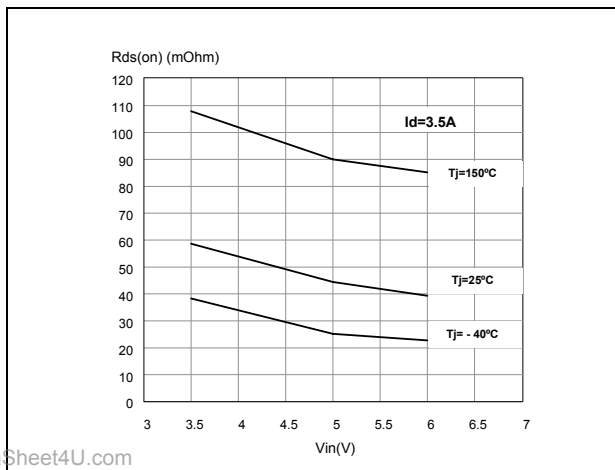


Figure 12. Static drain-source on resistance vs input voltage (part 2/2)

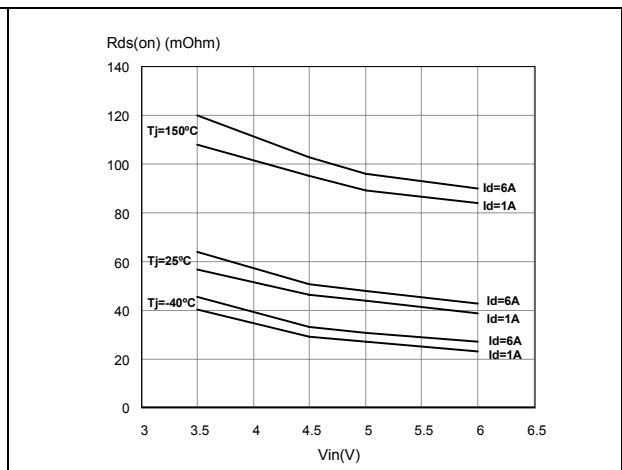


Figure 13. Source-drain diode forward characteristics

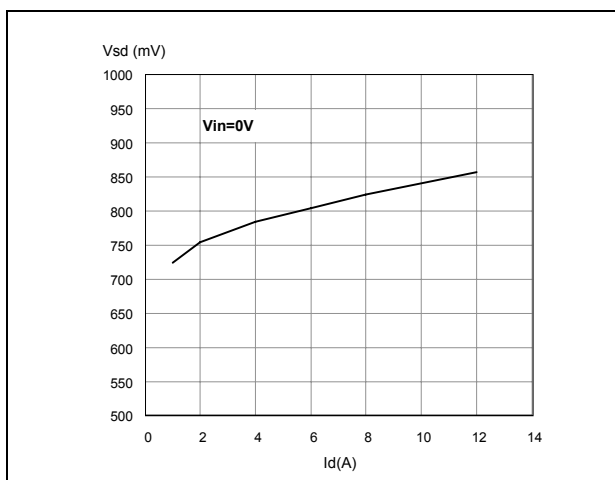
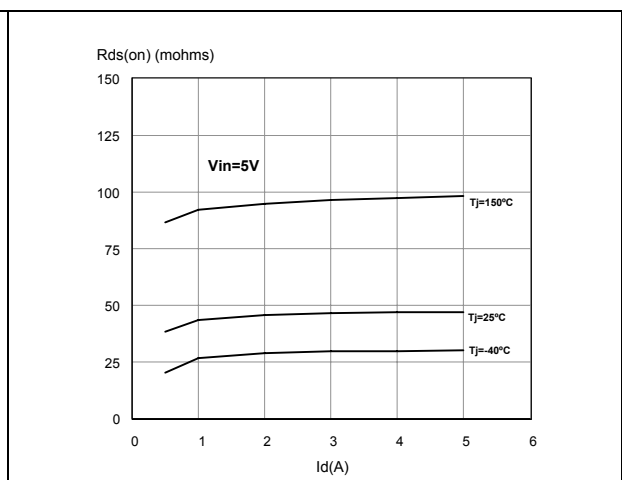


Figure 14. Static drain source on resistance



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Figure 15. Turn-on current slope (part 1/2)

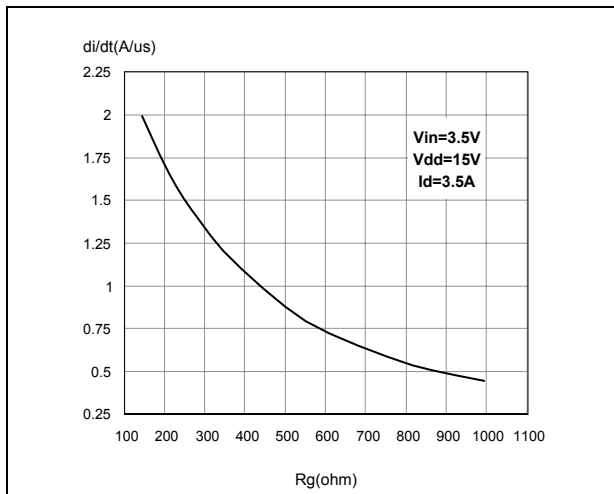


Figure 16. Turn-on current slope (part 2/2)

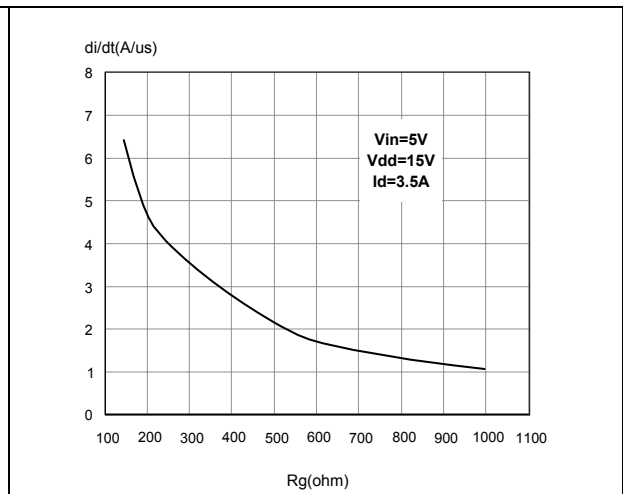


Figure 17. Transfer characteristics

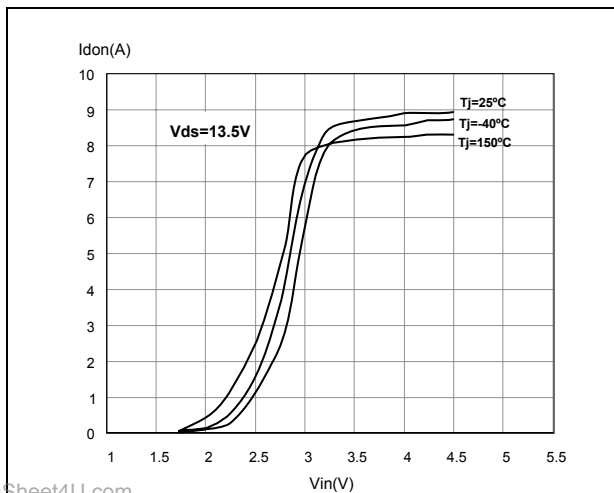


Figure 18. Static drain-source on resistance vs Id

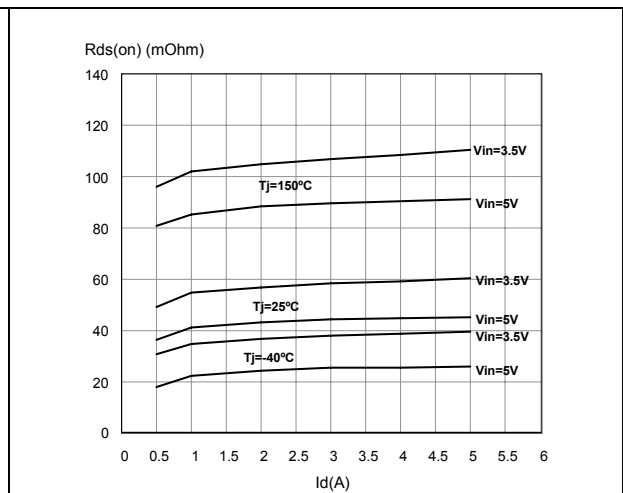


Figure 19. Input voltage vs input charge

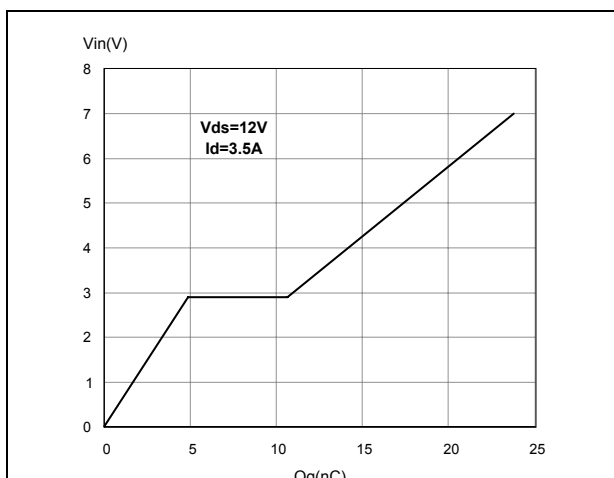
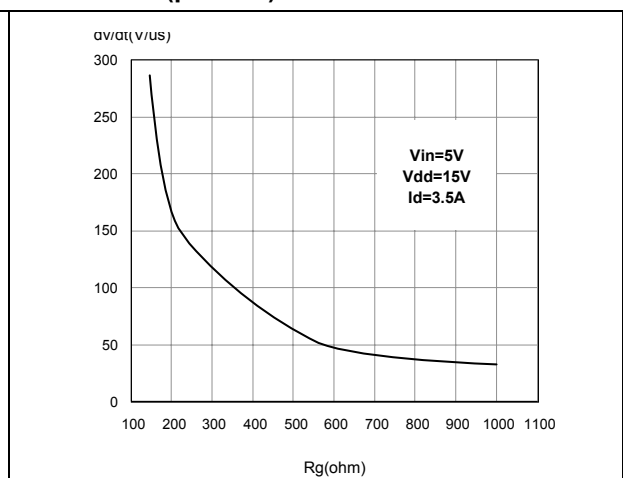


Figure 20. Turn-off drain source voltage slope (part 1/2)



Protection features

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Figure 21. Turn-off drain source voltage slope (part 2/2) Figure 22. Capacitance variations

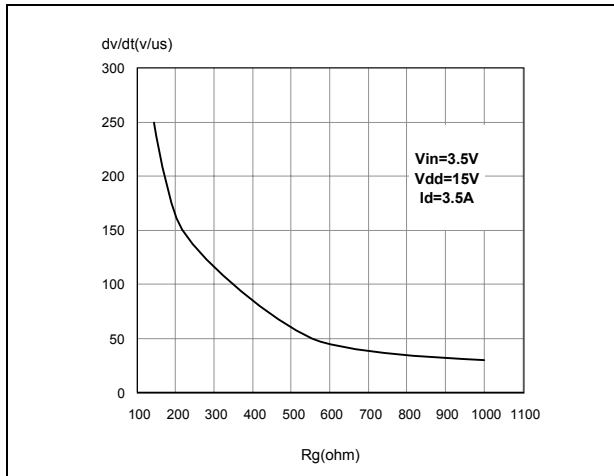


Figure 23. Output characteristics

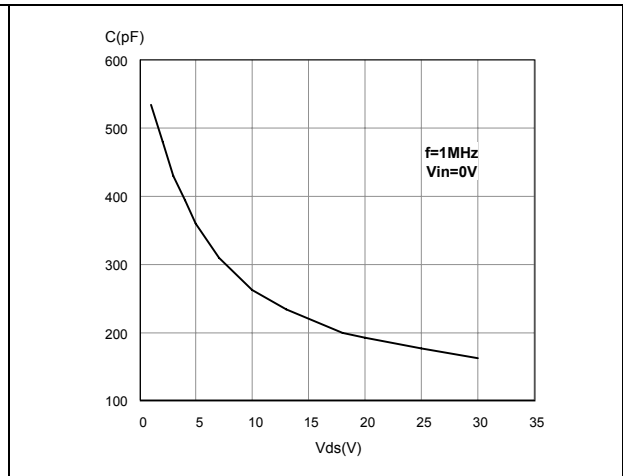


Figure 24. Normalized on resistance vs temperature

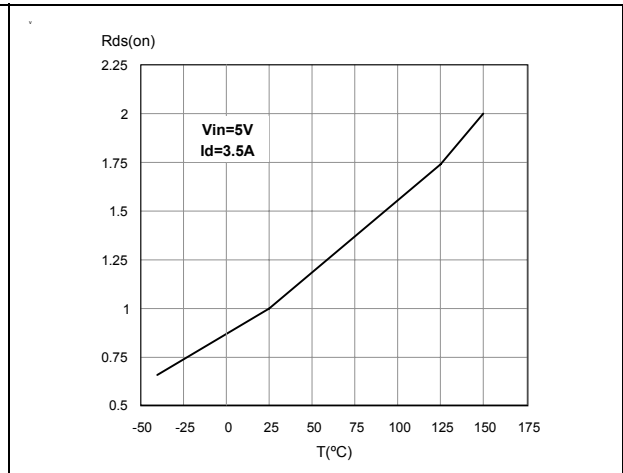
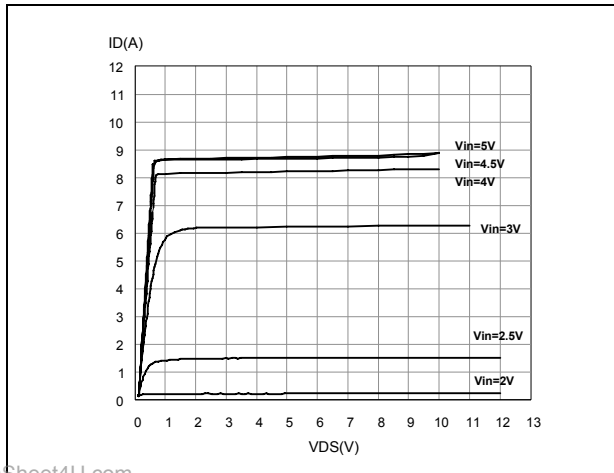
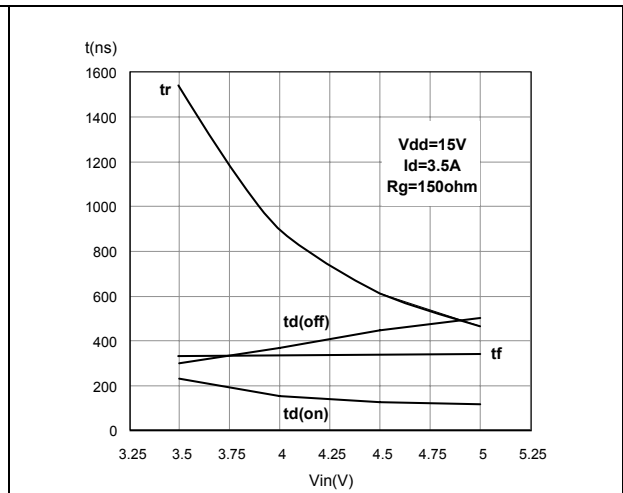
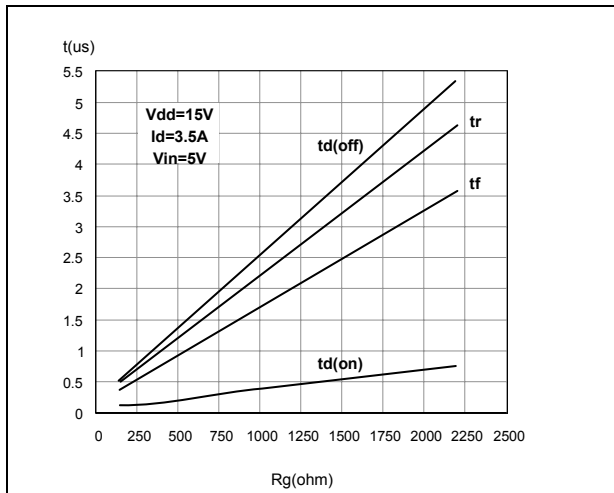
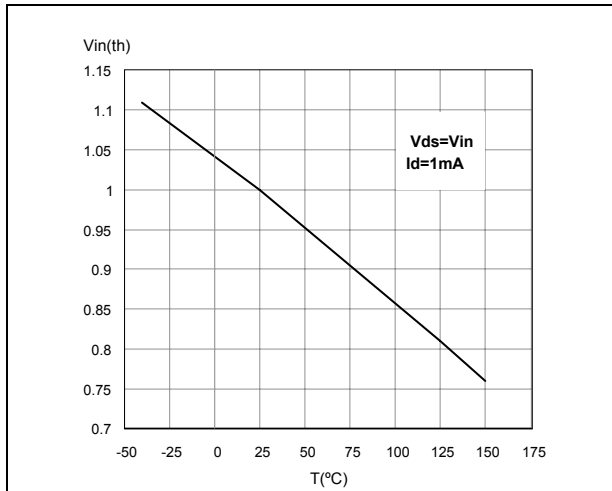


Figure 25. Switching time resistive load (part 1/2)

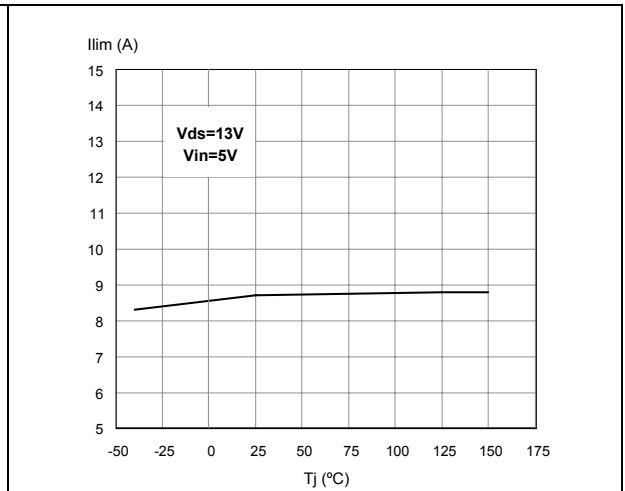
Figure 26. Switching time resistive load (part 2/2)



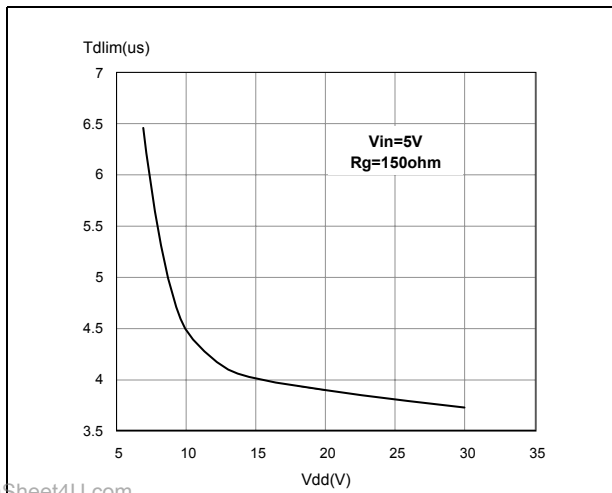
**Figure 27. Normalized input threshold voltage vs temperature**



**Figure 28. Normalized current limit vs junction temperature**



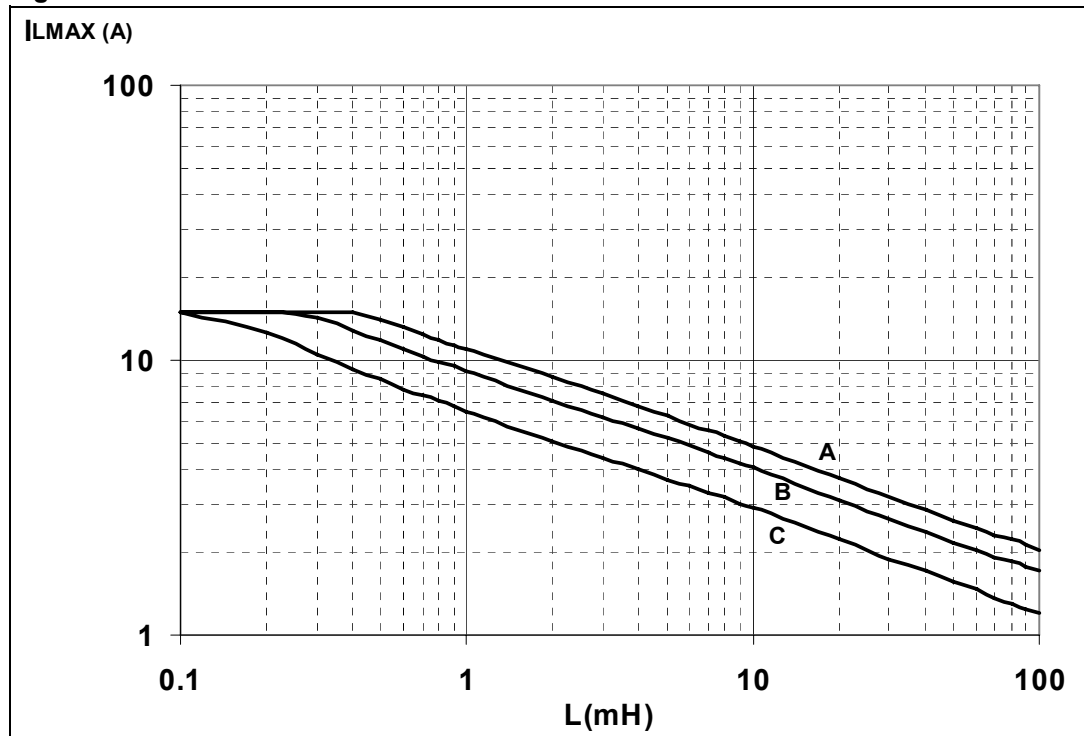
**Figure 29. Step response current limit**



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### 3.2 SO-8 maximum demagnetization energy

Figure 30. SO-8 maximum turn-off current versus load inductance



Legend

- A = Single Pulse at  $T_{Jstart}=150\text{ }^{\circ}\text{C}$
- B = Repetitive pulse at  $T_{Jstart}=100\text{ }^{\circ}\text{C}$
- C = Repetitive Pulse at  $T_{Jstart}=125\text{ }^{\circ}\text{C}$

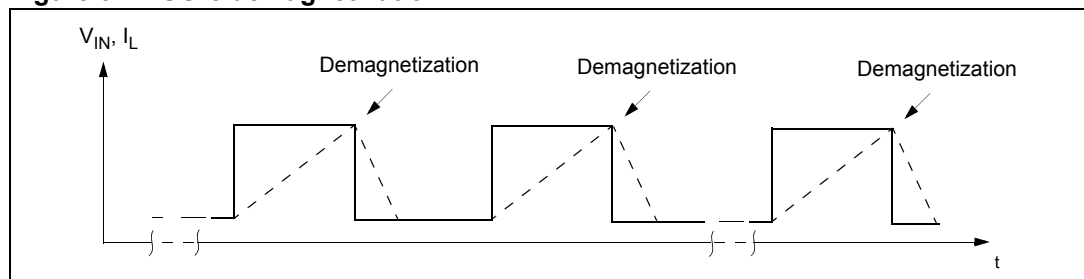
Conditions:

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$V_{CC}=13.5\text{ V}$

Values are generated with  $R_L=0\text{ }\Omega$ . In case of repetitive pulses,  $T_{Jstart}$  (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

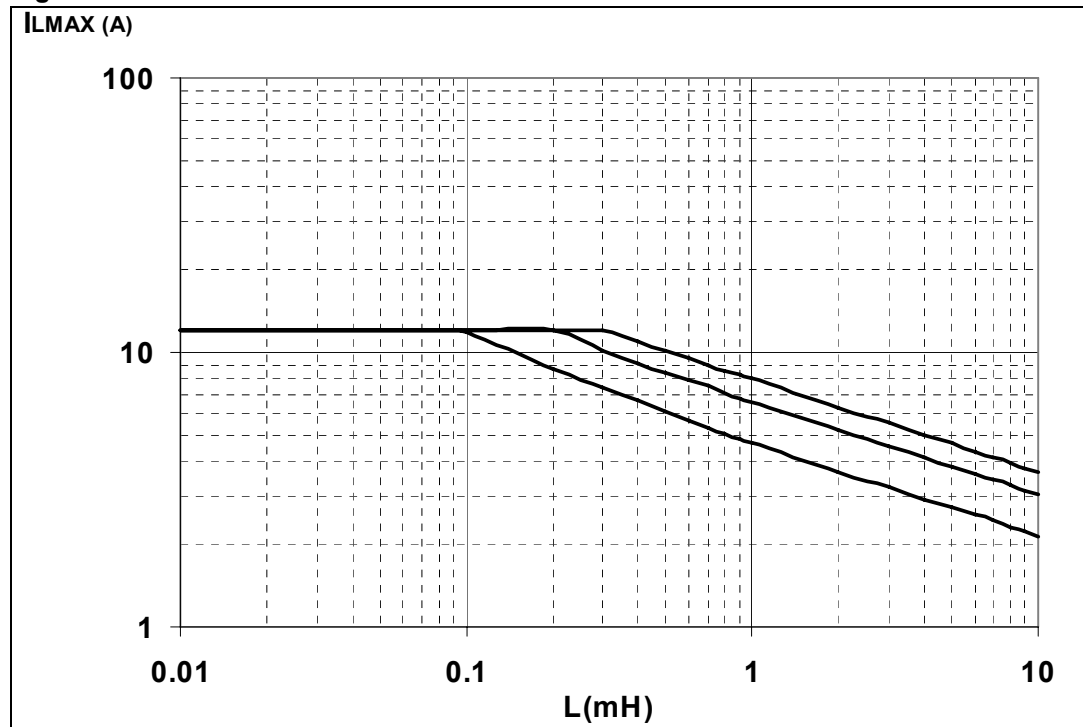
Figure 31. SO-8 demagnetization





### 3.3 SOT-223 maximum demagnetization energy

Figure 32. SOT-223 maximum turn-off current versus load inductance



Legend

A = Single Pulse at  $T_{Jstart}=150\text{ °C}$

B = Repetitive pulse at  $T_{Jstart}=100\text{ °C}$

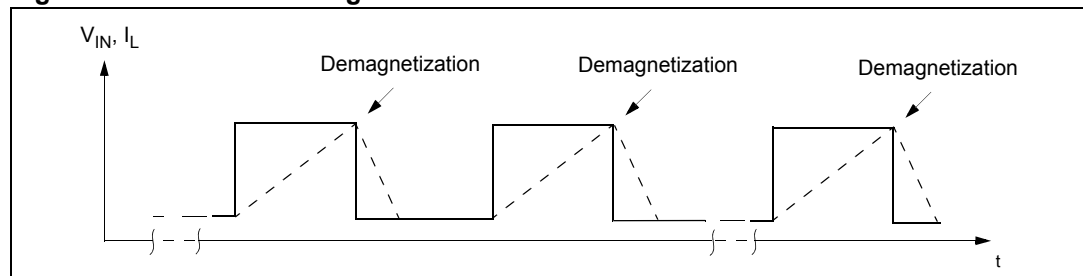
C = Repetitive Pulse at  $T_{Jstart}=125\text{ °C}$

Conditions:

$V_{CC}=13.5\text{ V}$

Values are generated with  $R_L=0\ \Omega$ . In case of repetitive pulses,  $T_{Jstart}$  (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

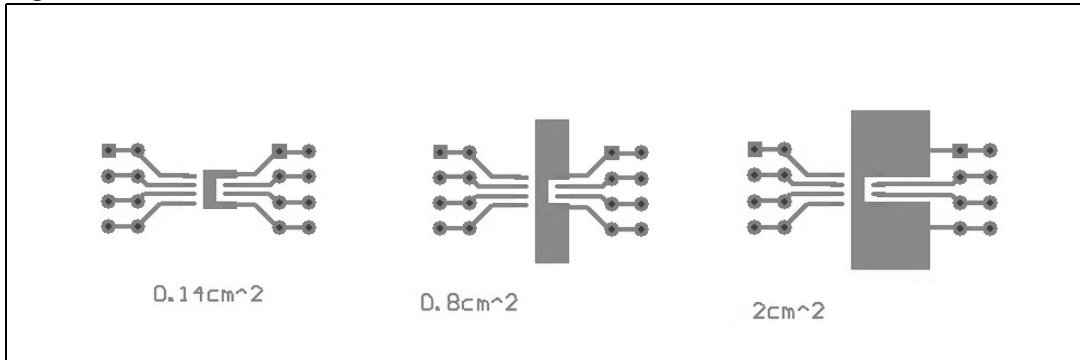
Figure 33. SOT-223 demagnetization



## 4 Package and PCB thermal data

### 4.1 SO-8 thermal data

Figure 34. SO-8 PC board



Note: Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB FR4 area=58 mm x 58 mm, PCB thickness=2 mm, Cu thickness=35  $\mu$ m, Copper areas: 0.14 cm<sup>2</sup>, 0.8 cm<sup>2</sup>, 2 cm<sup>2</sup>).

Figure 35.  $R_{thj-amb}$  vs PCB copper area in open box free air condition

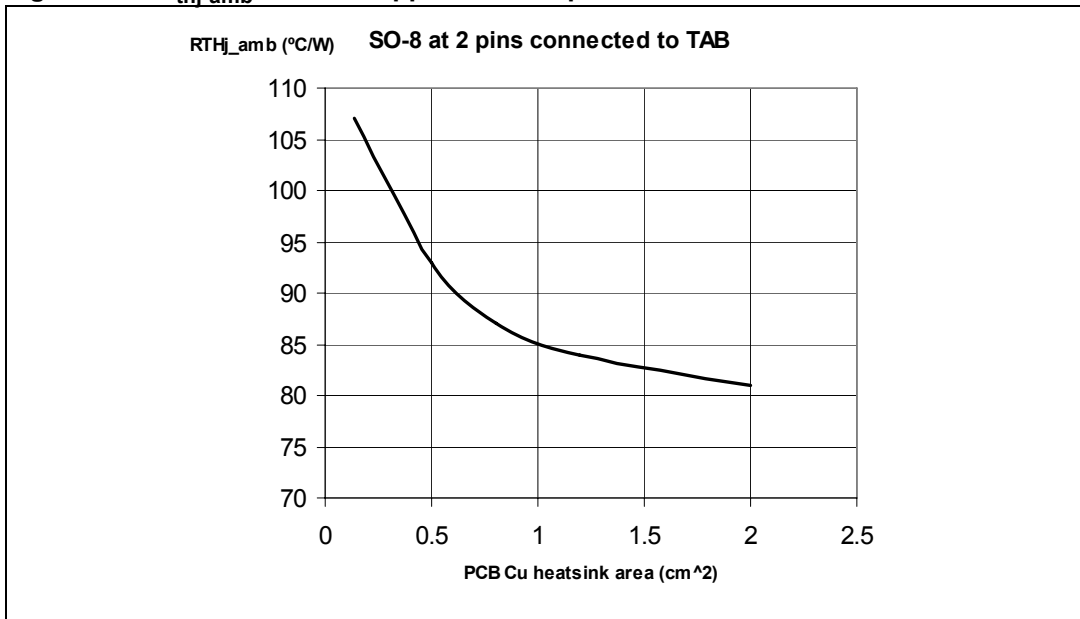


Figure 36. SO-8 thermal impedance junction ambient single pulse

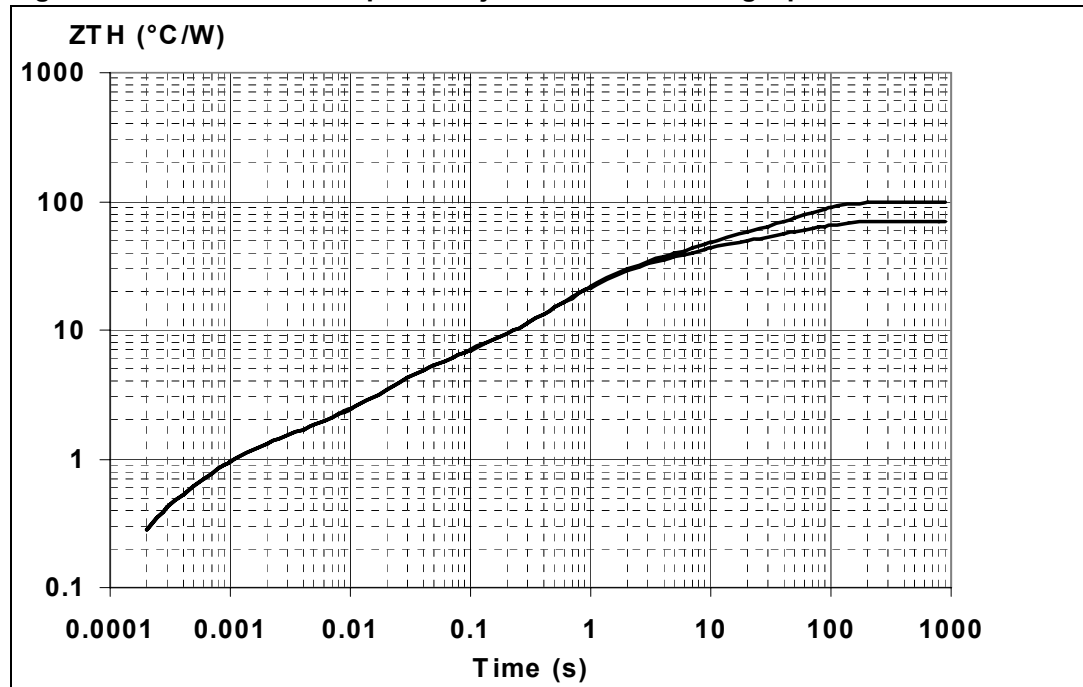
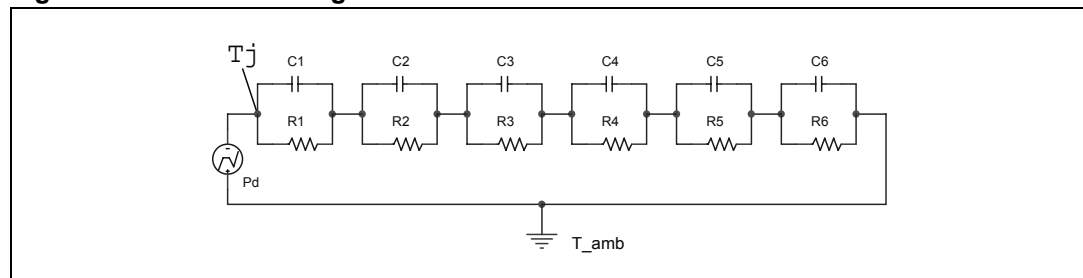


Figure 37. Thermal fitting model of an OMNIFET II in SO-8



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**Equation 1 Pulse calculation formula**

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

$$\text{where } \delta = t_p/T$$

Table 5. SO-8 thermal parameter

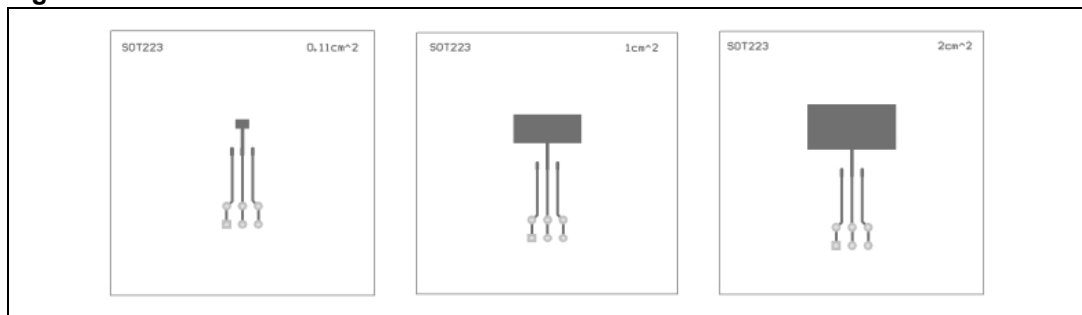
Area/island (cm <sup>2</sup> )	Footprint	2
R1 (°C/W)	0.2	
R2 (°C/W)	0.9	
R3 (°C/W)	3.5	
R4 (°C/W)	21	
R5 (°C/W)	16	
R6 (°C/W)	58	28
C1 (W.s/°C)	3.00E-04	

Table 5. SO-8 thermal parameter (continued)

Area/island (cm <sup>2</sup> )	Footprint	2
C2 (W.s/°C)	9.00E-04	
C3 (W.s/°C)	7.50E-03	
C4 (W.s/°C)	0.045	
C5 (W.s/°C)	0.35	
C6 (W.s/°C)	1.05	2

## 4.2 SOT-223 thermal data

Figure 38. SOT-223 PC board



Note: Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB FR4 area=58 mm x 58 mm, PCB thickness=2 mm, Cu thickness=35  $\mu$ m, Copper areas: 0.11 cm<sup>2</sup>, 1 cm<sup>2</sup>, 2 cm<sup>2</sup>).

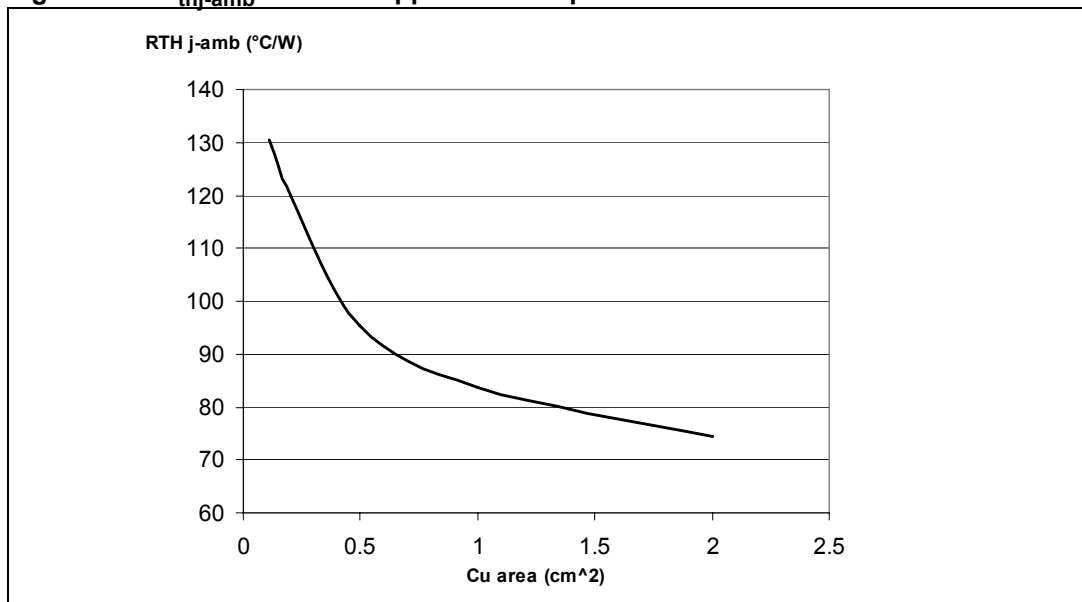
Figure 39.  $R_{thj-amb}$  vs PCB copper area in open box free air condition

Figure 40. SOT-223 thermal impedance junction ambient single pulse

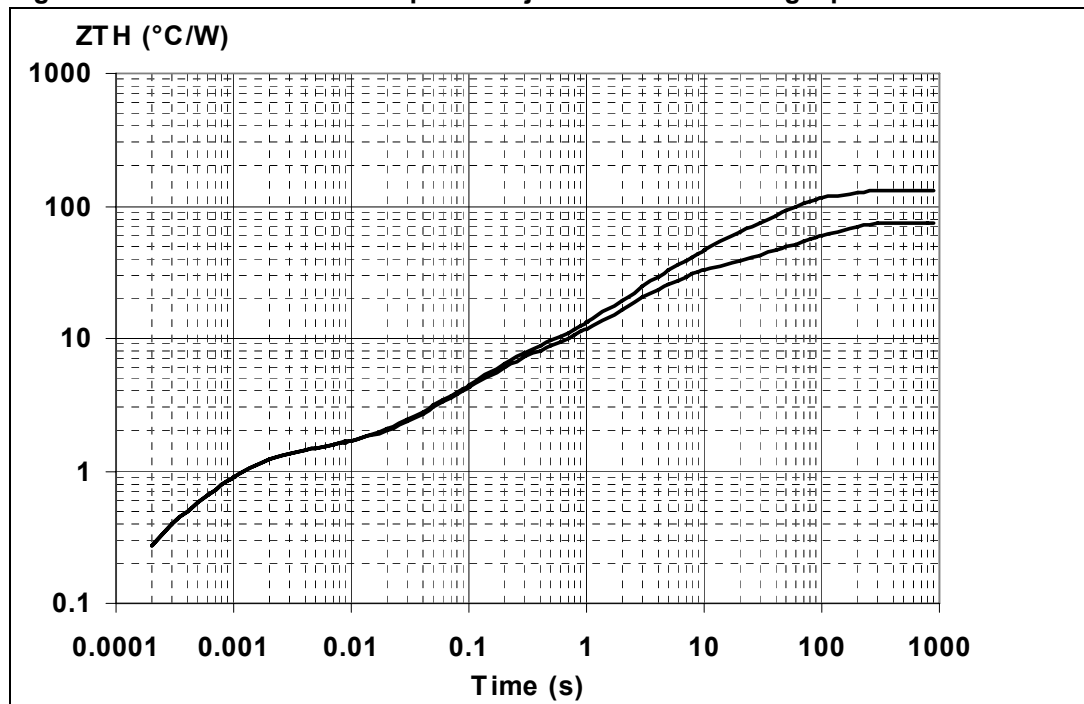
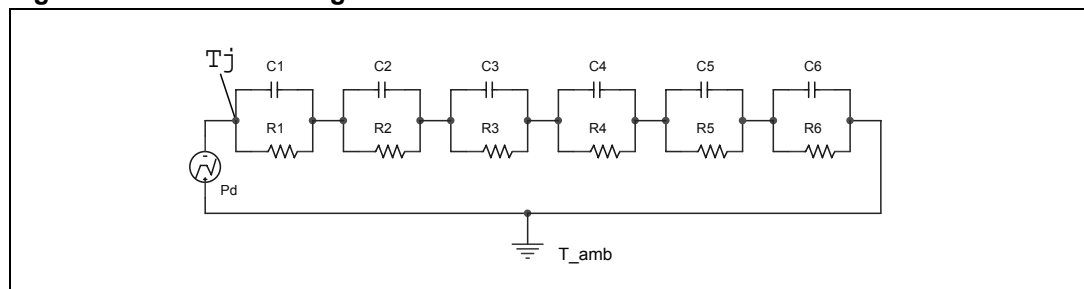


Figure 41. Thermal fitting model of an OMNIFET II in SOT-223



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**Equation 2 Pulse calculation formula**

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

Table 6. SOT-223 thermal parameter

Area/island (cm <sup>2</sup> )	Footprint	2
R1 (°C/W)	0.2	
R2 (°C/W)	1.1	
R3 (°C/W)	4.5	
R4 (°C/W)	24	
R5 (°C/W)	0.1	
R6 (°C/W)	100	45
C1 (W.s/°C)	3.00E-04	

Table 6. SOT-223 thermal parameter (continued)

Area/island (cm <sup>2</sup> )	Footprint	2
C2 (W.s/°C)	9.00E-04	
C3 (W.s/°C)	3.00E-02	
C4 (W.s/°C)	0.16	
C5 (W.s/°C)	1000	
C6 (W.s/°C)	0.5	2

## 5 Package and packing information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com).

ECOPACK® is an ST trademark.

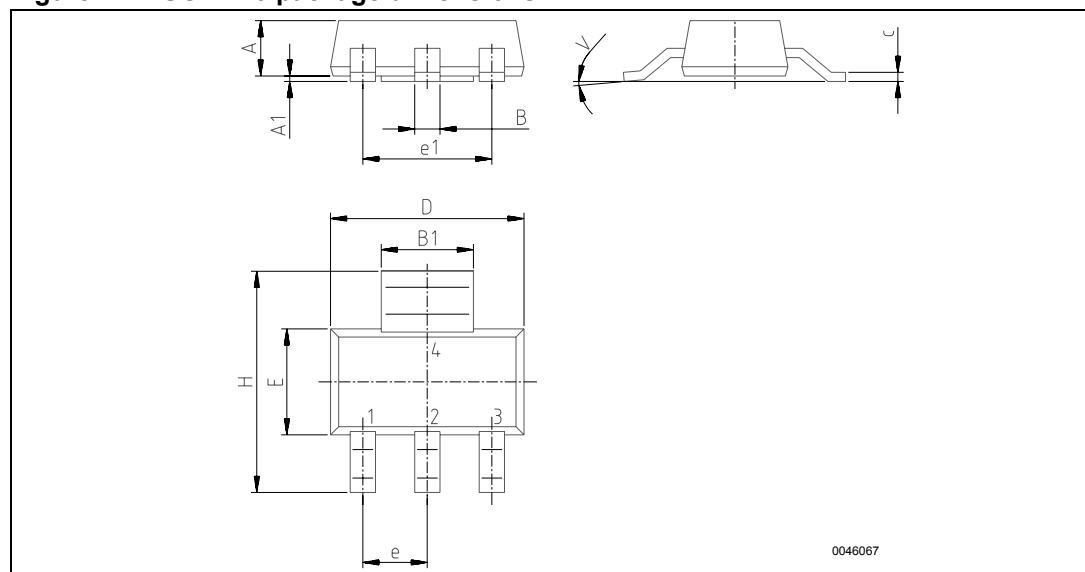
### 5.1 SOT-223 mechanical data

Table 7. SOT-223 mechanical data

Symbol	millimeters		
	Min.	Typ.	Max.
A			1.8
B	0.6	0.7	0.85
B1	2.9	3	3.15
c	0.24	0.26	0.35
D	6.3	6.5	6.7
e		2.3	
e1		4.6	
E	3.3	3.5	3.7
H	6.7	7	7.3
V	10 (max)		
A1	0.02		0.1

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Figure 42. SOT-223 package dimensions



## 5.2 SO-8 mechanical data

Table 8. SO-8 mechanical data

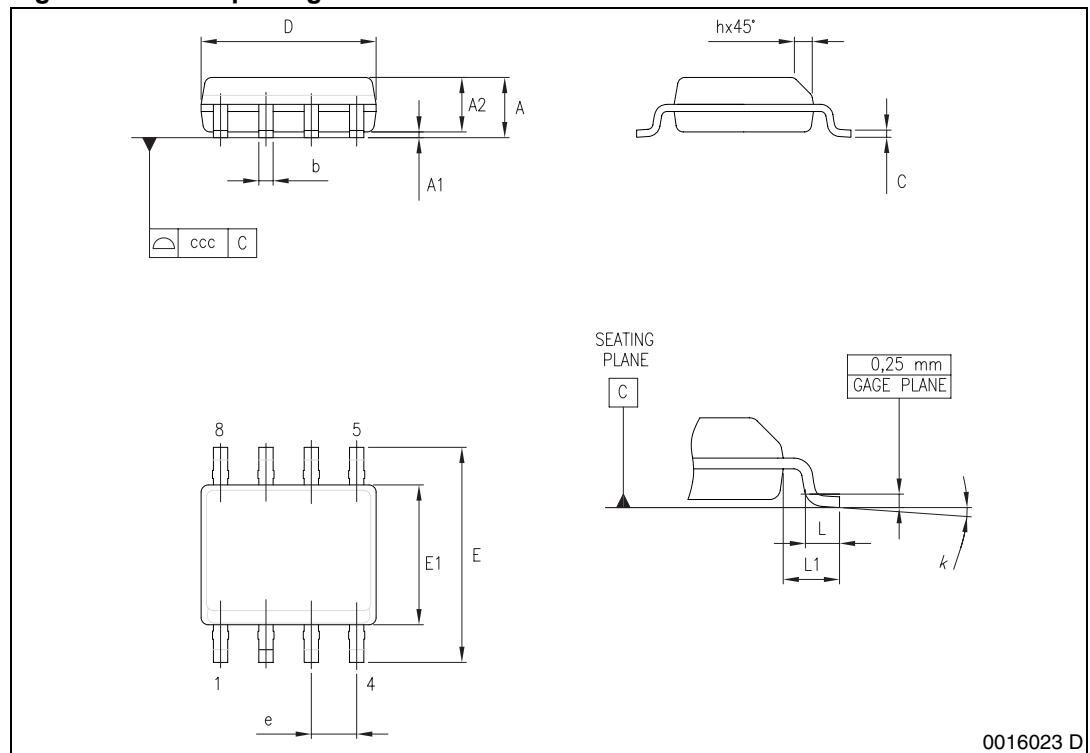
Symbol	millimeters		
	Min	Typ	Max
A			1.75
a1	0.1		0.25
a2			1.65
a3	0.65		0.85
b	0.35		0.48
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.28		0.48
c	0.17		0.23
D <sup>(1)</sup>	4.80	4.90	5.00
E	5.80	6.00	6.20
E1 <sup>(2)</sup>	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°
ccc			0.10

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1. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm in total (both side).
2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.

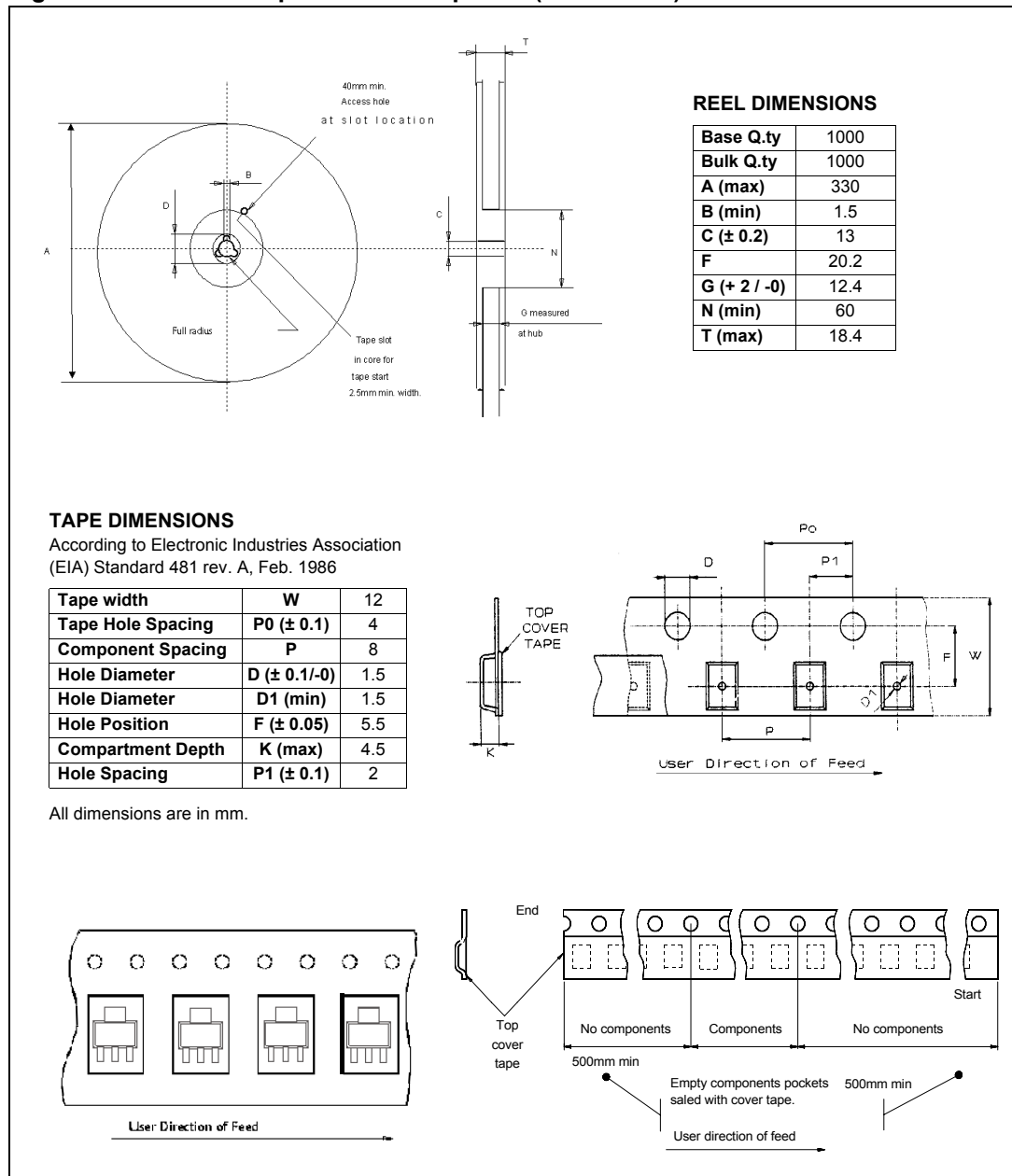


Figure 43. SO-8 package dimensions



### 5.3 SOT-223 packing information

Figure 44. SOT-223 tape and reel shipment (suffix "TR")



### 5.4 SO-8 packing information

Figure 45. SO-8 tube shipment (no suffix)

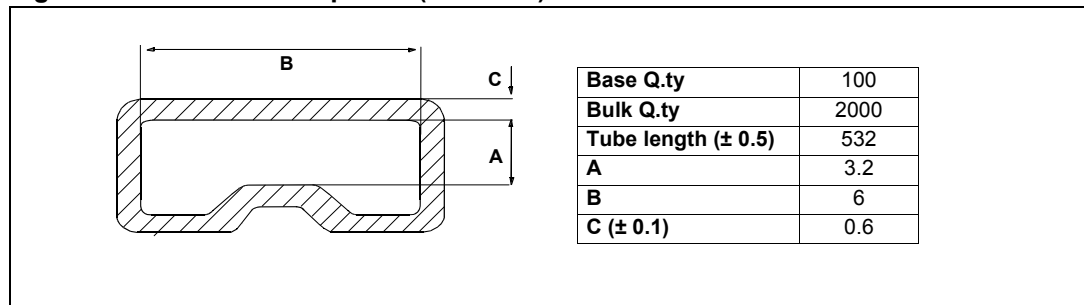
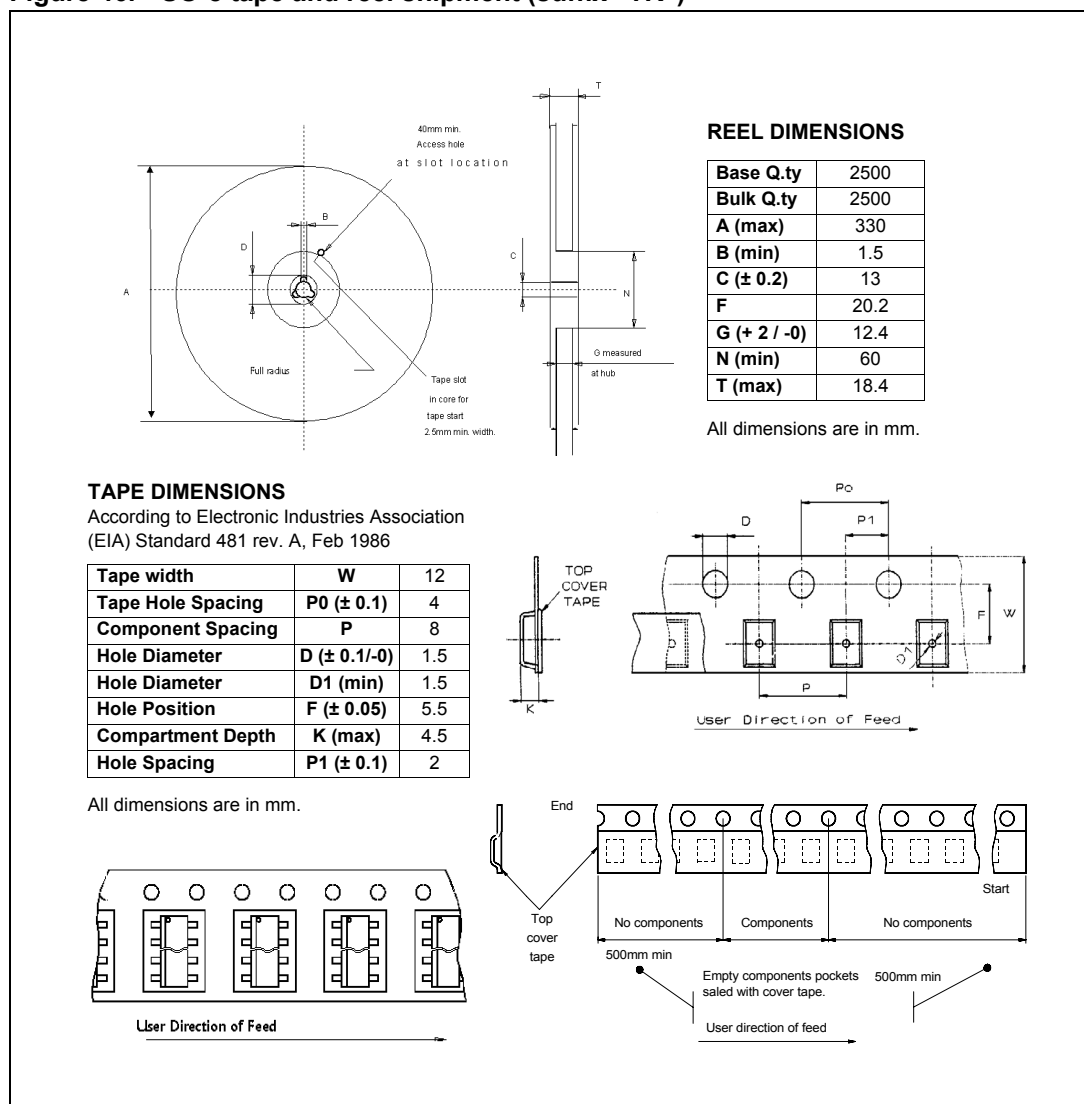


Figure 46. SO-8 tape and reel shipment (suffix "TR")



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## 6 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
15-Oct-2009	1	Initial release.

## VNN7NV04P-E, VNS7NV04P-E

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