Am21L41

4096x1 Static RAM

DISTINCTIVE CHARACTERISTICS

- Fully static storage and interface circuitry
- Automatic power-down when deselected
- Low power dissipation
  - Am21L41; 220 mW active, 27.5 mW power down
- High output drive
- TTL compatible interface levels
- No power-on current surge

GENERAL DESCRIPTION

The Am21L41 is a high-performance, 4096-bit, static, read/write, random-access memory. It is organized as 4096 words by one bit per word. All interface signal levels are identical to TTL specifications, providing good noise immunity and simplified system design. All inputs are purely capacitive MOS loads. The outputs will drive up to seven standard Schottky TTL loads or up to six standard TTL loads.

Only a single + 5-volt power supply is required. When deselected ($\overline{CS} \geqslant V_{IH}$), the Am21L41 automatically enters a power-down mode which reduces power dissipation by as much as 85%. When selected, the chip powers up again with no access time penalty.

Data In and Data Out use separate pins on the standard 18-pin package. Data Out is the same polarity as Data In. Data Out is a three-state signal allowing wired-OR operation of several chips. Data In and Data Out may be connected together for operation in a common data bus environment.
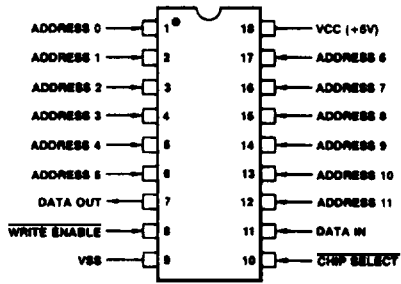
BLOCK DIAGRAM

BD000111
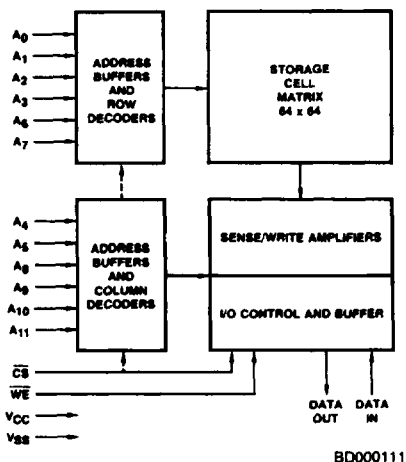
PRODUCT SELECTOR GUIDE

Part Number	Am21L41-12	Am21L41-15	Am21L41-20	Am21L41-25
Maximum Access Time (ns)	120	150	200	250
Maximum Active Current (mA)	55	40	40	40
Maximum Standby Current (mA)	10	5	5	5

CONNECTION DIAGRAM
Top View

Pin	Signal		Pin	Signal
ADDRESS 0	1		18	VCC (+5V)
ADDRESS 1	2		17	ADDRESS 6
ADDRESS 2	3		16	ADDRESS 7
ADDRESS 3	4		15	ADDRESS 8
ADDRESS 4	5		14	ADDRESS 9
ADDRESS 5	6		13	ADDRESS 10
DATA OUT	7		12	ADDRESS 11
WRITE ENABLE	8		11	DATA IN
VSS	9		10	CHIP SELECT

CD000161

Note: Pin 1 is marked for orientation.

METALLIZATION AND PAD LAYOUT

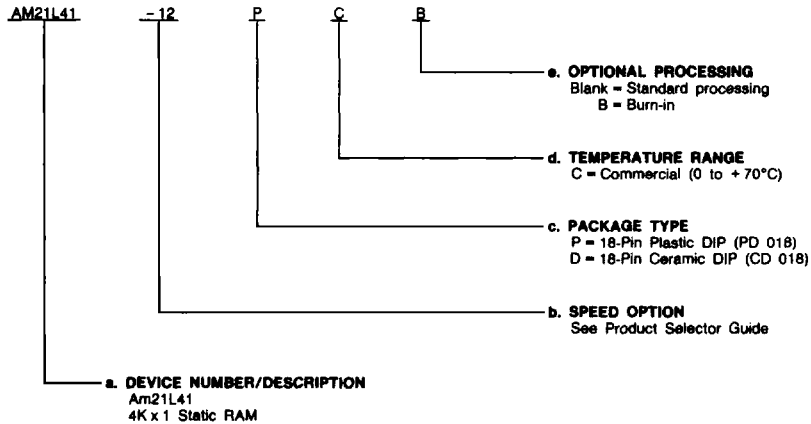| Address Designators	
External	Internal
A_0	A_2
A_1	A_5
A_2	A_4
A_3	A_3
A_4	A_8
A_5	A_7
A_6	A_1
A_7	A_0
A_8	A_{11}
A_9	A_9
A_{10}	A_{10}
A_{11}	A_6
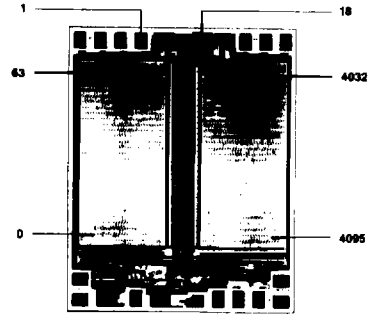
Die Size: 0.130" x 0.106"

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing

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AM21L41       -12      P      C      B
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e. OPTIONAL PROCESSING
Blank = Standard processing
B = Burn-in

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)

c. PACKAGE TYPE
P = 18-Pin Plastic DIP (PD 018)
D = 18-Pin Ceramic DIP (CD 018)

b. SPEED OPTION
See Product Selector Guide

a. DEVICE NUMBER/DESCRIPTION
Am21L41
4K x 1 Static RAM

Valid Combinations	
AM21L41-12	PC, PCB, DC, DCB
AM21L41-15	
AM21L41-20	
AM21L41-25	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

$A_0 - A_{11}$ Address (Inputs)
The address input lines select memory location from which to read or write.

$\overline{CS}$ Chip Select (Input, Active LOW)
The Chip Select line selects the memory device for active operation.

$\overline{WE}$ Write Enable (Input, Active LOW)
When both $\overline{CS}$ and $\overline{WE}$ are LOW, data on the input lines is written to the location presented on the address input lines.

D_{IN} Data In (Input)
This pin is used to enter data during write operations.

D_{OUT} Data Out (Output, Three-State)
The content of the selected memory location is presented on the Data Output line during read operations ($\overline{CS}$ LOW, $\overline{WE}$ HIGH). The line goes three-state during write operations.

V_{CC} Power Supply

V_{SS} Ground

ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature .... – 65 to + 150°C
Ambient Temperature with
Power Applied .... 0 to + 70°C
Supply Voltage .... – 0.5 V to + 7.0 V
All Signal Voltage with
Respect to Ground........................ – 1.5 V to + 7.0 V
Power Dissipation .... 1.2 W
DC Output Current .... 20 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES (Note 2)

Commcercial (C) Devices
Temperature (T_A)................................. 0 to + 70°C
Supply Voltage (V_{CC}) .... + 4.5 V to + 5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Am21L41-12		Am21L41-15, Am21L41-20, Am21L41-25		Units
				Min.	Max.	Min.	Max.	
I_{OH}	Output HIGH Current	V_{OH} = 2.4 V	V_{CC} = 4.5 V	– 4		– 4		mA
I_{OL}	Output LOW Current	V_{OL} = 0.4 V	T_A = 70°C	8		8		mA
V_{IH}	Input HIGH Voltage			2.0	6.0	2.0	6.0	V
V_{IL}	Input LOW Voltage			– 2.5	0.8	– 2.5	0.8	V
I_{IX}	Input Load Current	$V_{SS} \le V_I \le V_{CC}$			10		10	μA
I_{OZ}	Output Leakage Current	$V_{SS} \le V_O \le V_{CC}$ Output Disabled	T_A = 70°C	– 10	10	– 10	10	μA
I_{OS}	Output Short-Circuit Current	$V_{SS} \le V_O \le V_{CC}$ (Note 3)	0 to + 70°C	– 120	120	– 120	120	mA
I_{CC}	V_{CC} Operating Supply Current	Max. V_{CC}, $\overline{CS} \le V_{IL}$	T_A = 0°C		55		40	mA
I_{SB}	Automatic $\overline{CS}$ Power Down Current	Max. V_{CC}, ($\overline{CS} \ge V_{IH}$) (Note 5)			10		5.0	mA
C_I	Input Capacitance (Note 13)	Test Frequency = 1.0 MHz T_A = 25°C, All pins at 0 V			5.0		5.0	pF
C_O	Output Capacitance (Note 13)				6.0		6.0	pF

Notes: 1. Absolute Maximum Ratings are intended for user guidelines and are not tested.
2. For test and correlation purpose, operating temperature is defined as the "instant-ON" case temperature.
3. Short-circuit test duration should not exceed 30 seconds. Actual testing is performed for only 5 ms.
4. Test conditions assume signal transition times of 10 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.5 V and output loading of the specified I_{OL}/I_{OH} and C_L = 30 pF load capacitance (reference A. under Switching Test Circuit.).
5. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
6. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power up, otherwise I_{SB} will exceed values given.
7. Chip deselected greater than 55 ns prior to selection.
8. Chip deselected less than 55 ns prior to selection.
9. Transition is measured at V_{OH} – 500 mV and V_{OL} + 500 mV levels on the output from 1.5 V level on the input with load shown in Figure A using C_L = 5 pF (under switching test circuit).
10. $\overline{WE}$ is HIGH for read cycle.
11. Device is continuously selected, $\overline{CS}$ = V_{IL}.
12. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
13. These parameters are not 100% tested, but are evaluated at initial characterization and at anytime the design is modified where capacitance may be affected.
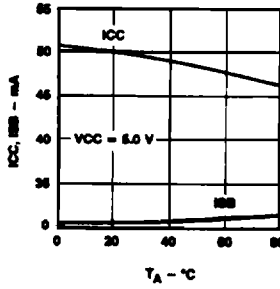
TYPICAL DC and AC CHARACTERISTICS
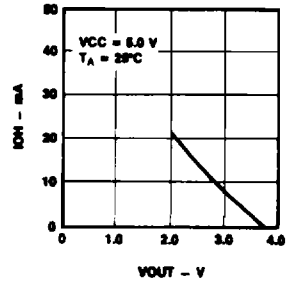
Supply Current Versus Supply Voltage
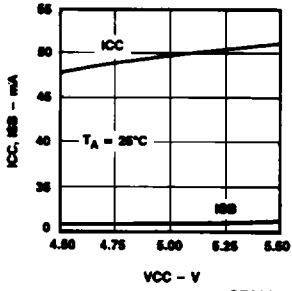
OP000820
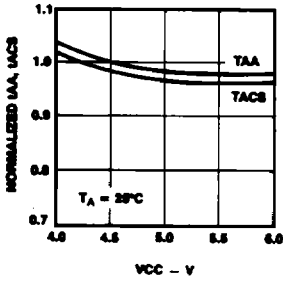
Supply Current Versus Ambient Temperature

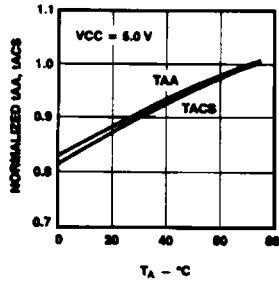

OP000831

Output Source Current Versus Output Voltage

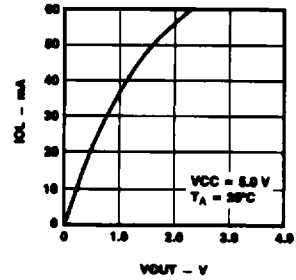
OP000841

Normalized Access Time Versus Supply Voltage

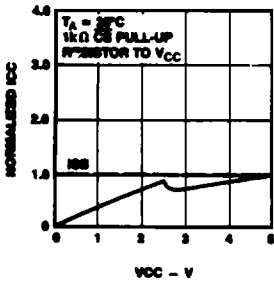OP000760

Normalized Access Time Versus Ambient Temperature

OP000851

Output Sink Current Versus Output Voltage
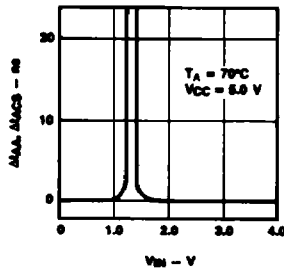

OP000861

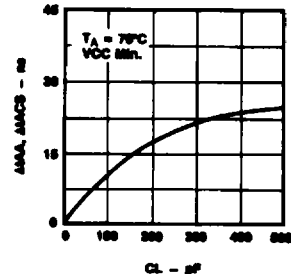### Typical Power-On Current Versus Power Supply

OP000871

Access Time Change Versus Input Voltage
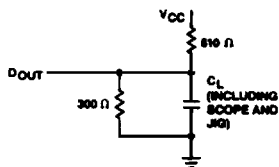

OP000801

Access Time Change Versus Output Loading

OP000881

SWITCHING TEST CIRCUIT

TC000031

A. Output Load

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (See Notes 4-12)

| No.	Parameter Symbol	Parameter Description		Am21L41-12 Min.	Am21L41-12 Max.	Am21L41-15 Min.	Am21L41-15 Max.	Am21L41-20 Min.	Am21L41-20 Max.	Am21L41-25 Min.	Am21L41-25 Max.	Units
Read Cycle												
1	t_{RC}	Address Valid to Address Do Not Care Time (Read Cycle Time)		120		150		200		250		ns
2	t_{AA}	Address Valid to Data Out Valid Delay (Address Access Time)			120		150		200		250	ns
3	t_{ASC1}	Chip Select LOW to Data Out Valid	(Note 7)		120		150		200		250	ns
4	t_{ASC2}		(Note 8)		130		160		200		250	ns
5	t_{LZ}	Chip Select LOW to Data Out On (Note 9, 13)		10		10		10		10		ns
6	t_{HZ}	Chip Select HIGH to Data Out Off (Note 9, 13)		0	60	0	60	0	60	0	60	ns
7	t_{OH}	Output hold after address change		10		10		10		10		ns
8	t_{PD}	Chip Select HIGH to Power LOW Delay (Note 13)			60		60		60		60	ns
9	t_{PU}	Chip Select LOW to Power HIGH Delay (Note 13)		0		0		0		0		ns
Write Cycle												
10	t_{WC}	Address Valid to Address Do Not Care Time (Write Cycle Time)		120		150		200		250		ns
11	t_{WP}	Write Enable LOW to Write Enable HIGH Time (Note 5)		60		60		60		75		ns
12	t_{WR}	Write Enable HIGH to Address Do Not Care Time		10		15		20		20		ns
13	t_{WZ}	Write Enable LOW to Data Out Off Delay (Notes 9, 13)		0	70	0	80	0	80	0	80	ns
14	t_{DW}	Data in Valid to Write Enable HIGH Time		50		60		60		75		ns
15	t_{DH}	Write Enable HIGH to Data In Do Not Care Time		10		10		10		10		ns
16	t_{AS}	Address Valid to Write Enable LOW Time		0		0		0		0		ns
17	t_{CW}	Chip Select LOW to Write Enable HIGH Time (Note 5)		110		135		180		230		ns
18	t_{OW}	Write Enable HIGH to Output Turn On (Notes 9, 13)		0		0		0		0		ns
19	t_{AW}	Address Valid to End of Write		110		135		180		230		ns

Notes: See notes following DC Characteristics table.

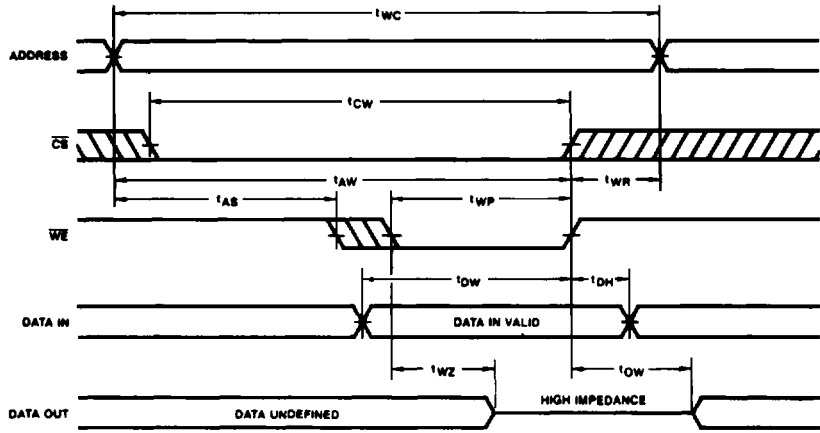## SWITCHING WAVEFORMS (Cont'd.)
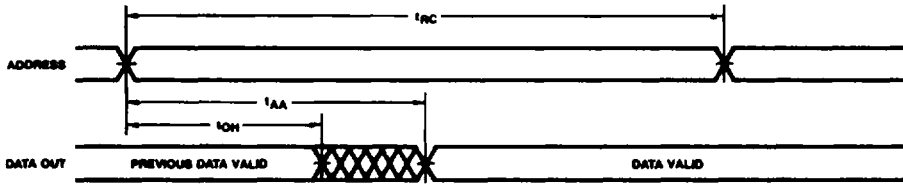
WF000231

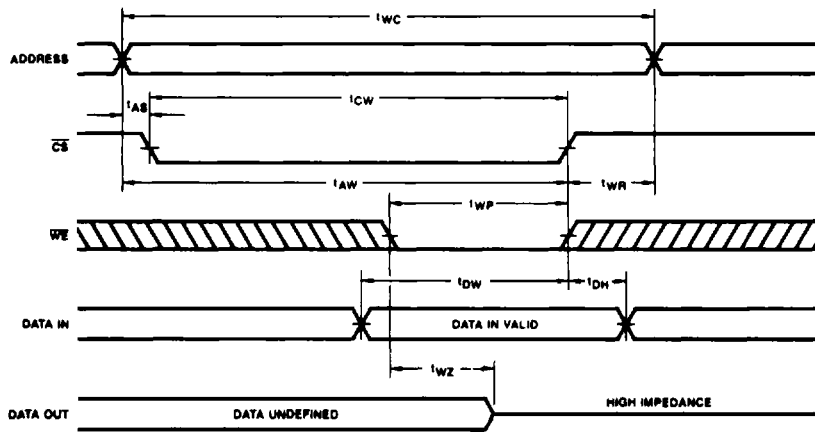**Read Cycle No. 1 (Notes 10 & 11)**
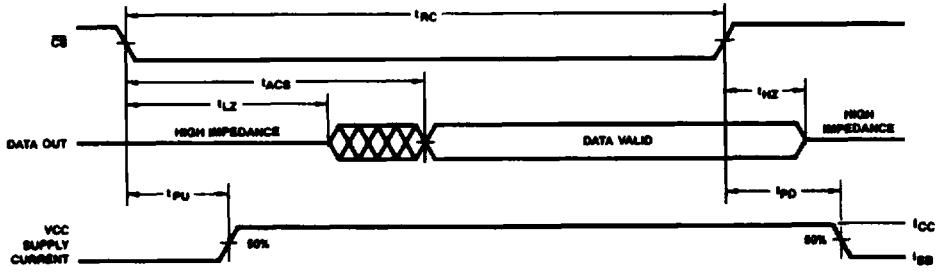
WF000241

Read Cycle No. 2 (Notes 10 & 12)

SWITCHING WAVEFORMS

WF000211

Write Cycle No. 1 ($\overline{WE}$ Controlled)

WF000221

Write Cycle No. 2 ($\overline{CS}$ Controlled)

Note: If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.