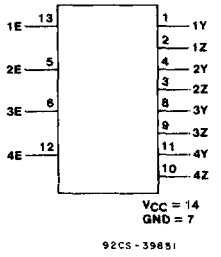
CD54/74HC4016
CD54/74HCT4016

File Number **1917**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Quad Bilateral Switch

Type Features:
- *Wide analog-input-voltage range: 0-10 V*
- *Low "ON" resistance: 45 Ω typ. @ V_{CC}=4.5 V*
  35 Ω typ. @ V_{CC}=6 V
  30 Ω typ. @ V_{CC}=9 V
- *Fast switching and propagation delay times*
- *Low "OFF" leakage current*
- *Built-in "Break-before-make" switching*
- *Suitable for Sample and Hold applications*

The RCA CD54/74HC/HCT4016 contains four independent digitally controlled analog switches that use silicon-gate CMOS technology to achieve operating speeds similar to LSTTL with the low power consumption of standard CMOS integrated circuits.

Each switch has two input/output terminals (nY,nZ) and an active high enable input (nE). Current through the switch will not cause additional V_{CC} current provided the analog voltage is maintained between V_{CC} and Gnd.

The CD54HC4016 and CD54HCT4016 are supplied in 14-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC4016 and CD74HCT4016 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:
- *Wide operating temperature range:*
  CD74HC/HCT: -40 to +125°C
- *CD54HC/CD74HC types:*
  2 V to 10 V operation
  High noise immunity:
  N_{IL} = 30%, N_{IH} = 30% of V_{CC} @ V_{CC} = 5 V
- *CD54HCT/CD74HCT types:*
  Direct LSTTL input logic compatibility
  V_{IL} = 0.8 V max., V_{IH} = 2 V min.
  CMOS input compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}
- *Alternate Source is Philips/Signetics*

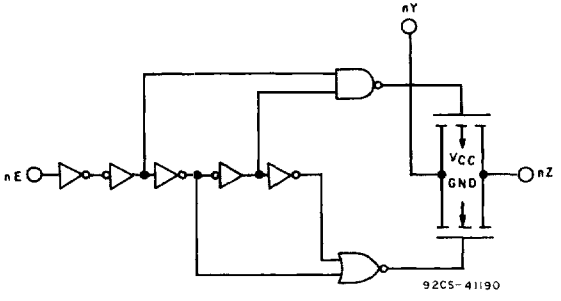


Fig. 1 - Logic diagram.

TRUTH TABLE

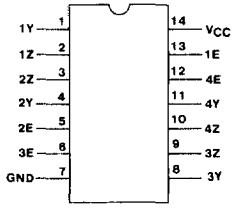
INPUT nE	SWITCH
L	OFF
H	ON

H = High Level Voltage
L = Low Level Voltage

CD54/74HC4016
CD54/74HCT4016

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}):
(Voltages referenced to ground)
HCT Types ..... -0.5 to +7 V
HC Types ..... -0.5 to +10.5 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5 V) ..... ±20 mA
DC SWITCH DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC}$ +0.5 V) ..... ±20 mA
DC SWITCH CURRENT, I_O (FOR $V_I > -0.5$ V OR $V_I < V_{CC}$ +0.5 V) ..... +25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) ..... ±50 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... -55 to +125°C
PACKAGE TYPE E, M ..... -40 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300°C



TERMINAL ASSIGNMENT

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	10	V
CD54/74HCT Types	4.5	5.5	
DC Input Voltage, V_C, and Analog Switch Voltage, $V_{I/O}$	0	V_{CC}	V
Operating Temperature, T_A:			
CD74 Types	-40	+125	°C
CD54 Types	-55	+125	
Input Rise and Fall Times, t_r,t_f (Control Inputs)			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	
at 9 V	0	250	

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC4016
CD54/74HCT4016

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS			74HC/54HC			74HC		54HC -55/ +125°C		TEST CONDITIONS			74HCT/54HCT			74HCT		54HCT -55/ +125°C		UNITS
	LOGIC V_I	SWITCH V_{IS}	V_{CC}	+25°C			-40/ +85°C		74HC -40/ +125°C		LOGIC V_I	SWITCH V_{IS}	V_{CC}	+25°C			-40/ +85°C		74HCT -40/ +125°C		
	V	V	V	Min	Typ	Max	Min	Max	Min	Max	V	V	V	Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—											
			6	4.2	—	—	4.2	—	4.2	—											
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	
			4.5	—	—	1.35	—	1.35	—	1.35											
			6	—	—	1.8	—	1.8	—	1.8											
"On" Resistance R_{on} I_O = 1 mA	V_{IL} or V_{IH}	V_{CC} or Gnd	4.5	—	45	180	—	225	—	270	V_{IL} or V_{IH}	V_{CC} or Gnd	4.5	—	45	180	—	225	—	270	Ω
			6	—	35	160	—	200	—	240				—	—	—	—	—	—	—	
			9	—	30	135	—	170	—	205				—	—	—	—	—	—	—	
	V_{IL} or V_{IH}	V_{CC} to Gnd	4.5	—	85	320	—	400	—	480	V_{IL} or V_{IH}	V_{CC} to Gnd	4.5	—	85	320	—	400	—	480	
			6	—	55	240	—	300	—	360				—	—	—	—	—	—	—	
			9	—	35	170	—	215	—	255				—	—	—	—	—	—	—	
Maximum "On" Resistance between any two switches ΔR_{on}	V_{IL} or V_{IH}	V_{CC} to Gnd	4.5	—	10	—	—	—	—	—	V_{IL} or V_{IH}	V_{CC} to Gnd	4.5	—	10	—	—	—	—	—	
			6	—	8.5	—	—	—	—	—				—	—	—	—	—	—	—	
Switch Off Leakage Current I_{IZ}	En=Gnd	V_{CC} or Gnd	6	—	—	±0.1	—	±1	—	±1	En=Gnd	V_{CC} or Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
			10	—	—	±0.1	—	±1	—	±1				—	—	—	—	—	—	—	
Logic Input Leakage Current I_I	V_{CC} or Gnd	—	6	—	—	±0.1	—	±1	—	±1	**	—	5.5	—	—	±0.1	—	±1	—	±1	
Quiescent Device Current I_{CC} I_O = 0 mA	V_{CC} or Gnd	V_{CC} or Gnd	6	—	—	2	—	20	—	40	V_{CC} or Gnd	—	5.5	—	—	2	—	20	—	40	
			10	—	—	16	—	160	—	320											
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*		—	—	—	—	—	—	—	—	—	V_{CC}-2.1	—	4.5 to 5.5	—	100	360	—	450	—	490	

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

**Any voltage between V_{CC} and Gnd.

HCT Input Loading Table

Input	Unit Loads*
E	1

*Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC4016
CD54/74HCT4016

SWITCHING CHARACTERISTICS (V_{CC}=5 V, T_A=25° C, Input t_r,t_f=6 ns)

CHARACTERISTIC		C_L (pF)	TYPICAL VALUES		UNITS
			HC	HCT	
Propagation Delay Time:					
Switch In to Switch Out	t_{PLH}, t_{PHL}	15	4	4	ns
Switch Turn Off E to Out	t_{PLZ}, t_{PHZ}		12	14	
Switch Turn On	t_{PZH}		16	14	
$\overline{E}$ to Out	t_{PZL}		16	22	
Power Dissipation Capacitance*	C_{PD}	—	12	12	pF

*C_{PD} is used to determine the dynamic power consumption, per package.

$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L + C_S) V_{CC}^2 f_o$ where

f_i = input frequency

f_o = output frequency

C_L = output load capacitance

C_S = switch capacitance

V_{CC} = supply voltage.

SWITCHING CHARACTERISTICS (C_L=50 pF, Input t_r,t_f=6 ns)

CHARACTERISTIC		V_{CC}	LIMITS												UNITS
			25° C				-40° C to +85° C				-55° C to +125° C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay Time Switch In to Out	t_{PLH}	2	—	60	—	—	—	75	—	—	—	90	—	—	ns
	t_{PHL}	4.5	—	12	—	12	—	15	—	15	—	18	—	18	
		6	—	10	—	—	—	13	—	—	—	15	—	—	
		9	—	8	—	—	—	10	—	—	—	12	—	—	
Switch Turn-On En to Out		2	—	190	—	—	—	240	—	—	—	285	—	—	
	t_{PZH}	4.5	—	38	—	35	—	48	—	44	—	57	—	53	
		6	—	32	—	—	—	41	—	—	—	48	—	—	
		9	—	28	—	—	—	35	—	—	—	42	—	—	
		2	—	190	—	—	—	240	—	—	—	285	—	—	
	t_{PZL}	4.5	—	38	—	52	—	48	—	65	—	57	—	73	
		6	—	32	—	—	—	41	—	—	—	48	—	—	
		9	—	28	—	—	—	35	—	—	—	42	—	—	
Switch Turn-Off En to Out		2	—	145	—	—	—	180	—	—	—	220	—	—	
	t_{PHZ}	4.5	—	29	—	35	—	36	—	44	—	44	—	53	
	t_{PLZ}	6	—	25	—	—	—	31	—	—	—	38	—	—	
		9	—	22	—	—	—	28	—	—	—	33	—	—	
Input (Control) Capacitance	C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	pF

CD54/74HC4016
CD54/74HCT4016

ANALOG CHANNEL CHARACTERISTICS - Typical Values at T_A = 25° C

CHARACTERISTIC	TEST CONDITIONS	V_{CC} V	HC	HCT	UNITS
Switch Frequency Response Bandwidth at -3 dB (Fig. 13)	Fig. 4 Notes 1 and 2	4.5	>200	>200	MHz
Crosstalk Between Any Two Switches (Fig. 14)	Fig. 5 Notes 2 and 3	4.5	TBE	TBE	dB
Total Harmonic Distortion	1 kHz, V_{IS}=4 V_{p-p} Fig. 6	4/5	0.078	0.078	%
	V_{IS}=8 V_{p-p}	9	0.018	0.018	
Control to Switch Feedthrough Noise	Fig. 7	4.5	TBE	TBE	mV
		9	TBE	TBE	
Switch "OFF" Signal Feedthrough (Fig. 14)	Fig. 8 Notes 2 and 3	4.5	-62	-62	dB
Switch Input Capacitance C_S	—	—	5	5	pF

Notes:

1. Adjust input level for 0 dBm at output, f = 1 MHz.
2. V_{IS} is centered at $V_{CC}/2$.
3. Adjust input for 0 dBm at V_{IS}.

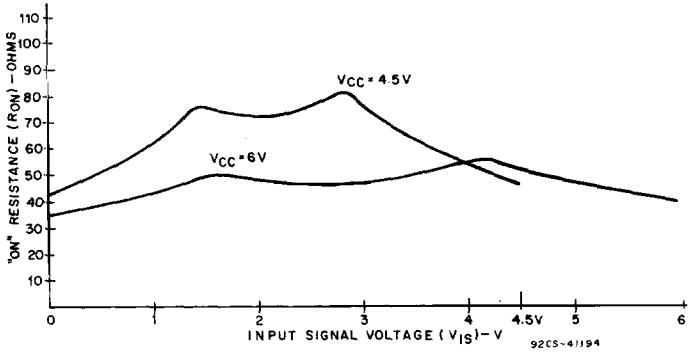


Fig. 2 - Typical "ON" resistance vs. input signal voltage.

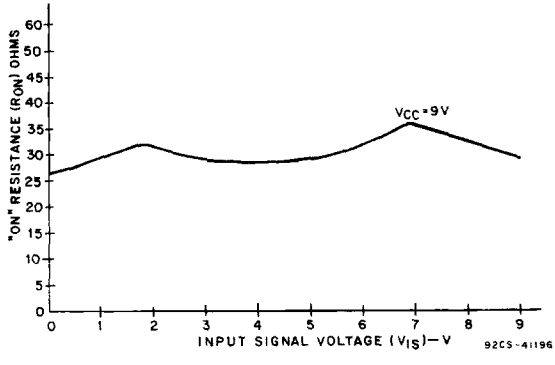


Fig. 3 - Typical "ON" resistance vs. input signal voltage.

CD54/74HC4016
CD54/74HCT4016

ANALOG TEST CIRCUITS

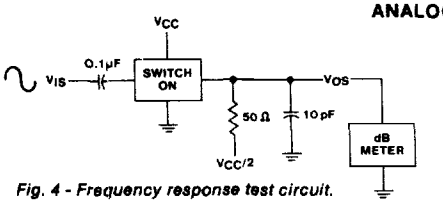


Fig. 4 - Frequency response test circuit.

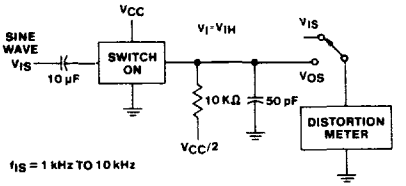


Fig. 6 - Total harmonic distortion test circuit.

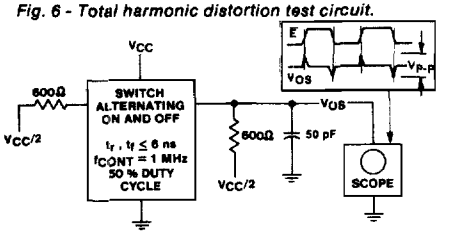


Fig. 7 - Control-to-switch feedthrough noise test circuit.

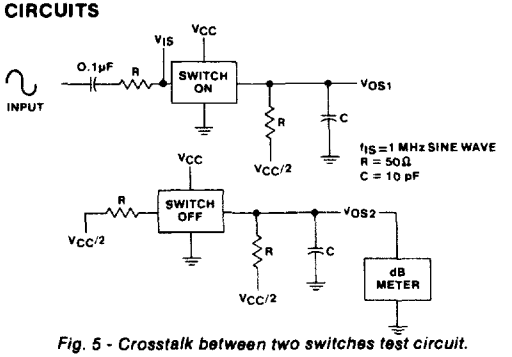


Fig. 5 - Crosstalk between two switches test circuit.

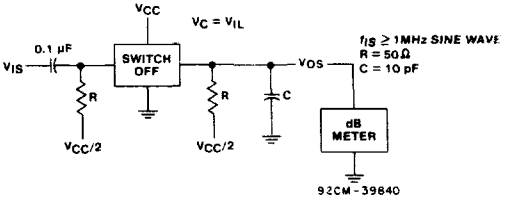


Fig. 8 - Switch off signal feedthrough.

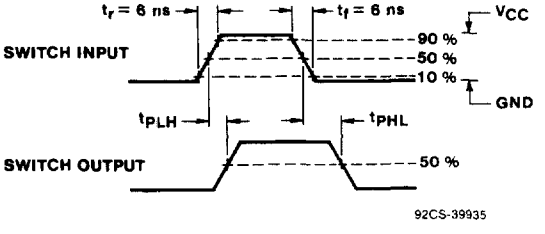


Fig. 9 - Switch propagation - delay times waveforms.

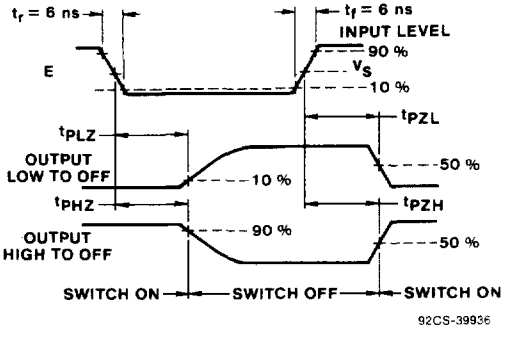


Fig. 10 - Switch turn-on and turn-off propagation delay times waveforms.

	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

CD54/74HC4016
CD54/74HCT4016

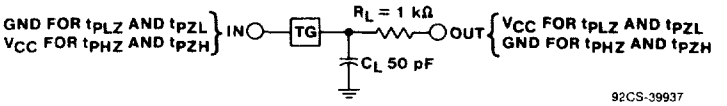


Fig. 11 - Switch on/off propagation delay time test circuit.

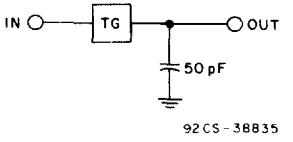


Fig. 12 - Switch-in to switch-out propagation delay time test circuit.

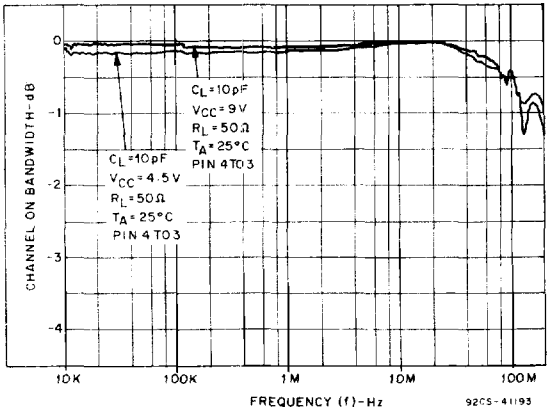


Fig. 13 - Switch frequency response.

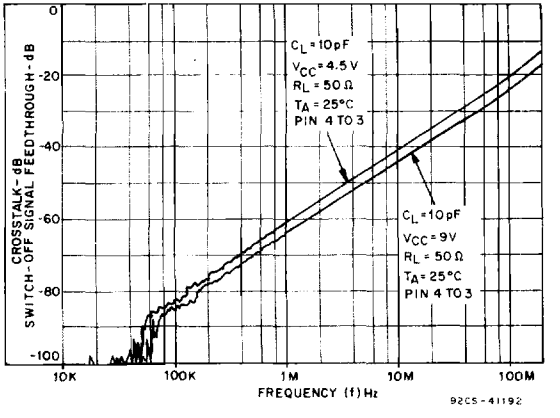


Fig. 14 - Switch-off signal feedthrough and crosstalk vs. frequency.