CYPRESS SEMICONDUCTOR

16 x 16 Multipliers

Features

- **Fast**
  - **— 38-ns clock cycle (commercial)**
  - **— 42-ns clock cycle (military)**
- **Low power**
  - **— I_{CC} (max. at 10 MHz) = 100 mA (commercial)**
  - **— I_{CC} (max. at 10 MHz) = 110 mA (military)**
- **V_{CC} margin of 5V ±10%**
  - **— All parameters guaranteed over commercial and military operating temperature range**
- **16 x 16 bit parallel multiplication with full precision 32-bit product output**
- **Two's complement, unsigned magnitude, or mixed-mode multiplication**
- **CY7C516 is pin compatible and functionally equivalent to Am29516, MPY016K, MPY016H**
- **CY7C517 is pin compatible and functionally equivalent to Am29517**

Functional Description

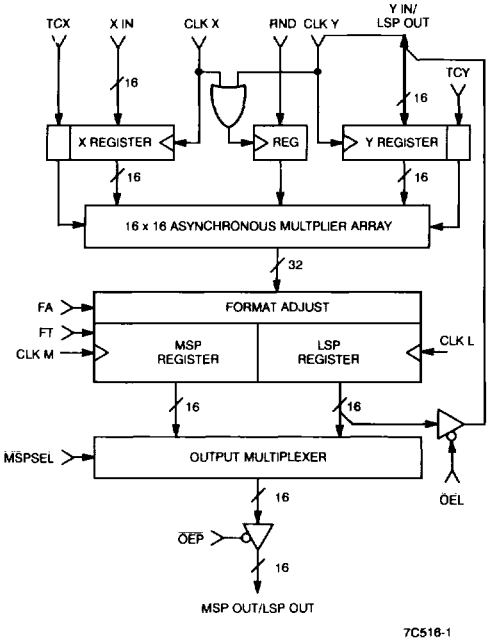
The CY7C516/517 are high-speed 16 x 16 parallel multipliers that operate at 38-ns clocked multiply times (26-MHz multiplication rate). The two input operands may be independently specified as either two's complement or unsigned magnitude numbers. Controls are provided for rounding and format adjustment of the full-precision 32-bit product.

On the 7C516, individually clocked input and output registers are provided to maximize throughput and to simplify bus interfacing. On the 7C517, a single clock (CLK) is provided, along with three register enables. This facilitates the use of the 7C517 in microprogrammed systems. The input and output registers are positive-edge-triggered D-type flip-flops. The output register may be made transparent for asynchronous output.

6 LOGIC

Logic Block Diagram

CY7C516



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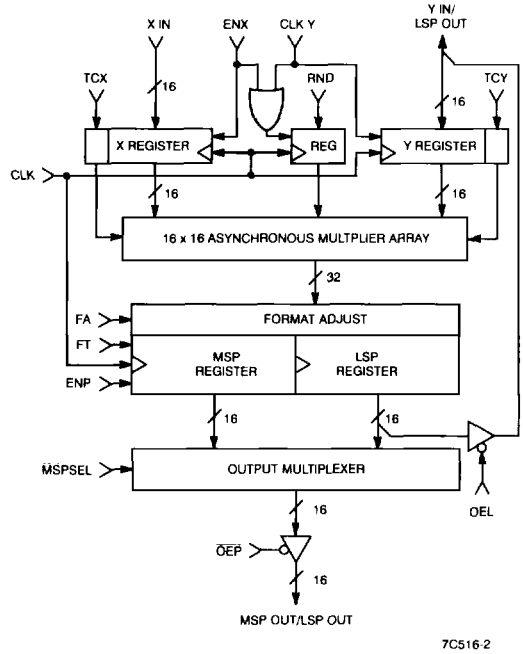
CY7C517



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Selection Guide

		7C516–38[1] 7C517–38	7C516–42 7C517–42	7C516–45 7C517–45	7C516–55 7C517–55	7C516–75 7C517–75
Maximum Multiply Time Clocked/Unclocked(ns)	Commercial	38/58		45/65	55/75	75/100
	Military		42/65		55/75	75/100

Notes:
1. 38-ns version available in cerDIP, LCC, PLCC, and PGA packages only.

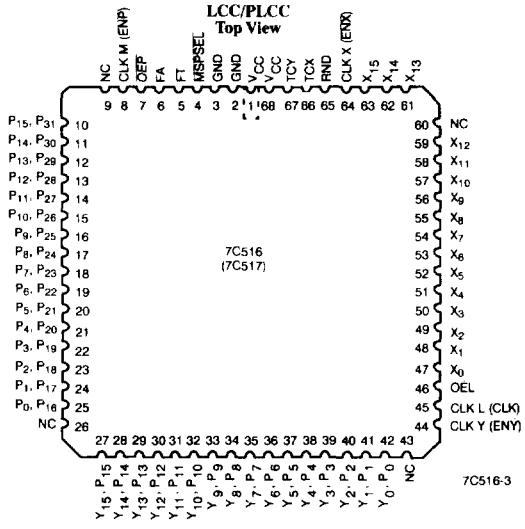
Functional Description (continued)

Two output modes may be selected by using the output multiplexer control, $\overline{\text{MSPSEL}}$. Holding $\overline{\text{MSPSEL}}$ LOW causes the most significant product (MSP) to be available at the dedicated output port. The LSP is simultaneously available at the bidirectional port shared with the Y inputs.

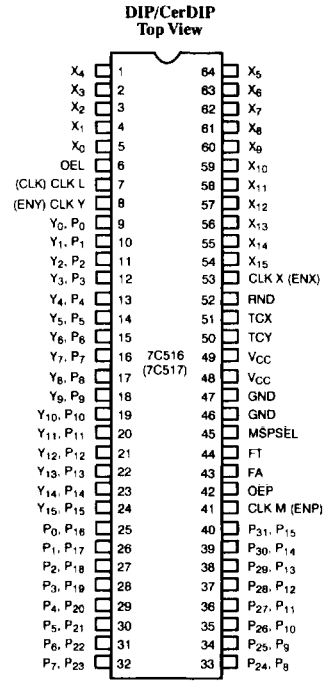
The other mode of output involves toggling the $\overline{\text{MSPSEL}}$ control, to allow both the MSP and LSP to be available for output through the dedicated 16-bit output port.

Pin Configurations

LCC/PLCC
Top View



DIP/CerDIP
Top View



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PGA
Top View

	51 NC	50 X_{13}	48 X_{15}	46 RND	44 TCY	42 V_{CC}	40 GND	38 FT	36 OEP	
53 X_{11}	52 X_{12}	49 X_{14}	47 CLK X (ENX)	45 TCX	43 V_{CC}	41 GND	39 MSPSEL	37 FA	35 CLK M (ENP)	34 NC
55 X_9	54 X_{10}								32 P_{30}, P_{14}	33 P_{31}, P_{15}
57 X_7	56 X_8								30 P_{28}, P_{12}	31 P_{29}, P_{13}
59 X_5	58 X_6								28 P_{26}, P_{10}	29 P_{27}, P_{11}
61 X_3	60 X_4								26 P_{24}, P_8	27 P_{25}, P_9
63 X_1	62 X_2								24 P_{22}, P_6	25 P_{23}, P_7
65 $\overline{OEL}$	64 X_0								22 P_{20}, P_4	23 P_{21}, P_5
67 CLK Y (ENY)	66 CLK L (CLK)								20 P_{18}, P_2	21 P_{19}, P_3
68 NC	17 Y_0, P_0	19 Y_2, P_2	21 Y_4, P_4	23 Y_6, P_6	25 Y_8, P_8	27 Y_{10}, P_{10}	29 Y_{12}, P_{12}	31 Y_{14}, P_{14}	18 P_{16}, P_0	19 P_{17}, P_1
■	18 Y_1, P_1	20 Y_3, P_3	22 Y_5, P_5	24 Y_7, P_7	26 Y_9, P_9	28 Y_{11}, P_{11}	30 Y_{13}, P_{13}	32 Y_{15}, P_{15}	17 NC	

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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Ambient Temperature Under Bias ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Voltage Applied to Outputs ..... −0.5V to V_{CC} Max.

Output Current into Outputs (LOW) ..... 10 mA

Static Discharge Voltage ..... >1000V
(Per MIL-STD-883 Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[2]	−55°C to +125°C	5V ±10%

Note:
2. T_A is the "instant on" case temperature.

Pin Definitions

Signal Name	I/O	Description
$X_{15} - X_0$	I	X-Input Data. This 16-bit number may be interpreted as two's complement or unsigned magnitude.
$Y_{15} - Y_0$ ($P_{15} - P_0$)	I O	Y-Input/LSP Output Data. This 16-bit number may be interpreted as two's complement or unsigned magnitude.
$P_{31} - P_{16}$ ($P_{15} - P_0$)	O	MSP-Out/LSP-Out. This 16-bit port may carry either the MSP ($P_{31} - P_{16}$) or the LSP ($P_{15} - P_0$).
FT	I	The MSP and LSP registers are made transparent (asynchronous operation) if FT is HIGH.
FA	I	Format Adjust Control. If FA is HIGH, a full 32-bit product is output. If FA is LOW, a left-shifted product is output, with the sign bit replicated in the LSP. FA must be HIGH for two's complement integer, unsigned magnitude, and mixed-mode multiplication.
$\overline{MSPSEL}$	I	Output Multiplexer Control. When $\overline{MSPSEL}$ is LOW, the MSP is available for output at the MSP output port, and the LSP is available at the Y input/LSP output port. When $\overline{MSPSEL}$ is HIGH, the LSP is available at both ports (above) and the MSP is not available.
RND	I	Round Control. When RND is HIGH, a one is added to the MSB of the LSP. This position is dependent on the FA control; FA = HIGH means RND adds to the 2^{-15} bit (P_{15}), FA = LOW means RND adds to the 2^{-16} bit (P_{14}).
TCX	I	Two's Complement Control X. X-input data are interpreted as two's complement when TCX is HIGH. TCX LOW means the data are interpreted as unsigned magnitude.
TCY	I	Two's Complement Control Y. Y-input data are interpreted as two's complement when TCY is HIGH. TCY LOW means the data are interpreted as unsigned magnitude.
$\overline{OEP}$	I	MSP-Out/LSP-Out Three-State Control. When $\overline{OEP}$ is LOW, the output port is enabled; when $\overline{OEP}$ is HIGH, drivers are in a high-impedance state.
$\overline{OEL}$	I	Y-In/LSP Out Three-State Control. When $\overline{OEL}$ is LOW, the timeshared port is enabled for LSP output. When $\overline{OEL}$ is HIGH, the output drivers are in a high-impedance state. This is required for Y input.
CY7C516 Only		
CLK X	I	X-Register Clock. X-input data and TCX are latched in at the rising edge of CLK X.
CLK Y	I	Y-Register Clock. Y-input data and TCY are latched in at the rising edge of CLK Y.
CLK M	I	MSP Register Clock. The most significant product (MSP) is latched in at the MSP Register at the rising edge of CLK M.
CLK L	I	LSP Register Clock. The least significant product (LSP) is latched in at the LSP Register at the rising edge of CLK L.
CY7C517 Only		
CLK	I	Clock. All enabled registers latch in their data at the rising edge of CLK.
$\overline{ENX}$	I	X-Register Enable. When $\overline{ENX}$ is LOW, the X register is enabled. X-input data and TCX will be latched in at the rising edge of CLK when the register is enabled. When $\overline{ENX}$ is HIGH, the X register is in hold mode.
$\overline{ENY}$	I	Y-Register Enable. $\overline{ENY}$ enables the Y register (see $\overline{ENX}$).
$\overline{ENP}$	I	Product Register Enable. $\overline{ENP}$ enables the product register. Both the MSP and LSP sections are enabled by $\overline{ENP}$ (see $\overline{ENX}$).

Input Formats (All Devices)

Fractional Two's Complement Input Format

TCX, TCY = 1

X_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}
(Sign)															

Y_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}
(Sign)															

Input Formats (All Devices) (continued)

Integer Two's Complement Input Format

TCX, TCY = 1

	X_{IN}																Y_{IN}															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-2^{15} (Sign)	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	-2^{15} (Sign)	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Unsigned Fractional Input Format

TCX, TCY = 0

	X_{IN}																Y_{IN}															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}

Unsigned Integer Input Format

TCX, TCY = 0

	X_{IN}																Y_{IN}															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Output Formats (All Devices)

Fractional Two's Complement (Shifted) Output[3]

FA = 0

	MSP																LSP															
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-2^{0} (Sign)	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	-2^{0} (Sign)	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}

Fractional Two's Complement Output

FA = 1

	MSP																LSP															
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-2^{1} (Sign)	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}

Integer Two's Complement Output

FA = 1

	MSP																LSP															
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-2^{31} (Sign)	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Unsigned Fractional Output

FA = 1

	MSP																LSP															
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}	2^{-31}	2^{-32}

Unsigned Integer Output

FA = 1

	MSP																LSP															
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Note:
3. In this format an overflow occurs in the attempted multiplication of the two's complement number 1.000... (−1) with itself, yielding a product of 1.000... or −1.

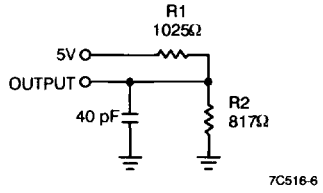
Electrical Characteristics Over Operating Range[4]

Parameters	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 0.4 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.0		V
V_{IL}	Input LOW Voltage				0.8	V
I_{OH}	Output HIGH Current	V_{CC} = Min., V_{OH} = 2.4V		− 0.4		mA
I_{OL}	Output LOW Current	V_{CC} = Min., V_{OL} = 0.4V		4.0		mA
I_{IX}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{CC}$, V_{CC} = Max.		− 10	+10	μA
I_{OS}[5]	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0V		− 3	− 30	mA
I_{OZL}	Output OFF (Hi-Z) Current	V_{CC} = Max., $\overline{OE}$ = 2.0V			− 25	μA
I_{OZH}	Output OFF (Hi-Z) Current	V_{CC} = Max., $\overline{OE}$ = 2.0V		25		μA
$I_{CC}(Q_1)$[6]	Supply Current (Quiescent)	GND ≤ V_{IN} ≤ V_{IL} or V_{IH} ≤ V_{IN} ≤ V_{CC}; $\overline{OE}$ = HIGH	Commercial (−38)		40	mA
			Military (−42)		45	
			All Others		30	
$I_{CC}(Q_2)$[6]	Supply Current (Quiescent)	GND ≤ V_{IN} ≤ 0.4V or 3.85V ≤ V_{IN} ≤ V_{CC}; $\overline{OE}$ = HIGH	Commercial		20	mA
			Military		25	
I_{CC}(Max.)[6]	Supply Current	V_{CC} = Max., f_{CLK} = 10 MHz; $\overline{OE}$ = HIGH	Commercial		100	mA
			Military		110	

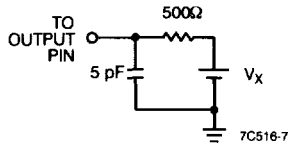
Capacitance[7]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		10	pF

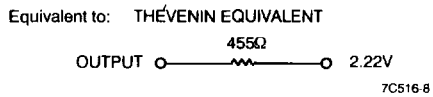
Output Loads Used for AC Performance Characteristics



Normal Load (Load 1)



Three-State Delay Load (Load 2)



Notes:

4. See the last page of this specification for Group A subgroup testing information.
5. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
6. Two quiescent figures are given for different input voltage ranges. To calculate I_{CC} at any given clock frequency, use 30 mA + I_{CC}(AC) where I_{CC}(AC) = (7 mA/MHz) × Clock Frequency for the commercial temperature range. I_{CC}(AC) = (8 mA/MHz) × Clock Frequency for military temperature range.
7. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics Over Operating Range[2]

Parameters	Description		Test Conditions	7C516–38[1] 7C517–38		7C516–42 7C517–42		7C516–45 7C517–45		Units
				Min.	Max.	Min.	Max.	Min.	Max.	
t_{MUC}	Unclocked Multiply Time		Load 1		58		65		65	ns
t_{MC}	Clocked Multiply Time				38		42		45	ns
t_S	X_i, Y_i, RND, TCX, TCY Set-Up Time			7		8		20		ns
t_H	X_i, Y_i, RND, TCX, TCY Hold Time			3		3		3		ns
t_{SE}	$\overline{ENX}$, $\overline{ENY}$, $\overline{ENP}$ Set-Up Time (7C517 Only)			10		15		20		ns
t_{HE}	$\overline{ENX}$, $\overline{ENY}$, $\overline{ENP}$ Hold Time (7C517 Only)			3		3		3		ns
t_{PWH}, t_{PWL}	Clock Pulse Width (HIGH and LOW)			10		10		20		ns
t_{PDSEL}	$\overline{MSPSEL}$ to Product Out				18		21		25	ns
t_{PDP}	Output Clock to P				25		30		30	ns
t_{PDY}	Output Clock to Y				25		30		30	ns
t_{PHZ}	$\overline{OEP}$ Disable Time	HIGH to Z	Load 2		15		17		25	ns
t_{PLZ}		LOW to Z			15		17		25	ns
t_{PZH}	$\overline{OEP}$ Enable Time	Z to HIGH			23		25		30	ns
t_{PZL}		Z to LOW			23		25		30	ns
t_{LHZ}	$\overline{OEL}$ Disable Time	HIGH to Z			15		17		25	ns
t_{LLZ}		LOW to Z			15		17		25	ns
t_{LZH}	$\overline{OEL}$ Enable Time	Z to HIGH			23		25		30	ns
t_{LZL}		Z to LOW			23		25		30	ns
t_{HCL}	Clock LOW Hold Time CLK XY Relative to CLK ML[8]		Load 1	0		0		0		ns

Parameters	Description		Test Conditions	7C516–55 7C517–55		7C516–75 7C517–75		Units
				Min.	Max.	Min.	Max.	
t_{MUC}	Unclocked Multiply Time		Load 1		75		100	ns
t_{MC}	Clocked Multiply Time				55		75	ns
t_S	X_i, Y_i, RND, TCX, TCY Set-Up Time			20		25		ns
t_H	X_i, Y_i, RND, TCX, TCY Hold Time			3		3		ns
t_{SE}	$\overline{ENX}$, $\overline{ENY}$, $\overline{ENP}$ Set-Up Time (7C517 Only)			20		25		ns
t_{HE}	$\overline{ENX}$, $\overline{ENY}$, $\overline{ENP}$ Hold Time (7C517 Only)			3		3		ns
t_{PWH}, t_{PWL}	Clock Pulse Width (HIGH and LOW)			25		30		ns
t_{PDSEL}	$\overline{MSPSEL}$ to Product Out				25		30	ns
t_{PDP}	Output Clock to P				30		35	ns
t_{PDY}	Output Clock to Y				30		35	ns
t_{PHZ}	$\overline{OEP}$ Disable Time	HIGH to Z	Load 2		25		30	ns
t_{PLZ}		LOW to Z			25		30	ns
t_{PZH}	$\overline{OEP}$ Enable Time	Z to HIGH			30		35	ns
t_{PZL}		Z to LOW			30		35	ns
t_{LHZ}	$\overline{OEL}$ Disable Time	HIGH to Z			25		30	ns
t_{LLZ}		LOW to Z			25		30	ns
t_{LZH}	$\overline{OEL}$ Enable Time	Z to HIGH			30		35	ns
t_{LZL}		Z to LOW			30		35	ns
t_{HCL}	Clock LOW Hold Time CLK XY Relative to CLK ML[8]		Load 1	0		0		ns

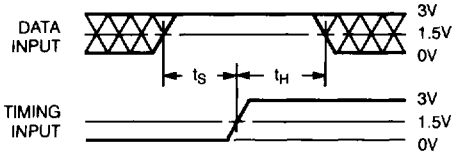
Note:
8. To ensure that the correct product is entered in the output registers, new data may not be entered into the input registers before the output registers have been clocked.

Test Waveforms

Parameter	V_X	Output Waveform—Measurement Level
All t_{PD}s	V_{CC}	V_{OH}, V_{OL}, 1.5V
t_{PHZ}, t_{LHZ}	0.0V	V_{OH}, 0.5V, 0.0V
t_{PLZ}, t_{LLZ}	2.6V	V_{OL}, 0.5V, 2.6V
t_{PZH}, t_{LZH}	0.0V	0.0V, 1.5V, V_{OH}
t_{PZL}, t_{LZL}	2.6V	2.6V, 1.5V, V_{OL}

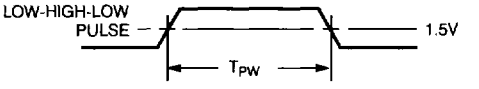
7C516-9

Set-Up and Hold Time[9]



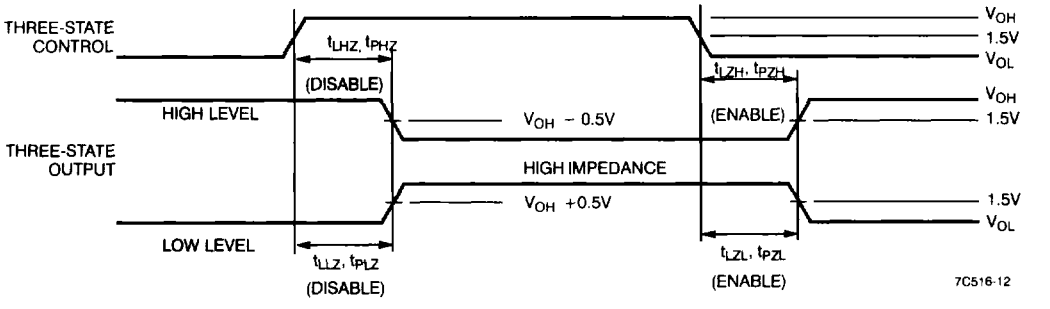
7C516-10

Pulse Width[10]



7C516-11

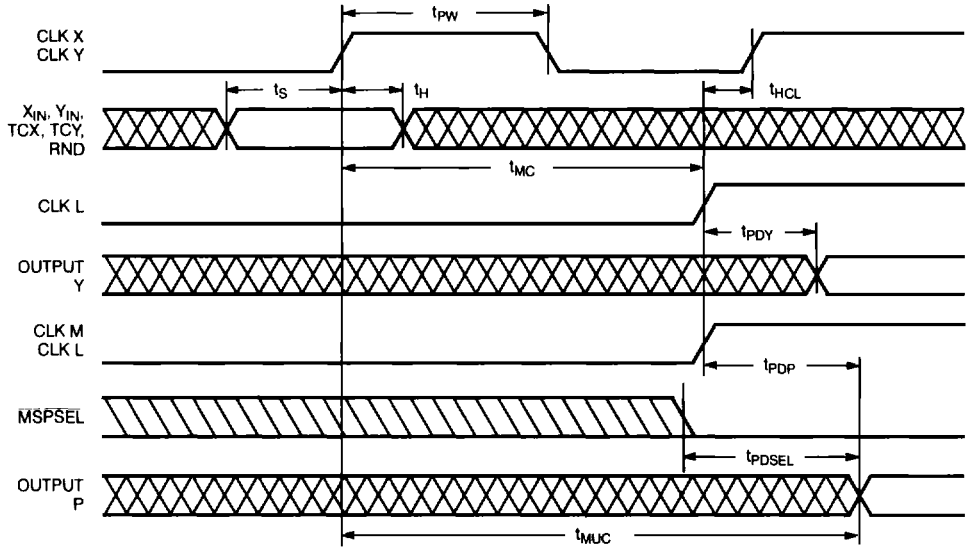
Three-State Timing Diagram



7C516-12

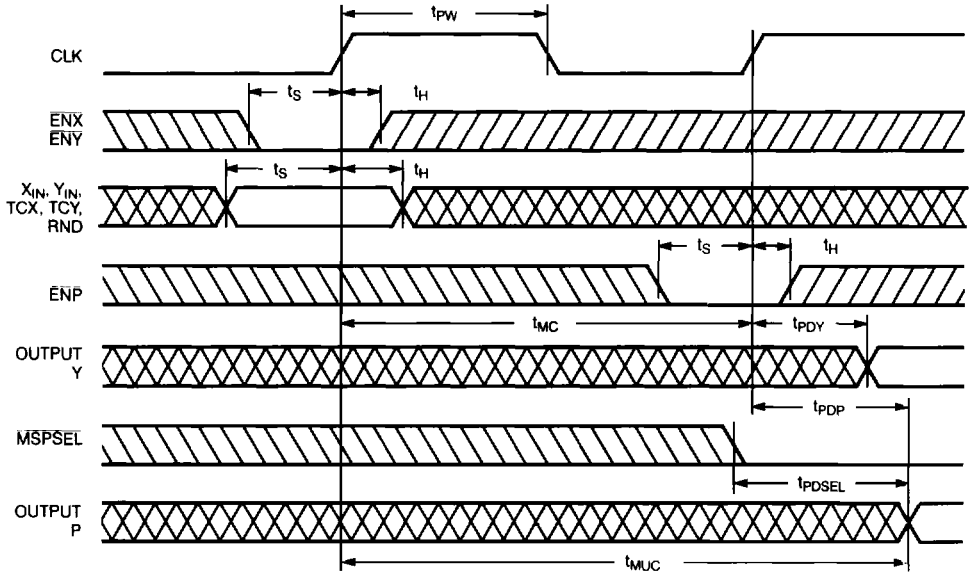
Notes:
9. Cross-hatched area is don't care condition.
10. Diagram shown for HIGH data only. Output transition may be opposite sense.

Timing Diagram 7C516



7C516-13

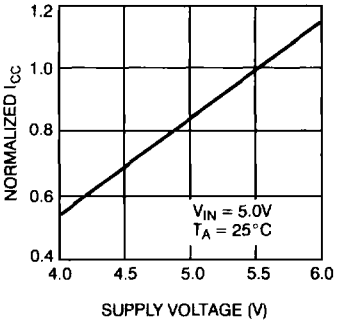
Timing Diagram 7C517



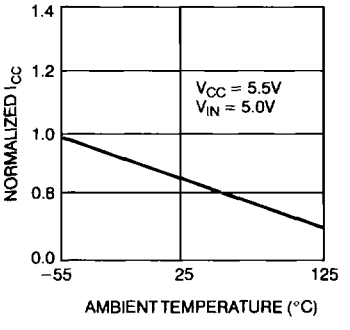
7C516-14

Typical DC and AC Characteristics

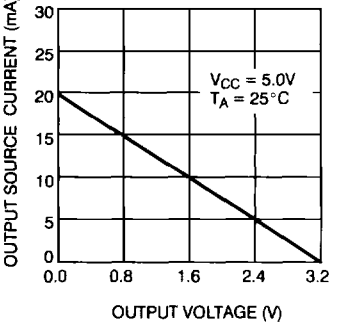
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



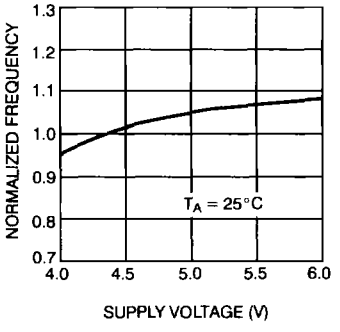
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



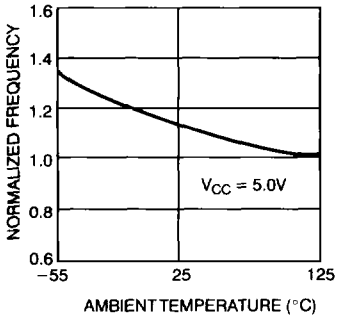
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



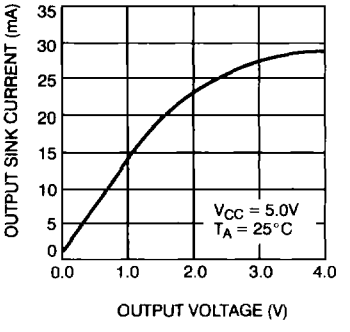
NORMALIZED FREQUENCY vs. SUPPLY VOLTAGE



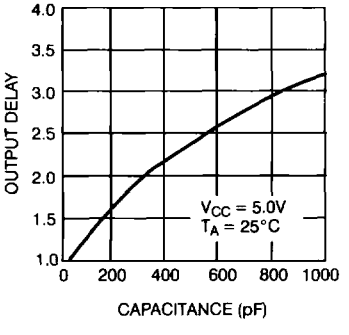
NORMALIZED FREQUENCY vs. AMBIENT TEMPERATURE



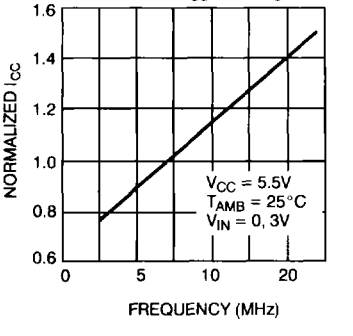
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



NORMALIZED CURRENT DELAY vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. FREQUENCY



7C516-15

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
38	CY7C516-38DC	D30	
	CY7C516-38GC	G68	
	CY7C516-38JC	J81	
	CY7C516-38LC	L81	
42	CY7C516-42DMB	D30	Military
	CY7C516-42GMB	G68	
	CY7C516-42LMB	L81	
45	CY7C516-45DC	D30	Commercial
	CY7C516-45GC	G68	
	CY7C516-45JC	J81	
	CY7C516-45LC	L81	
	CY7C516-45PC	P29	
55	CY7C516-55DC	D30	Commercial
	CY7C516-55GC	G68	
	CY7C516-55JC	J81	
	CY7C516-55LC	L81	
	CY7C516-55PC	P29	
	CY7C516-55DMB	D30	Military
	CY7C516-55GMB	G68	
	CY7C516-55LMB	L81	
75	CY7C516-75DC	D30	Commercial
	CY7C516-75GC	G68	
	CY7C516-75JC	J81	
	CY7C516-75LC	L81	
	CY7C516-75PC	P29	
	CY7C516-75DMB	D30	Military
	CY7C516-75GMB	G68	
	CY7C516-75LMB	L81	

Speed (ns)	Ordering Code	Package Type	Operating Range
38	CY7C517-38DC	D30	
	CY7C517-38GC	G68	
	CY7C517-38JC	J81	
	CY7C517-38LC	L81	
42	CY7C517-42DMB	D30	Military
	CY7C517-42GMB	G68	
	CY7C517-42LMB	L81	
45	CY7C517-45DC	D30	Commercial
	CY7C517-45GC	G68	
	CY7C517-45JC	J81	
	CY7C517-45LC	L81	
	CY7C517-45PC	P29	
55	CY7C517-55DC	D30	Commercial
	CY7C517-55GC	G68	
	CY7C517-55JC	J81	
	CY7C517-55LC	L81	
	CY7C517-55PC	P29	
	CY7C517-55DMB	D30	Military
	CY7C517-55GMB	G68	
	CY7C517-55LMB	L81	
75	CY7C517-75DC	D30	Commercial
	CY7C517-75GC	G68	
	CY7C517-75JC	J81	
	CY7C517-75LC	L81	
	CY7C517-75PC	P29	
	CY7C517-75DMB	D30	Military
	CY7C517-75GMB	G68	
	CY7C517-75LMB	L81	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{OH}	1, 2, 3
I_{OL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OS}	1, 2, 3
I_{OZL}	1, 2, 3
I_{OZH}	1, 2, 3
$I_{CC}(Q_1)$	1, 2, 3
$I_{CC}(Q_2)$	1, 2, 3
I_{CC}(Max.)	1, 2, 3

Switching Characteristics

Parameters	Subgroups
t_{MUC}	7, 8, 9, 10, 11
t_{MC}	7, 8, 9, 10, 11
t_S	7, 8, 9, 10, 11
t_H	7, 8, 9, 10, 11
t_{SE}	7, 8, 9, 10, 11
t_{HE}	7, 8, 9, 10, 11
t_{PWH}, t_{PWL}	7, 8, 9, 10, 11
t_{PDSEL}	7, 8, 9, 10, 11
t_{PDP}	7, 8, 9, 10, 11
t_{PDY}	7, 8, 9, 10, 11
t_{PHZ}	7, 8, 9, 10, 11
t_{PLZ}	7, 8, 9, 10, 11
t_{PZH}	7, 8, 9, 10, 11
t_{LZL}	7, 8, 9, 10, 11
t_{LZH}	7, 8, 9, 10, 11
t_{LLZ}	7, 8, 9, 10, 11
t_{LHZ}	7, 8, 9, 10, 11
t_{PZL}	7, 8, 9, 10, 11
t_{HCL}	7, 8, 9, 10, 11

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