64Kx4 Static RAM CMOS, High Speed Monolithic

ADVANCE INFORMATION

The EDI8466CA is a high performance CMOS Static RAM organized as 65,536 locations x 4 bits.

The EDI8466CA offers an Output Enable function ($\overline{G}$) for use in managing the Data Bus.

This very high speed device is ideal for use in high performance systems which contain high speed memory arrays, i.e. cache, writeable control stores, and vector arrays.

Inputs and tri-state outputs are TTL compatible and allow for direct interfacing with common bus system structures.

Features

64Kx4 bit CMOS Static Random Access Memory

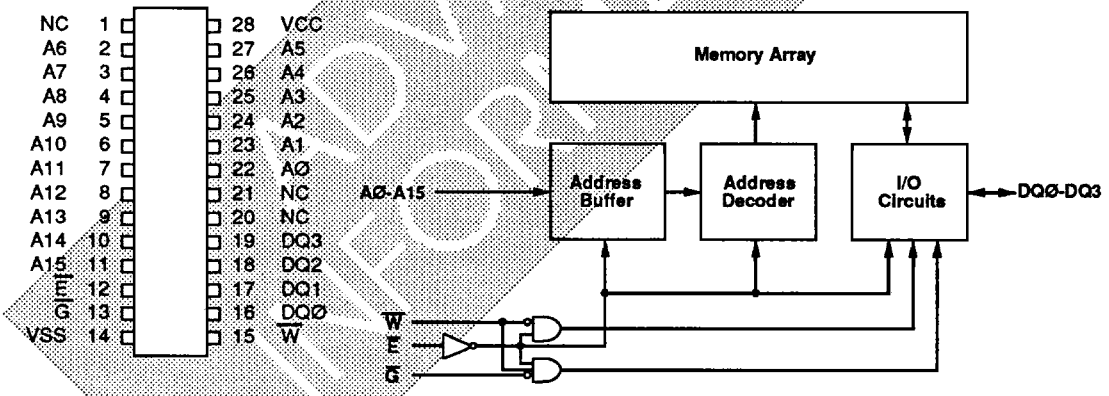
- Access Times: 10, 12 and 15 ns
- Output Enable Function for Bus Control
- Fully Static, No Clocks
- TTL Compatible I/O

Surface Mount and Thru-hole Package Styles

- 28 Lead SOJ, No. 20
- 28 Pin Plastic DIP, 300 mils wide, No. 81
- Common Data Inputs and Outputs

Single +5V (±10%) Supply Operation

Pin Configuration and Block Diagram



Pin Names

AØ-A15	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQØ-DQ3	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground
NC	No Connection

Absolute Maximum Ratings*

Voltage on any pin relative to VSS ..... -0.5V to 7.0V
Operating Temperature TA (Ambient)
Commercial ..... 0°C to +70°C
Storage Temperature
Plastic ..... -65°C to +150°C
Power Dissipation ..... 1 Watt
Output Current (Note 1) ..... ±40 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Note 1: Outputs should be in shorted condition for a time period of ≤ 30 seconds. Only one output should be shorted at any one time.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	–	VCC+0.5	V
Input Low Voltage	VIL	-0.5	–	0.8	V

AC Test Conditions

Input Pulse Levels ..... VSS to 3.0V
Input Rise and Fall Times 3ns
Input and Output Timing Levels 1.5V
Output Load. ..... 1TTL, CL =Fig. 1
(note: For TEHQZ and TWLQZ, CL = Fig. 2)

Figure 1

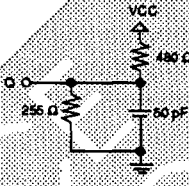
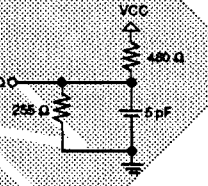


Figure 2



DC Electrical Characteristics

Parameter	Sym	Conditions	Min	Typ*	Max	Units
Power Supply Operating Current	ICC1	Min Cycle All Pins ≤VIL or ≥VIH, II/O = 0 mA $\overline{E}$=VIL, 50% Read Cycles	—	200	Note 1	mA
Dynamic TTL Standby Current	ICC2	$\overline{E}$ ≥ VIH, All Pins ≤ VIL or ≥ VIH, Min Cycle	—		85	mA
Full Standby Power Supply Current	ICC3	$\overline{E}$≥ VCC -0.2V, f = 0 All Pins ≥ VCC -0.2V or ≤ 0.2V	—	—	5	mA
Input Leakage Current	ILI	VIN = 0V to VCC	—	—	±10	µA
Output Leakage Current	ILO	V I/O = 0V to VCC	—	—	±10	µA
Output High Voltage	VOH	IOH = -4.0mA	2.4	—	—	V
Output Low Voltage	VOL	IOL = 8.0mA	—	—	0.4	V

*Typical: TA = 25°C, VCC = 5.0V
Note 1: See ICC1 in AC Characteristic Tables.

Truth Table

$\overline{E}$	$\overline{W}$	$\overline{G}$	Mode	Input/Output	Power
H	X	X	Standby	HIGH Z	ICC2, ICC3
L	H	L	Read	DOUT	ICC1
L	L	X	Write	DIN	ICC1
L	H	H	Deselect	HIGH Z	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Address Lines	CI	6	pF
Data Lines	CD/Q	8	pF

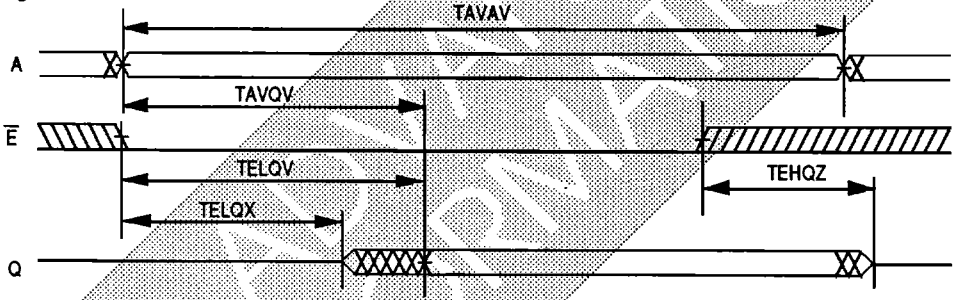
These parameters are sampled, not 100% tested.

AC Characteristics
Read Cycle

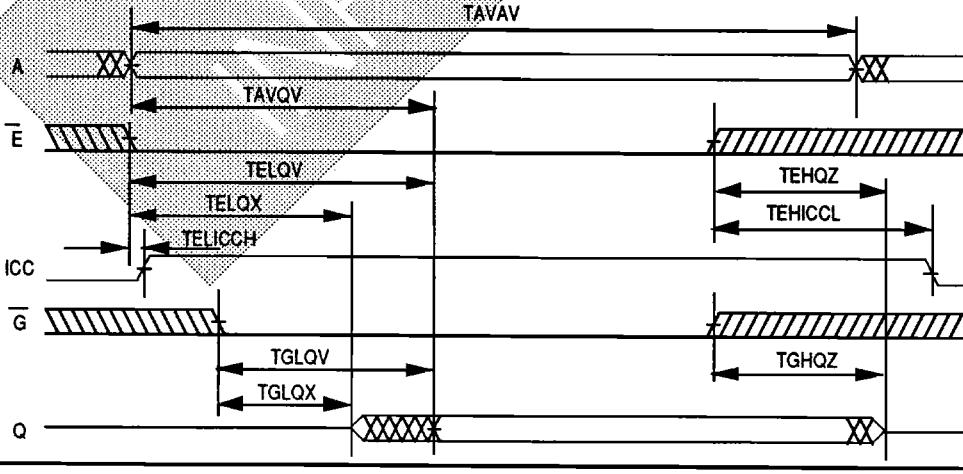
Parameter	Symbol JEDEC	Symbol Alt.		10ns Min	10ns Max	12ns Min	12ns Max	15ns Min	15ns Max	Units
Operating Power Supply Current (2)	ICC1	ICC1R			250		235		215	mA
Read Cycle Time	TAVAV	TRC		10		12		15		ns
Address Access Time	TAVQV	TAA			10		12		15	ns
Chip Enable Access Time	TELQV	TACS			10		12		15	ns
Chip Enable to Output Low Z (1)	TELQX	TCLZ		2		2		2		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ			5		6		7	ns
Output Hold from Address Change	TAVQX	TOH		3		3		3		ns
Output Enable to Output Valid	TGLQV	TOE			5		6		7	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ		0		0		0		ns
Output Disable to Output in High Z (1)	TGHQZ	TOHZ			5		6		7	ns
Chip Enable to Power Up (1)	TELICCH	TPU		0		0		0		ns
Chip Enable to Power Down (1)	TEHICCL	TPD			10		12		15	ns

Note 1: Parameter guaranteed, but not tested.
Note 2: $\overline{E}$ = VSS, I/O= 0mA.

Read Cycle 2
$\overline{W}$ High



Read Cycle 2
$\overline{W}$ High



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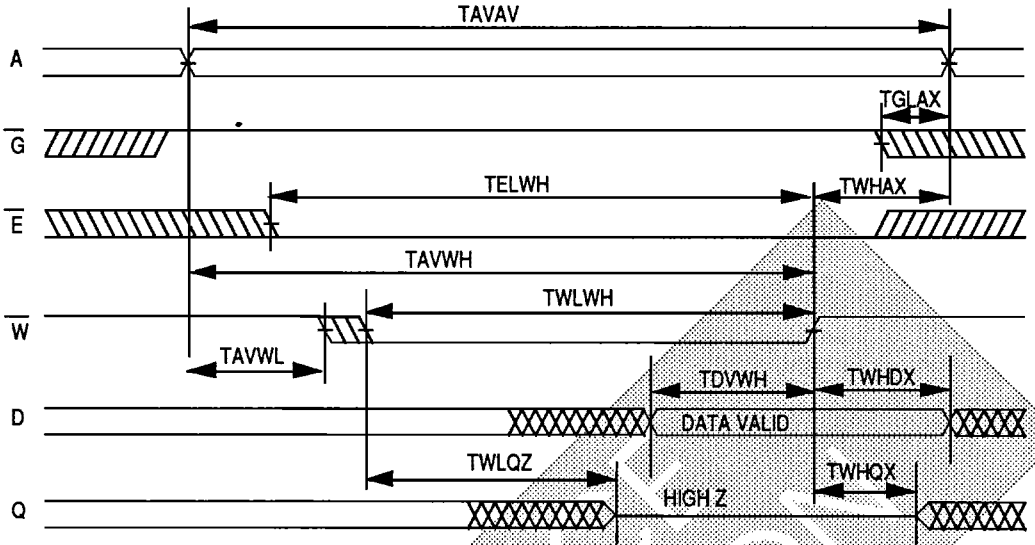
AC Characteristics
Write Cycle

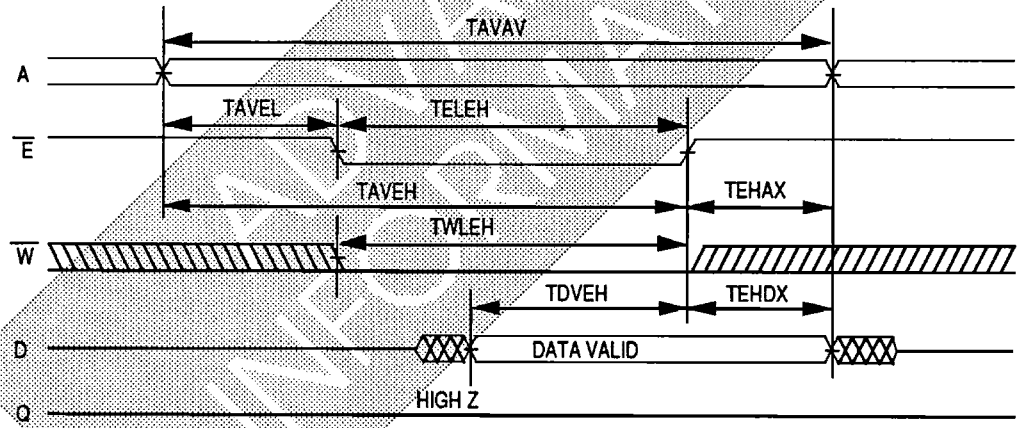
Parameter	Symbol			10ns		12ns		15ns		Units
	JEDEC	Alt.		Min	Max	Min	Max	Min	Max	
Operating Power Supply Current (2)	ICC1	ICC1W			235		215		195	mA
Write Cycle Time	TAVAV	TWC		10		12		15		ns
Chip Enable to End of Write	TELWH	TCW		8		10		10		ns
	TELEH	TCW		8		10		10		ns
Address Setup Time	TAVWL	TAS		0		0		0		ns
	TAVEL	TAS		0		0		0		ns
Address Valid to End of Write	TAVWH	TAW		8		10		10		ns
	TAVEH	TAW		8		10		10		ns
Write Pulse Width	TWLWH	TWP		8		10		10		ns
	TWLEH	TWP		8		10		10		ns
Write Recovery Time	TWHAX	TWR		0		0		0		ns
	TEHAX	TWR		0		0		0		ns
Data Hold Time	TWHDX	TDH		0		0		0		ns
	TEHDX	TDH		0		0		0		ns
Write to Output in High Z (1)	TWLQZ	TWHZ		0	4	0	6	0	6	ns
Data to Write Time	TDVWH	TDW		4		6		6		ns
	TDVEH	TDW		4		6		6		ns
Output Active from End of Write (1)	TWHQX	TWLZ		0		0		0		ns

Note 1: Parameter guaranteed, but not tested.
Note 2: $\overline{E}$ = VSS, I/O= 0mA.

Write Cycle 1
$\overline{W}$ Controlled



Write Cycle 2
$\overline{E}$ Controlled



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Ordering Information

Part No.	Speed (ns)	Leads	Package Style	No.
EDI8466CA10MC	10	28	SOJ	20
EDI8466CA12MC	12	28	SOJ	20
EDI8466CA15MC	15	28	SOJ	20
EDI8466CA10RC	10	28	0.3 DIP	81
EDI8466CA12RC	12	28	0.3 DIP	81
EDI8466CA15RC	15	28	0.3 DIP	81