



SRAM

32K x 8 SRAM

AVAILABLE AS MILITARY SPECIFICATIONS

- SMD 5962-88662
- MIL-STD-883

FEATURES

- Ultra high speed 12, 15ns
- High speed: 20, 25, 35 and 45ns
- Battery backup: 2V data retention
- Low power standby
- High-performance, low-power, CMOS double-metal process
- Single +5V ($\pm 10\%$) power supply
- Easy memory expansion with \overline{CE}
- All inputs and outputs are TTL compatible

OPTIONS

- Timing
 - 12ns access (Contact factory) -12
 - 15ns access -15
 - 20ns access -20
 - 25ns access -25
 - 35ns access -35
 - 45ns access -45
 - 55ns access -55*
 - 70ns access -70*

MARKING

- Packages

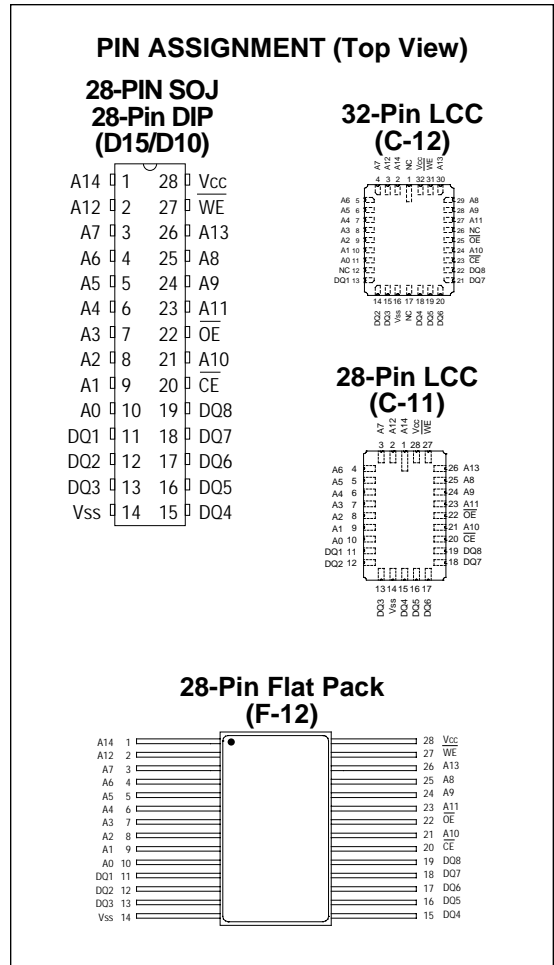
Ceramic DIP (300 mil)	C	No. 108
Ceramic DIP (600 mil)	CW	No. 110
Ceramic LCC (28 leads)	EC	No. 204
Ceramic LCC (32 leads)	ECW	No. 208
Ceramic Flat Pack	F	No. 302
Ceramic SOJ	DCJ	No. 500

- 2V data retention, low power standby L
 - Radiation Tolerant (EPI) E
- *Electrical characteristics identical to those provided for the 45ns access devices.

GENERAL DESCRIPTION

The Austin Semiconductor SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Austin Semiconductor SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Austin Semiconductor offers chip enable (\overline{CE}) and output enable (\overline{OE}) capability. These enhancements can place the



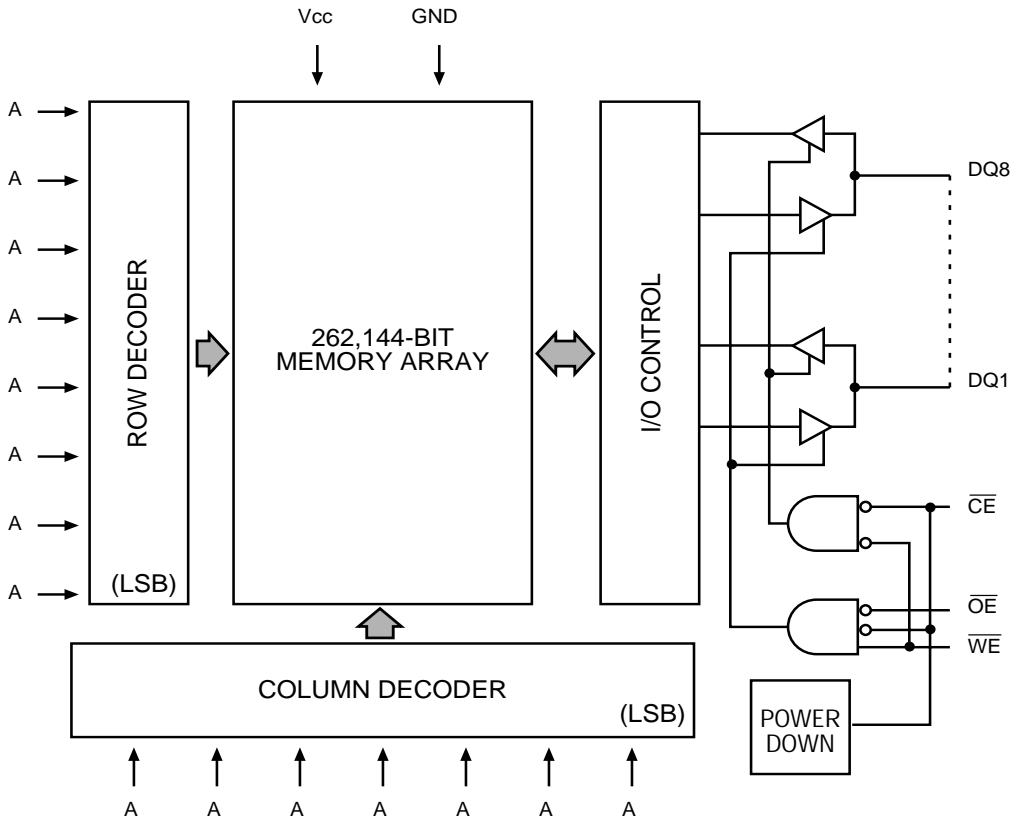
outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable (\overline{WE}) and \overline{CE} inputs are both LOW. Reading is accomplished when \overline{WE} remains HIGH and \overline{CE} and \overline{OE} go LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.



The "L" version provides an approximate 50 percent reduction in CMOS standby current (I_{sbc2}) over the standard version. All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	\overline{OE}	\overline{CE}	\overline{WE}	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Input or DQ Relative to Vss -2V to +7V
 Voltage on Vcc Supply Relative to Vss -1V to +7V
 Storage Temperature -65°C to +150°C
 Power Dissipation 1W
 Short Circuit Output Current 50mA
 Lead Temperature (soldering 10 seconds) +260°C
 Junction Temperature +175°C

*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(-55°C ≤ T_C ≤ 125°C; V_{CC} = 5V ± 10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V _{IH}	2.2	V _{CC} +1.0	V	1
Input Low (Logic 0) Voltage		V _{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V _{IN} ≤ V _{CC}	I _{LI}	-5	5	μA	
Output Leakage Current	Outputs Disabled 0V ≤ V _{OUT} ≤ V _{CC}	I _{LO}	-5	5	μA	
Output High Voltage	I _{OH} = -4.0mA	V _{OH}	2.4		V	1
Output Low Voltage	I _{OL} = 8.0mA	V _{OL}		0.4	V	1

DESCRIPTION	CONDITIONS	SYMBOL	MAX						UNITS	NOTES
			-12	-15	-20	-25	-35	-45		
Power Supply Current: Operating	$\overline{CE} \leq V_{IL}; V_{CC} = \text{MAX}$ f = MAX = 1/τ _{RC} (MIN) Output Open	I _{CC}	190	165	150	140	135	130	mA	3
Power Supply Current: Standby	$\overline{CE} \geq V_{IH}; V_{CC} = \text{MAX}$ f = MAX = 1/τ _{RC} (MIN) Output Open	I _{SBT1}	60	50	45	40	40	40	mA	
	$\overline{CE} \geq V_{IH}$, All Other Inputs ≤ V _{IL} or ≥ V _{IH} , V _{CC} = MAX f = 0 Hz	I _{SBT2}	25	25	25	25	25	25	mA	
	$\overline{CE} \geq V_{CC} - 0.2V; V_{CC} = \text{MAX}$ V _{IL} ≤ V _{SS} + 0.2V V _{IH} ≥ V _{CC} - 0.2V; f = 0 Hz	I _{SBC2}	5	5	5	5	5	5	mA	
	“L” Version Only	I _{SBC2}	4	4	4	4	4	4	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T _A = 25°C, f = 1MHz	C _i		8	pF	4
Output Capacitance	V _{CC} = 5V	C _o		8	pF	4



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (-55°C ≤ T_C ≤ 125°C; V_{CC} = 5V ± 10%)

DESCRIPTION	SYM	-12		-15		-20		-25		-35		-45		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ Cycle															
READ cycle time	t _{RC}	12		15		20		25		35		45		ns	
Address access time	t _{AA}		12		15		20		25		35		45	ns	
Chip Enable access time	t _{ACE}		12		15		20		25		35		45	ns	
Output hold from address change	t _{OH}	2		2		2		2		2		2		ns	
Enable to output in Low-Z	t _{LZCE}	2		2		2		2		2		2		ns	7
disable to output in High-Z	t _{HZCE}		7		8		9		10		14		15	ns	6, 7
Chip Enable to power-up time	t _{PU}	0		0		0		0		0		0		ns	4
Chip disable to power-down time	t _{PD}		12		15		20		25		35		45	ns	4
Output Enable access time	t _{AOE}		6		8		9		10		14		15	ns	
Output Enable to output in Low-Z	t _{LZOE}	0		0		0		0		0		0		ns	
Output disable to output in High-Z	t _{HZOE}		4		6		8		10		14		15	ns	6
WRITE Cycle															
WRITE cycle time	t _{WC}	12		15		20		25		35		45		ns	
Chip Enable to end of write	t _{CW}	10		12		15		18		20		25		ns	
Address valid to end of write	t _{AW}	10		12		15		18		20		25		ns	
Address setup time	t _{AS}	0		0		0		0		0		0		ns	
Address hold from end of write	t _{AH}	2		2		2		2		2		2		ns	
WRITE pulse width	t _{WP}	10		12		15		17		20		25		ns	
Data setup time	t _{DS}	6		7		10		12		15		20		ns	
Data hold time	t _{DH}	0		0		0		0		0		0		ns	
Write disable to output in Low-Z	t _{LZWE}	2		2		2		2		2		2		ns	7
Write Enable to output in High-Z	t _{HZWE}	0	6	0	7	0	10	0	11	0	14	0	15	ns	6, 7



AC TEST CONDITIONS

Input pulse levels	Vss to 3V
Input rise and fall times	5ns
Input timing reference level	1.5V
Output reference level	1.5V
Output load	See figures 1 and 2

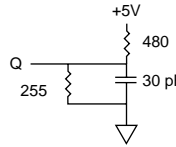


Fig. 1 OUTPUT LOAD EQUIVALENT

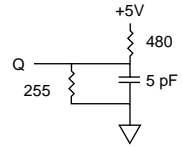


Fig. 2 OUTPUT LOAD EQUIVALENT

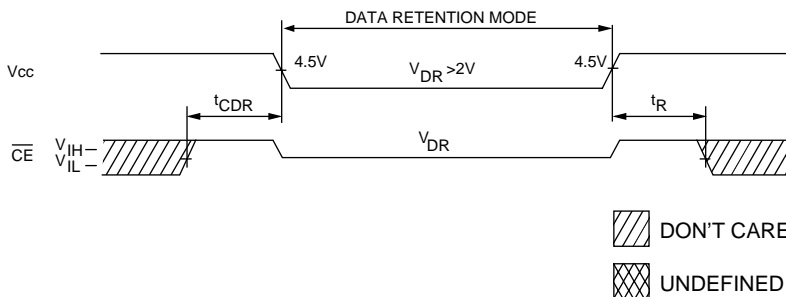
NOTES

- All voltages referenced to Vss (GND).
- 3V for pulse width < 20ns.
- Icc is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded, and $f = \frac{1}{t_{RC} (MIN)}$ Hz.
- This parameter is guaranteed but not tested.
- Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
- ^tHZCE, ^tHZOE and ^tHZWE are specified with CL = 5 pF as in Fig. 2. Transition is measured ± 500mV typical from steady state voltage, allowing for actual tester RC time constant.
- At any given temperature and voltage condition, ^tHZCE is less than ^tLZCE and ^tHZWE is less than ^tLZWE.
- \overline{WE} is HIGH for READ cycle.
- Device is continuously selected. Chip enable and output enable are held in their active state.
- Address valid prior to or coincident with latest occurring chip enable.
- ^tRC = READ cycle time.
- Chip enable (\overline{CE}) and write enable (\overline{WE}) can initiate and terminate a WRITE cycle.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

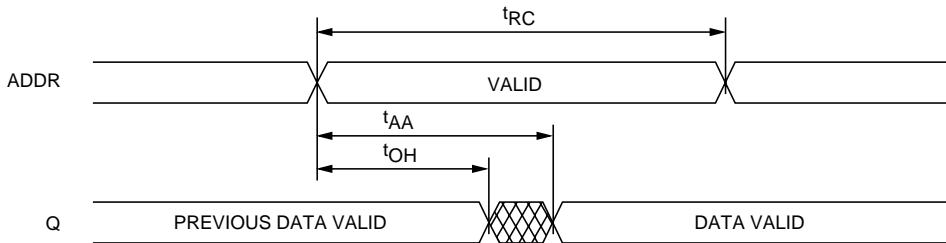
DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Vcc for Retention Data		VDR	2	—	V	
Data Retention Current	$\overline{CE} \geq (V_{CC} - 0.2V)$ $V_{IN} \geq (V_{CC} - 0.2V)$ or $\leq 0.2V$	IccDR	Vcc = 2V	1.0		mA
	Vcc = 3V		1.5		mA	
Chip Deselect to Data Retention Time		^t CDR	0	—	ns	4
Operation Recovery Time		^t R	^t RC		ns	4, 11

LOW Vcc DATA RETENTION WAVEFORM

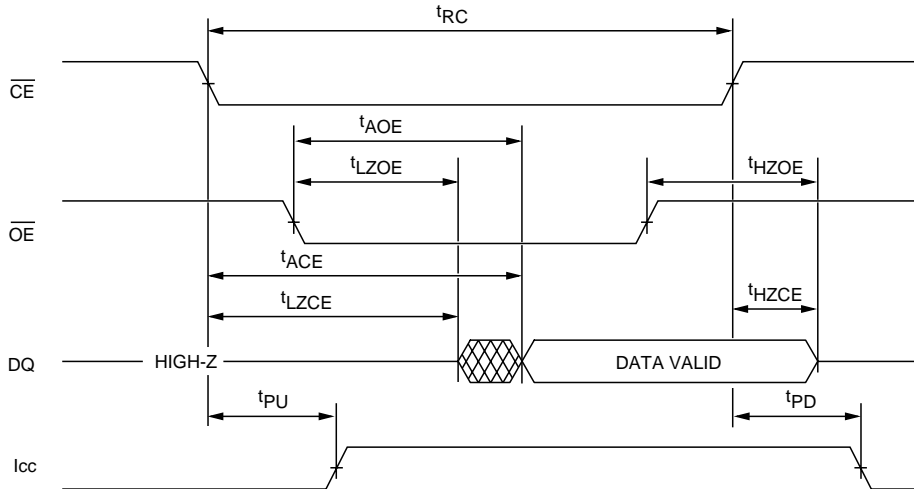




READ CYCLE NO. 1 8, 9



READ CYCLE NO. 2 7, 8, 10

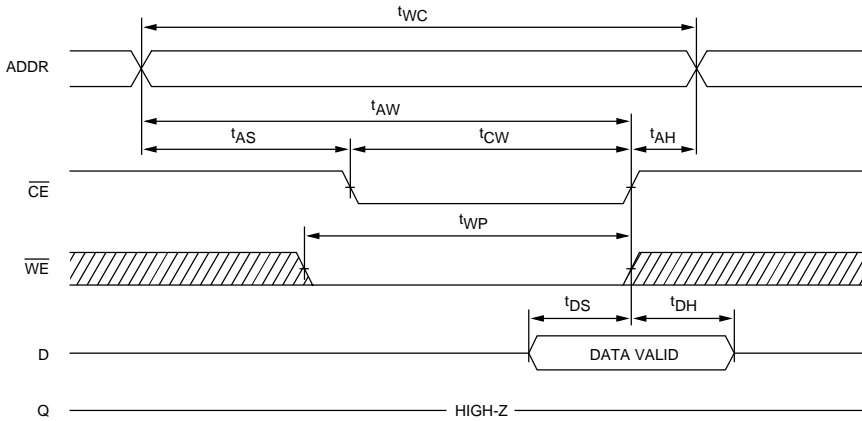


 DON'T CARE

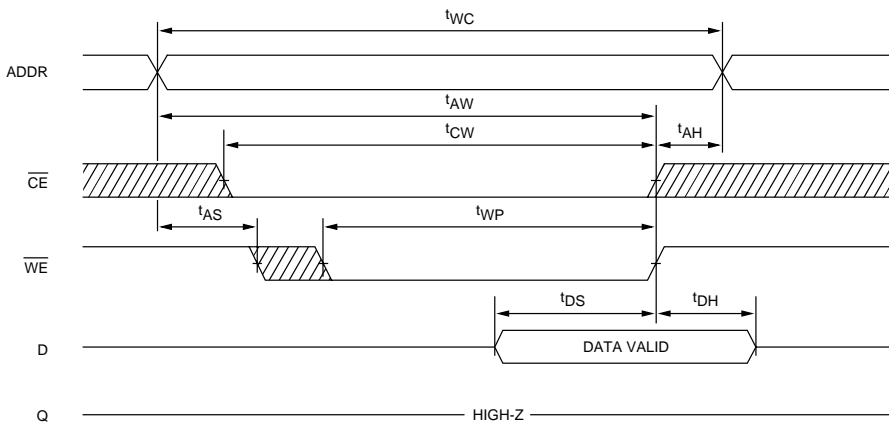
 UNDEFINED





WRITE CYCLE NO. 1¹²
(Chip Enable Controlled)



WRITE CYCLE NO. 2^{7, 12}
(Write Enable Controlled)



 DON'T CARE
 UNDEFINED

NOTE: Output enable (\overline{OE}) is inactive (HIGH).



ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (per Method 5005, Table I)
INTERIM ELECTRICAL (PRE-BURN-IN) TEST PARAMETERS (Method 5004)	2, 8A, 10
FINAL ELECTRICAL TEST PARAMETERS (Method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
GROUP A TEST REQUIREMENTS (Method 5005)	1, 2, 3, 4**, 7, 8, 9, 10, 11
GROUP C AND D END-POINT ELECTRICAL PARAMETERS (Method 5005)	1, 2, 3, 7, 8, 9, 10, 11

* PDA applies to subgroups 1 and 7.

** Subgroup 4 shall be measured only for initial qualification and after process or design changes, which may affect input or output capacitance.