PBL 3736 Subscriber Line Interface Circuit

Description

The PBL 3736 Subscriber Line Interface Circuit (SLIC) is a bipolar integrated circuit in 75V technology, which performs the telephone line interface function.

The programmable battery feed circuit incorporates a switching regulator to minimize on-chip power dissipation and to maintain line feed characteristics independent of battery variations.

Tip-ring polarity is reversible without altering SLIC supervisory and voice frequency (vf) signal functions. In addition, tip and ring outputs can be forced to high-impedance states. These and other operating modes can be set via a parallel four-bit control word.

An external resistor sets the off-hook detector threshold current. The ring trip detector can operate with both balanced and unbalanced ringing systems. Both detectors are read via a common output.

Ring and test relay drivers are provided.

A stand-by mode minimizes idle power dissipation while leaving the supervisory functions active.

The complex or real two-wire impedance is set by a single, lumped-element network.

2- to 4-wire and 4- to 2-wire signal conversion is provided by the SLIC in conjunction with either conventional or programmable CODEC/filters.

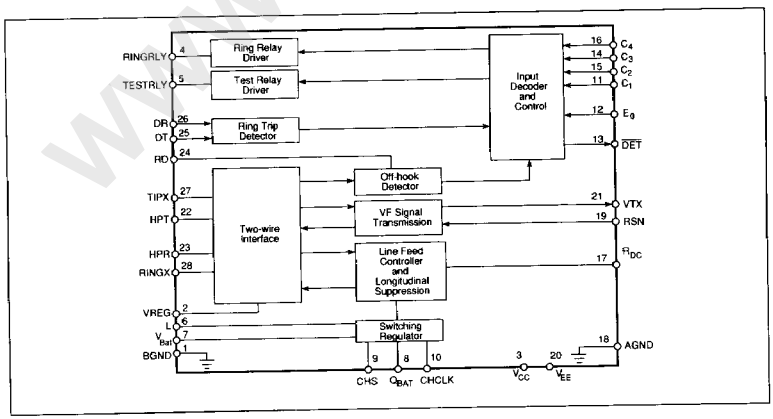
Longitudinal line voltages are suppressed by a control loop within the SLIC.

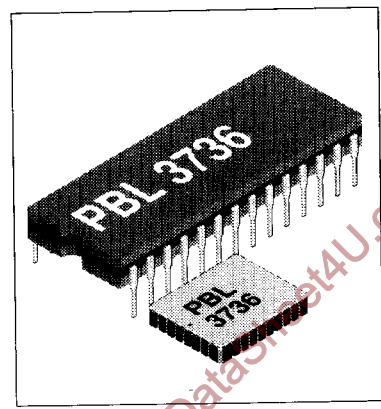
The SLIC package is ceramic 28-pin dual-in-line or ceramic 32-pin leadless chip carrier.

The PBL 3736 is fully compatible with AMD SLIC, Am 7950.

Key Features

- On-chip switching regulator to minimize power dissipation
- Programmable line-feed resistance
- Line feed characteristics independent of battery variations
- Tip-ring polarity reversal function
- Tip, ring open circuit states
- Programmable off-hook detector
- Ring trip detector
- Ring and test relay drivers
- Line terminating impedance (complex or real) set by a simple external network
- Hybrid function with conventional or programmable CODEC/filters
- Longitudinal signal suppression





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Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Temperature				
Storage temperature range	T_{Stg}	-55	150	°C
Operating temperature range	T_{Amb}	0	70	°C
Operating junction temperature range, Note 1	T_J		125	°C
Power supply, dissipation				
V_{CC} with respect to AGND	V_{CC}	-0.4	7	V
V_{EE} with respect to AGND	V_{EE}	-7	0.4	V
V_{Bat} with respect to BGND	V_{Bat}	-70	0.4	V
Dissipation at T_{Amb} = 70°C, Note 14			1.7	W
R_L = 50 ohms, R_{Feed} = 2 x 250 ohms				
Ground				
Voltage between AGND and BGND		-0.3	0.3	V
Switching regulator				
Peak current through regulator switch	I_{LPeak}		150	mA
Peak regulator switch-off voltage	V_L		2	V
Relay drivers				
Test relay supply voltage	V_{Test}	V_{Bat}	V_{CC}	V
Ring relay supply voltage	V_{Ring}	V_{Bat}	V_{CC}	V
Test relay current	I_{Test}		50	mA
Ring relay current	I_{Ring}		50	mA
Ring trip comparator				
Input voltage	V_{DT}, V_{DR}	V_{Bat}	0	V
Input current, t_p = 10ms	I_{DT}, I_{DR}	-2	2	mA
Digital inputs, outputs C_1 — C_4, E_0, $\overline{DET}$, CHCLK				
Input voltage	V_{ID}	-0.4	V_{CC}	V
Output voltage ($\overline{DET}$ not active)	V_{OD}	-0.3	V_{CC}	V
Output current	I_{OD}		3	mA
TIPX and RINGX terminals				
TIPX or RINGX voltage, continuous, referenced to AGND, Note 2	V_{TA}, V_{RA}	V_{Bat}	1	V
TIPX or RINGX, pulse < 10 ms, t_{rep} > 10 s, Note 2	V_{TA}, V_{RA}	V_{Bat}	5	V
TIPX or RINGX, pulse < 1 µs, t_{rep} > 10 s, Note 2	V_{TA}, V_{RA}	V_{Bat} - 20	10	V
TIP or RING, pulse < 250 ns, t_{rep} > 10 s, Note 13	V_{TA}, V_{RA}	V_{Bat} - 50	15	V
TIPX or RINGX current	I_M	-105	105	mA

Recommended Operating Conditions, Note 3

Parameter	Symbol	Min	Max	Unit
Ambient temperature	T_{Amb}	0	70	°C
V_{CC} with respect to AGND	V_{CC}	4.75	5.25	V
V_{EE} with repect to AGND	V_{EE}	-5.25	-4.75	V
V_{Bat} with respect to BGND	V_{Bat}	-64	-40.5	V
B_{GND} with respect to AGND	V_{AB}	-100	100	mV

Electrical Characteristics

T_{Amb} = 25°C, V_{CC} = +5 V ±5%, V_{EE} = -5 V ±5%, V_{Bat} = -40.5 to -64V, AGND = BGND, 2-wire ac impedance, Z_{TR} = 600 ohms, R_{DC1} = R_{DC2} = 20 kohms, C_{HP} = 0.22 µF, C_{DC} = 0.15 µF unless otherwise specified

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Two-wire port						
Overload level, V_{TRO}	1	Z_L = 600 ohms, 1% THD f = 1kHz, E_L = 0, Note 4	3.1			V_{Peak}
Input impedance, Z_{TR}		Note 5				
Longitudinal impedance, R_{LT}, R_{LR}		f < 100 Hz		20	40	ohm/wire
Longitudinal current limit, I_{LT}, I_{LR}		active state	28	36.8		mA_{Peak}/wire
		stand-by state	9	16.8		mA_{Peak}/wire
Longitudinal to metallic balance, B_{LM}		IEEE standard 455-1985 0.2 kHz < f < 3.4 kHz, note 6	48	55		dB
Metallic to longitudinal balance, B_{ML}		FCC part 68, paragraph 68.310				
		0.2 kHz < f < 1.0 kHz	35	48		dB
		1.0 kHz < f < 4.0 kHz, note 6	35	42		dB
Longitudinal to metallic balance, B_{LME}	2	0.2 kHz < f < 3.4 kHz	48	55		dB
Longitudinal to four-wire balance, B_{LFE}	2	0.2 kHz < f < 3.4 kHz	48	55		dB
Metallic to longitudinal balance, B_{MLE}	2	0.2 kHz < f < 4 kHz	35	42		dB
Four-wire to longitudinal balance, B_{FLE}	2	0.2 kHz < f < 4 kHz	35	42		dB
Two-wire return loss, r		$r = 20 \cdot \text{Log} \frac{\lvert Z_{TR} + Z_L \rvert}{\lvert Z_{TR} - Z_L \rvert}$				
		0.2 kHz < f < 0.5 kHz	35	40		dB
		0.5 kHz < f < 1.0 kHz	30	35		dB
		1.0 kHz < f < 3.4 kHz, Note 6	20	28		dB
Polarity reversal time, t_{PR}		Normal to reversed or reversed to normal		15		ms
TIPX idle voltage, V_{TI}		V_{Bat} = -50V	-5.5	-4.3	-3.0	V
		V_{Bat} = -64V Normal polarity	-5.5	-4.3	-3.0	V
RINGX idle voltage, V_{RI}		V_{Bat} = -50V	-42	-40	-38	V
		V_{Bat} = -64V Normal polarity	-55	-53	-51	V

Figure 1. Test circuit for transmission parameters.

$\frac{1}{\omega C} << R_L$, R_L = 600 ohms

R_T = 600 kohms, R_{RX} = 300 kohms

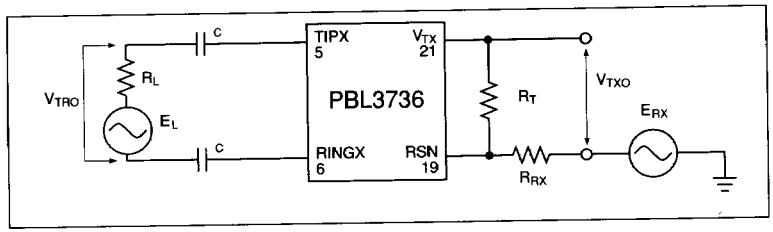
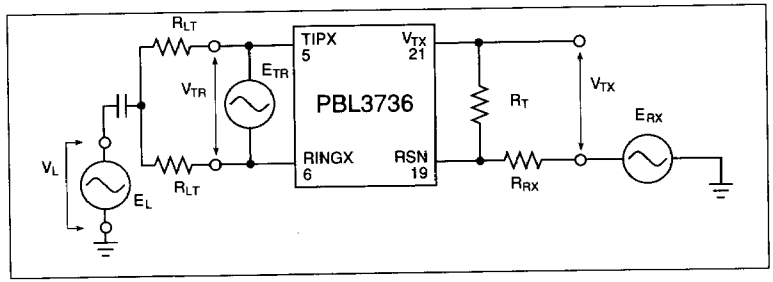


Figure 2. Test circuit for longitudinal balance.

$\frac{1}{\omega C} << 150$ ohms, R_{LT} = R_{LR} = 300 ohms

R_T = 600 kohms, R_{RX} = 300 kohms

Longitudinal to metallic balance, $B_{LME} = 20 \cdot \log \left| \frac{E_L}{V_{TR}} \right|$, E_R = 0, omit E_{TR}



Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Four-wire transmit port (V_{TX})						
Overload level, V_{TXO}	1	Load impedance > 20 kohms, f = 1kHz, 1% THD, E_{RX} = 0, Note 7	3.1			V_{Peak}
Output offset voltage, ΔV_{TX}			-30	± 20	30	mV
Output impedance, z_{TX}		0.2 kHz < f < 3.4 kHz		10	20	ohm
Four-wire receive port (RSN)						
Receive summing node (RSN) dc voltage		I_{RSN} = 0	-10	0	10	mV
Receive summing node (RSN) impedance		0.2 kHz < f < 3.4 kHz			20	ohm
Receive summing node (RSN) current (I_{RSN}) to metallic loop current (I_M) gain, G_{RX}		0.2 kHz < f < 3.4 kHz R_T = 600 kohms	980	1000	1020	ratio
Frequency response						
Two-wire to four-wire, g_{2-4}	1	0.3 kHz < f < 3.4 kHz relative to 0 dBm, 1.0 kHz, Note 8	-0.1	±0.03	0.1	dB
Four-wire to two-wire, g_{4-2}	1	0.3 kHz < f < 3.4 kHz relative to 0 dBm, 1.0 kHz, Note 8	-0.1	±0.03	0.1	dB
Four-wire to four-wire, g_{4-4}	1	0.3 kHz < f < 3.4 kHz relative to 0 dBm, 1.0 kHz, note 8	-0.1	±0.06	0.1	dB
Insertion loss						
Two-wire to four-wire, G_{2-4}	1	0 dBm, 1.0 kHz, Notes 8, 9	-0.15	±0.1	0.15	dB
Four-wire to two-wire, G_{4-2}	1	0 dBm, 1.0 kHz, Notes 8, 9, 10	-0.15	±0.1	0.15	dB
Gain tracking						
Two-wire to four-wire	1	Ref. -10 dBm, 1.0 kHz, Note 8				
		-30 dBm to 3 dBm	-0.1		0.1	dB
		-55 dBm to -30 dBm		±0.1		dB
Four-wire to two-wire	1	Ref. -10 dBm, 1.0 kHz, Note 8				
		-30 dBm to 3 dBm	-0.1		0.1	dB
		-55 dBm to -30 dBm		±0.1		dB
Noise						
Idle channel noise (two-wire or four-wire)	1	C-message weighting		14	16	dBrnC
		Psophometrical weighting		-76	-74	dBmp
		R_{Feed} = 2 x 250 ohms, Note 11				
Single-frequency out-of-band noise						
Metallic	3	12 kHz to 1 MHz		-55	-50	dBV
Longitudinal	3	12 kHz to 90 kH		-68	-63	dBV
		90 kHz to 1 MHz		-50	-48	dBV
		Note 12				

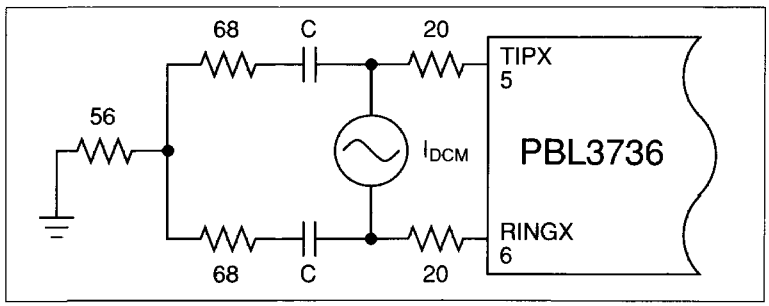


Figure 3. Single-frequency noise test Circuit.

$\frac{1}{\omega C}$ << 100 ohms

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Total harmonic distortion						
Two-wire to four-wire and four-wire to two-wire		0 dBm, 1.0 kHz test signal 0.3 kHz < f < 3.4 kHz		-64	-50	dB
Intermodulation						
Type $2f_1 - f_2$		0.3 kHz < f_1, f_2 < 3.4 kHz				
2-wire to 4-wire		Level $f_1 = f_2$ = -25dBV to 0dBV		-60	-45	dBV
4-wire to 2-wire		$f_1 \neq n \cdot f_2$, $f_2 \neq n \cdot f_1$		-60	-45	dBV
Type $f_1 \pm 50$Hz		0.3 kHz < f_1 < 3.4 kHz Level 50Hz = Level f_1 - 14dB Level f_1 = -15dBV to 0dBV				
2-wire to 4-wire		$f_1 \neq n \cdot 50$ Hz		-65	-50	-dB
Battery feed characteristics						
Apparent battery voltage			47.5	50	52.5	V
Feed resistance to programming resistance ($R_{DC1} + R_{DC2}$) conversion factor, K_1			47.5	50	52.5	ratio
Stand-by state loop current limit conversion factor, K_{LIM}		R_L > 50 ohms $I_{LIM} = K_{LIM} \cdot I_{LDET} = \frac{375V}{R_D}$	1.25	1.8	2.2	ratio
Loop current detector threshold (I_{LDet})						
Tolerance with respect to programmed I_{LDet}		$I_{LDet} = \frac{375V}{R_D}$, R_D in kohms	$0.8 \cdot I_{LDet}$	I_{LDet}	$1.2 \cdot I_{LDet}$	mA
Dial pulse distortion				4	10	%
Ring trip detector inputs (D_T, D_R)						
Offset voltage			-20	±10	20	mV
Bias current, I_B		$I_B = (I_{DT} + I_{DR})/2$		0.1	1	µA
Input resistance		Balanced Unbalanced	1 3			Mohms Mohms
Common mode range, V_{TA}, V_{RA}			$V_{Bat} + 1$		-2	V
Relay driver outputs (RINGRLY, TESTRLY)						
On-state voltage		I = 25mA	$V_{CC} - 1.8$	$V_{CC} - 1.3$	$V_{CC} - 1.0$	V
Off-state leakage current		Output voltage = V_{Bat}		5	100	µA
Clamp voltage		I = 25mA	$V_{Bat} - 2.0$		$V_{Bat} - 1.0$	V
Digital Inputs (C_1 ... C_4, E_0, CHCLK)						
Input low voltage					0.7	V
Input high voltage			2.0			V
Input low current		V_{IL} = 0.4V	-0.4			mA
Input high current		V_{IH} = 2.4V			40	µA
Digital Output ($\overline{DET}$)						
Output low voltage		I_{OL} = 1.0mA			0.45	V
Output high voltage		I_{OH} = -0.1mA	2.4			V
Resistive pull-up		Internal resistor	10	15	22	kohm
Switching regulator transistor output (L)						
Saturation voltage, V_{LOSAT}		I_L = 100mA			1.5	V
Leakage current, I_{LK}		V_{LO} = 0V			200	µA
Switching regulator clock input (CHCLK)						
Clock frequency, f_{CHCLK}			253	256	259	kHz

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Power dissipation (relay drivers off)						
V_{CC} supply current		On/off hook, normal mode		7	10	mA
V_{EE} supply current		On/off hook, normal mode		2	3	mA
V_{Bat} supply current		On hook, normal mode		4	6	mA
On-hook total dissipation		V_{Bat} = -60 V, open circuit mode		50	90	mW
On-hook total dissipation		V_{Bat} = -60 V, stand-by mode		200	350	mW
On-hook total dissipation		V_{Bat} = -60 V, normal mode		325	400	mW
Off-hook total dissipation		V_{Bat} = -60 V, normal mode R_L = 600 ohms, $R_{DC1} + R_{DC2}$ = 40 kohms		800	1000	mW
Thermal resistance						
Junction to ambient, Θ_{JA}		28-pin ceramic DIL		29		°C/W
		32-pin ceramic leadless chip carrirer		29		°C/W

Notes

1. The circuit includes thermal protection. Operation at or above 125 °C junction temperature may degrade device reliability.
2. A diode in series with the V_{Bat} input increases the permitted continuous voltage and pulse < 10ms to -70V and pulse < 1µs to the greater of |-70V| or |V_{Bat} - 40V|.
3. BGND and AGND must be connected before supply voltages. Application of V_{Bat} with a low rate of change is recommended. Refer to section "Power-up sequence".
4. The overload level is specified at the two-wire port with the signal source at the four-wire port.
5. The two-wire impedance is programmable by selection of external component values according to:

   Z_{TRX} = $Z_T/|G_{TX} \cdot G_{RX}|$ where:

   Z_{TRX} = impedance between the TIPX and RINGX terminals

   Z_T = programming network between the V_{TX} and RSN terminals

   G_{TX} = transmit gain, nominally = 1

   G_{RX} = receive current gain, nominally = -1000 (current defined as positive flowing into the receive summing node, RSN pin 19).
6. The indicated balance and two-wire return loss values do not include errors caused by external components (e.g. R_{F1}, R_{F2}, R_T).
7. The overload level is specified at the four-wire transmit port, V_{TX}, with the signal source at the two-wire port. Note that the gain from the two-wire port to the four-wire transmit port is G_{TX} = 1.
8. The level is specified in dBm, 600 ohms impedance level.
9. Fuse resistors, R_F, impact insertion loss as explained in the text, section Transmission.
10. The indicated insertion loss tolerance does not include errors caused by external components.
11. The two-wire idle noise is specified with the port terminated in 600 ohms (R_L) and with the four-wire receive port grounded (E_{RX} = 0).

    The four-wire idle channel noise at V_{TX} is specified with the two-wire port terminated in 600 ohms (R_L). The noise specification is with respect to a 600 ohms impedance level at V_{TX}. The four-wire receive port is grounded (E_{RX} = 0).
12. These specifications are valid for a longitudinal impedance of 90 ohms and a metallic impedance of 135 ohms.
13. R_{F1}, $R_{F2} \geq$ 20 ohms is also required. Pulse is supplied to TIP and RING outside R_{F1}, R_{F2}.
14. Value applies for momentarely junction temperature of 120 °C for 28-pin DIL without heatsink.

Pin Descriptions

Refer to figure 4 (28-pin dual-in-line package, 32-pin ceramic leadless chip carrier (LLCC). Pin x/y = LLCC terminal /DIPterminal.

LLCC	DIP	Symbol	Description
1	1	BGND	Battery ground.
2	2	V_{REG}	Regulated negative voltage for power amplifiers. The switching regulator inductor, filter capacitor, and RC stabilization network connect to this pin.
3	3	V_{CC}	+5 V power supply.
4	-	NC	No internal connection
5	4	RINGRLY	Ring relay driver output. Sources up to 50 mA from V_{CC}.
6	5	TESTRLY	Test relay driver output. Sources up to 50 mA from V_{CC}.
7	6	L	Switching regulator drive transistor output. The 1 mH inductor and the catch diode connect to this pin. These components must be connected with shortest possible lead lengths. The catch diode, including connecting leads, must exhibit a low inductance to effectively clamp when the regulator switch opens.
8	7	V_{Bat}	Battery supply voltage, -64 V to -40.5 V. Negative with respect to BGND, pin 1/1.
9	8	Q_{Bat}	Quiet battery. An external filter capacitor connects between this pin and AGND to provide filtered battery supply to signal processing circuits.
10	9	CHS	Switching regulator stabilization network input. From this pin, a capacitor connects to AGND and a series RC network to V_{REG}, pin 2/2.
11	10	CHCLK	Switching regulator TTL-compatible clock input. Nominal frequency: 256 kHz.
12	11	C_4	C_1 (pin 17/16), C_2 (pin 15/14), C_3 (pin 16/15), and C_4 are TTL-compatible inputs controlling the SLIC operating modes and states.
13	12	E_0	Read enable. A logic high enables $\overline{DET}$ (pin 14/13). A logic low disables $\overline{DET}$. TTL-compatible input.
14	13	$\overline{DET}$	Detector output. Inputs C_1, C_2 and C_3 select the detector to be connected to this output. When $\overline{DET}$ is enabled via E_0 (pin 13/12), a logic low indicates that the selected detector has been tripped. The $\overline{DET}$ output is open collector with internal pull-up resistor (approx, 15 kohm) to V_{CC} (pin 3/3). When disabled, $\overline{DET}$ thus appears to be a resistor connected to V_{CC}.
15	14	C_2	Refer to pin 12/11 description.

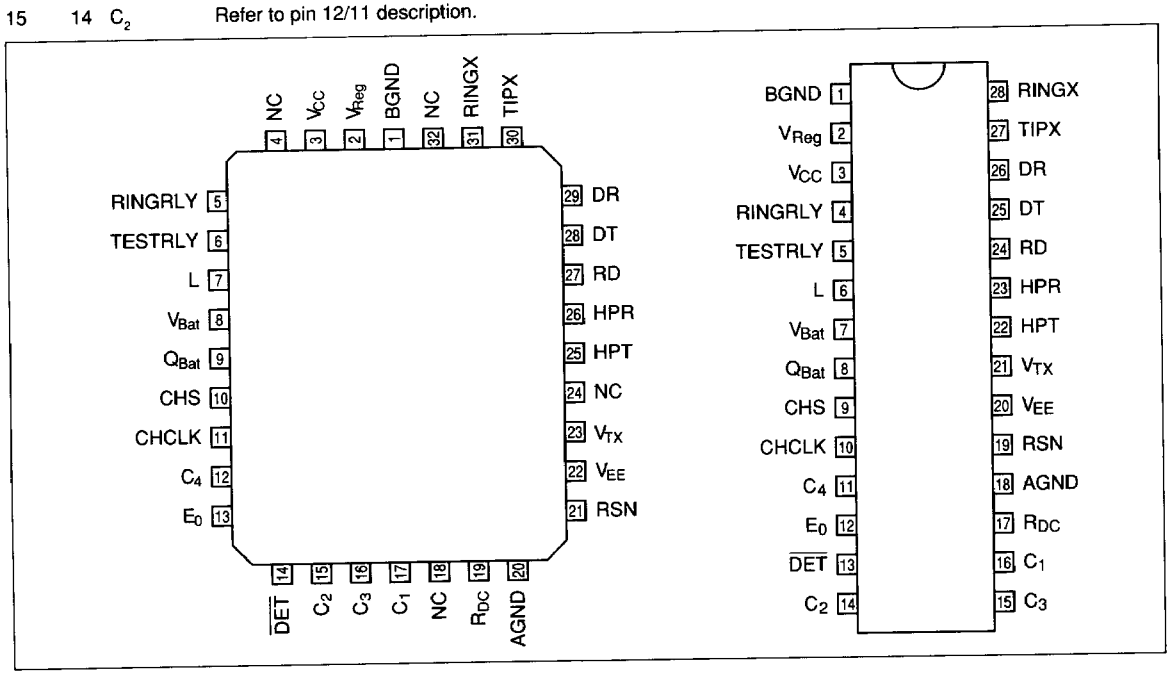
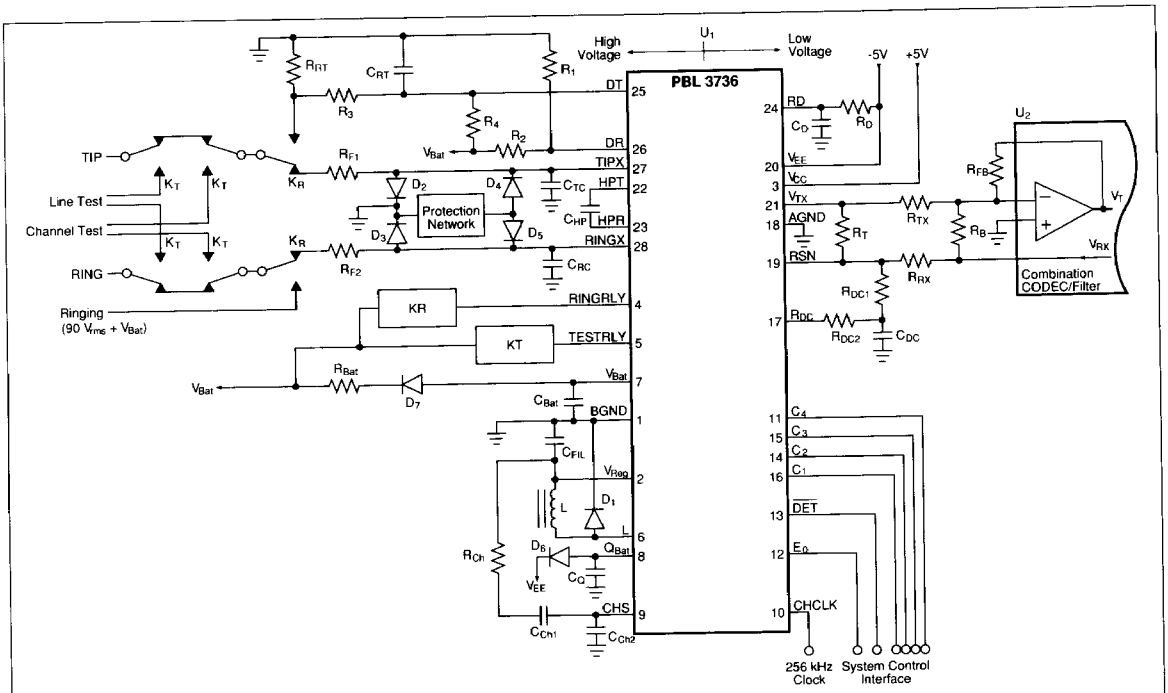


Figure 4. Pin configuration, top view

LLCC	DIP	Symbol	Description
16	15	C_3	Refer to pin 12/11 description.
17	16	C_1	Refer to pin 12/11 description.
18	-	NC	No internal connection
19	17	R_{DC}	DC feed resistance is programmed by two resistors connected in series from this pin to the receive summing node (RSN, pin 19). The resistor junction point is decoupled to AGND to filter noise and disturbances before reaching the RSN pin. V_{RDC} polarity is negative for normal tip-ring polarity and positive for reversed tip-ring polarity. $\|V_{RDC}\| = \|(\| V_{HPT} - V_{HPR} \| - 50V) / 20\|$
20	18	AGND	Analog and digital ground. Analog ground is a quiet ground for vf signal processing circuits.
21	19	RSN	Receive summing node. 1000 times the current (dc and ac) flowing into this pin equals the metallic (transversal) current flowing between TIPX (pin 30/27) and RINGX (pin 31/28). Programming networks for feed resistance, 2-wire impedance, and recieve gain connect to the receive summing node.
22	20	V_{EE}	-5V power supply.
23	21	V_{TX}	Transmit vf output. The ac voltage difference between TIPX (pin 30/27) and RINGX (pin 31/28), the ac metallic voltage, is reproduced as an unbalanced AGND-referenced signal at V_{TX} with a gain of one. The two-wire impedance programming network connects between V_{TX} and RSN (pin 21/19).
24	-	NC	No internal connection
25	22	HPT	Ring side (HPR) and tip side (HPT) of ac/dc separation capacitor.
26	23	HPR	
27	24	RD	Off-hook detector programming resistor connects from RD to V_{EE} (pin 22/20). A filter capacitor, C_D, connects from RD to AGND. In the stand-by mode, the maximum loop current is 1.5 times the threshold current set by R_D.
28	25	DT	Non-inverting (DR) and inverting (DT) inputs to ring trip comparator.
29	26	DR	
30	27	TIPX	The TIPX and RINGX pins connect to the tip and ring leads of the 2-wire line interface via over-voltage-
31	28	RINGX	protection components, ring and test relays.
32	-	NC	No internal connection.



U1	PBL 3736, SLIC (Subscriber Line Interface Circuit)
U2	Combination CODEC/filter (SLAC, or any other programmable CODEC/filter may be used for improved line interface flexibility)
K_R	Relay, 48 V coil, 2C contacts, 1500 V rating
K_T	Relay, 48 V coil, 4C contacts, 1500 V rating
L	Choke, 1 mH, RF
D_1	Diode, 100 V, 100 mA, 10 ns, (e.g. 1N4448)
D_2-D_5,	100 V, 3 A
D_6,	Diode 100 V, 100 mA
D_7	Diode 100 V, 500 mA
R_{F1}, R_{F2}	Line resistor, 2*20 Ω, 1% match (e.g. Ericsson Components PBR 5067)
R_1, R_3	200 kΩ, 3%, 1/4 W
R_2	910 kΩ, 5%, 1/4 W
R_4,	1.2 MΩ, 5%, 1/4 W
R_{CH},	680 Ω, 5%, 1/4 W
R_D,	51.1 kΩ, 1%, 1/4 W (sets off-hook threshold and stand by current)*
R_T,	562 kΩ, 1%, 1/4 W (sets 2-wire impedance)*
R_{RX},	280 kΩ, 1%, 1/4 W (sets receive gain)*
R_{DC1}, R_{DC2}	20 kΩ, 1%, 1/4 W (sets battery feed resistance)*
R_{TX},	20 kΩ, 1%, 1/4 W (sets transmit gain)*

R_B,	24.3 kΩ, 1%, 1/4 W (sets transhybrid balance)*
C_{RT},	0.39 µF, 20%, 100 V
C_{HP},	0.22 µF, 20%, 100 V
C_{TC}, C_{RC}	2200 pF, 20%, 100 V
C_{FIL},	0.47 µF, 20%, 100 V
C_{BAT}	0.47 µF, 20%, 100 V
C_D	0.33 µF, 20%, 100 V
C_{CH1},	0.047 µF, 20%, 100 V
C_{CH2},	560 pF, 20%, 100 V
C_D,	0.01µF, 20%, 10 V (sets off-hook filtering)*

Protection network, e.g. RCA surgector; SGT06U13

Note : The parts marked by an asterisk (*) are user programmable. The values shown can be altered to suit the application.

Figure 5. Single-channel subscriber line interface with PBL 3736 SLIC and combination CODEC/filter.

Transmission

General

A simplified ac model of the transmission circuits is shown in figure 6. Circuit analysis yields:

$$V_{TR} = V_{TX} + I_M \cdot 2R_F \quad (1)$$

$$\frac{V_{TX}}{Z_T} + \frac{V_{RX}}{Z_{RX}} = \frac{I_M}{1000} \quad (2)$$

$$V_{TR} = E_G - I_M \cdot Z_L \quad (3)$$

where:

V_{TX} is a ground referenced unity gain version of the ac metallic voltage between the TIPX and RINGX terminals.

V_{TR} is the ac metallic voltage between tip and ring.

E_G is the line open circuit ac metallic voltage.

I_M is the ac metallic current.

R_F is a fuse resistor.

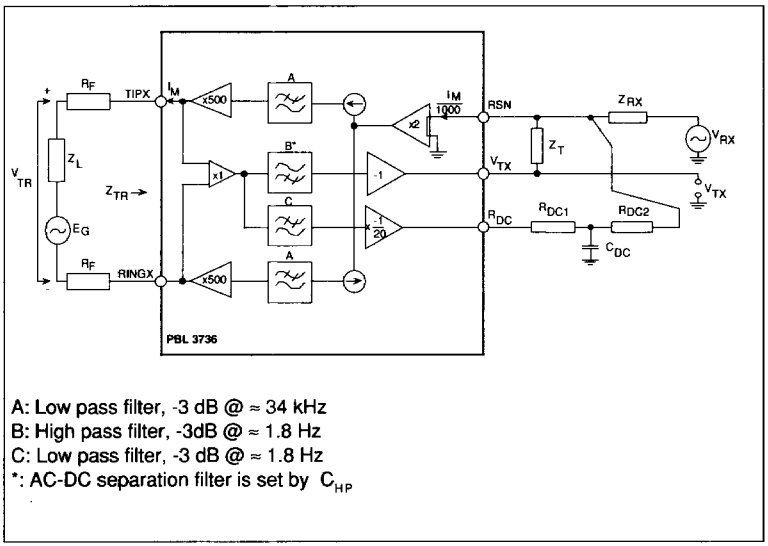
Z_L is the line impedance.

Z_T determines the SLIC TIPX to RINGX impedance.

Z_{RX} controls four- to two-wire gain.

V_{RX} is the analog ground referenced receive signal.

The low-pass filter, block A, shown in figure 6 will impact the 2-wire to 4-wire, 4-wire to 2-wire, and 4-wire to 4-wire phase response in the voice frequency band. At 3.4 kHz, the phase shift is 3 to 5 degrees. Contact the factory for additional information. Note that equations (1), (2) and (3) above do not account for this phase shift.



A: Low pass filter, -3 dB @ ≈ 34 kHz
B: High pass filter, -3dB @ ≈ 1.8 Hz
C: Low pass filter, -3 dB @ ≈ 1.8 Hz
*: AC-DC separation filter is set by C_{HP}

Figure 6. Simplified ac transmission circuit

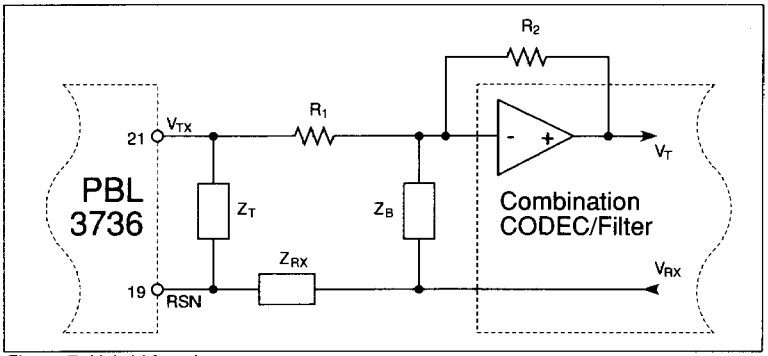


Figure 7. Hybrid function.

Two-wire impedance

To calculate Z_{TR}, the impedance presented to the two-wire line by the SLIC including the fuse resistors R_F, let:

$V_{RX} = 0$.

Then, from (1) and (2):

$$Z_{TR} = Z_T/1000 + 2R_F$$

Thus with Z_{TR} and R_F known:

$$Z_T = 1000 \cdot (Z_{TR} - 2R_F)$$

Example:

Calculate Z_T to make $Z_{TR} = 900\ \Omega$ in series with $2.16\ \mu F$. $R_F = 20\ \Omega$

$$Z_T = 1000 \cdot \left(900 + \frac{1}{j\cdot\omega \cdot 2.16 \cdot 10^{-6}} - 2 \cdot 20\right)$$

which yields:

$Z_T = 860\ k\Omega$ in series with 2.16 nF.

Two-wire to four-wire gain

From (1) and (2) with $V_{RX} = 0$:

$$G_{2\text{-}4} = \frac{V_{TX}}{V_{TR}} = \frac{Z_T/1000}{Z_T/1000 + 2R_F}$$

Four-wire to two-wire gain

From (1), (2) and (3) with $E_G = 0$:

$$G_{4\text{-}2} = \frac{V_{TR}}{V_{RX}} = -\frac{Z_T}{Z_{RX}} \cdot \frac{Z_L}{Z_T/1000 + 2R_F + Z_L}$$

For applications where $Z_T/1000 + 2R_F$ is chosen to be equal to Z_L, the expression for $G_{4\text{-}2}$ simplifies to:

$$G_{4\text{-}2} = -\frac{Z_T}{Z_{RX}} \cdot \frac{1}{2}$$

Four-wire to four-wire gain

From (1), (2) and (3) with $E_G = 0$:

$$G_{4\text{-}4} = \frac{V_{TX}}{V_{RX}} = -\frac{Z_T}{Z_{RX}} \cdot \frac{Z_L + 2R_F}{Z_T/1000 + 2R_F + Z_L}$$

Hybrid function

The PBL 3736 SLIC forms a particularly flexible and compact line interface when used with a SLAC (Subscriber Line Audio Processing Circuit) or other programmable CODEC/filter. The SLAC allows for system controller adjustment of hybrid balance to accommodate different line impedances without change of hardware. In addition, the SLAC permits transmit and receive gain adjustments in 0.1 dB steps. Please, refer to SLAC or other programmable CODEC/filter data sheets for design information.

The hybrid function can also be implemented utilizing the uncommitted amplifier in conventional CODEC/filter combinations. Please, refer to figure 7. Via impedance Z_B a current proportional to V_{RX} is injected into the summing node of the combination CODEC/filter amplifier. As can be seen from the expression for the four-wire to four-wire gain a voltage proportional to V_{RX} is returned to V_{TX}. This voltage is converted by R_{TX} to a current into the same summing node. These currents can be made to cancel by letting:

$$\frac{V_{TX}}{R_{TX}} + \frac{V_{RX}}{Z_B} = 0, (E_G = 0)$$

The four-wire to four-wire gain, $G_{4\text{-}4}$, includes the required phase shift and thus the balance network Z_B can be calculated from:

$$Z_B = -R_{TX} \cdot \frac{V_{RX}}{V_{TX}}$$

$$= R_{TX} \cdot \frac{Z_{RX}}{Z_T} \cdot \frac{Z_T/1000 + 2R_F + Z_L}{Z_L + 2R_F}$$

Longitudinal impedance

A feedback loop counteracts longitudinal voltages at the two-wire port by injecting longitudinal currents in opposing phase. Thus longitudinal disturbances will appear as longitudinal currents and the TIPX and RINGX terminals will experience very small longitudinal voltage excursions, leaving the metallic voltages well within the SLIC common-mode range. This is accomplished by comparing the instantaneous two-wire longitudinal voltage to an internal longitudinal reference voltage, V_{LBias}. As shown below, the SLIC appears as 20 ohms per wire to longitudinal disturbances. It should be noted that longitudinal currents may exceed the dc loop current without disturbing the vf transmission. Refer to figure 8. Circuit analysis yields:

$(V_L/2 + V_L/2)/20$ kohms$= I_L/1000$

which reduces to $R_{LT} = R_{LR} = V_L/I_L = 20$ ohms where:

$R_{LT} = R_{LR}$ = longitudinal resistance/wire

V_L = longitudinal voltage at TIPX, RINGX

I_L = longitudinal current

Ac transmission circuit stability

To ensure stability of the feedback loop shown in block diagram form in figure 6, two compensation capacitors C_{RC} and C_{TC} are required. Figure 5 includes these capacitors. Recommended value is 2200 pF.

Battery Feed

Line feed characteristics

Figure 9 shows the battery feed control loop. Circuit analysis for the normal polarity case yields:

$$I_{DCMET} = \frac{|V_{DCMET}| - 50V}{(R_{DC1} + R_{DC2})/50}$$

where V_{DCMET} is the dc metallic voltage between TIPX and RINGX terminals and I_{DCMET} is the dc loop current. The loop thus has an apparent feed voltage of 50V with a feed resistance of

$$R_{Feed} = (R_{DC1} + R_{DC2})/50$$

The polarity-reversal transition time is dependent on the time constant formed by R_{DC1}, R_{DC2} and C_{DC}. This time constant should be set to between 0.4 and 1.0 ms. $R_{DC1} = R_{DC2}$ results in the smallest C_{DC} value.

The PBL 3736 dc feed programming components may then be calculated from:

$$R_{DC1} + R_{DC2} = 1/2 \cdot 50 (R_{Feed} - 2R_F)$$

(Note that the fuse resistors have been included as part of the total feed resistance in this expression.)

and:

$$C_{DC} = T \cdot (R_{DC1} + R_{DC2})/(R_{DC1} \cdot R_{DC2})$$

where R_{Feed} is the desired feed resistance, $2R_F$ is the value of the two fuse resistors, normally 20 ohms each, and T is between 0.4 and 1.0 ms.

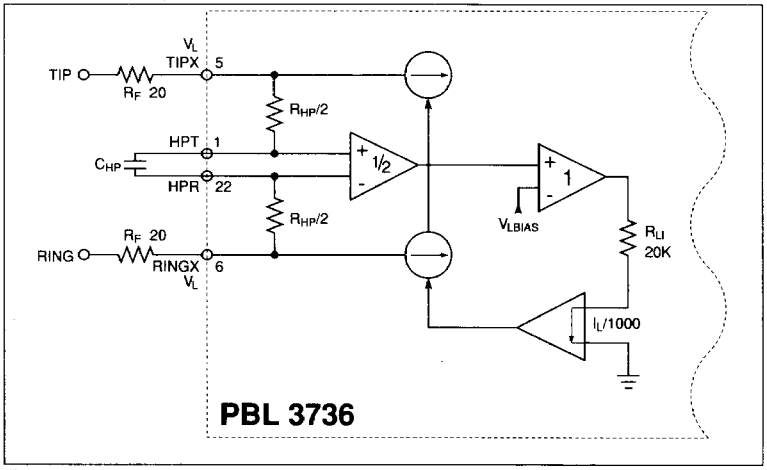


Figure 8. Longitudinal impedance.

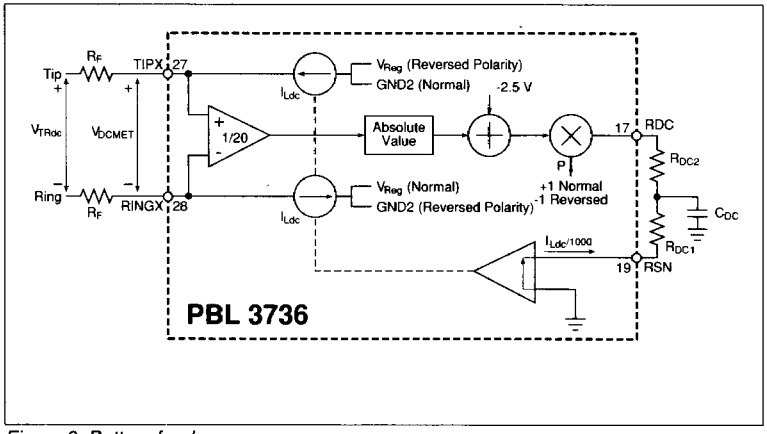


Figure 9. Battery feed.

The switching regulator supplies a voltage to the line drivers of:

$| V_{REG} | = | V_{DCMET} | + V_{Bias}$

where V_{Bias} is approximately 15V.

It is necessary for $| V_{REG} | < | V_{Bat} |$ to maintain a resistive feed characteristic. With V_{Bat} = -50V, the maximum $| V_{DCMET} |$ = 50V - 15V = 35V. To feed the loop with at least 18mA, a maximum loop resistance of 35V/18mA = 1940 ohms can then be achieved with V_{Bat} = -50V. The feed resistance to design for would be 15V/18mA = 830 ohms. Longer loops are accommodated by selecting a higher V_{Bat} voltage, while not exceeding the maximum allowable V_{Bat} voltage..

Switching regulator

Refer to figure 10. The regulator input voltage is V_{Bat} (pin 7). This voltage is converted with high efficiency to V_{REG} (pin 2) which supplies the line drivers. The regulator reference voltage V_{REF} is derived from the TIPX-to-RINGX dc metallic voltage according to:

$V_{REG} = V_{REF} = |V_{DCMET}| + V_{Bias}$

where V_{Bias} is approximately 15V. Thus the voltage supplying the line drivers is never more than is necessary and consequently the power dissipation in the SLIC is substantially reduced.

The components associated with the switching regulator must be connected by the shortest possible trace lengths. Other circuits should be kept isolated from this area. The L pin (pin 6) voltage variations are large and very fast. The catch diode (e.g. 1N4448) should withstand 70V reverse voltage, conduct an average of 50mA (150 mA peak) and turn off in less than 10 ns. The inductor should be 1mH with a series resistance of approximately 10 ohms and a capacitance of less than 10 pF. The inductor must withstand peak currents of 150 mA without saturating. Iron-core is suggested to avoid inductor saturation. J. W. Miller 9220-28 or Nytronics RFC-S are possible choices. Ferrite-pot core inductors may also be used. Note, however, that a saturated, low-loss inductor may result in SLIC damage due to excessive regulator switching current.

Closed magnetic path inductor cores (e.g. toroid, pot core) are less prone to generate interfering magnetic fields than inductors wound on open cores and may thus reduce possible 256kHz interference.

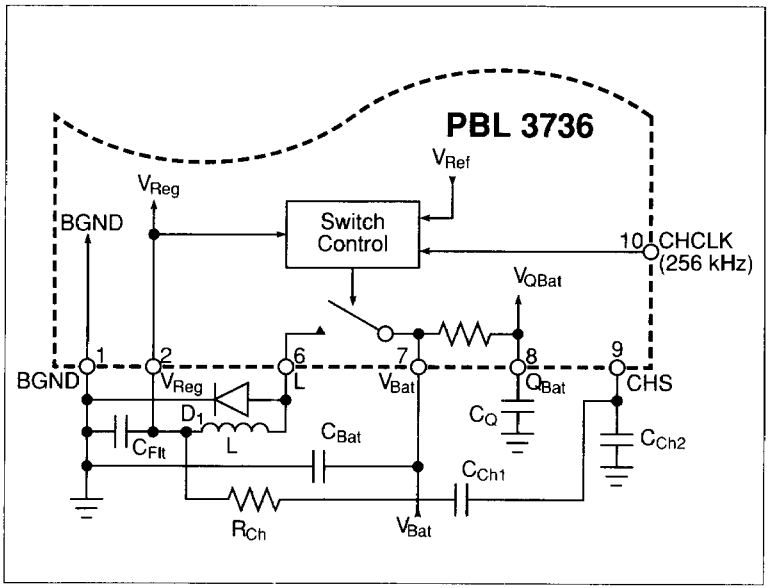


Figure 10. Switching regulator.

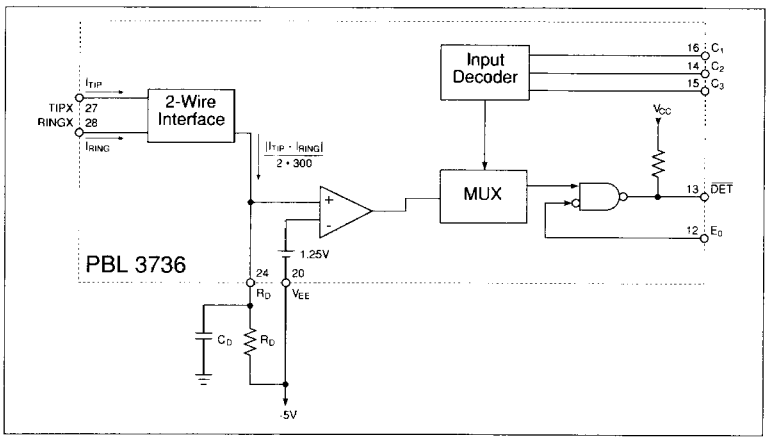


Figure 11. Loop current detector.

Loop Monitoring Functions

The PBL 3736 includes two loop-monitoring functions: loop current and ring trip detection. These two detectors report their status through a common output, $\overline{DET}$ (pin 13). The detector to be connected to $\overline{DET}$ is selected via decoder inputs C_1 through C_3. The $\overline{DET}$ output is enabled via the read-enable input E_0 (pin 12).

Loop current detector

The loop current value, at which the loop current detector changes state, is programmable by selecting the value of resistor R_D. R_D connects between pins RD (24) and V_{EE} (20). A filter capacitor, C_D, should be connected between R_D (24) and AGND. The C_D capacitor may be omitted if the $\overline{DET}$ output is filtered (e.g. software routine).

Figure 11 shows a block diagram of the loop current detector. The two-wire interface produces a current flowing out of pin RD (pin 24):

$I_{RD} = |I_{TIP} - I_{RING}|/(2 \cdot 300) = I_L/300$

where I_{TIP} and I_{RING} are currents flowing into the TIPX and RINGX terminals and I_L

is the loop current. The voltage generated by I_{RD} across the programming resistor R_D is compared to an internal 1.25 V reference. A logic low results at $\overline{DET}$, when I_{RD} exceeds the corresponding threshold current, $I_{RD} = I_{Thresh} = I_{LDet}/300$. The programming resistor can then be calculated as $R_D = 1.25/I_{Thresh} = 375/I_{LTH}$, when the desired threshold current I_{LTH} is known. R_D is in kohms for I_{Thresh}, I_{LTH} in mA. The filter capacitor is calculated according to $C_D = T/R_D$ with time constant T = 0.25 ms.

Ring trip detector

Ring trip detection is accomplished by connecting an external network to a comparator in the SLIC with inputs DT (pin 25) and DR (pin 26). The ringing source can be balanced or unbalanced, superimposed on V_{Bat}. The unbalanced ringing source may be applied to either the ring lead or the tip lead with return via the other wire. A ring relay driven by the SLIC ring relay driver connects the ringing source to tip and ring.

Figure 12 shows a balanced ringing circuit configuration. R_1 and R_2 are the ring feed resistors, which connect the balanced ringing generator E_{R+} and E_{R-} to the telephone line via ring relay K_R. R_{B1}, R_{B2}, R_3, and R_4 together with the SLIC comparator provide the ring trip detection function. for unbalanced ringing, E_{R+} would be zero. Figure 13 shows an example of a ring trip network for unbalanced ringing.

The ring trip function is based on a polarity change at the comparator input when the line goes off-hook. In the on-hook state no dc current flows through the loop and the voltage at comparator input DT is more positive than the voltage at input DR. When the line goes off-hook, dc current flows and the comparator input voltage reverses polarity.

The capacitors, C_{RT1} and C_{RT2}, reduce the ringing voltage amplitude at the comparator inputs, DT and DR, to be within the maximum allowable voltage range. They also reduce comparator oscillating at the ringing frequency near the threshold. In the balanced ringing case, C_{RT1} and C_{RT2} can be combined into one capacitor of half-value, connected between the DT and DR terminals. For 20Hz ringing, it is suitable to calculate the capacitor(s) for a 50ms time constant (e.g., $t_1 = C_{RT1} \cdot R_{B1} \cdot R_3 / (R_{B1} + R_3)$).

For balanced ringing, R_3 = R4. Select $R_{B1} = R_{B2} = R_3 (R_1 + R_2 + R_{Line}) / R_{Line}$ where R_{Line} is the maximum line resistance to be detected as off-hook.

Detector output

The loop current detector and the ring trip comparator share a common output, $\overline{DET}$ (pin 13). Via control inputs C_1 through C_3, one of the two is selected to be connected to $\overline{DET}$. When input E_0 is set to logic high, the $\overline{DET}$ output is logic low for tripped detector condition and logic high for non-tripped condition. The $\overline{DET}$ output is open collector with built-in pull-up resistor. When E_0 is set to logic low, the $\overline{DET}$ output is disabled, i.e., connected to V_{CC} via the internal pull-up resistor.

Control Inputs

The PBL 3736 SLIC has four TTL-compatible control inputs, C_1 through C_4. A decoder in the SLIC interprets the control input conditions and sets up the commanded operating state. C_1 through C_3 allow for eight operating states. The C_4 logic level determines whether the test relay is energized or not during the selected operating state. The control inputs interface directly with the programmable CODEC/filter devices (e.g. SLAC, Subcriber Line Audio-processing Circuit). Via serial I/O ports on the SLAC, a micro-processor can communicate with all the SLIC-SLAC pairs on a line card. Refer to programmable CODEC/filter device literature for details.

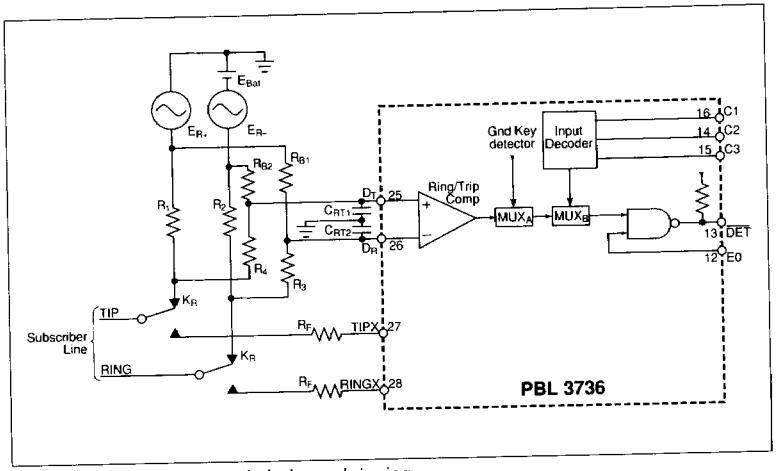


Figure 12. Ring trip network, balanced ringing.

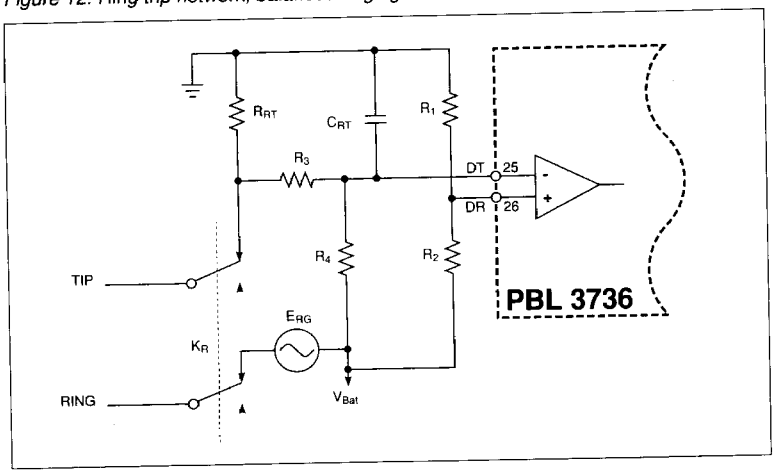


Figure 13. Ring trip network, unbalanced ringing.

Test relay control (C_4)

With C_4 set to logic level low, the test relay driver (TESTRLY) is activated and sourcing up to 25mA from V_{CC}. With C_4 set to logic level high, the test relay driver is switched off. The test relay driver control input C_4 is independent of C_1, C_2 and C_3 logic levels.

Open circuit state (C_3, C_2, C_1 = 0, 0, 0)

In the open circuit state, both the TIPX and RINGX power amplifiers present a high-impedance to the line. The loop current detector is not active in this state.

Ringing state (C_3, C_2, C_1 = 0, 0, 1)

The ring relay driver (RINGRLY) is activated and the ring trip detector is connected to the detector output ($\overline{DET}$). TIPX and RINGX are in the high-impedance state and signal transmission is inhibited.

Normal state (C_3, C_2, C_1 = 0, 1, 0)

TIPX is the terminal closest to ground and sources loop current, while RINGX is the more-negative terminal and sinks loop current. Signal transmission is normal and the loop current detector is gated to the DET output.

Stand-by state (C_3, C_2, C_1 = 0, 1, 1)

The loop current is limited to 1.5 times the loop current detector threshold current. The TIPX and RINGX power amplifiers can still handle 20mA (10mA/wire) longitudinal currents. The loop current detector is connected to the DET output.

TIPX open circuit state (C_3, C_2, C_1 = 1, 0, 0)

The TIPX power amplifier presents a high-impedance to the line, while RINGX sinks a maximum of 35mA to V_{Bat}. The loop current detector is connected to the DET output, but in this state tripping at a RINGX current equal to $750/R_D$.

Reserved state (C_3, C_2, C_1 = 1, 0, 1)

This state is reserved (no function assigned).

Polarity reversal state (C_3, C_2, C_1 = 1, 1, 0)

TIPX and RINGX polarity is reversed from the normal state; RINGX is closest to ground and sources current, while TIPX is the more-negative terminal and sinks current. Transition time from normal state is approximately 15ms. The loop current detector is connected to the DET output. Signal transmission is normal.

Polarity reversal and stand-by state (C_3, C_2, C_1 = 1, 1, 1)

Polarity reversal as described under state C_3, C_2, C_1 = 1, 1, 0 and stand-by as described under state C_3, C_2, C_1 = 0, 1, 1.

Overvoltage Protection

The PBL 3736 SLIC must be protected against overvoltages and power crosses. Refer ot "Maximum ratings," TIPX and RINGX terminals for maximum allowable transient voltages that may be applied to the SLIC. The circuit shown in figure 5 utilizes diodes together with a clamping device to protect against high voltage transients. Diodes D_2 and D_3 clamp positive transients directly to ground. These two diodes are reverse biased by the normal, negative tip and ring operating voltages.

Diodes, D_4 and D_5, clamp negative transients to ground via a device, which is not conducting when exposed to the normal, negative tip and ring operating voltages, but will conduct when exposed to negative transient voltages. This device is necessary since D_4 and D_5 would otherwise be forward biased in the normal operating mode. A zener diode type device (e.g. General Semiconductor Tranzorb) is suitable for lower energy transients and an SCR type device (e.g. RCA Surgector) is suitable for higher energy transients due to its voltage foldback characteristic. In applications requiring protection only against low energy transients, it is acceptable to connect the anodes of D_4 and D_5 directly to the V_{Bat} supply rail, thus eliminating the need for a device to block normal operating voltages. The line resistors, R_F, serve the dual purpose of being non-destructing energy dissipaters, when transients are clamped and of being fuses when the line is exposed to a power cross. Ericsson Components line resistor PBR 5067 is designed for this application.

Printed Circuit Board Lay-out

Care in PCB lay-out is essential for proper PBL 3736 function. The components connecting to the RSN pin (pin 19) should be in close proximity of that pin such that no interference is injected into the RSN terminal. Ground plane surrounding the RSN pin is advisable.

The switching regulator components must be located near the pins to which they connect. It is particularly important that the catch diode and the inductor be connected via the shortest possible trace lengths.

Power-up sequence

The voltage at pin V_{Bat} sets the substrate voltage, which must at all times be kept more negative than the voltage at any other pin to prevent possible latch-up. The correct power-up sequence is ground and V_{Bat}, then other supplies and signal leads.

A diode with a 2A current rating connected with its cathode to V_{EE} and anode to V_{Bat} ensures the presence of the most-negative supply voltage at the V_{Bat} pin, if the V_{Bat} supply voltage should be absent. The V_{Bat} pin should not be applied at a faster rate than corresponds to the time constant formed by a 5.1ohm resistor in series with the V_{Bat} pin and a 0.47µF capacitor from the V_{Bat} pin to ground. This RC network may be shared by several SLICs.

Ordering information

Package	Temp. Range	Part No.
Ceramic DIP	0°C to 70°C	PBL 3736J
LLCC	0°C to 70°C	PBL 3736CC

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