

## Rad-hard 550 MHz low noise operational amplifier

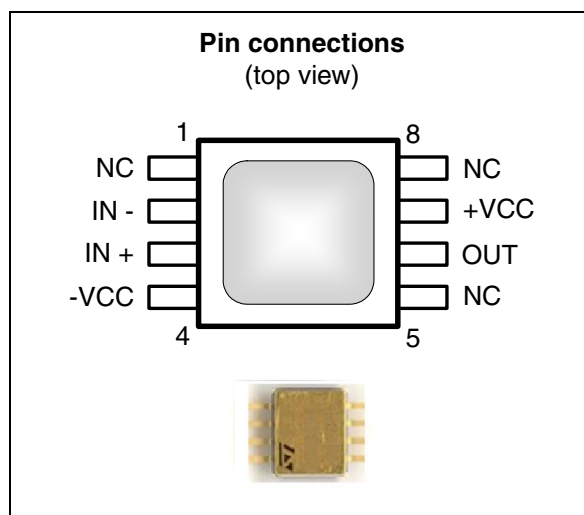
Preliminary data

### Features

- Bandwidth: 550 MHz (unity gain)
- Quiescent current: 4.1 mA
- Slew rate: 940 V/μs
- Input noise: 1.5 nV/√Hz
- Distortion: SFDR = -66 dBc (10 MHz, 1V<sub>pp</sub>)
- 2.8 V<sub>pp</sub> minimum output swing on 100 Ω load for a +5 V supply
- 5 V power supply
- 300 krad MIL-STD-883 1019.7 ELDRS free compliant
- SEL immune at 125° C, LET up to 110 MEV.cm<sup>2</sup>/mg
- SET characterized, LET up to 110 MEV.cm<sup>2</sup>/mg
- QMLV qualified under SMD 5962-0723201
- Mass: 0.45 g

### Applications

- Communication satellites
- Space data acquisition systems
- Aerospace instrumentation
- Nuclear and high energy physics
- Harsh radiation environments
- ADC drivers



### Description

The RHF350 is a current feedback operational amplifier that uses very high speed complementary technology to provide a bandwidth of up to 410 MHz while drawing only 4.1 mA of quiescent current. With a slew rate of 940 V/μs and an output stage optimized for driving a standard 100 Ω load, this circuit is highly suitable for applications where speed and power-saving are the main requirements. The device is a single operator available in a Flat-8 hermetic ceramic package, saving board space as well as providing excellent thermal and dynamic performance.

**Table 1. Device summary**

Order code	SMD pin	Quality level	Package	Lead finish	Marking	EPPL	Packing
RHF350K1	-	Engineering model	Flat-8	Gold	RHF350K1	-	Strip pack
RHF350K-01V	5962F0723201VXC	QMLV-Flight	Flat-8	Gold	5962F0723201VXC	-	

*Note:* Contact your ST sales office for information on the specific conditions for products in QML-Q versions.

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# 1 Absolute maximum ratings and operating conditions

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage <sup>(1)</sup>	6	V
$V_{id}$	Differential input voltage <sup>(2)</sup>	+/-0.5	V
$V_{in}$	Input voltage range <sup>(3)</sup>	+/-2.5	V
$T_{oper}$	Operating free-air temperature range	-40 to + 85	°C
$T_{stg}$	Storage temperature	-65 to +150	°C
$T_j$	Maximum junction temperature	150	°C
$R_{thja}$	Flat-8 thermal resistance junction to ambient	50	°C/W
$R_{thjc}$	Flat-8 thermal resistance junction to case	30	°C/W
$P_{max}$	Flat-8 maximum power dissipation <sup>(4)</sup> ( $T_{amb} = 25^{\circ}C$ ) for $T_j = 150^{\circ}C$	830	mW
ESD	HBM: human body model <sup>(5)</sup> pins 1, 4, 5, 6, 7 and 8 pins 2 and 3	2 0.5	kV
	MM: machine model <sup>(6)</sup> pins 1, 4, 5, 6, 7 and 8 pins 2 and 3	200 60	V
	CDM: charged device model <sup>(7)</sup> pins 1, 4, 5, 6, 7 and 8 pins 2 and 3	1.5 1.5	kV
	Latch-up immunity	200	mA

1. All voltages values are measured with respect to the ground pin.
2. Differential voltage are non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of input and output voltage must never exceed  $V_{CC} + 0.3V$ .
4. Short-circuits can cause excessive heating. Destructive dissipation can result from short-circuits on all amplifiers.
5. Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 k $\Omega$  resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
6. This is a minimum value.  
Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5  $\Omega$ ). This is done for all couples of connected pin combinations while the other pins are floating.
7. Charged device model: all pins and package are charged together to the specified voltage and then discharged directly to the ground through only one pin.

**Table 3. Operating conditions**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage	4.5 to 5.5	V
$V_{icm}$	Common mode input voltage	$-V_{CC} + 1.5V$ to $+V_{CC} - 1.5V$	V

## 2 Electrical characteristics

**Table 4. Electrical characteristics for  $V_{CC} = \pm 2.5$  V, (unless otherwise specified)**

Symbol	Parameter	Test conditions	Temp. (1)	Min.	Typ.	Max.	Unit
DC performance							
V <sub>io</sub>	Input offset voltage		+125°C	TBD		TBD	mV
			+25°C	0.35	0.8	4	
			-55°C	TBD		TBD	
I <sub>ib+</sub>	Non-inverting input bias current		+125°C			TBD	μA
			+25°C		12	35	
			-55°C			TBD	
I <sub>ib-</sub>	Inverting input bias current		+125°C			TBD	μA
			+25°C		1	20	
			-55°C			TBD	
CMR	Common mode rejection ratio 20 log (ΔV <sub>ic</sub> /ΔV <sub>io</sub> )	ΔV <sub>ic</sub> = ±1 V	+125°C	TBD			dB
			+25°C	54	60		
			-55°C	TBD			
SVR	Supply voltage rejection ratio 20 log (ΔV <sub>CC</sub> /ΔV <sub>out</sub> )	ΔV <sub>CC</sub> = 3.5 V to 5 V	+125°C	67			dB
			+25°C	68	81		
			-55°C	67			
PSRR	Power supply rejection ratio 20 log (ΔV <sub>CC</sub> /ΔV <sub>out</sub> )	ΔV <sub>CC</sub> = 200 mV <sub>pp</sub> at 1 kHz	+25°C		51		dB
I <sub>CC</sub>	Supply current	No load	+125°C			TBD	mA
			+25°C		4.1	4.9	
			-55°C			TBD	
Dynamic performance and output characteristics							
R <sub>OL</sub>	Transimpedance	ΔV <sub>out</sub> = ±1 V, R <sub>L</sub> = 1k Ω	+125°C	TBD			kΩ
			+25°C	170	270		
			-55°C	TBD			
Bw	Small signal -3 dB bandwidth	R <sub>L</sub> = 100 Ω, A <sub>V</sub> = +1	+25°C		550		MHz
		R <sub>L</sub> = 100 Ω, A <sub>V</sub> = +2	+25°C		390		
		R <sub>L</sub> = 100 Ω, A <sub>V</sub> = +10	+25°C		125		
		R <sub>L</sub> = 100 Ω, A <sub>V</sub> = -2	+125°C	TBD			
			+25°C	250	370		
			-55°C	TBD			

**Table 4. Electrical characteristics for  $V_{CC} = \pm 2.5$  V, (unless otherwise specified) (continued)**

Symbol	Parameter	Test conditions	Temp. (1)	Min.	Typ.	Max.	Unit
SR	Slew rate	$V_{out} = 2 V_{pp}$ , $A_V = +2$ , $R_L = 100 \Omega$	+25°C		940		V/ $\mu$ s
$V_{OH}$	High level output voltage	$R_L = 100 \Omega$	+125°C	1.5			V
			+25°C	1.55	1.65		
			-55°C	1.5			

1.  $T_{min} < T_{amb} < T_{max}$ : worst case of the parameter on a standard sample across the temperature range. The evaluation is done on 50 units in the SO-8 plastic package.

**Table 5. Closed-loop gain and feedback components**

Gain (V/V)	+ 1	- 1	+ 2	- 2	+ 10	- 10
$R_{fb} (\Omega)$	820	300	300	300	300	300

Figure 1. Frequency response, positive gain      Figure 2. Flatness, gain = +1

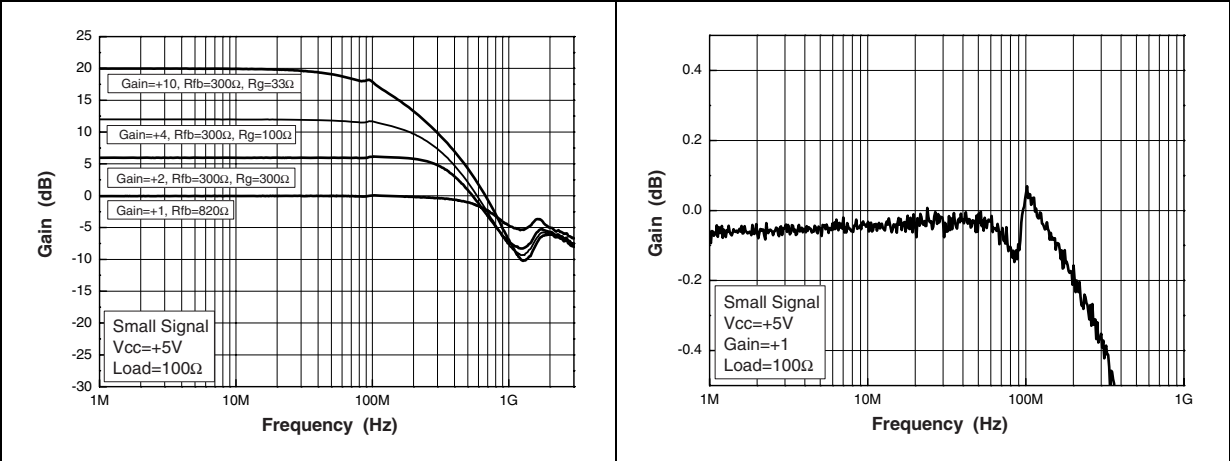


Figure 3. Flatness, gain = +2      Figure 4. Flatness, gain = +4

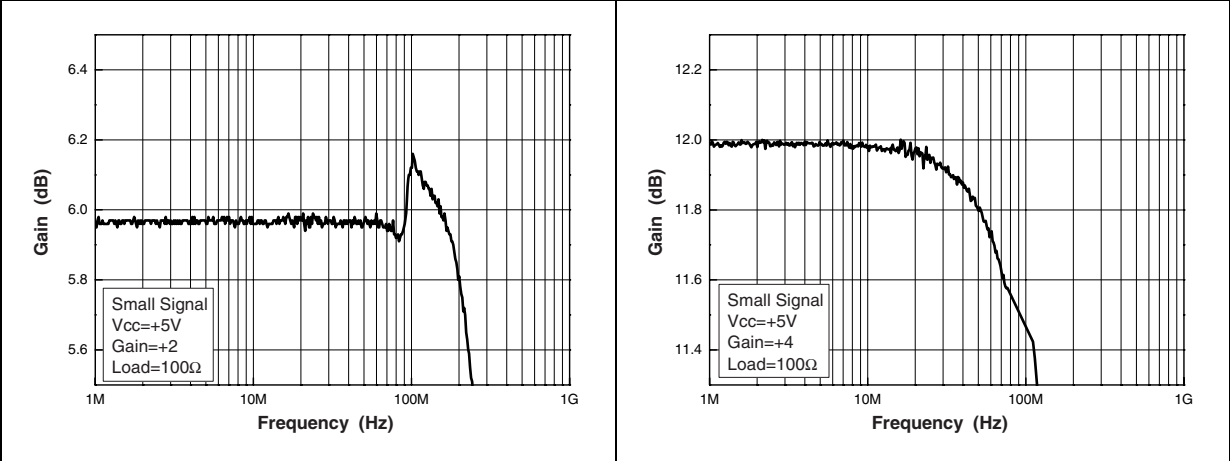


Figure 5. Flatness, gain = +10      Figure 6. Slew rate

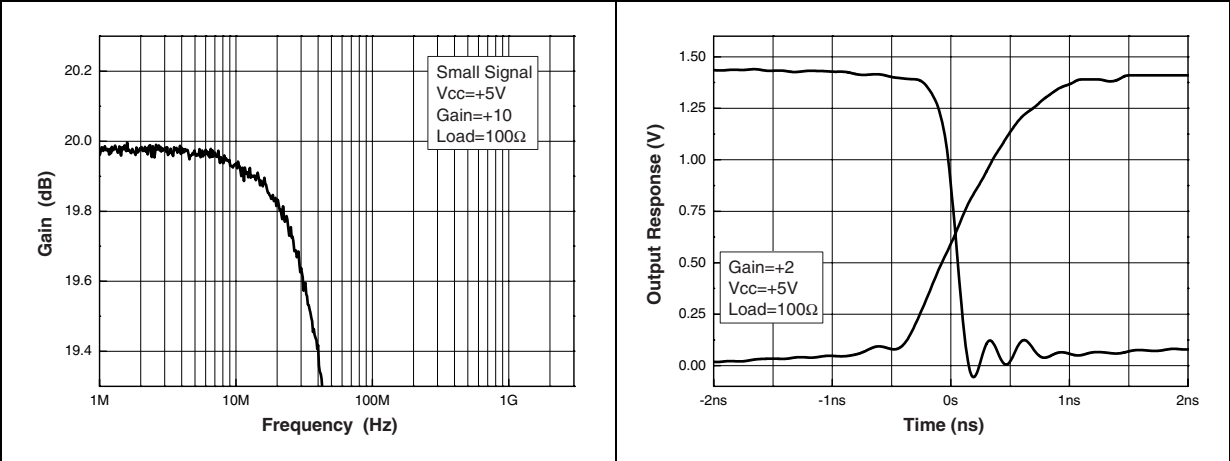


Figure 7.  $I_{\text{sink}}$

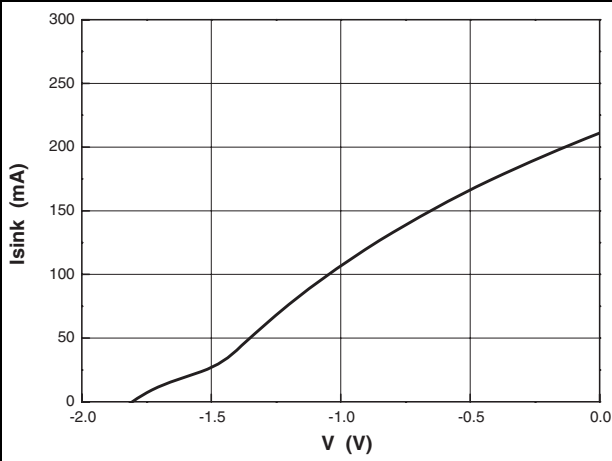


Figure 8.  $I_{\text{source}}$

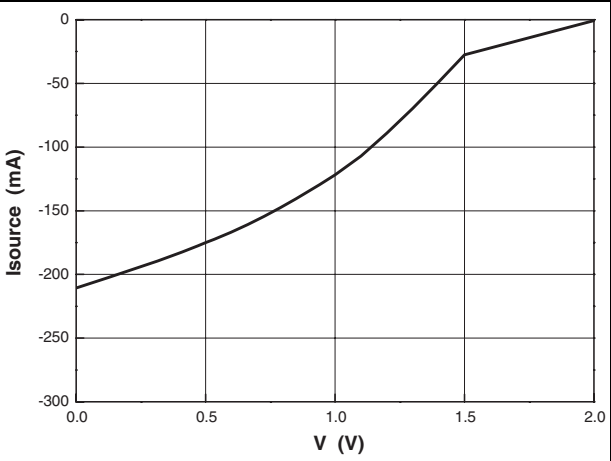


Figure 9. Input current noise vs. frequency

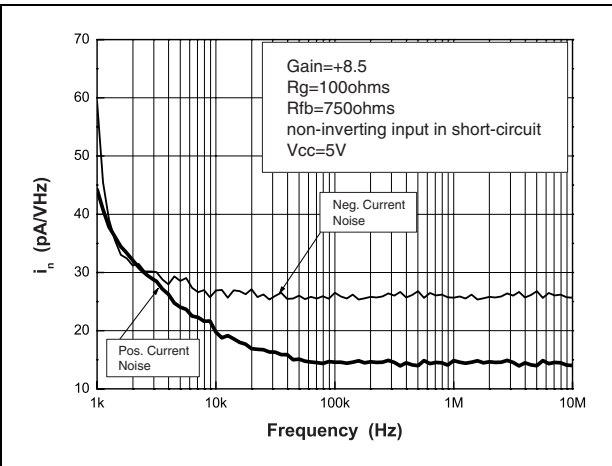


Figure 10. Input voltage noise vs. frequency

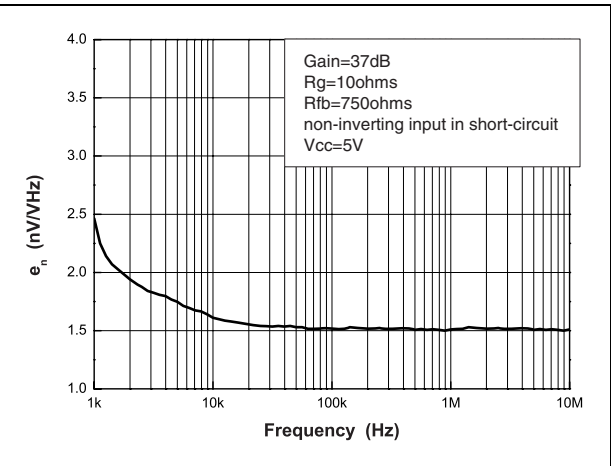


Figure 11. Quiescent current vs.  $V_{CC}$

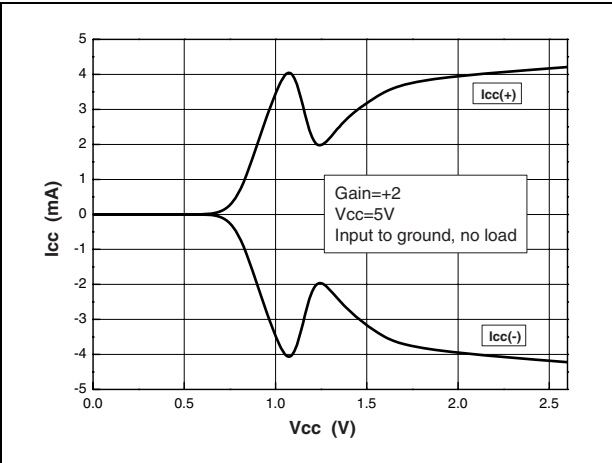


Figure 12. Noise

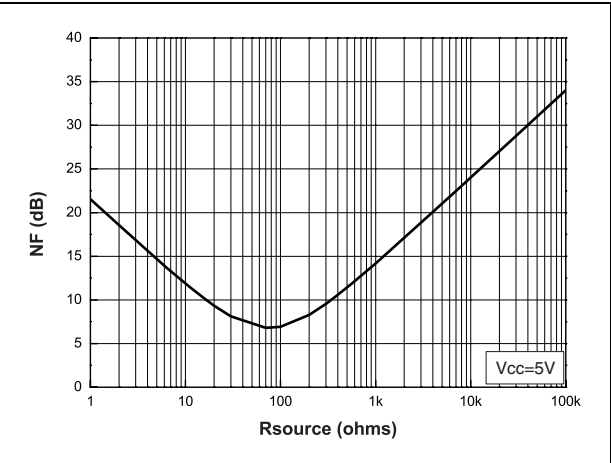


Figure 13. Distortion vs. output amplitude

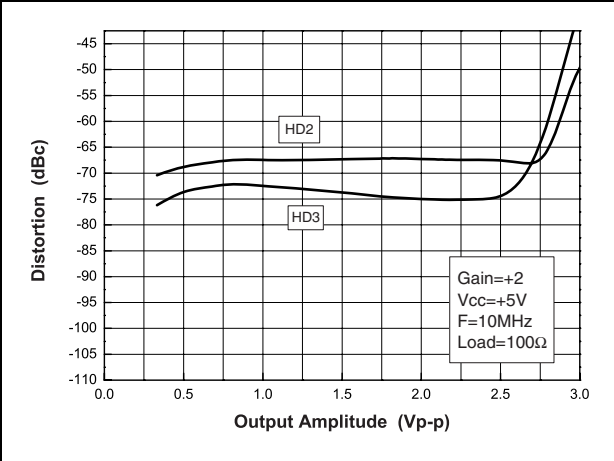


Figure 14. Output amplitude vs. load

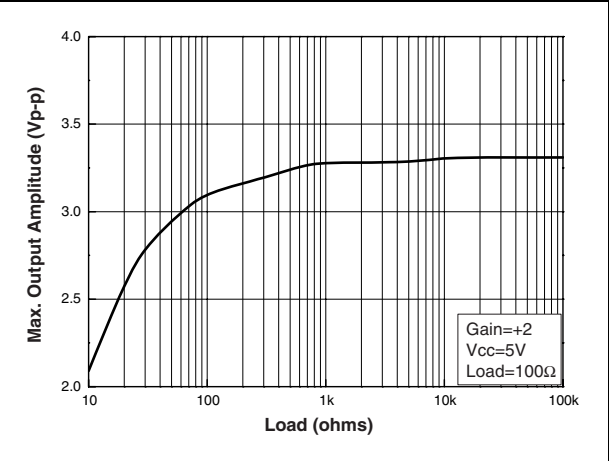


Figure 15. Reverse isolation vs. frequency

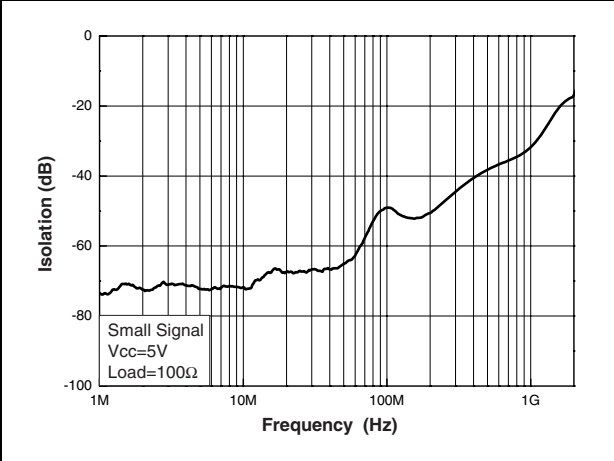


Figure 16. SVR vs. temperature

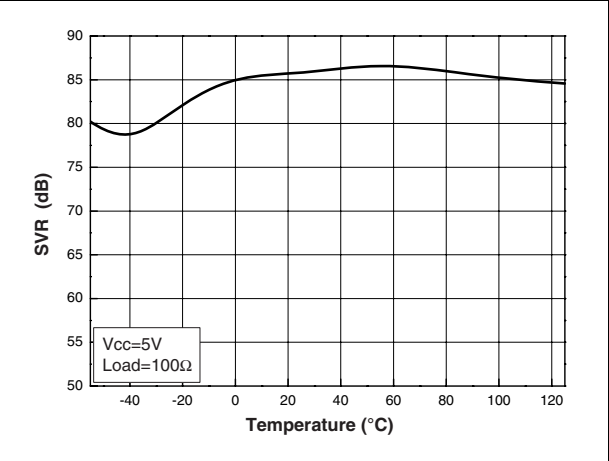


Figure 17.  $I_{out}$  vs. temperature

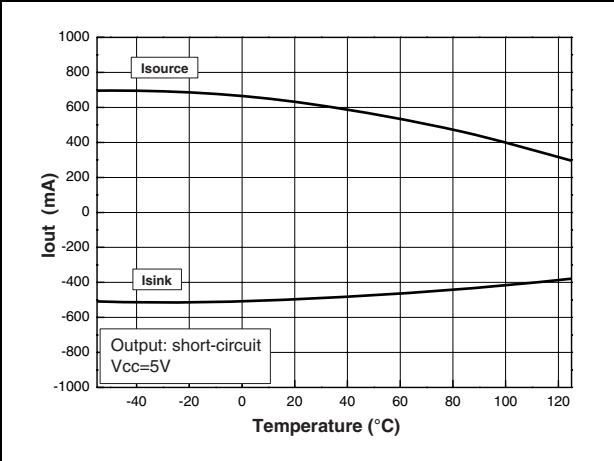


Figure 18.  $R_{OL}$  vs. temperature

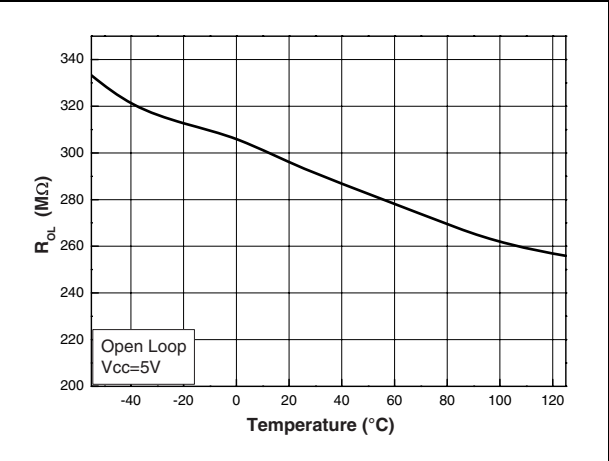




Figure 19. CMR vs. temperature

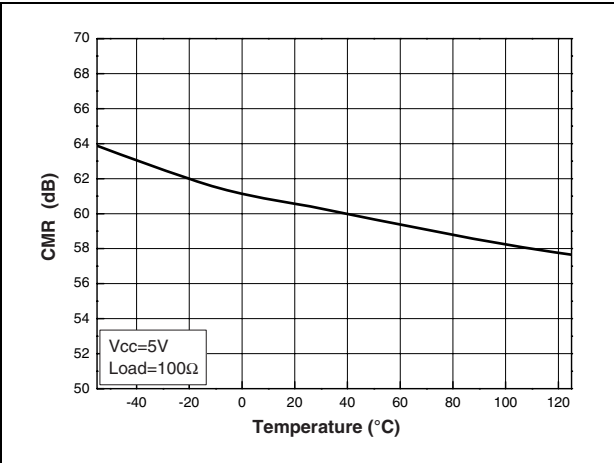


Figure 20.  $I_{bias}$  vs. temperature

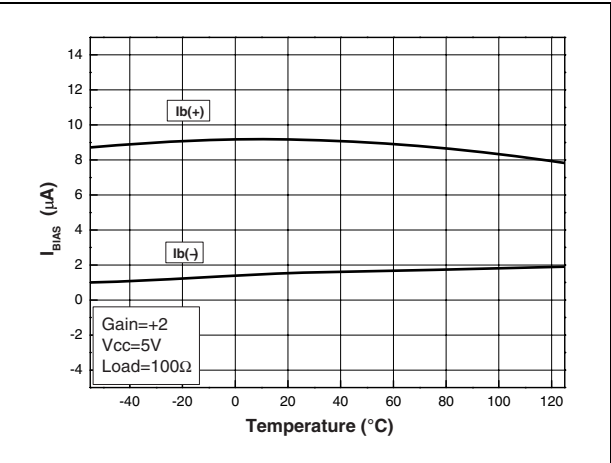


Figure 21.  $V_{io}$  vs. temperature

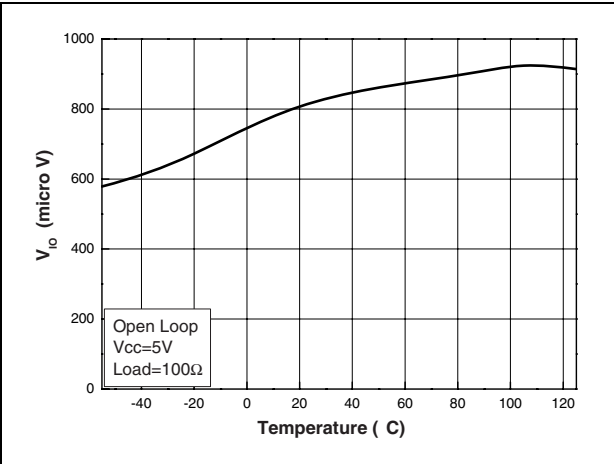


Figure 22.  $V_{OH}$  and  $V_{OL}$  vs. temperature

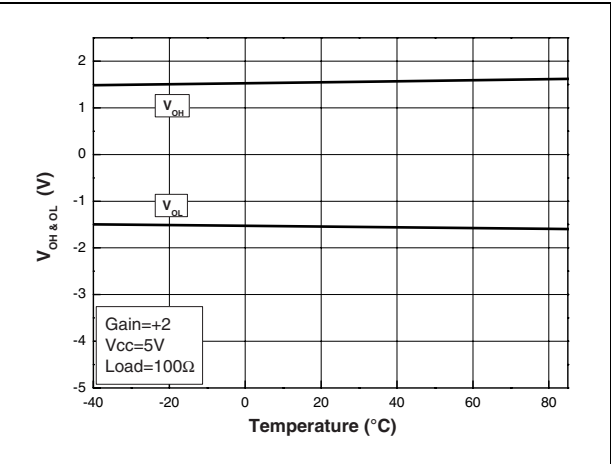
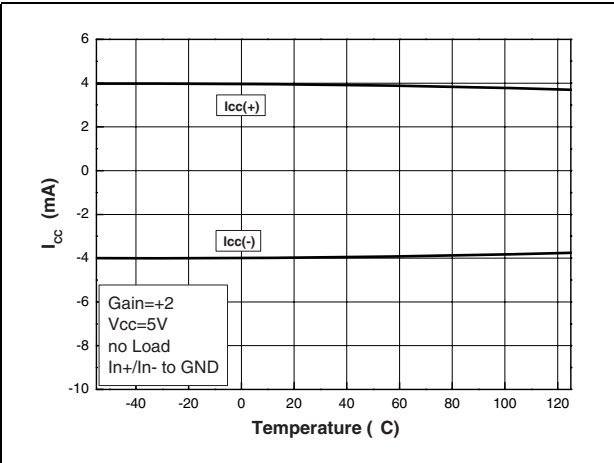


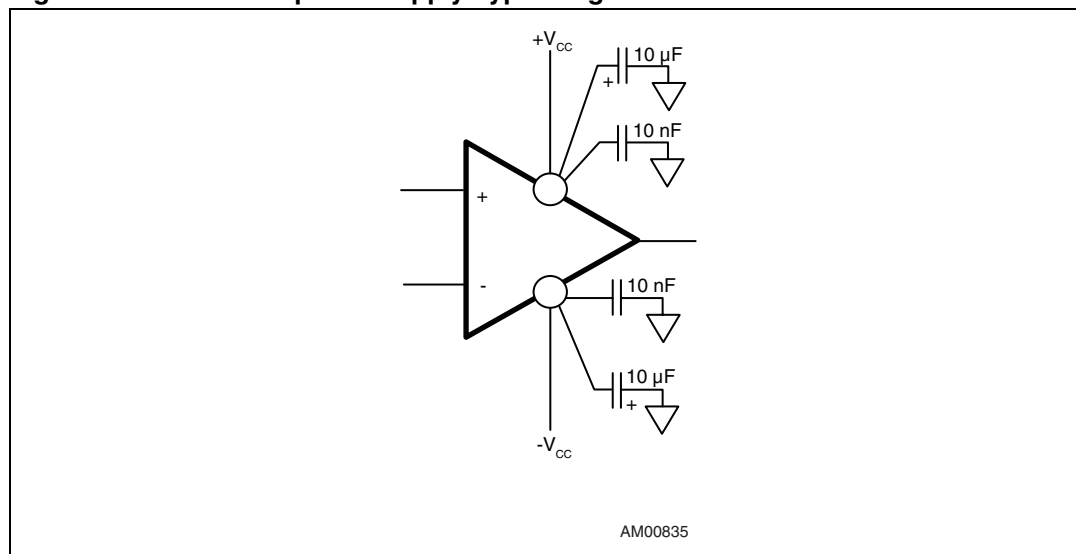
Figure 23.  $I_{CC}$  vs. temperature



### 3 Power supply considerations

Correct power supply bypassing is very important to optimize performance in high-frequency ranges. The bypass capacitors should be placed as close as possible to the IC pins to improve high-frequency bypassing. A capacitor greater than  $1\ \mu\text{F}$  is necessary to minimize the distortion. For better quality bypassing, a  $10\ \text{nF}$  capacitor can be added. It should also be placed as close as possible to the IC pins. The bypass capacitors must be incorporated for both the negative and positive supply.

**Figure 24. Circuit for power supply bypassing**



#### 3.1 Single power supply

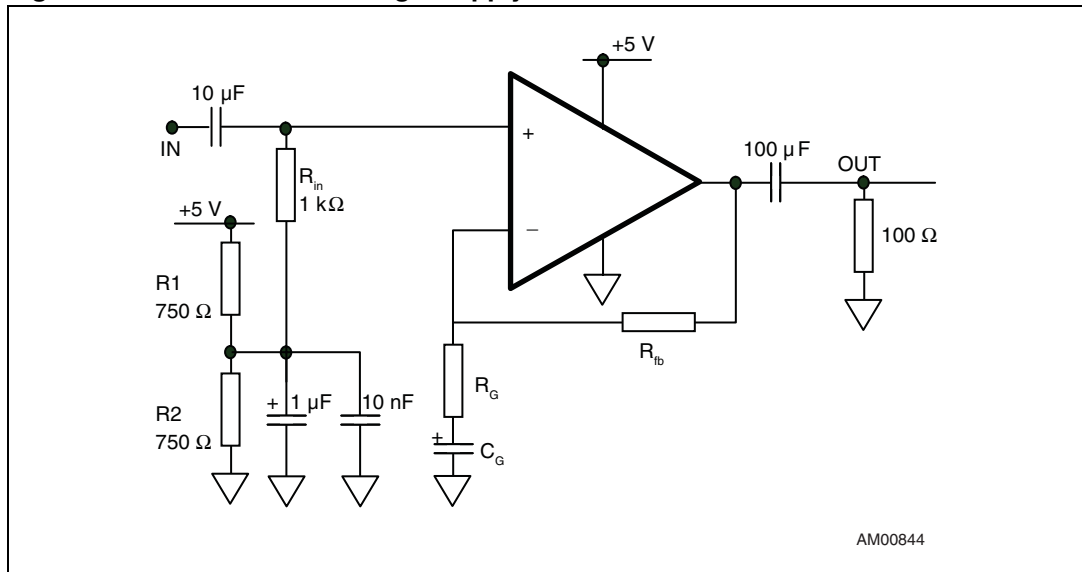
In the event that a single supply system is used, biasing is necessary to obtain a positive output dynamic range between the  $0\ \text{V}$  and  $+V_{\text{CC}}$  supply rails. Considering the values of  $V_{\text{OH}}$  and  $V_{\text{OL}}$ , the amplifier provides an output swing from  $+0.9\ \text{V}$  to  $+4.1\ \text{V}$  on a  $100\ \Omega$  load.

The amplifier must be biased with a mid-supply (nominally  $+V_{\text{CC}}/2$ ), in order to maintain the DC component of the signal at this value. Several options are possible to provide this bias supply, such as a virtual ground using an operational amplifier or a two-resistance divider (which is the cheapest solution). A high resistance value is required to limit the current consumption. On the other hand, the current must be high enough to bias the non-inverting input of the amplifier. If we consider this bias current ( $35\ \mu\text{A}$  maximum) as 1% of the current through the resistance divider, to keep a stable mid-supply two resistances of  $750\ \Omega$  can be used.

The input provides a high-pass filter with a break frequency below  $10\ \text{Hz}$  which is necessary to remove the original  $0\ \text{V}$  DC component of the input signal, and to set it at  $+V_{\text{CC}}/2$ .

*Figure 25 on page 11* illustrates a  $5\ \text{V}$  single power supply configuration. A capacitor  $C_G$  is added to the gain network to ensure a unity gain at low frequencies in order to keep the right DC component at the output.  $C_G$  contributes to a high-pass filter with  $R_{\text{fb}}/R_G$  and its value is calculated with regard to the cut-off frequency of this low-pass filter.

Figure 25. Circuit for +5 V single supply

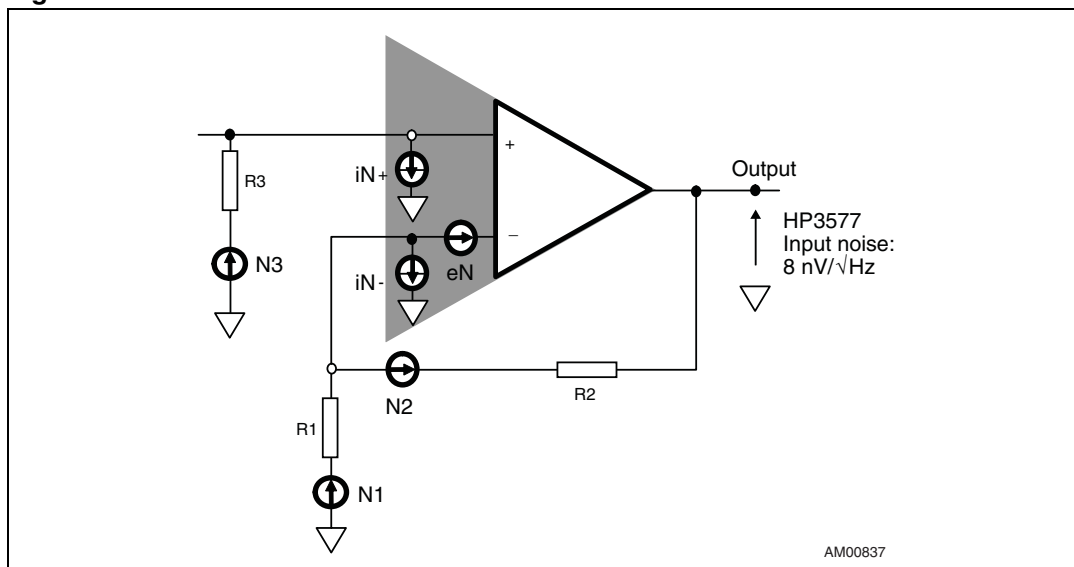


## 4 Noise measurements

The noise model is shown in [Figure 26](#).

- $eN$ : input voltage noise of the amplifier.
- $iNn$ : negative input current noise of the amplifier.
- $iNp$ : positive input current noise of the amplifier.

**Figure 26. Noise model**



The thermal noise of a resistance  $R$  is:

$$\sqrt{4kTR\Delta F}$$

where  $\Delta F$  is the specified bandwidth.

On a 1 Hz bandwidth the thermal noise is reduced to:

$$\sqrt{4kTR}$$

where  $k$  is the Boltzmann's constant, equal to  $1,374.E(-23)J/^{\circ}K$ .  $T$  is the temperature ( $^{\circ}K$ ).

The output noise  $eNo$  is calculated using the superposition theorem. However,  $eNo$  is not the simple sum of all noise sources, but rather the square root of the sum of the square of each noise source, as shown in [Equation 1](#).

### Equation 1

$$eNo = \sqrt{V1^2 + V2^2 + V3^2 + V4^2 + V5^2 + V6^2}$$

**Equation 2**

$$eNo^2 = eN^2 \times g^2 + iNn^2 \times R2^2 + iNp^2 \times R3^2 \times g^2 + \frac{R2^2}{R1} \times 4kTR1 + 4kTR2 + 1 + \frac{R2^2}{R1} \times 4kTR3$$

The input noise of the instrumentation must be extracted from the measured noise value.  
The real output noise value of the driver is:

**Equation 3**

$$eNo = \sqrt{(\text{Measured})^2 - (\text{instrumentation})^2}$$

The input noise is called **equivalent input noise** because it is not directly measured but is evaluated from the measurement of the output divided by the closed loop gain ( $eNo/g$ ).

After simplification of the fourth and the fifth term of [Equation 2](#) we obtain:

**Equation 4**

$$eNo^2 = eN^2 \times g^2 + iNn^2 \times R2^2 + iNp^2 \times R3^2 \times g^2 + g \times 4kTR2 + 1 + \frac{R2^2}{R1} \times 4kTR3$$

## 4.1 Measurement of the input voltage noise $eN$

If we assume a short-circuit on the non-inverting input ( $R3=0$ ), from [Equation 4](#) we can derive:

**Equation 5**

$$eNo = \sqrt{eN^2 \times g^2 + iNn^2 \times R2^2 + g \times 4kTR2}$$

In order to easily extract the value of  $eN$ , the resistance  $R2$  will be chosen to be as low as possible. On the other hand, the gain must be large enough.

$R3=0$ , gain:  $g=100$

## 4.2 Measurement of the negative input current noise $iNn$

To measure the negative input current noise  $iNn$ , we set  $R3=0$  and use [Equation 5](#). This time, the gain must be lower in order to decrease the thermal noise contribution.

$R3=0$ , gain:  $g=10$

## 4.3 Measurement of the positive input current noise $iNp$

To extract  $iNp$  from [Equation 3](#), a resistance  $R3$  is connected to the non-inverting input. The value of  $R3$  must be chosen in order to keep its thermal noise contribution as low as possible against the  $iNp$  contribution.

$R3=100 \text{ W}$ , gain:  $g=10$

## 5 Intermodulation distortion product

The non-ideal output of the amplifier can be described by the following series of equations.

$$V_{out} = C_0 + C_1 V_{in} + C_2 V_{in}^2 + \dots + C_n V_{in}^n$$

Where the input is  $V_{in} = A \sin \omega t$ ,  $C_0$  is the DC component,  $C_1(V_{in})$  is the fundamental and  $C_n$  is the amplitude of the harmonics of the output signal  $V_{out}$ .

A one-frequency (one-tone) input signal contributes to harmonic distortion. A two-tone input signal contributes to harmonic distortion and to the intermodulation product.

The study of the intermodulation and distortion for a two-tone input signal is the first step in characterizing the driving capability of multi-tone input signals.

In this case:

$$V_{in} = A \sin \omega_1 t + A \sin \omega_2 t$$

then:

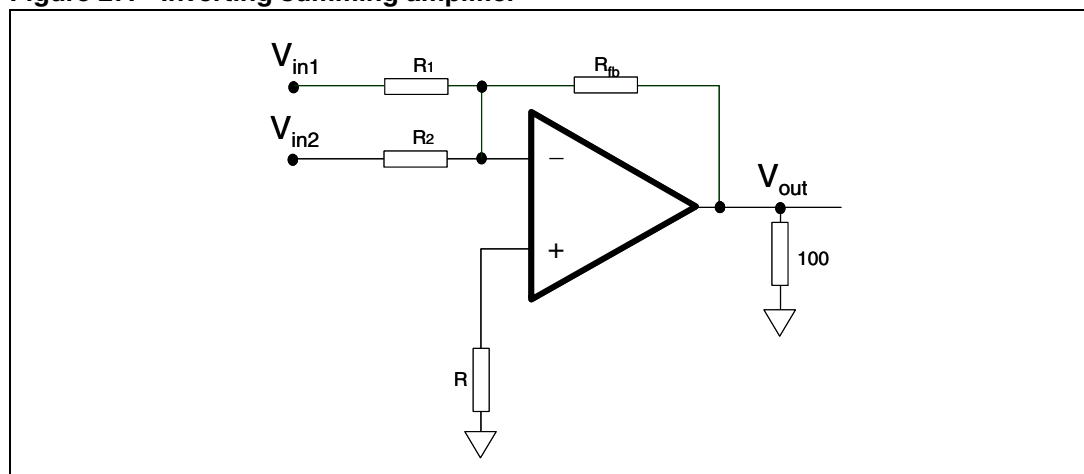
$$V_{out} = C_0 + C_1 (A \sin \omega_1 t + A \sin \omega_2 t) + C_2 (A \sin \omega_1 t + A \sin \omega_2 t)^2 + \dots + C_n (A \sin \omega_1 t + A \sin \omega_2 t)^n$$

From this expression, we can extract the distortion terms, and the intermodulation terms from a single sine wave.

- Second-order intermodulation terms IM2 by the frequencies  $(\omega_1 - \omega_2)$  and  $(\omega_1 + \omega_2)$  with an amplitude of  $C_2 A^2$ .
- Third-order intermodulation terms IM3 by the frequencies  $(2\omega_1 - \omega_2)$ ,  $(2\omega_1 + \omega_2)$ ,  $(-\omega_1 + 2\omega_2)$  and  $(\omega_1 - 2\omega_2)$  with an amplitude of  $(3/4)C_3 A^3$ .

The intermodulation product of the driver is measured by using the driver as a mixer in a summing amplifier configuration ([Figure 27](#)). In this way, the non-linearity problem of an external mixing device is avoided.

**Figure 27. Inverting summing amplifier**



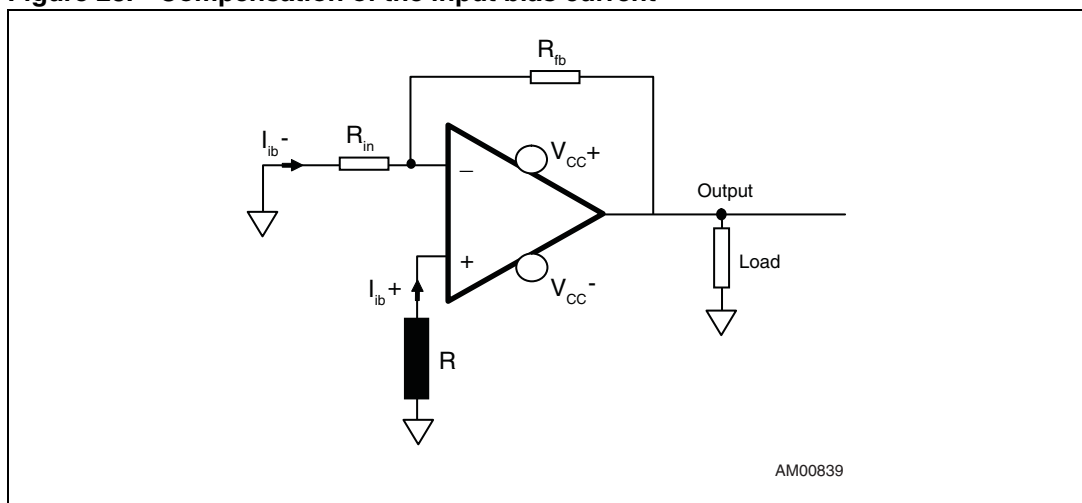
## 6 Inverting amplifier biasing

A resistance is necessary to achieve good input biasing, such as resistance R shown in [Figure 28](#).

The value of this resistance is calculated from the negative and positive input bias current. The aim is to compensate for the offset bias current, which can affect the input offset voltage and the output DC component. Assuming  $I_{ib-}$ ,  $I_{ib+}$ ,  $R_{in}$ ,  $R_{fb}$  and a 0 V output, the resistance R is:

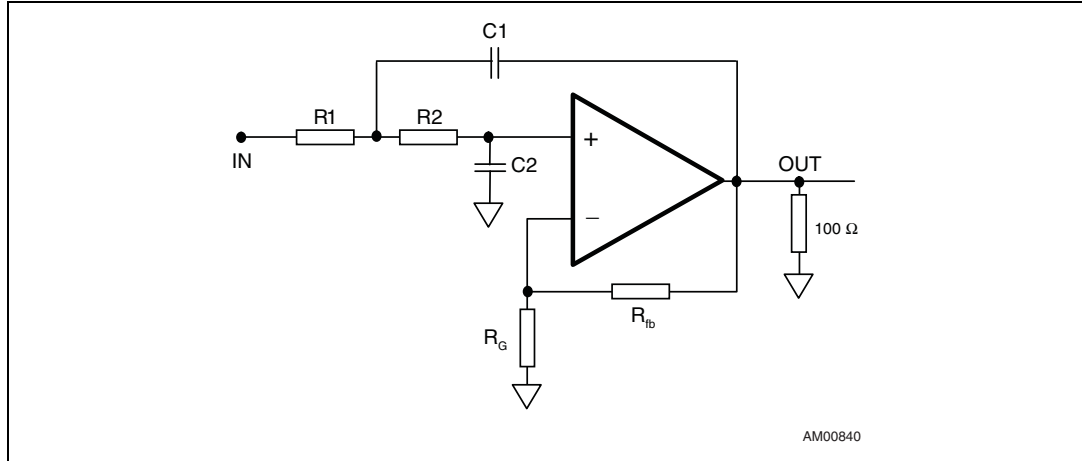
$$R = \frac{R_{in} \times R_{fb}}{R_{in} + R_{fb}}$$

**Figure 28. Compensation of the input bias current**



## 7 Active filtering

Figure 29. Low-pass active filtering, Sallen-Key



From the resistors  $R_{fb}$  and  $R_G$  we can directly calculate the gain of the filter in a classic non-inverting amplification configuration.

$$A_V = g = 1 + \frac{R_{fb}}{R_g}$$

We assume the following expression is the response of the system.

$$T_{j\omega} = \frac{V_{out_{j\omega}}}{V_{in_{j\omega}}} = \frac{g}{1 + 2\zeta \frac{j\omega}{\omega_t} + \frac{(j\omega)^2}{\omega_t^2}}$$

The cut-off frequency is not gain-dependent and so becomes:

$$\omega_t = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

The damping factor is calculated by the following expression.

$$\zeta = \frac{1}{2} \omega_t (C_1 R_1 + C_1 R_2 + C_2 R_1 - C_1 R_1 g)$$

The higher the gain, the more sensitive the damping factor is. When the gain is higher than 1, it is preferable to use very stable resistor and capacitor values. In the case of  $R_1 = R_2 = R$ :

$$\zeta = \frac{2C_2 - C_1 \frac{R_{fb}}{R_g}}{2\sqrt{C_1 C_2}}$$

Due to a limited selection of capacitor values in comparison with resistor values, we can set  $C_1 = C_2 = C$ , so that:

$$\zeta = \frac{2R_2 - R_1 \frac{R_{fb}}{R_g}}{2\sqrt{R_1 R_2}}$$



## 8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

## 8.1 Ceramic Flat-8 package information

Figure 30. Ceramic Flat-8 package mechanical drawing

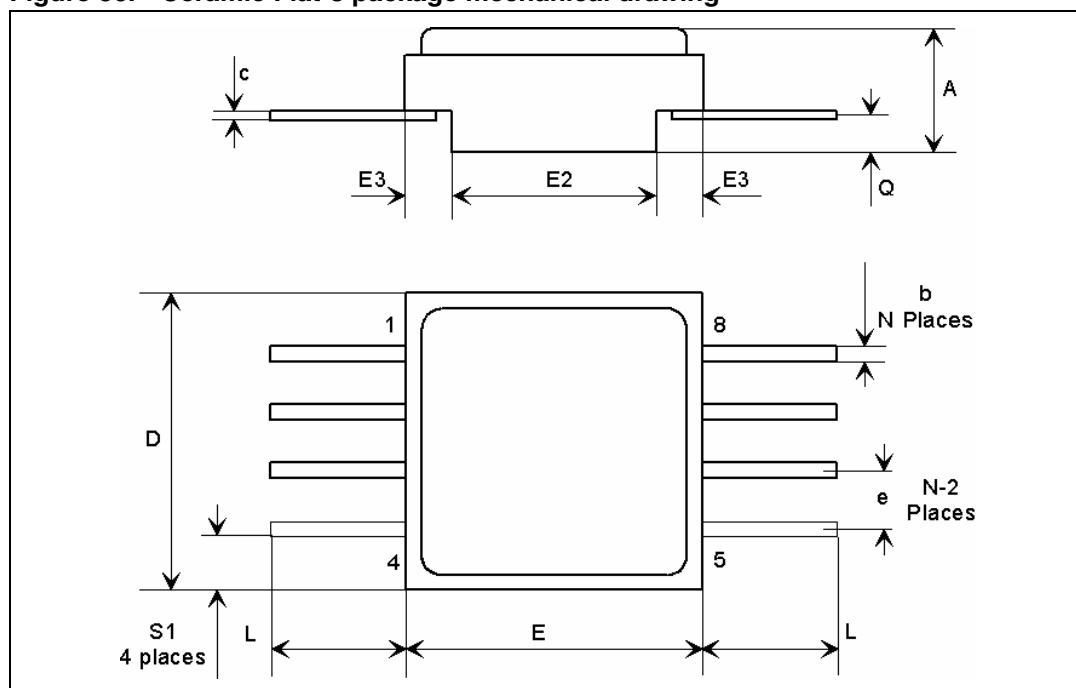


Table 6. Ceramic Flat-8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.24	2.44	2.64	0.088	0.096	0.104
b	0.38	0.43	0.48	0.015	0.017	0.019
c	0.10	0.13	0.16	0.004	0.005	0.006
D	6.35	6.48	6.61	0.250	0.255	0.260
E	6.35	6.48	6.61	0.250	0.255	0.260
E2	4.32	4.45	4.58	0.170	0.175	0.180
E3	0.88	1.01	1.14	0.035	0.040	0.045
e		1.27			0.050	
L		3.00			0.118	
Q	0.66	0.79	0.92	0.026	0.031	0.092
S1	0.92	1.12	1.32	0.036	0.044	0.052
N	08			08		

## 9 Revision history

**Table 7. Document revision history**

Date	Revision	Changes
20-May-2009	1	Initial release.
12-Jul-2010	2	Added <i>Mass</i> in <a href="#">Features</a> on cover page. Added <a href="#">Table 1: Device summary</a> on cover page, with full ordering information. Changed temperature limits in <a href="#">Table 4</a> .

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