2-WIRE CMOS SERIAL E^{2}PROM S-24C01B/02B/04B

The S-24C01B/02B/04B is a 2-wired, low power and wide range operation 1k bit, 2k bit, 4k bit E^{2}PROM organized as 128 words × 8 bits, 256 words × 8 bits, and 512 words × 8 bits in each.
Page write and sequential read are available.

■ Features

- Low power consumption Standby : 1.0 μA Max. (V_{CC}=5.5 V)
  Oprating : 0.8 mA Max. (V_{CC}=5.5 V)
  0.3 mA Max. (Vcc=3.3 V)
- Wide operating voltage range : 2.0 to 5.5
- Page write : 8 bytes / page (S-24C01B/02B)
  16 bytes / page (S-24C04B)
- Sequential read
- Operating Frequency : 400 kHz (V_{CC}=5 V±10 %)
- Endurance : 10^6 cycles/word
- Data retention : 10 years
- Write protection S-24C01B : 100%
  S-24C02B/04B : 50%
- S-24C01B : 1k bit
- S-24C02B : 2k bit
- S-24C04B : 4k bit

■ Package

Package name	Drawing code		
	Package	Tape	Reel
8-Pin DIP	DP008-A	–	–
	DP008-C	–	–
	DP008-E	–	–
8-Pin SOP(JEDEC)	FJ008-A	FJ008-D	FJ008-D
	FJ008-A	FJ008-E	FJ008-E
8-Pin MSOP	FN008-A	FN008-A	FN008-A

Remark For details, please refer to **"Product Code Structure"**.

Caution This product is intended to use in general electronic devices such as consumer electronics, office equipment, and communications devices. Before using the product in medical equipment or automobile equipment including car audio, keyless entry and engine control unit, contact to SII is indispensable.

■ Pin Assignment

8-Pin DIP
Top view

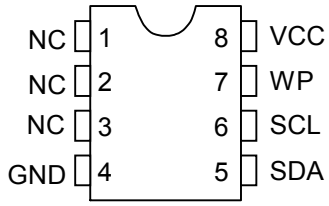


Figure 1

S-24C01BDP
S-24C02BDP
S-24C04BDP

Table 1

Pin Number	Pin Name	Function
1	NC	No Connection*1
2	NC	No Connection*1
3	NC	No Connection*1
4	GND	Ground
5	SDA	Serial data input/output
6	SCL	Serial clock input
7	WP	Write Protection pin Connected to Vcc: Protection valid Connected to GND: Protection invalid
8	VCC	Power supply

∗**1.** Connect to GND or Vcc.

Remark See Dimensions for details of the package drawings.

8-Pin SOP(JEDEC)
Top view

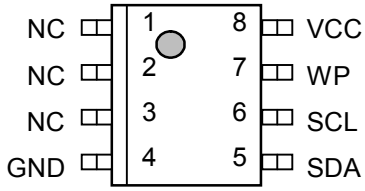


Figure 2

S-24C01BFJ
S-24C02BFJ
S-24C04BFJ

Table 2

Pin Number	Pin Name	Function
1	NC	No Connection*1
2	NC	No Connection*1
3	NC	No Connection*1
4	GND	Ground
5	SDA	Serial data input/output
6	SCL	Serial clock input
7	WP	Write Protection pin Connected to Vcc: Protection valid Connected to GND: Protection invalid
8	VCC	Power supply

∗**1.** Connect to GND or Vcc.

Remark See Dimensions for details of the package drawings.

8-Pin MSOP
Top view

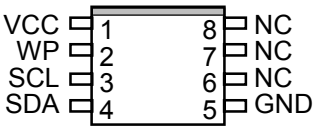


Figure 3

S-24C01BMFN
S-24C02BMFN
S-24C04BMFN

Table 3

Pin Number	Name	Function
8	NC	No Connection*1
7	NC	No Connection*1
6	NC	No Connection*1
5	GND	Ground
4	SDA	Serial data input/output
3	SCL	Serial clock input
2	WP	Write Protection pin Connected to Vcc: Protection valid Connected to GND: Protection invalid
1	VCC	Power supply

∗**1.** Connect to GND or Vcc.

Remark See Dimensions for details of the package drawings.

■ Block Diagram

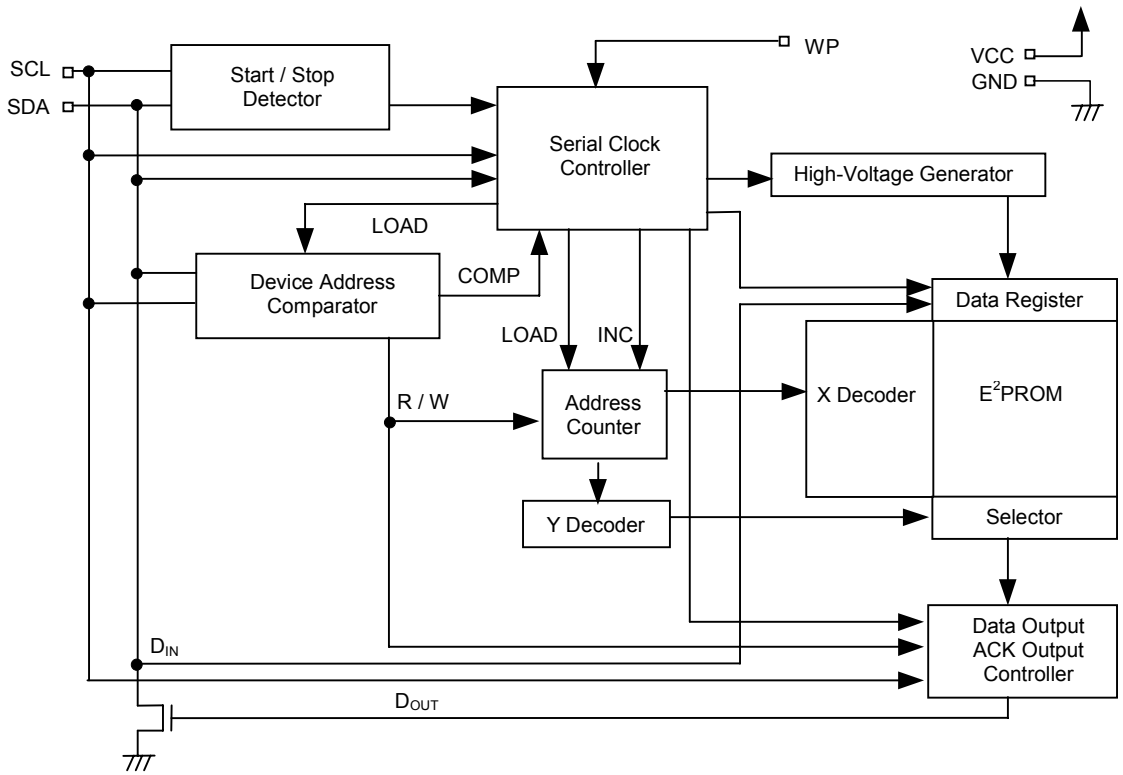


Figure 4

■ Absolute Maximum Ratings

Table 4

Parameter	Symbol	Ratings	Unit
Power supply voltage	V_{CC}	−0.3 to +7.0	V
Input voltage	V_{IN}	−0.3 to V_{CC}+0.3	
Output voltage	V_{OUT}	−0.3 to V_{CC}	
Storage temperature	T_{stg}	−65 to +150	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any condition.

■ Recommended Operating Conditions

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage	V_{CC}	−	2.0	−	5.5	V
High level input voltage	V_{IH}	V_{CC}=2.5 to 5.5 V	0.7×V_{CC}	−	V_{CC}	
		V_{CC}=2.0 to 2.5 V	0.8×V_{CC}	−	V_{CC}	
Low level input voltage	V_{IL}	V_{CC}=2.5 to 5.5 V	0.0	−	0.3×V_{CC}	
		V_{CC}=2.0 to 2.5 V	0.0	−	0.2×V_{CC}	
Operating temperature	T_{opr}	−	−40	−	+85	°C

■ Pin Capacitance

Table 6

(Ta=25 °C, f=1.0 MHz, Vcc=5 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	V_{IN}=0 V (SCL, WP)	−	−	10	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$=0 V (SDA)	−	−	10	pF

■ Endurance

Table 7

Parameter	Symbol	Operating temperatrue	Min.	Typ.	Max.	Unit
Endurance	N_W	−40 to +85 °C	10^6	−	−	cycles/word

■ DC Electrical Characteristics

Table 8

Parameter	Symbol	Conditions	Vcc=4.5 to 5.5 V			V_{CC}=2.5 to 4.5 V			V_{CC}=2.0 to 2.5 V			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Current consumption (READ)	I_{CC1}	–	–	–	0.8	–	–	0.3	–	–	0.2	mA
Current consumption (PROGRAM)	I_{CC2}	–	–	–	4.0	–	–	1.5	–	–	1.5	mA

Table 9

Parameter	Symbol	Conditions	V_{CC}=4.5 to 5.5 V			V_{CC}=2.5 to 4.5 V			V_{CC}=2.0 to 2.5 V			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Standby current consumption	I_{SB}	V_{IN}=V_{CC} or GND	–	–	1.0	–	–	0.6	–	–	0.4	μA
Input leakage current	I_{LI}	V_{IN}=GND to V_{CC}	–	0.1	1.0	–	0.1	1.0	–	0.1	1.0	μA
Output leakage current	I_{LO}	V_{OUT}=GND to V_{CC}	–	0.1	1.0	–	0.1	1.0	–	0.1	1.0	μA
Low level output voltage	V_{OL}	I_{OL}=3.2 mA	–	–	0.4	–	–	0.4	–	–	–	V
		I_{OL}=1.5 mA	–	–	0.3	–	–	0.3	–	–	0.5	V
Current address hold voltage	V_{AH}	–	1.5	–	5.5	1.5	–	4.5	1.5	–	2.5	V

■ AC Electrical Characteristics

Table 10 Measurement Conditions

Input pulse voltage	$0.1\times V_{CC}$ to $0.9\times V_{CC}$
Input pulse rising/falling time	20 ns
Output judgment voltage	$0.5\times V_{CC}$
Output load	100 pF+ Pullup resistance 1.0 kΩ

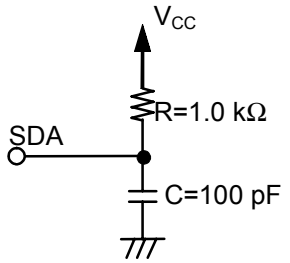


Figure 5 Output Load Circuit

Table 11

Parameter	Symbol	V_{CC}=4.5 to 5.5 V			V_{CC}=2.0 to 4.5 V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	0	–	400	0	–	100	kHz
SCL clock time "L"	t_{LOW}	1.0	–	–	4.7	–	–	µs
SCL clock time "H"	t_{HIGH}	0.9	–	–	4.0	–	–	µs
SDA output delay time	t_{AA}	0.1	–	0.9	0.1	–	3.5	µs
SDA output hold time	t_{DH}	50	–	–	100	–	–	ns
Start condition setup time	$t_{SU.STA}$	0.6	–	–	4.7	–	–	µs
Start condition hold time	$t_{HD.STA}$	0.6	–	–	4.0	–	–	µs
Data input setup time	$t_{SU.DAT}$	100	–	–	200	–	–	ns
Data input hold time	$t_{HD.DAT}$	0	–	–	0	–	–	ns
Stop condition setup time	$t_{SU.STO}$	0.6	–	–	4.7	–	–	µs
SCL • SDA rising time	t_R	–	–	0.3	–	–	1.0	µs
SCL • SDA falling time	t_F	–	–	0.3	–	–	0.3	µs
Bus release time	t_{BUF}	1.3	–	–	4.7	–	–	µs
Noise suppression time	t_I	–	–	50	–	–	100	ns

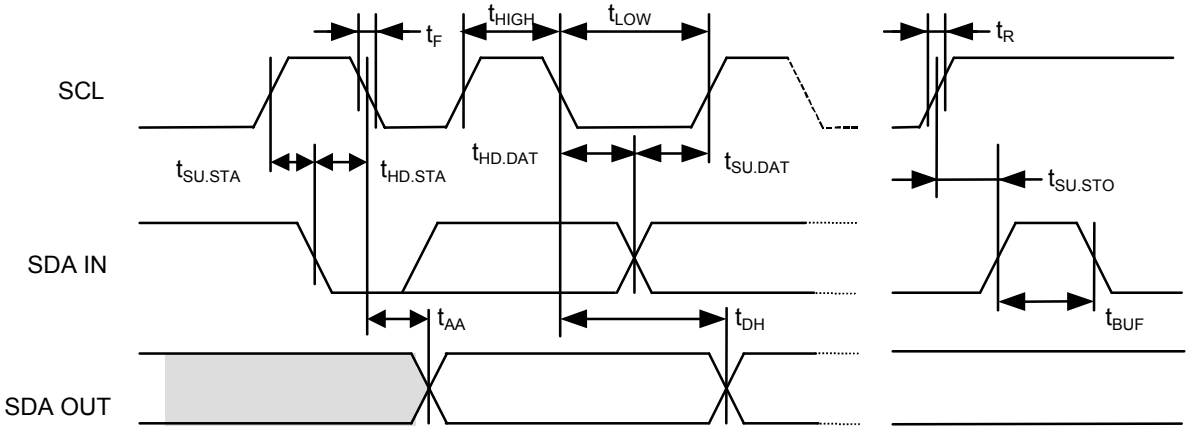


Figure 6 Bus Timing

Table 12

Item	Symbol	Min.	Typ.	Max.	Unit
Write time	t_{WR}	—	4.0	10.0	ms

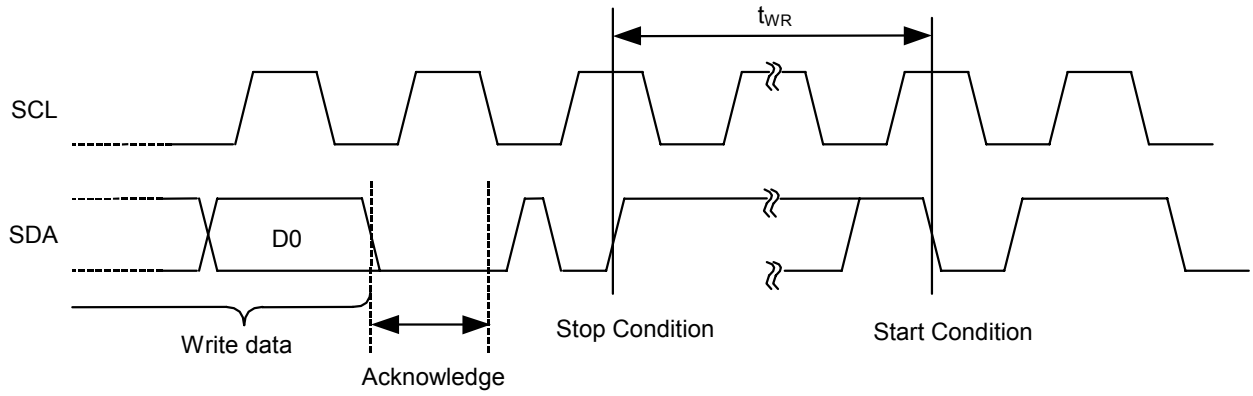


Figure 7 Write Cycle Timing

■ Pin Functions

1. SDA (Serial Data Input/Output) Pin

The SDA pin is used for bilateral transmission of serial data. It consists of a signal input pin and an Nch open-drain transistor output pin.
Usually pull up the SDA line via resistance to the V_{CC}, and use it with other open-drain or open-collector output devices connected in a wired OR configuration.

2. SCL (Serial Clock Input) Pin

The SCL pin is used for serial clock input. It is capable of processing signals at the rising and falling edges of the SCL clock input signal. Make sure the rising time and falling time conform to the specifications.

3. WP Pin

The WP pin is used for write protection. When there is no need for write protection, connect the pin to the GND; when there is a need for write protection, connect the pin to the Vcc.

Remark Please refer to the Application Note "**TIPS,TRICKS AND TRAPS WHEN USING THE S-24C/24CS SERIES**" for equivalent circuit of each pin.

■ Operation

1. Start Condition

When the SCL line is “H” the SDA line changes from “H” to “L”. This allows the device to go to the start condition.
All operations begin from the start condition.

2. Stop Condition

When the SCL line is “H” the SDA line changes from “L” to “H”. This allows the device to go to the stop condition.
When the device receives the stop condition signal during a read sequence, the read operation is interrupted, and the device goes to standby mode.
When the device receives the stop condition signal during write sequence, the retrieval of write data is halted, and the E^{2}PROM initiates rewrite.

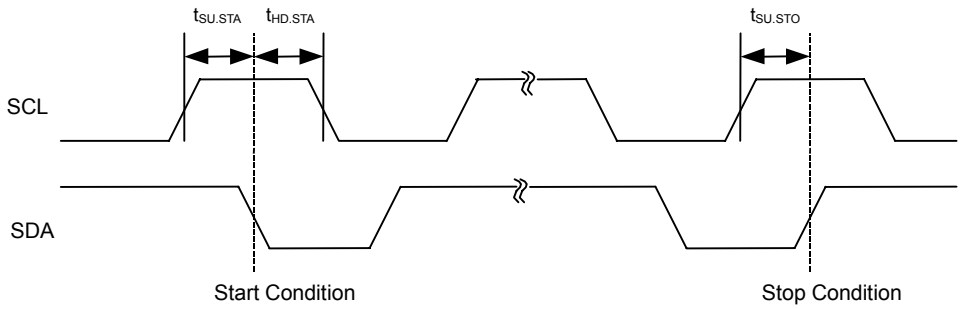


Figure 8 Start/Stop Condition

3. Data Transmission

Changing the SDA line while the SCL line is “L” allows the data to be transmitted. A start or stop condition is recognized when the SDA line changes while the SCL line is “H”.

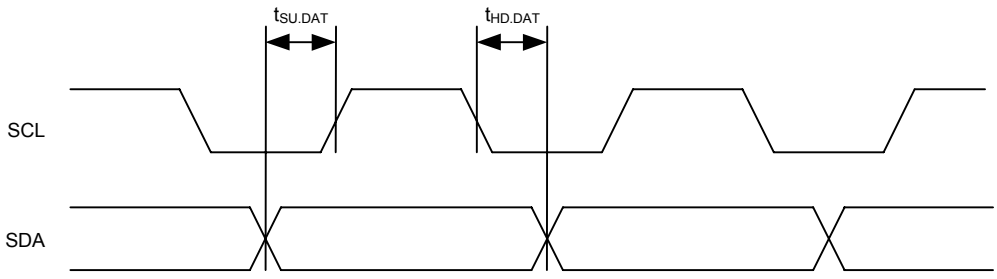


Figure 9 Data Transmission Timing

4. Acknowledgment

The unit of data transmission is 8 bits. By turning the SDA line “L” the slave device mounted on the system bus which receives the data during the 9th clock cycle outputs the acknowledgment signal verifying the data reception. When the E^{2}PROM is rewriting, the device does not output the acknowledgment signal.

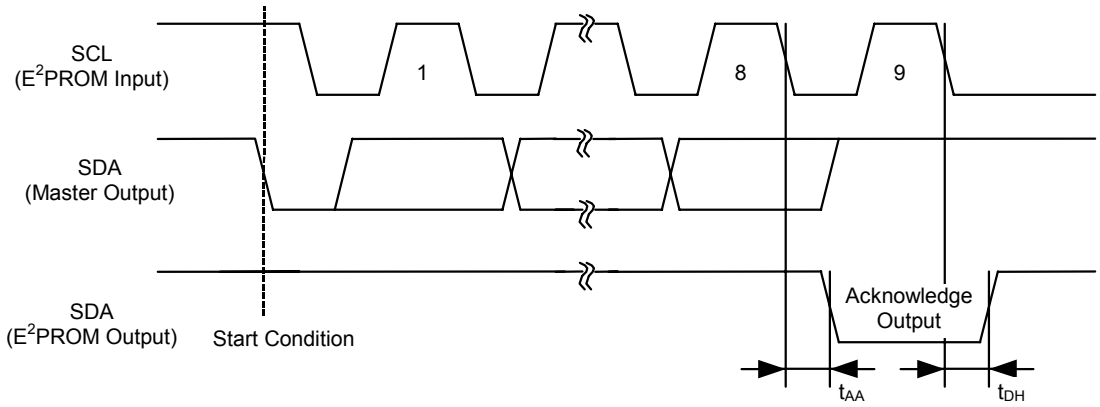


Figure 10 Acknowledge Output Timing

5. Device Addressing

To perform data communications, the master device mounted on the system outputs the start condition signal to the slave device. Next, the master device outputs 7-bit length device address and a 1-bit length read/write instruction code onto the SDA bus.
Upper 4 bits of the device address are called the “Device Code”, and set to “1010”. Successive 3 bits are “don’t care” bits.
When the comparison results match, the slave device outputs the acknowledgment signal during the 9th clock cycle.

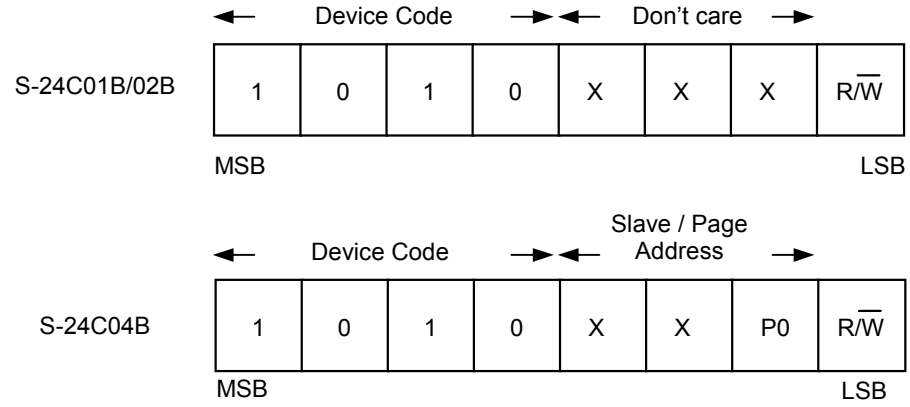


Figure 11 Device Address

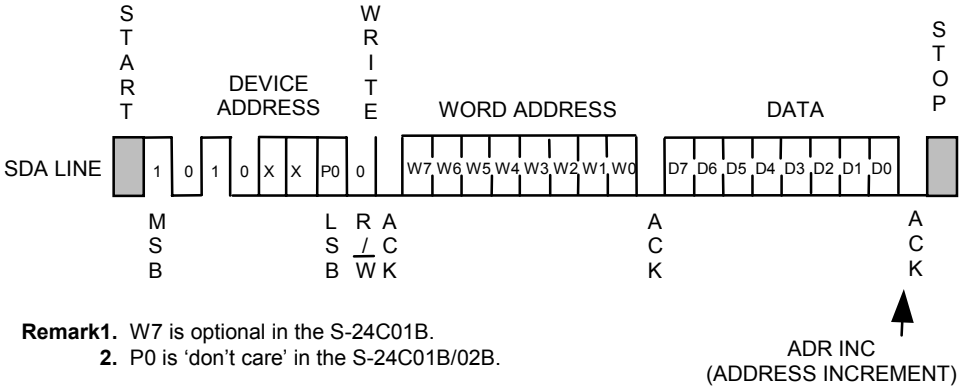
In the S-24C04B, 7th bit becomes “P0”. “P0” is a page address bit and is equivalent to an additional uppermost bit of the word address. Accordingly, when P0=”0”, the former half area corresponding to 2 k bits (addresses from 000h to 0FFh) in the entire memory are selected; when P0=”1”, the latter half area corresponding to 2 k bits (addresses from 100h to 1FFh) in all areas of the memory are selected.

6. Write

6.1 Byte Write

When the E^{2}PROM receives a 7-bit length device address and a 1-bit read/write instruction code “0”, following the start condition signal, it outputs the acknowledgment signal. Next, when the E^{2}PROM receives an 8-bit length word address, it outputs the acknowledgment signal.
After the E^{2}PROM receives 8-bit write data and outputs the acknowledgment signal, it receives the stop condition signal. Next, the E^{2}PROM at the specified memory address starts to rewrite.

When the E^{2}PROM is rewriting, all operations are prohibited and the acknowledgment signal is not output.

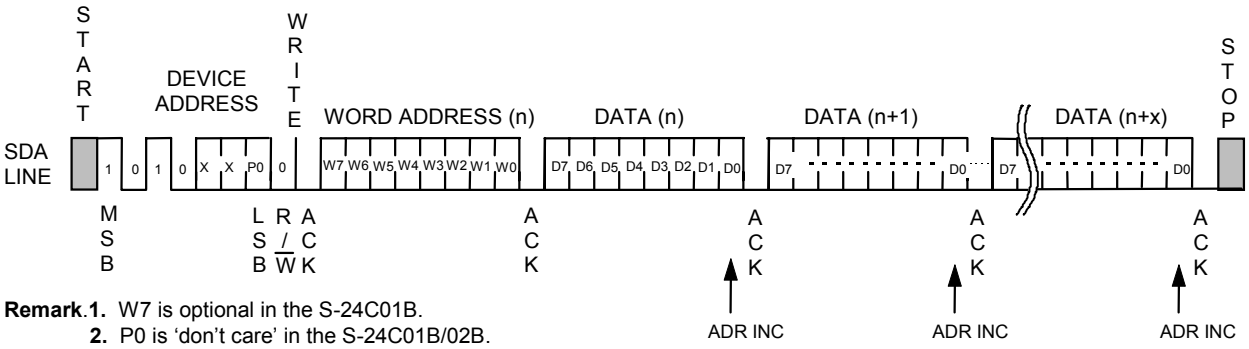


Remark1. W7 is optional in the S-24C01B.
2. P0 is ‘don’t care’ in the S-24C01B/02B.

Figure 12 Byte Write

6.2 Page Write

Up to 8 bytes per page can be written in the S-24C01/02B.
Up to 16 bytes per page can be written in the S-24C04B.
Basic data transmission procedures are the same as those in the "Byte Write". However, when the E²PROM receives 8-bit write data which corresponds to the page size, the page can be written.
When the E²PROM receives a 7-bit length device address and a 1-bit read/write instruction code "0", following the start condition signal, it outputs the acknowledgment signal. When the E²PROM receives an 8-bit length word address, it outputs the acknowledgment signal.
After the E²PROM receives 8-bit write data and outputs the acknowledgment signal, it receives 8-bit write data corresponding to the next word address, and outputs the acknowledgment signal. The E²PROM repeats reception of 8-bit write data and output of the acknowledgment signal in succession. It is capable of receiving write data corresponding to the maximum page size.
When the E²PROM receives the stop condition signal, it starts to rewrite, corresponding to the size of the page, on which write data, starting from the specified memory address, is received.



Remark.1. W7 is optional in the S-24C01B.
2. P0 is 'don't care' in the S-24C01B/02B.

Figure 13 Page Write

In the S-24C01/02B, the lower 3 bits of the word address are automatically incremented each when the E²PROM receives 8-bit write data.
Even if the write data exceeds 8 bytes, the upper 5 bits at the word address remain unchanged, the lower 3 bits are rolled over and overwritten.

In the S-24C04B, the lower 4 bits at the word address are automatically incremented each when the E²PROM receives 8-bit write data.
Even when the write data exceeds 16 bytes, the upper 4 bits of the word address and page address P0 remain unchanged, and the lower 4 bits are rolled over and overwritten.

6.3 Acknowledgment Polling

Acknowledgment polling is used to know when the rewriting of the E^{2}PROM is finished.
After the E^{2}PROM receives the stop condition signal and once it starts to rewrite, all operations are prohibited. Also, the E^{2}PROM cannot respond to the signal transmitted by the master device.
Accordingly, the master device transmits the start condition signal and the device address read/write instruction code to the E^{2}PROM (namely, the slave device) to detect the response of the slave device. This allows users to know when the rewriting of the E^{2}PROM is finished.
That is, if the slave device does not output the acknowledgment signal, it means that the E^{2}PROM is rewriting; when the slave device outputs the acknowledgment signal, you can know that rewriting has been completed. It is recommended to use read instruction "1" for the read/write instruction code transmitted by the master device.

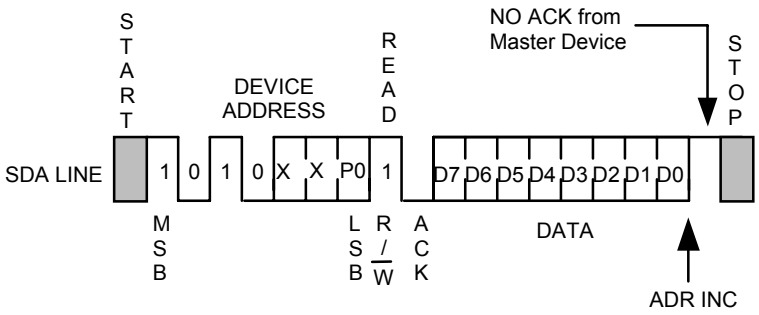
6.4 Write Protection

The S-24C01B/02B/04B are capable of protecting the memory. When the WP pin is connected to V_{CC}, writing to all memory area is prohibite in the S-24C01B, writing to 50% of the latter half of memory area is prohibited in the S-24C02B/04B. (prohibited adress are 080h to 0FFh in the S-24C02B; 100h to 1FFh in the S-24C04B) Even when writing is prohibited, since the controller inside the IC is operating, the response to the signal transmitted by the master device is not available during the time of writing (t_{WR}).
When the WP pin is connected to GND, the write protection becomes invalid, and writing in all memory area becomes available. However, when there is no need for using write protection, always connect the WP pin to GND. The write protection is valid in the operating voltage range.

7. Read

7.1 Current Address Read

The E^{2}PROM is capable of storing the last accessed memory address during both writing and reading. The memory address is stored as long as the power voltage is more than the retention voltage V_{AH}.
Accordingly, when the master device recognizes the position of the address pointer inside the E^{2}PROM, data can be read from the memory address of the current address pointer without assigning a word address. This is called "Current Address Read".
"Current Address Read" is explained for when the address counter inside the E^{2}PROM is an "n" address. When the E^{2}PROM receives a 7-bit length device address and a 1-bit read/write instruction code "1", following the start condition signal, it outputs the acknowledgment signal. However, in the S-24C04B, page address P0 becomes invalid, and the memory address of the current address pointer becomes valid.
Next, 8-bit length data at an "n" address is output from the E^{2}PROM, in synchronization with the SCL clock. The address counter is incremented at the falling edge of the SCL clock by which the 8th bit of data is output, and the address counter goes to address n+1.
The master device does not output the acknowledgment signal and transmits the stop condition signal to finish reading.



Remark P0 is 'don't care' in the S-24C01B/02B

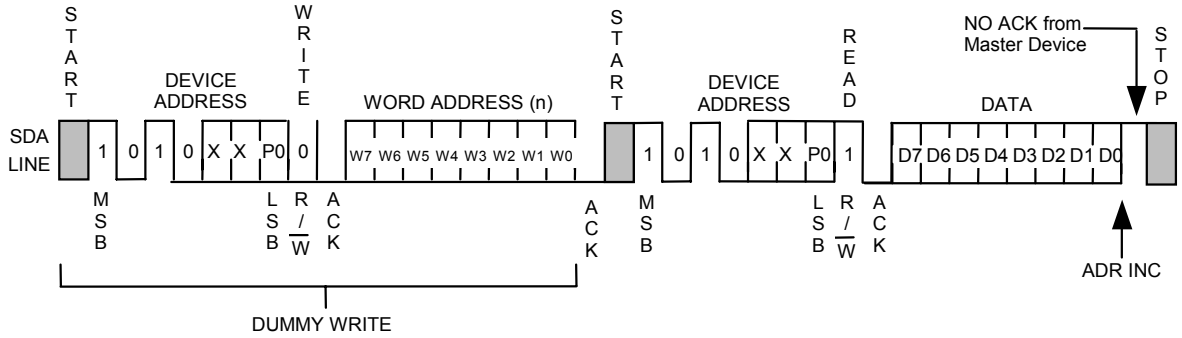
Figure 14 Current Address Read

For recognition of the address pointer inside the E^{2}PROM, take into consideration the following:
The memory address counter inside the E^{2}PROM is automatically incremented for every falling edge of the SCL clock by which the 8th bit of data is output during the time of reading. During the time of writing, upper bits of the memory address (upper 5 bits of the word address in the S-24C01B/02B; upper 4 bits of the word address and page address P0 in the S-24C04B) are left unchanged and are not incremented.

***1.** S-24C01B/02B is the upper 5 bits of the word address.
S-24C04B is the upper 4 bits of the word address and the page address P0.

7.2 Random Read

Random read is a mode used when the data is read from arbitrary memory addresses.
To load a memory address into the address counter inside the E^{2}PROM, first perform a dummy write according to the following procedures:
When the E^{2}PROM receives a 7-bit length device address and a 1-bit read/write instruction code “0”, following the start condition signal, it outputs the acknowledgment signal.
Next, the E^{2}PROM receives an 8-bit length word address and outputs the acknowledgment signal. Last, the memory address is loaded into the address counter of the E^{2}PROM.
the E^{2}PROM receives the write data during byte or page writing. However, data reception is not performed during dummy write.
The memory address is loaded into the memory address counter inside the E^{2}PROM during dummy write. After that, the master device can read the data starting from the arbitrary memory address by transmitting a new start condition signal and performing the same operation as that in the “Current Address Read”.
That is, when the E^{2}PROM receives a 7-bit length device address and a 1-bit read/write instruction code “1”, following the start condition signal, it outputs the acknowledgment signal.
Next, 8-bit length data is output from the E^{2}PROM, in synchronization with the SCL clock. The master device does not output an acknowledgment signal and transmits the stop condition signal to finish reading.



Remark1. W7 is optional in the S-24C01B.
2. P0 is “don’t care” in the S-24C01B/02B.

Figure 15 Random Read

7.3 Sequential Read

When the E²PROM receives a 7-bit length device address and a 1-bit read/write instruction code “1” in both current and random read operations, following the start condition signal, it outputs the acknowledgment signal.

When 8-bit length data is output from the E²PROM, in synchronization with the SCL clock, the memory address counter inside the E²PROM is automatically incremented at the falling edge of the SCL clock, by which the 8th data is output.

When the master device transmits the acknowledgment signal, the next memory address data is output.

When the master device transmits the acknowledgment signal, the memory address counter inside the E²PROM is incremented and read data in succession. This is called “Sequential Read”.

When the master device does not output an acknowledgement signal and transmits the stop condition signal, the read operation is finished.

Data can be read in the “Sequential Read” mode in succession. When the memory address counter reaches the last word address, it rolls over to the first memory address.

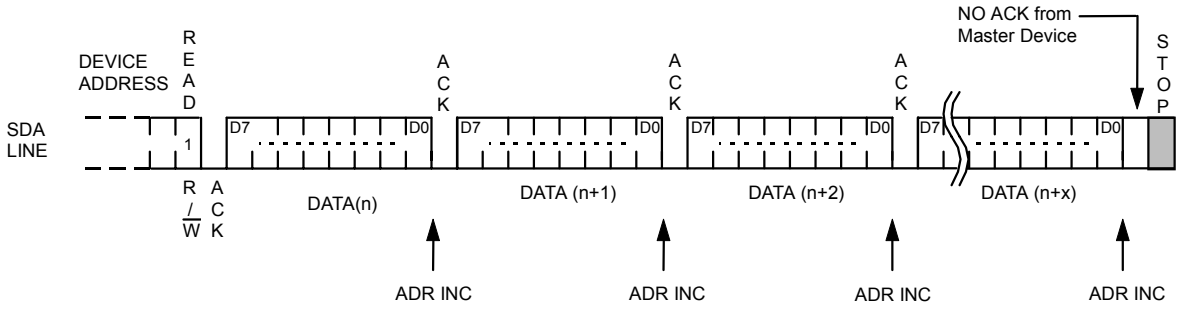


Figure 16 Sequential Read

8. Address Increment Timing

The address increment timing is as follows. During reading operation, the memory address counter is automatically incremented at the falling edge of the SCL clock (the 8th read data is output).
During writing operation, the memory address counter is also automatically incremented at the falling edge of the SCL clock when the 8th bit write data is fetched.

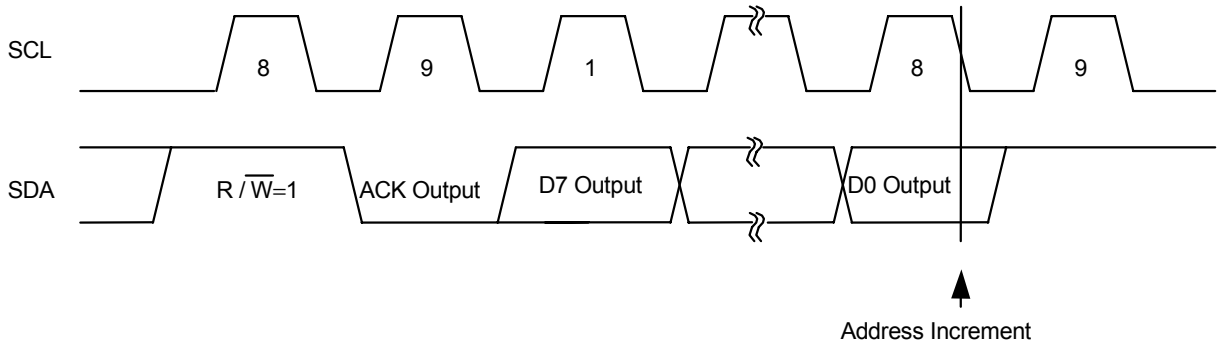


Figure 17 Address Increment Timing in Reading

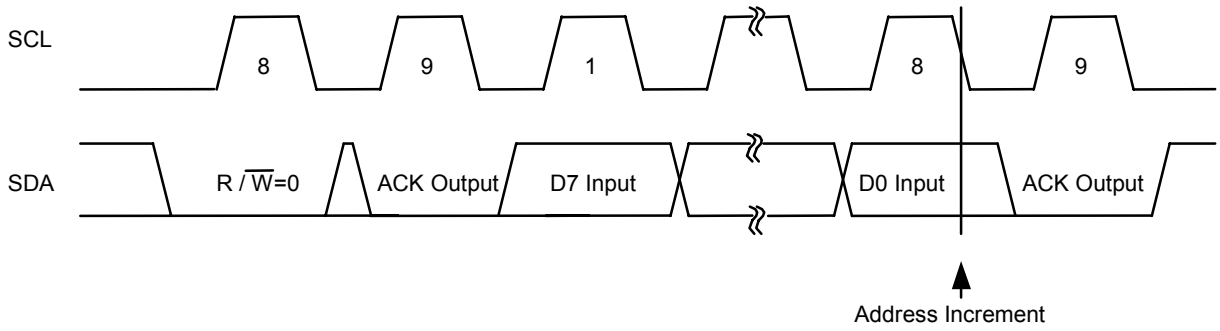


Figure 18 Address Increment Timing in Writing

■ Precautions

- Generally, an E^{2}PROM may cause a malfunction by the operation in low voltage range induced by power ON/OFF. The S-24C01B/02B/04B initialize themselves by the power on clear circuit at power on. Attention should be paid to the followings so as to operate the power on clear circuit correctly, otherwise malfunction may occur.
  1. All input and output pins should be connected to the V_{CC} or the GND level so as not to be floating.
  2. Raise the power voltage up to the operation voltage from 0 V without staying at middle range.
  3. Raising speed of the power voltage should be faster than 40 ms/V.
  4. Power off interval before power on should be longer than 100 ms.

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.

- SII claims no responsibility for any and all disputes arising out of or in connection with any infringement of the products including this IC upon patents owned by a third party.

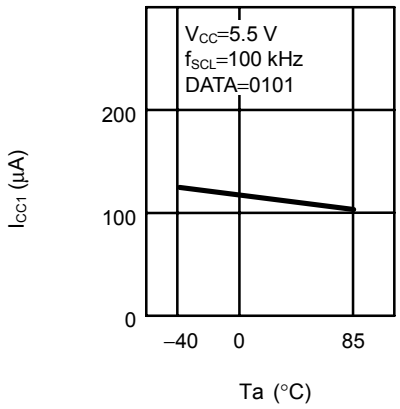
■ I^{2}C Bus License

Purchase of I^{2}C components of Seiko Instruments Inc., conveys a license under the Philips I^{2}C Patent. Rights to use these components in an I^{2}C system, is granted provided that the system conforms to the I^{2}C Standard Specification as defined by Philips.
Please note that a product or a system incorporating this IC may infringe upon the Philips I^{2}C Patent Rights depending upon its configuration. In the event of such infringement Seiko Instruments Inc., shall not bear any responsibility for any matters with regard to and arising from such patent infringement.

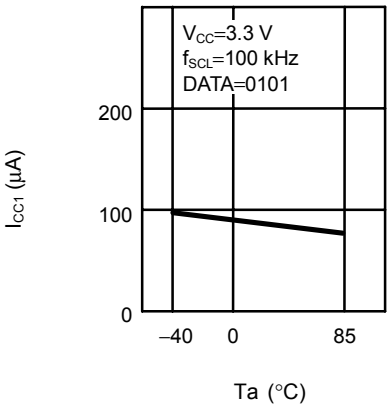
■ Characteristics

1. DC Characteristics

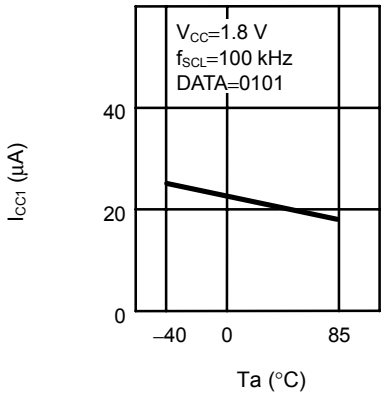
1.1 Current consumption (READ) I_{CC1} – Ambient temperature Ta



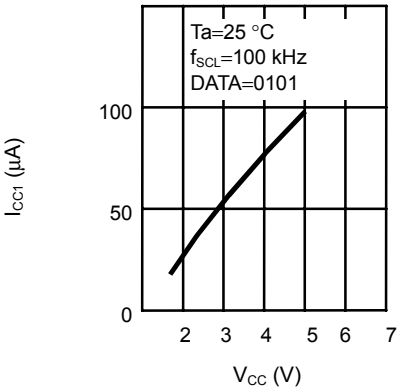
1.2 Current consumption (READ) I_{CC1} – Ambient temperature Ta



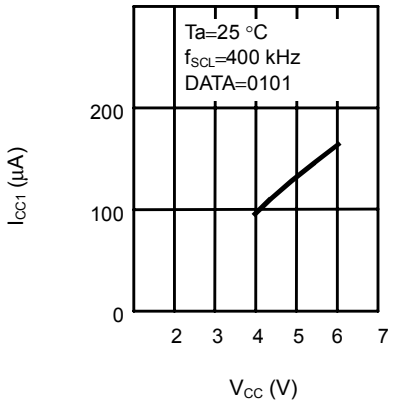
1.3 Current consumption (READ) I_{CC1} – Ambient temperature Ta



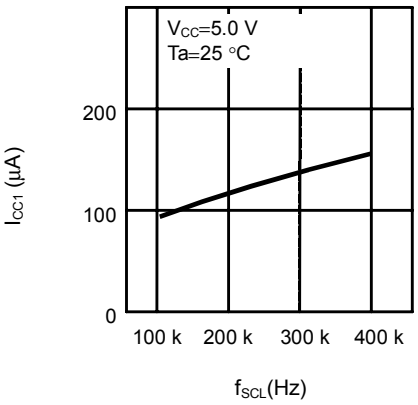
1.4 Current consumption (READ) I_{CC1} – Power supply voltage V_{CC}



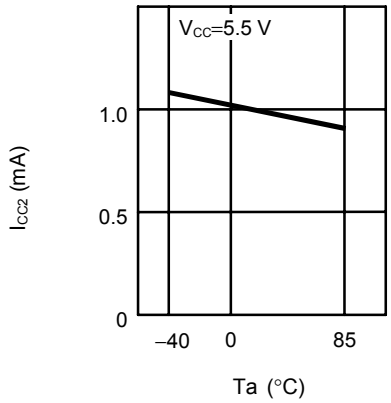
1.5 Current consumption (READ) I_{CC1} – Power supply voltage V_{CC}



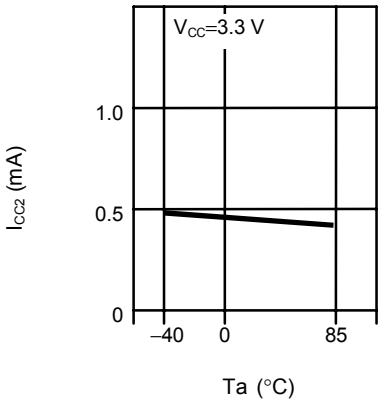
1.6 Current consumption (READ) I_{CC1} – Clock frequency fscl



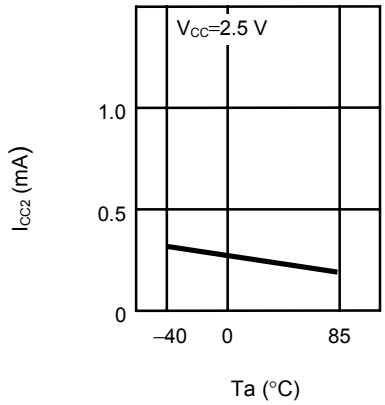
1.7 Current consumption (PROGRAM) I_{CC2} – Ambient temperature Ta



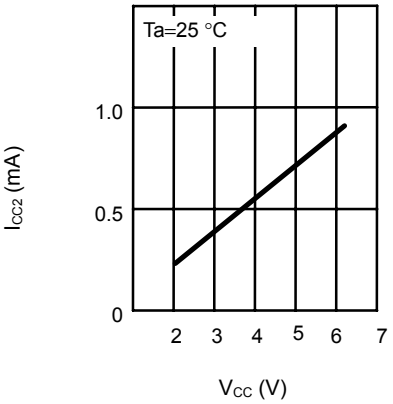
1.8 Current consumption (PROGRAM) I_{CC2} – Ambient temperature Ta



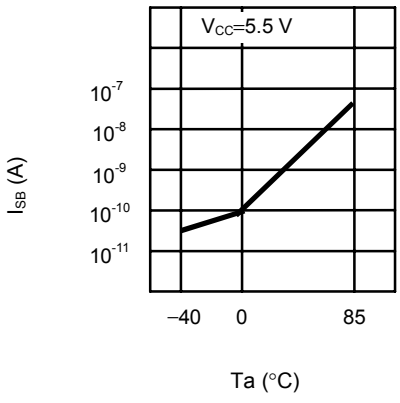
1.9 Current consumption (PROGRAM) I_{CC2} – Ambient temperature Ta



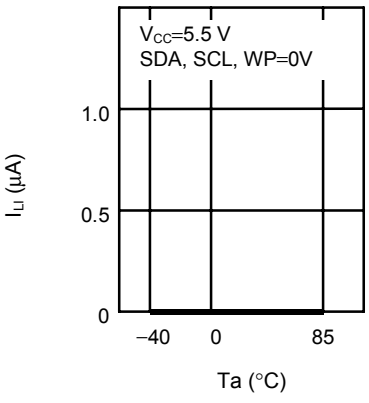
1.10 Current consumption (PROGRAM) I_{CC2} – Power supply voltage V_{CC}



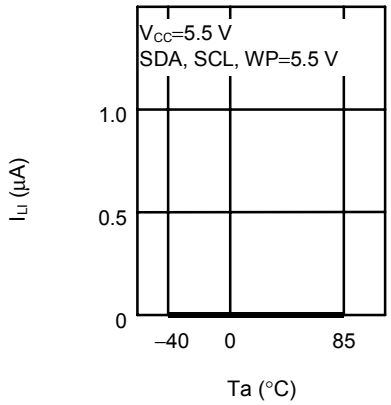
1.11 Standby current consumption I_{SB} – Ambient temperature Ta



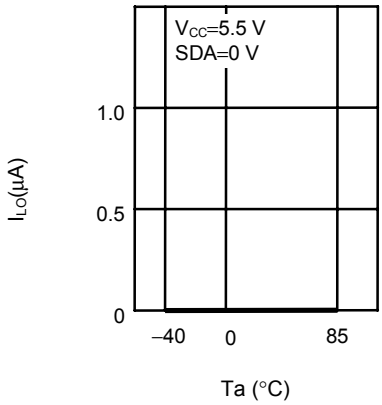
1.12 Input leakage current I_{LI} – Ambient temperature Ta



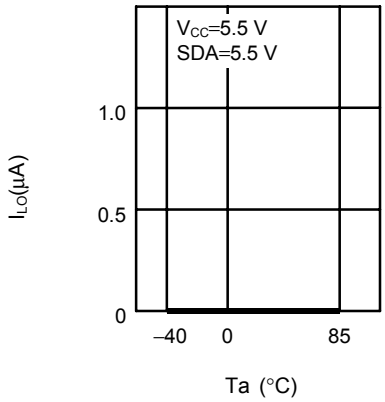
1.13 Input leakage current I_{LI} – Ambient temperature Ta



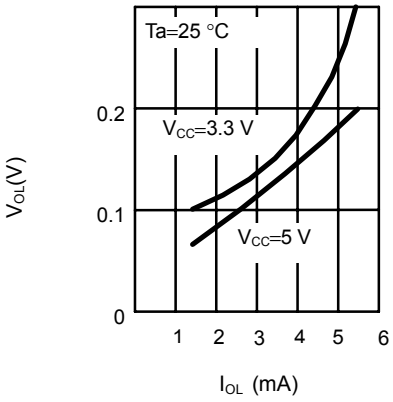
1.14 Output leakage current I_{LO} – Ambient temperature Ta



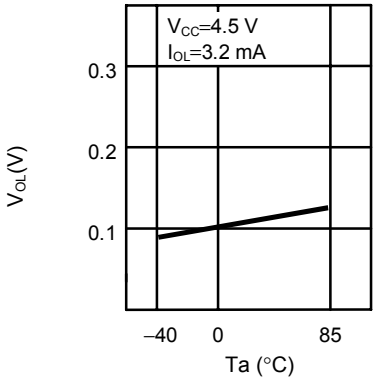
1.15 Output leakage current I_{LO} – Ambient temperature Ta



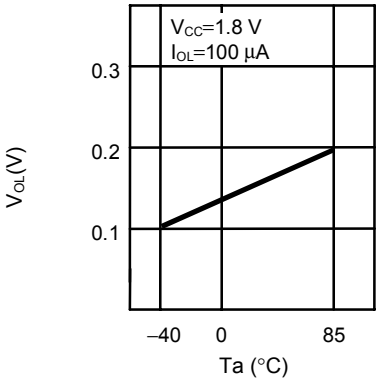
1.16 Low level output voltage V_{OL} – Low level output current I_{OL}



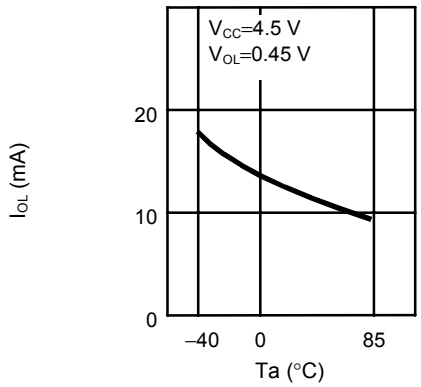
1.17 Low level output voltage V_{OL} – Ambient temperature Ta



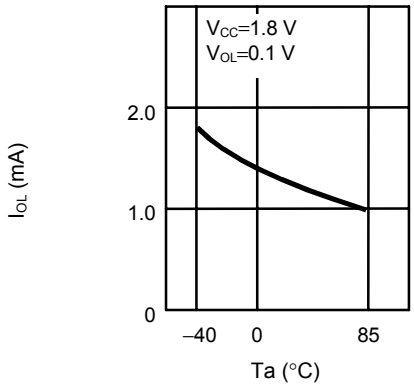
1.18 Low level output voltage V_{OL} – Ambient temperature Ta



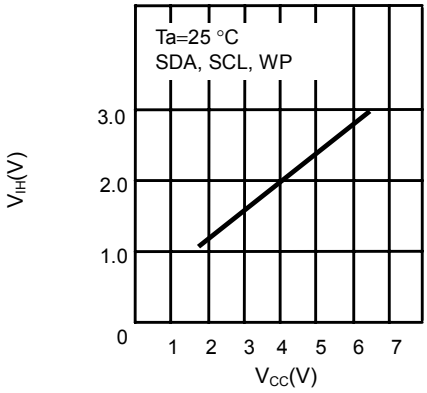
1.19 Low level output current I_{OL} – Ambient temperature Ta



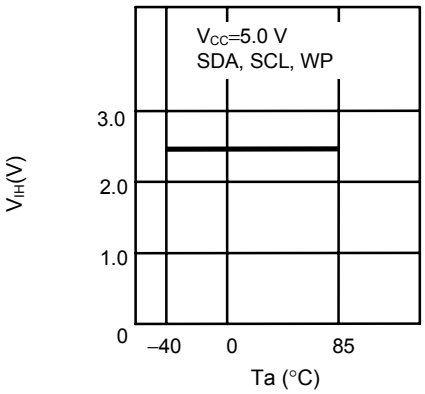
1.20 Low level output current I_{OL} – Ambient temperature Ta



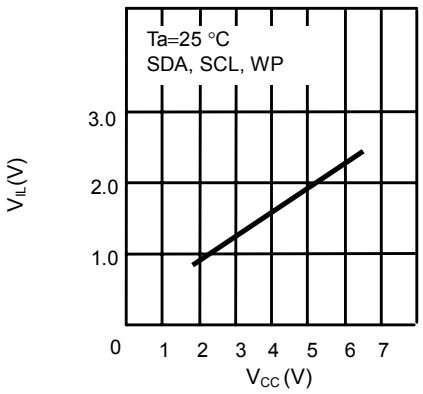
1.21 High input inversion voltage VIH – Power supply voltageV_{CC}



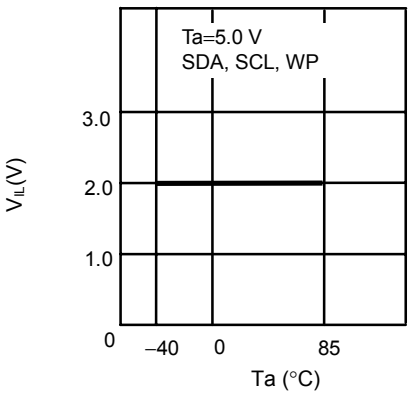
1.22 High input inversion voltage VIH – Ambient temperature Ta



1.23 Low input inversion voltage VIL – Power supply voltageV_{CC}

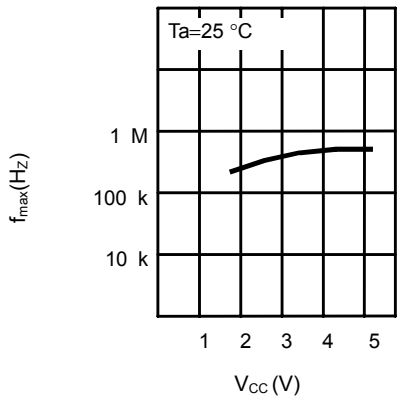


1.24 Low input inversion voltage VIL – Ambient temperature Ta

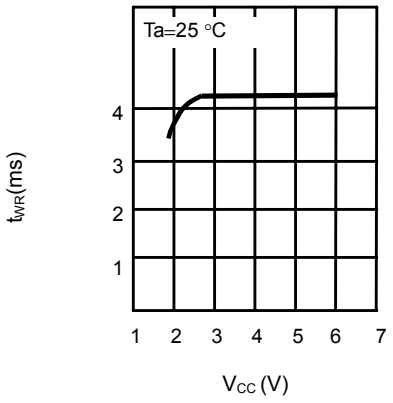


2. AC Characteristics

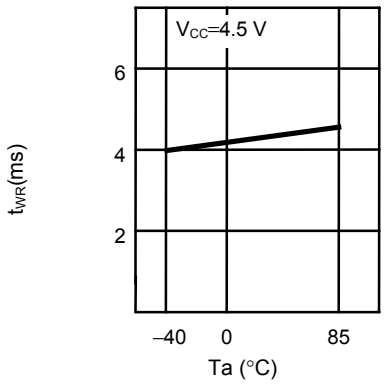
2.1 Maximum operating frequency fmax – Power supply voltage V_{CC}



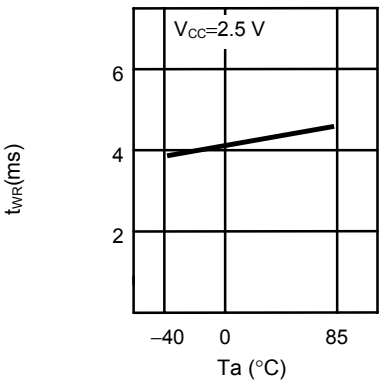
2.2 Write time t_{WR} – Power supply voltage V_{CC}



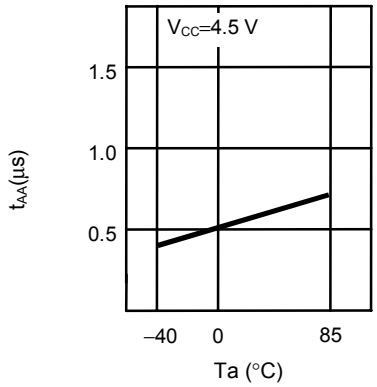
2.3 Write time t_{WR} – Ambient temperature Ta



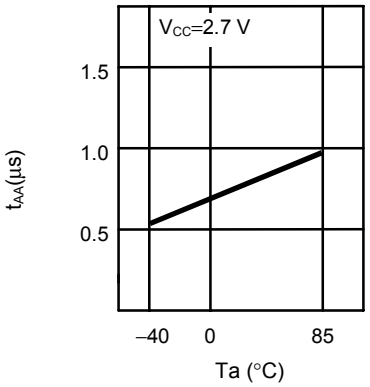
2.4 Write time t_{WR} – Ambient temperature Ta



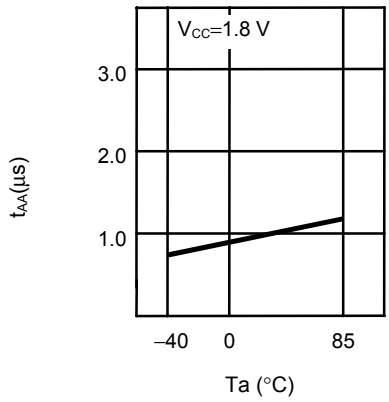
2.5 SDA output delay time t_{AA} – Ambient temperature Ta



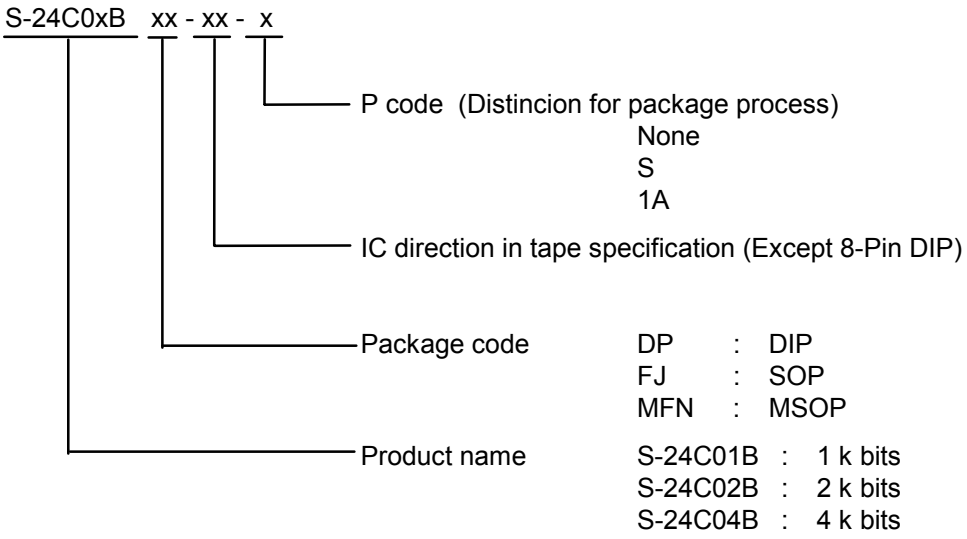
2.6 SDA output delay time t_{AA} – Ambient temperature Ta



2.7 Data output delay time t_{AA} – Ambient temperature Ta

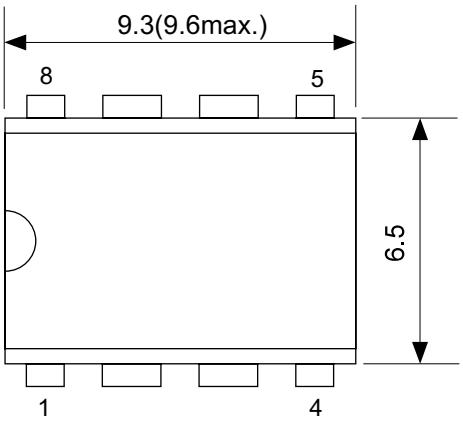


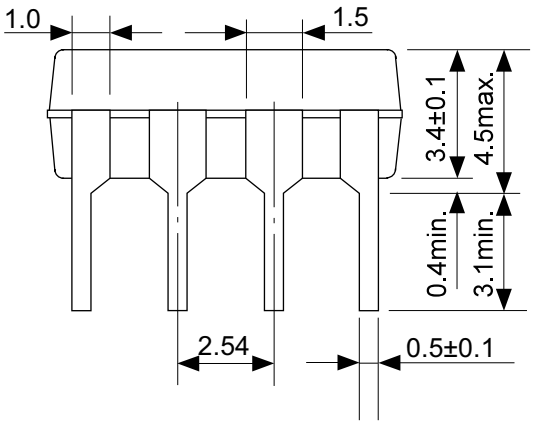
■ Product Code Structure

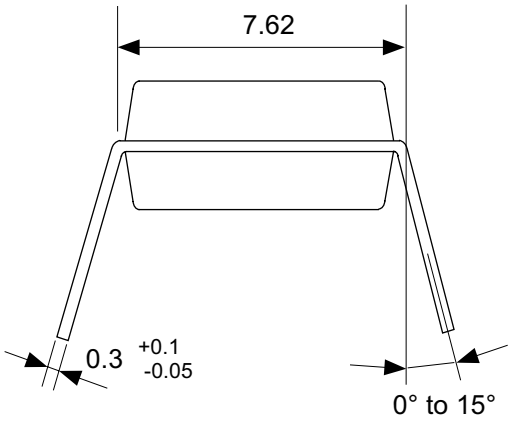


Product name	Package code	Taping specification	P code	Package drawing	Tape drawing	Reel drawing
S-24C01B S-24C02B S-24C04B	DP	–	–	DP008-A	–	–
			S	DP008-A	–	–
				DP008-E	–	–
			-1A	DP008-C	–	–
	FJ	-TB	–	FJ008-A	FJ008-D	FJ008-J
			S	FJ008-A	FJ008-D	FJ008-D
				FJ008-A	FJ008-E	FJ008-E
	MFN	-TB	–	FN008-A	FJ008-A	FN008-N

NOTE **1.** Package dimensions of FJ(SOP) are same in the range of deviation.
2. Please contact an SII local representative for details.

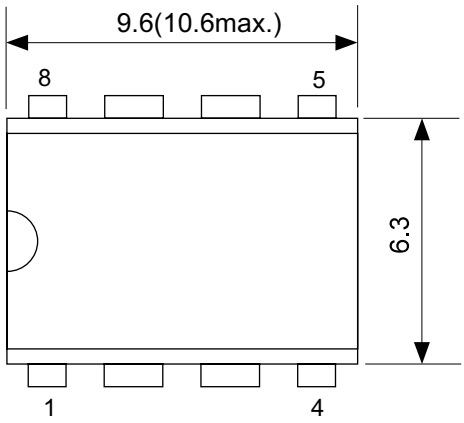


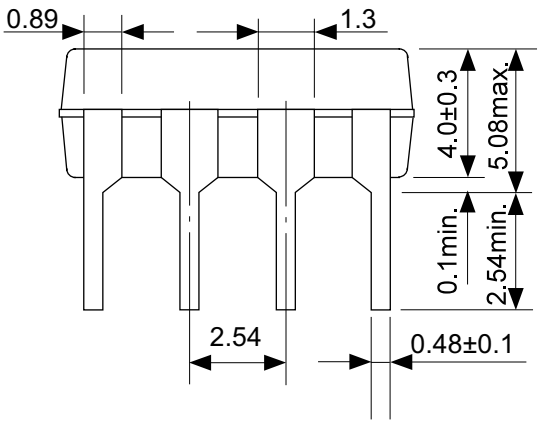


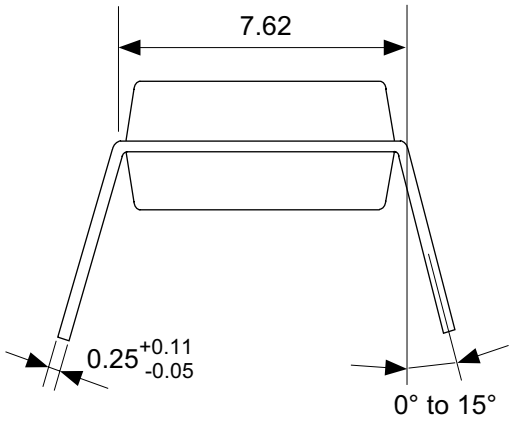


No. DP008-A-P-SD-1.1

TITLE	DIP8-A-PKG Dimensions
No.	DP008-A-P-SD-1.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	







No. DP008-C-P-SD-1.1

TITLE	DIP8-C-PKG Dimensions
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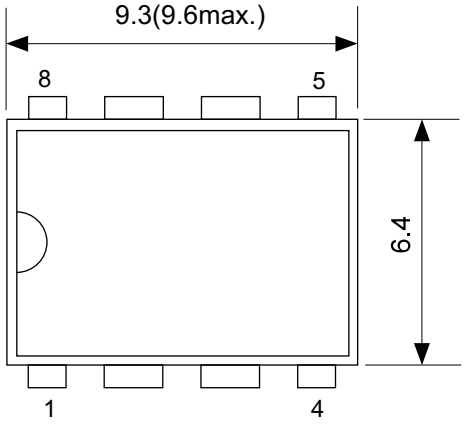
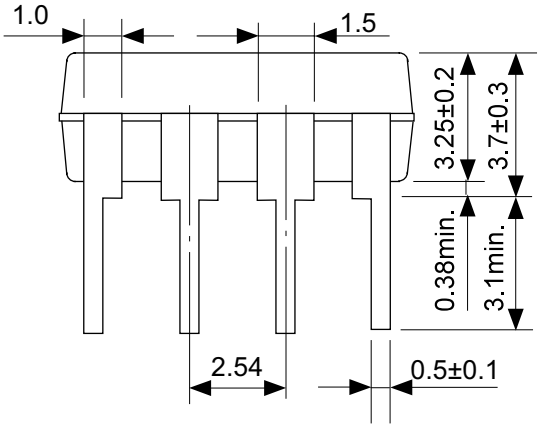
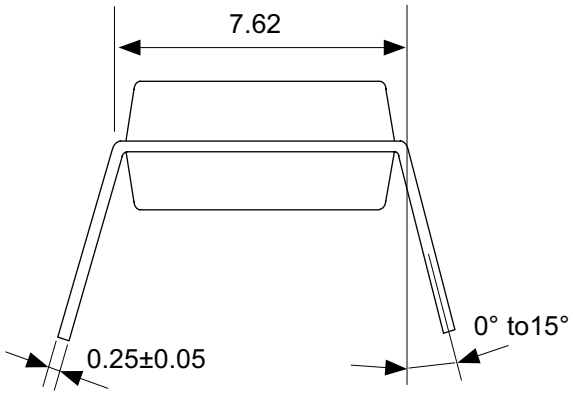
SCALE	
UNIT	mm
Seiko Instruments Inc.	







No. DP008-E-P-SD-2.1

TITLE	DIP8-E-PKG Dimensions
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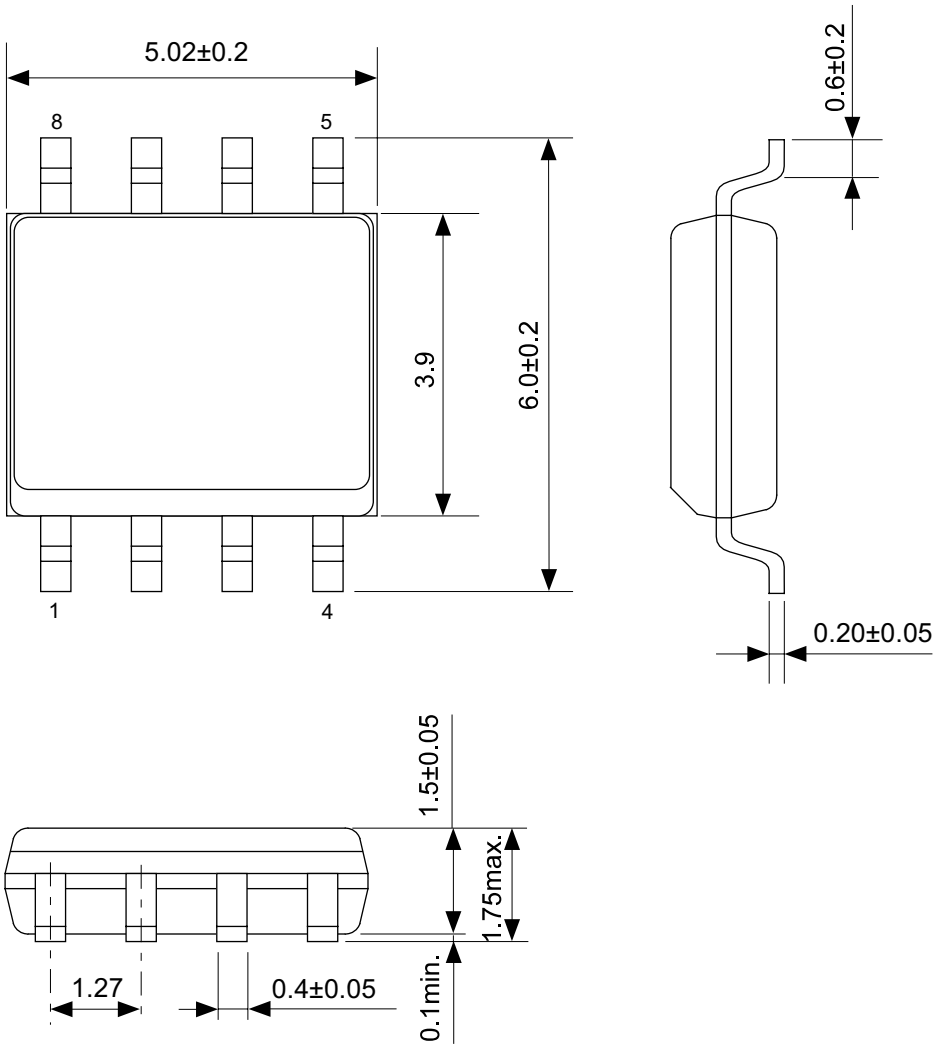
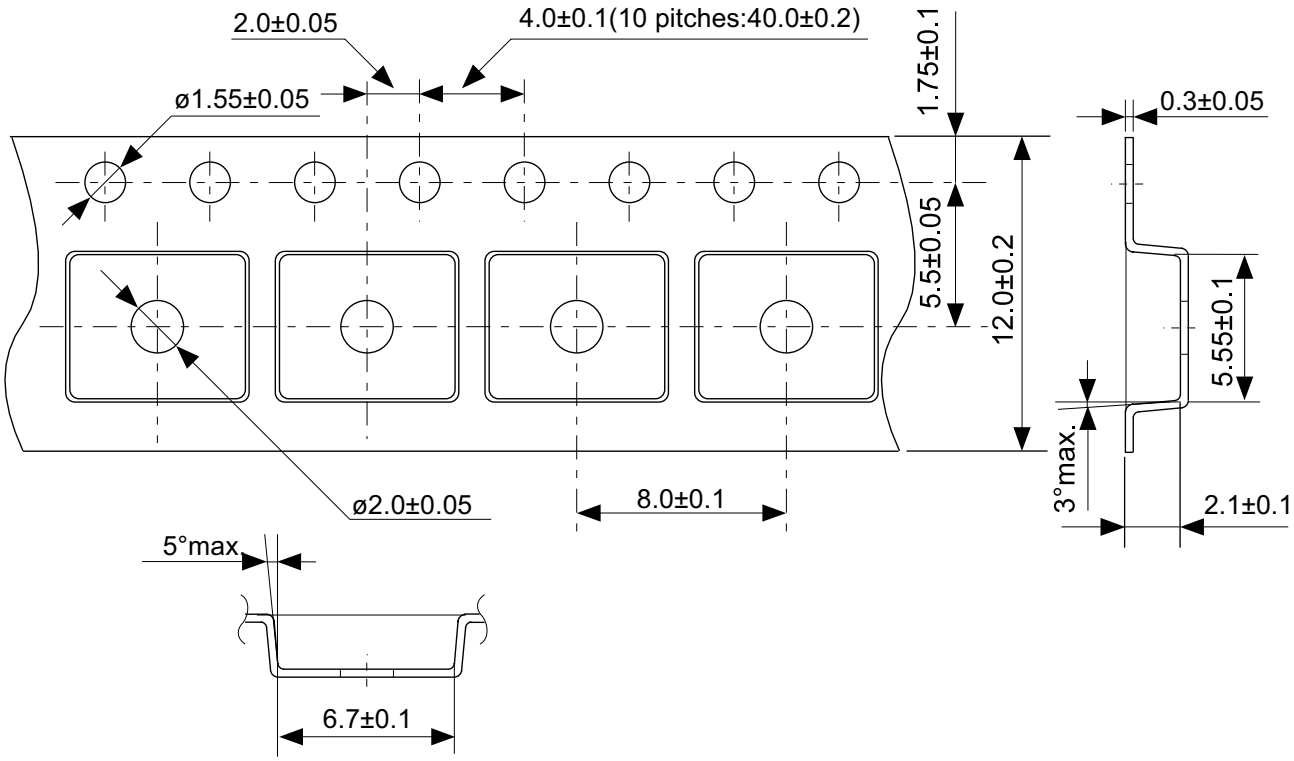
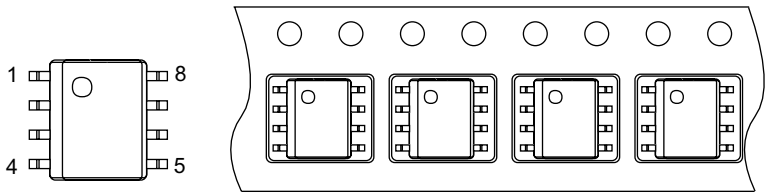
SCALE	
UNIT	mm
Seiko Instruments Inc.	



No. FJ008-A-P-SD-2.1

TITLE	SOP8J-A-PKG Dimensions
No.	FJ008-A-P-SD-2.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	

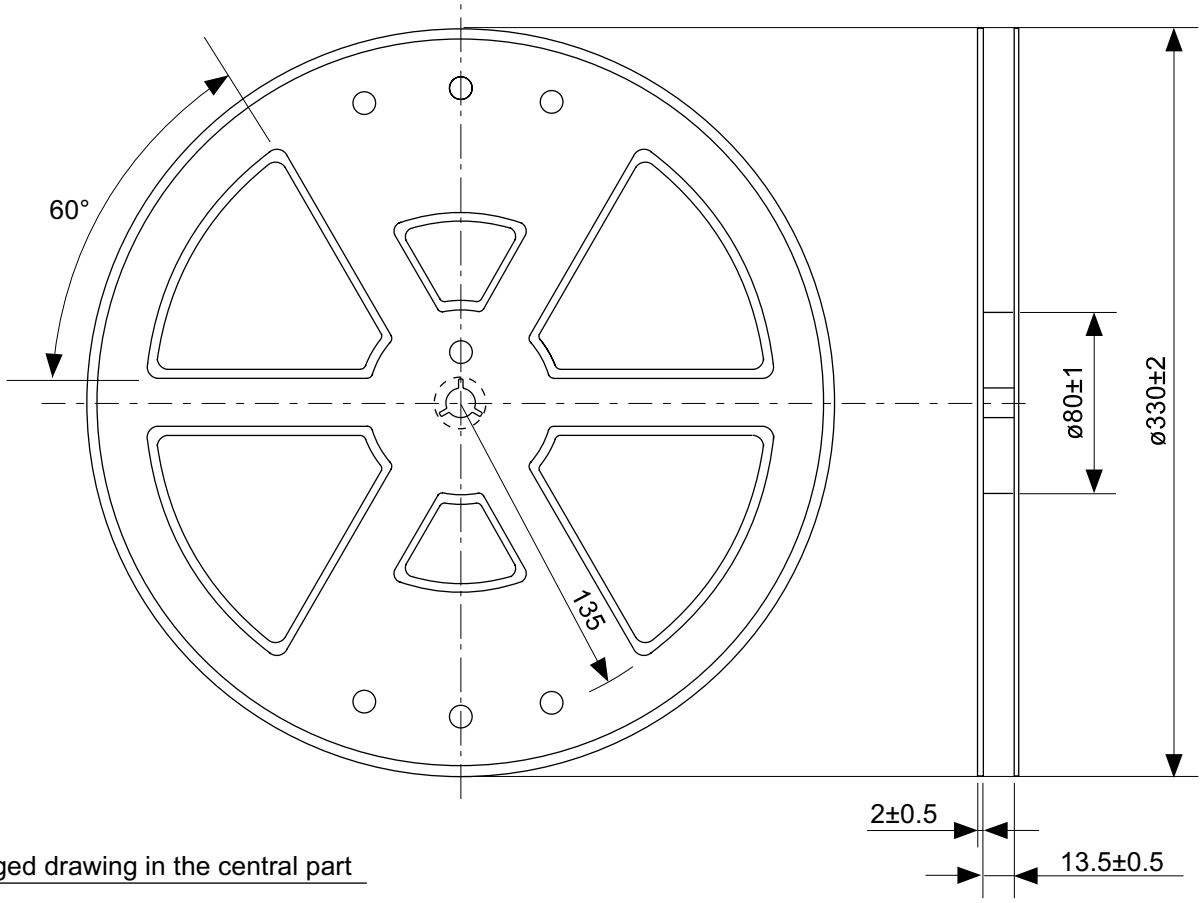




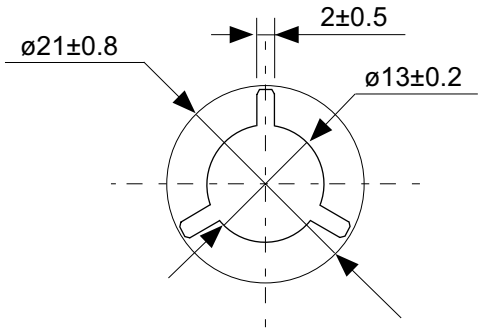
Feed direction

No. FJ008-D-C-SD-1.1

TITLE	SOP8J-D-Carrier Tape
No.	FJ008-D-C-SD-1.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	

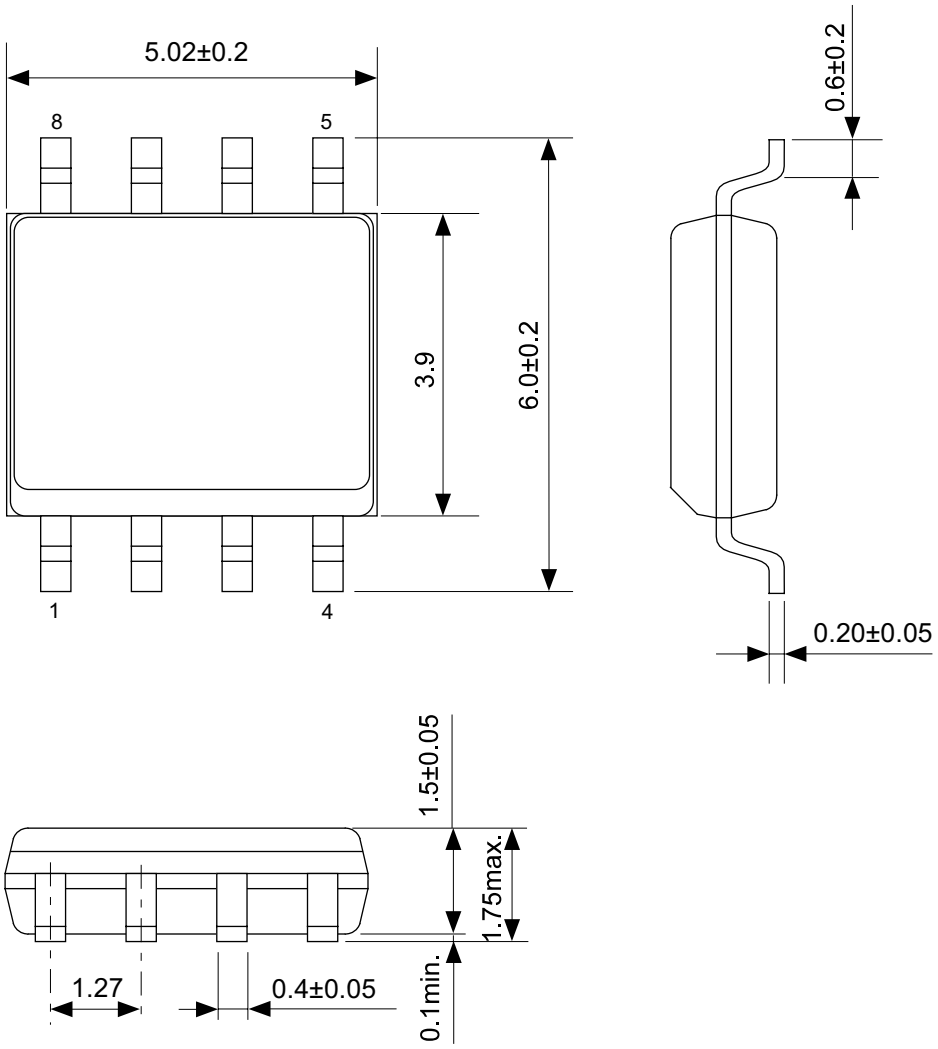


Enlarged drawing in the central part



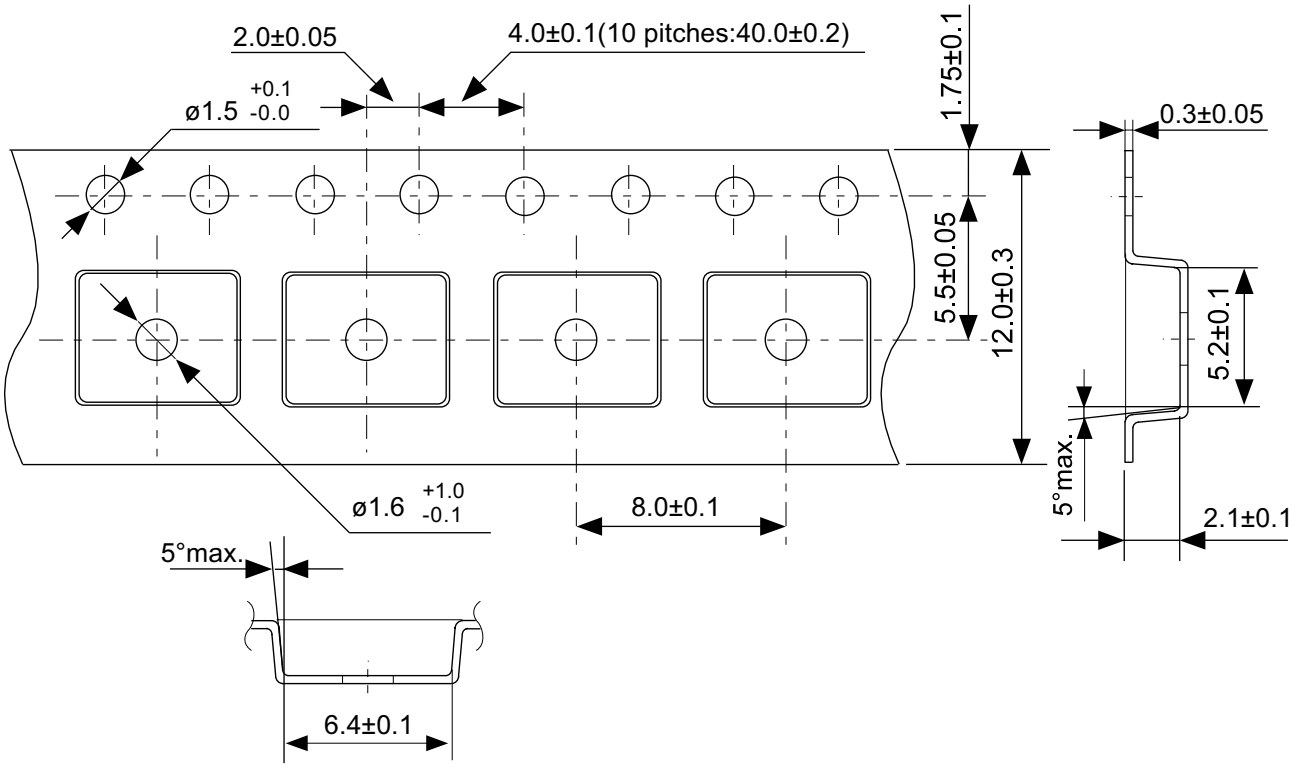
No. FJ008-D-R-SD-1.1

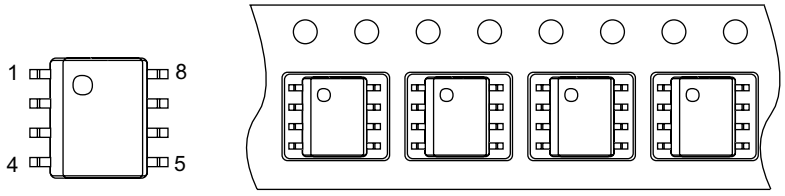
TITLE	SOP8J-D-Reel		
No.	FJ008-D-R-SD-1.1		
SCALE		QTY.	2,000
UNIT	mm		
Seiko Instruments Inc.			



No. FJ008-A-P-SD-2.1

TITLE	SOP8J-A-PKG Dimensions
No.	FJ008-A-P-SD-2.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	

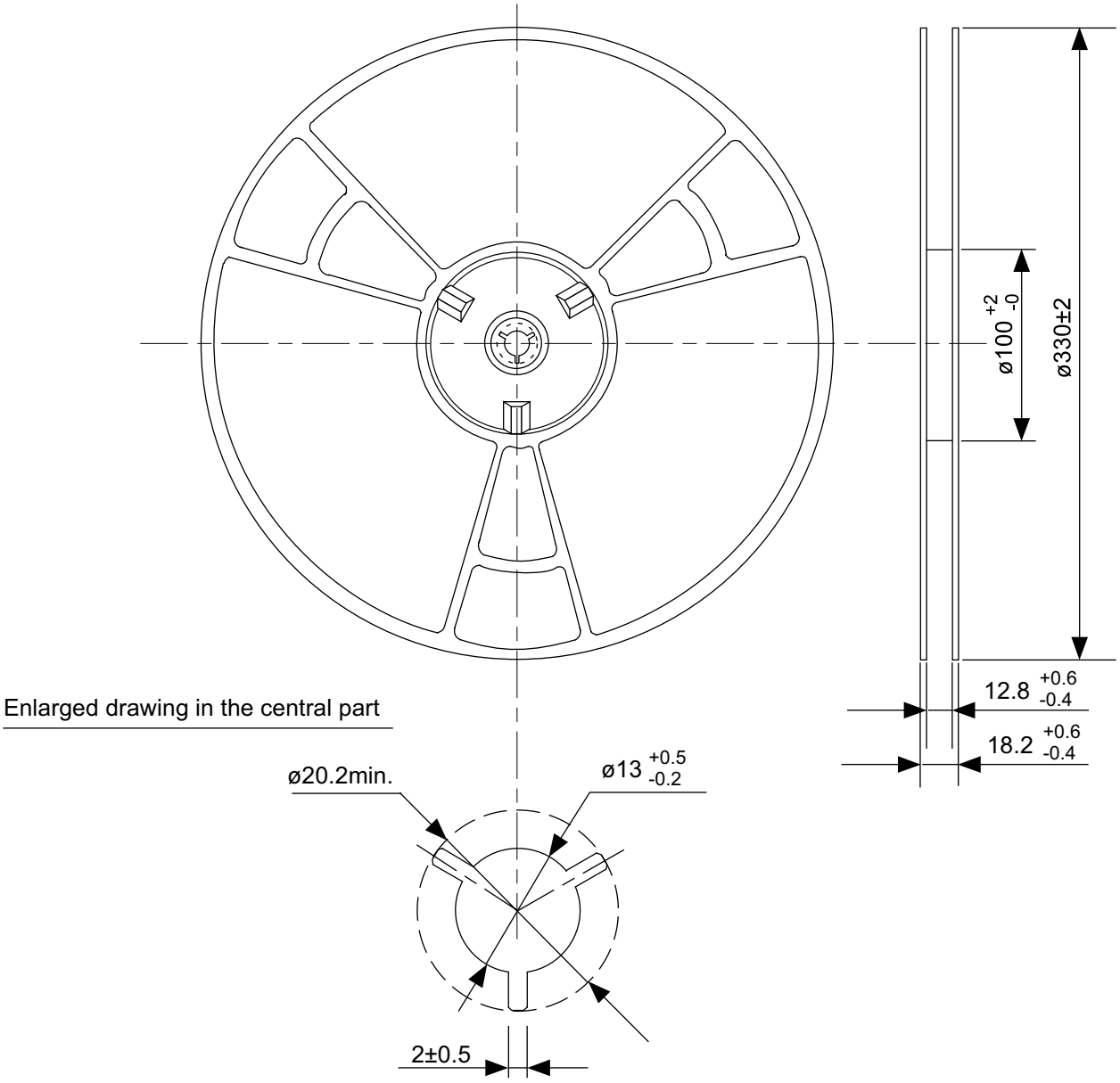




Feed direction

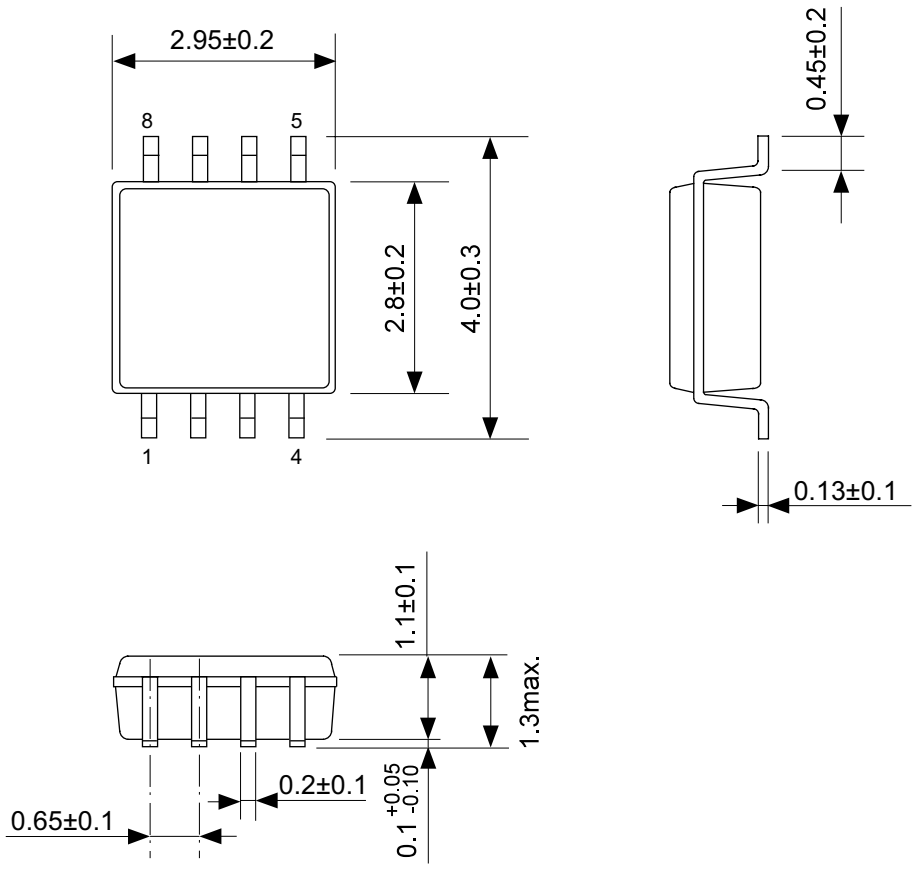
No. FJ008-E-C-SD-1.1

TITLE	SOP8J-E-Carrier Tape
No.	FJ008-E-C-SD-1.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	



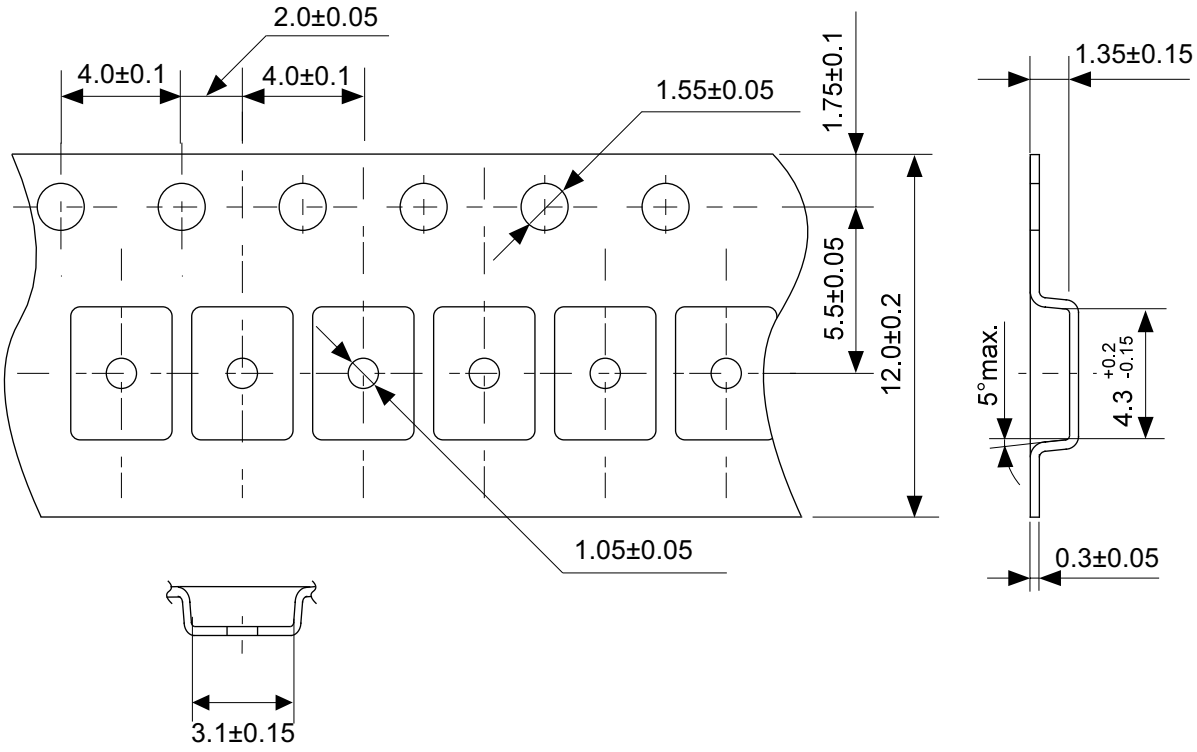
No. FJ008-E-R-SD-1.1

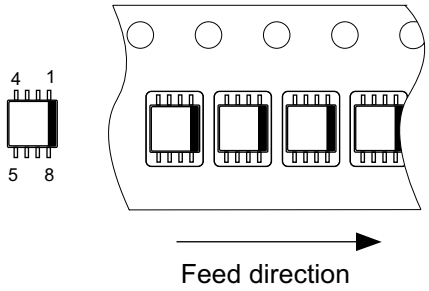
TITLE	SOP8J-E-Reel		
No.	FJ008-E-R-SD-1.1		
SCALE		QTY.	2,000
UNIT	mm		
Seiko Instruments Inc.			



No. FN008-A-P-SD-1.1

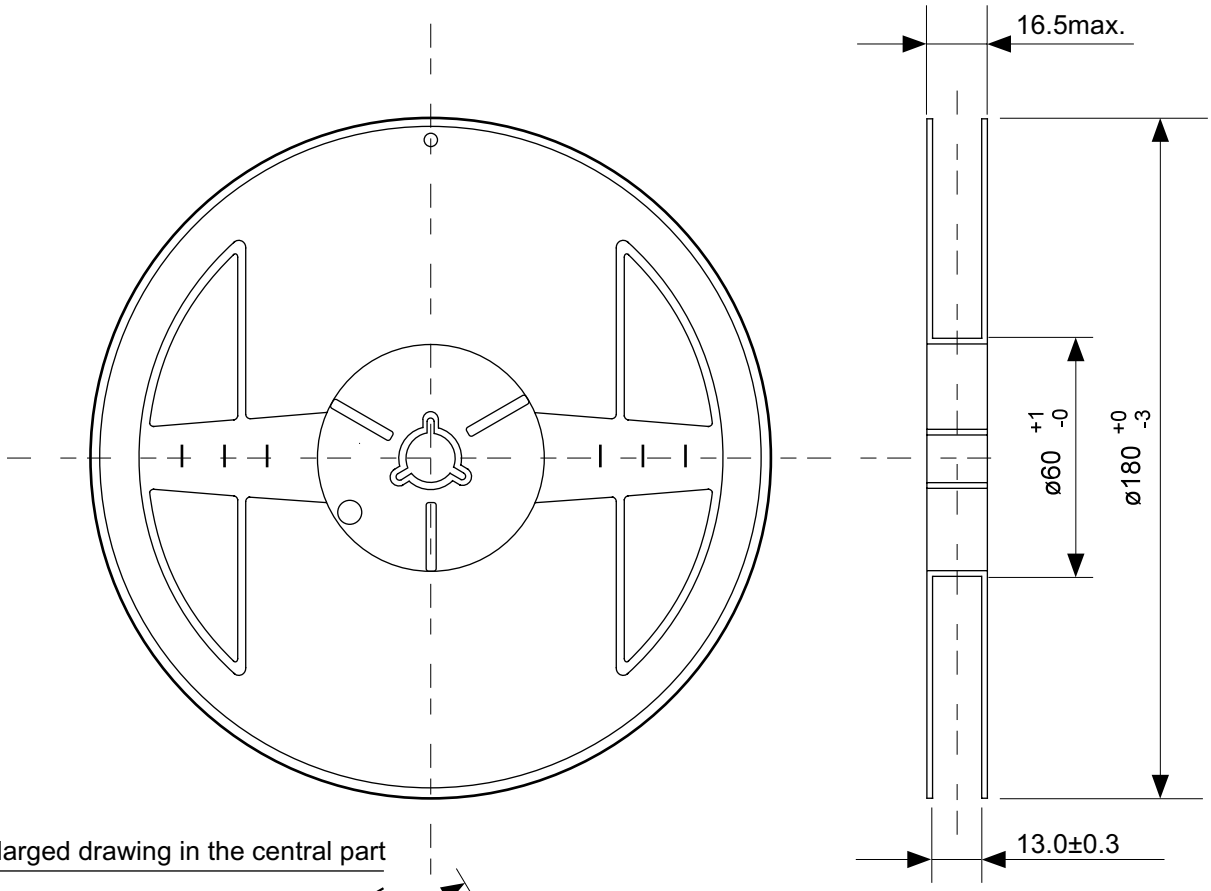
TITLE	MSOP8-A-PKG Dimensions
No.	FN008-A-P-SD-1.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	



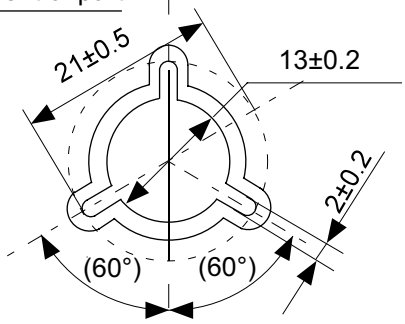


No. FN008-A-C-SD-1.1

TITLE	MSOP8-A-Carrier Tape
No.	FN008-A-C-SD-1.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	



Enlarged drawing in the central part



No. FN008-A-R-SD-1.1

TITLE	MSOP8-A-Reel		
No.	FN008-A-R-SD-1.1		
SCALE		QTY.	3,000
UNIT	mm		
Seiko Instruments Inc.			

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