DDC
ILC DATA DEVICE CORPORATION®

SSP-21120

28 VDC SOLID-STATE POWER CONTROLLER MODULE

DESCRIPTION

The SSP-21120 Series of 28 Vdc, Solid-State Power Controllers (SSPCs) replace electromagnetic circuit breakers and solid state relays rated for 40, 60, and 80 amperes. The SSPCs offer status outputs and permit external input logic control allowing for remote location near to the load. The three models in the series differ only in rated current, so that fault and I^2T trip characteristics can be selected to protect wiring and loads.

Using Power MOSFET switches, these Power Controllers offer low "on" resistance, low voltage drop, high "off" impedance, and low power dissipation.

Built with Power MOSFETs and custom monolithics and using thick film hybrid technology, they offer small size, low power, and high reliability in a module.

Built-In-Test (BIT) has been provided to monitor, in real time, the status of the internal circuitry as well as circuitry external to the SSPC. This BIT monitors MOSFET failure and control circuit failure.

The SSP-21120 Series will operate over the temperature range from -55°C to +85°C with no thermal derating, see ordering information.

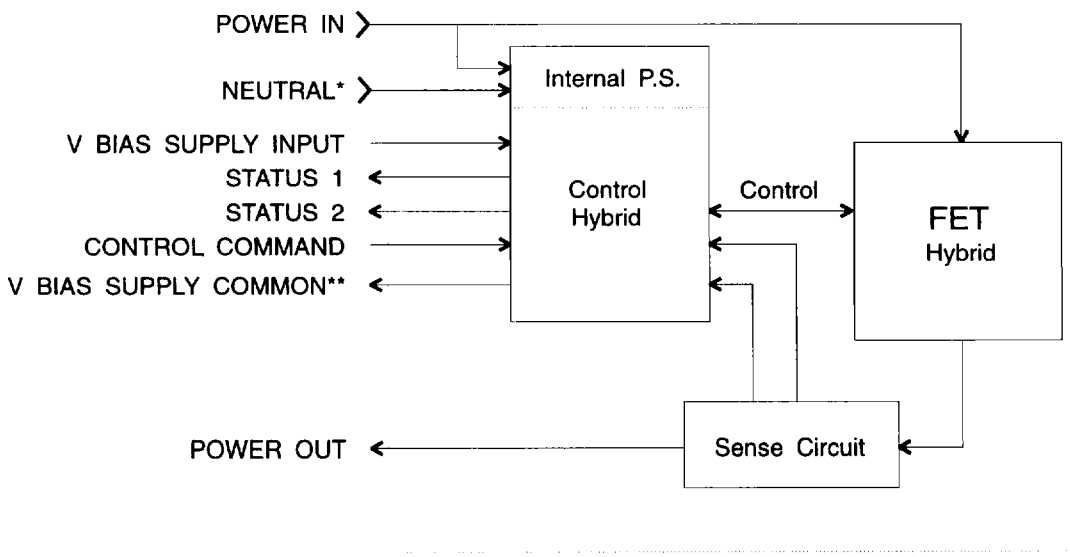
APPLICATIONS

Designed to replace circuit breakers in land, air, and space vehicles, these Solid State Power Controller Modules provide status outputs for light and heavy overloads as well as minimum load current.

FEATURES

- ***True I^2T Protection***
- ***No Thermal Derating***
- ***Isolated Control Circuitry***
- ***MIL-STD-704 Compliant***
- ***Status Outputs***
- ***Instant Trip Protection***
- ***Low Power Dissipation***
- ***Solid-State Reliability***

SSP-21120



NOTE: *NEUTRAL = POWER GROUND; **V BIAS SUPPLY COMMON = SIGNAL GROUND

FIGURE 1. SSP 21120 BLOCK DIAGRAM

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TABLE 1. ABSOLUTE MAXIMUM RATINGS		
PARAMETER	UNIT	VALUE
Power Input To Power Ground	Vdc	50 continuous 100 Volts, 50 ms transient
Control Input To Signal Ground	Vdc	-0.5 to +7.0
Power Ground To Signal Ground	Vdc	-100 to +100
Bias voltage	Vdc	-0.5 to +7.0
Pin-to-case	Vdc	-1000 to +1000
Junction Temperature	°C	+150

Note: Power Ground = Neutral; Bias Supply Common = Signal Ground

TABLE 2. RECOMMENDED OPERATING CONDITIONS		
PARAMETER	UNIT	VALUE
Power Input To Power Ground	Vdc	+9.0 to +40.0
Control Input To Signal Ground	Vdc	+4.5 to V Bias
Power Ground To Signal Ground	Vdc	-40 to +40
V Bias voltage	Vdc	+4.5 to +5.5

Note: Power Ground = Neutral; Bias Supply Common = Signal Ground

TABLE 3. SSP-21120 SPECIFICATIONS (SEE NOTES 1 AND 2)			
PARAMETER	CONDITIONS	UNIT	VALUE
CONTROL CIRCUIT			
Logic Type			TTL/CMOS
V Bias Supply Current	V_{CC} = 4.5 to 5.5 Vdc	mA	10 max
Control Turn-On Voltage		V	2.0 to 5.5
Control Turn-Off Voltage		V	-0.5 to 0.8
Control Input Current	control voltage = 5.0 V	µA	50 max
Control Input Current	control voltage = 2.4 V	µA	50 max
Control Input Current	control voltage = 0.8 V	µA	-50 min
Status Output Voltage	V_{CC}= 4.5 V, I_{OL}= 2.5 mA	V	0.4 max
Status Output Voltage	V_{CC}= 4.5 V, I_{OH}= -1.0 mA	V	2.4 min
Status Truth Table	see TABLE 5		
POWER CIRCUIT			
Power to Internal PWR supply	Nominal 28 V	mA	14 typ
Max. Continuous Current			See Table 4
'On' Resistance			See Table 4
Power Dissipation			See Table 4
Power Out Leakage Current to Power Ground	Power In = 9 - 40 V (see note 2)	mA/A	0.1 max
Max Load Capacitance for Start-Up	Power In = 9 - 40 V (see note 2)	µF/A	28 typ
Signal to Neutral Ground Isolation	at 100 Vdc	pF	1000 typ
Output Capacitance	see note 2	pF/A	300 typ
Trip Reset Time		ms	30 min
Rupture Capacity	Unlimited	A	Unlimited
Output-to Input Parasitic Diode, Continuous Current Per Amp Of Rated Current	Power Out Voltage > Power In Voltage	A	1.0 typ
Output-to Input Parasitic Diode, Pulsed Current Per Amp Of Rated Current	Power Out Voltage > Power In Voltage Pulse Width ≤ 100 µS	A	4.0 typ

TABLE 3. SSP-21120 SPECIFICATIONS (SEE NOTES 1 AND 2)			
PARAMETER	CONDITIONS	UNIT	VALUE
POWER CIRCUIT (continued)			
Output-to Input Parasitic Diode, Forward Voltage at Continuous Current	Power Out Voltage > Power In Voltage	V	2.0 max
Isolation Resistance, Any Pin to Case	Pin-to-Case Voltage = 100 Vdc	MΩ	50 min
Isolation Resistance Power Ground to Signal Ground	Power Ground to Signal Ground Voltage = 50 Vdc	MΩ	50 min
Voltage Drop	across stud 1 and 2	Vdc	0.25 max
Trip Characteristics	see FIGURE 2		
Response Time	see FIGURE 3		
TEMPERATURE RANGE			
Operating (Base plate)		°C	-55 to +85
Storage		°C	-55 to +125
THERMAL RESISTANCE			
Case to Sink (θ_{CS})		°C/W	0.1 max
Case to Ambient (θ_{CA})		°C/W	10 max
Temperature Rise, Junction-to-Case	Rated Load	°C	10
PHYSICAL CHARACTERISTICS	see FIGURE 4		
Size		oz	18 max
Weight		g	510.3 max

Notes:
1. -55°C ≤ Case Temperature ≤ 85°C.
2. 'A' is Amps of Rated Module Current.
3. Power Ground = neutral; Bias Supply Common = Signal Ground
4. Control Input must never be left floating.

TABLE 4.			
PART NUMBER	I-MAX*(Amps)	'ON' RESISTANCE (Ohms)**	POWER DISSIPATION (Watts)**
SSP21120-040***	40	0.0063	12.0
SSP21120-060***	60	0.0042	17.0
SSP21120-080	80	0.0032	22.0

* I-MAX is the maximum continuous current.
** Specified for -55°C to +85°C.
*** Contact factory for availability.
Note: Other Amp ratings are available, consult factory.

FUNCTIONAL DESCRIPTION

The SSP-21120 series of Solid-State Power Controller Modules incorporate the wire protection feature of electromechanical circuit breakers and the reliability of solid-state relays. In addition to the solid-state relays input logic compatibility, the SSP-21120 series provide logic compatible status outputs.

A TTL/CMOS compatible input provides external control of the power switch's "ON/OFF" state. A logic high on this control input turns the power to the load "on." A logic low will turn the power switch off, which removes power from the load.

In the event of an overload, the SSP-21120 series will trip, just like a circuit breaker, and automatically remove power from the load. In order to turn back on, the control input must be brought to a logic low, and then returned to a logic high state.

As in a circuit breaker, the SSPC's time to trip depends on the current level. Slight overloads will cause longer trip times. Heavy overloads will cause shorter trip times. The fault ("Instant Trip") and I^2T trip curve, FIGURE 2, shows the trip time as a function of current for a single trip or repetitive trips with at least 10 milli-seconds between trip and turn on. Attempts to repeatedly turn on into an overload will result in the thermal memory shortening each trip time. This "memory" protects the wire, load, and the Solid-State Power Controller module.

The status lines are TTL/CMOS compatible outputs which reflect the state of the SSPC, the load and the Built-In-Test (BIT) circuits. The status permits an external subsystem to monitor and ultimately control the SSPC. TABLE 5 defines the status lines' states which indicate the various states of the SSPC. Further explanation of the status lines appears in the applications information section.

The SSP-21120 series are characterized by their current rating and maximum "on" resistance listed in TABLE 4. These parameters are established by the number of Power FETs placed in parallel within the FET Hybrid.

The trip function is implemented by two separate circuits, a true I^2T trip comparator and a short circuit fault comparator. They are independent of each other but work together to protect the system.

If the load current is less than 110% of rated current, the SSPC will never trip. If the load current is greater than 145%, the SSPC will always trip.

For load currents less than 600%, the trip time can be found from FIGURE 2 by drawing a horizontal line on FIGURE 2 at the current level of interest. The SSPC will always trip at a time between the two curves. This is true I^2T tripping.

When the SSPC trips in accordance with the I^2T characteristics, the fall time is 200 µs, maximum.

For load currents greater than 1000%, the SSPC will turn off in less than 25 µs. Between 600% and 1000%, the SSPC will turn off in a time less than the"max. trip limit" shown in FIGURE 2 and may turn off in less than 25 µs.

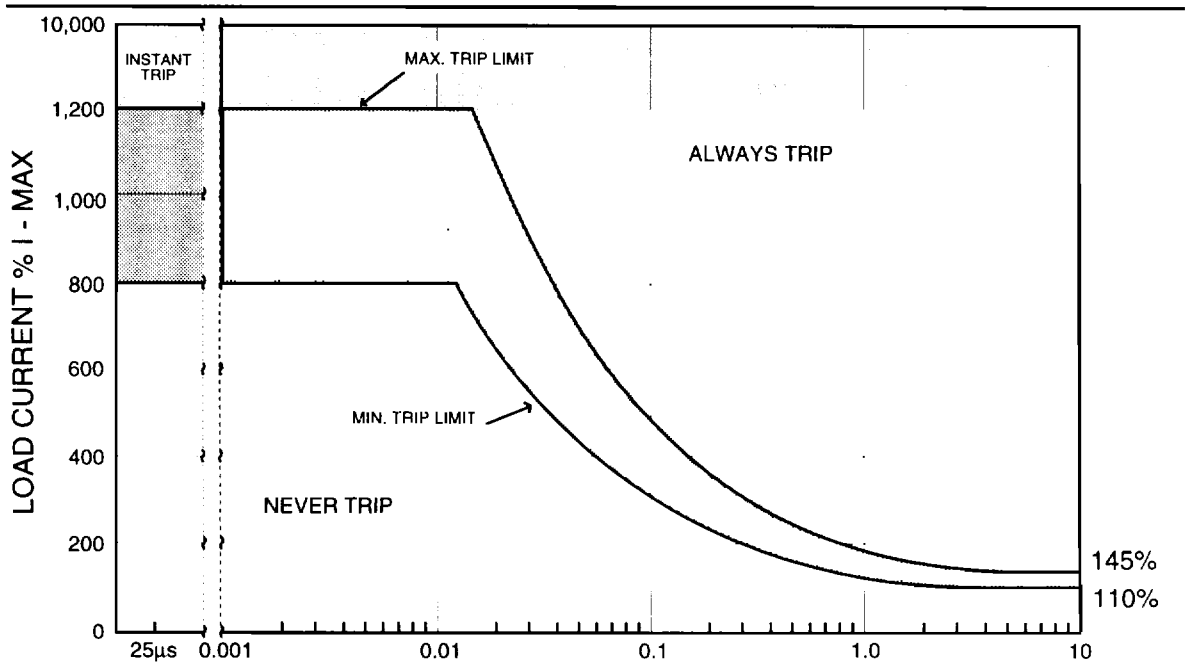

FIGURE 2. TRIP CHARACTERISTICS

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When the SSPC turns off under these fault conditions, the fall time is less than 25 µs. While the SSPC will always turn off in less than 25 µs when the load current is greater than 1000%, the actual current may 'spike' to a value higher than 1000% due to circuit delays. The MOSFETs inherently self-limit the maximum current, depending on the number of MOSFETs and their rating.

During turn-on and turn-off the rise and fall time of the output voltage is controlled to be less than 200 µs. This value is a compromise between faster response time with a greater amount of RFI and EMI generated, and slower response time with less RFI and EMI but greater power dissipated in the SSPC during transitions. Since the Power MOSFET switches are not saturated during transitions the switching power dissipation is much greater than the static dissipation, and longer transitions result in a larger temperature rise. If the SSPC is rapidly turned on and off, the high average dissipation could result in a significant temperature rise in the SSPC. For this reason do not turn the SSPC off and on more rapidly than 30 msec. This will limit the maximum temperature of the switches to a safe level.

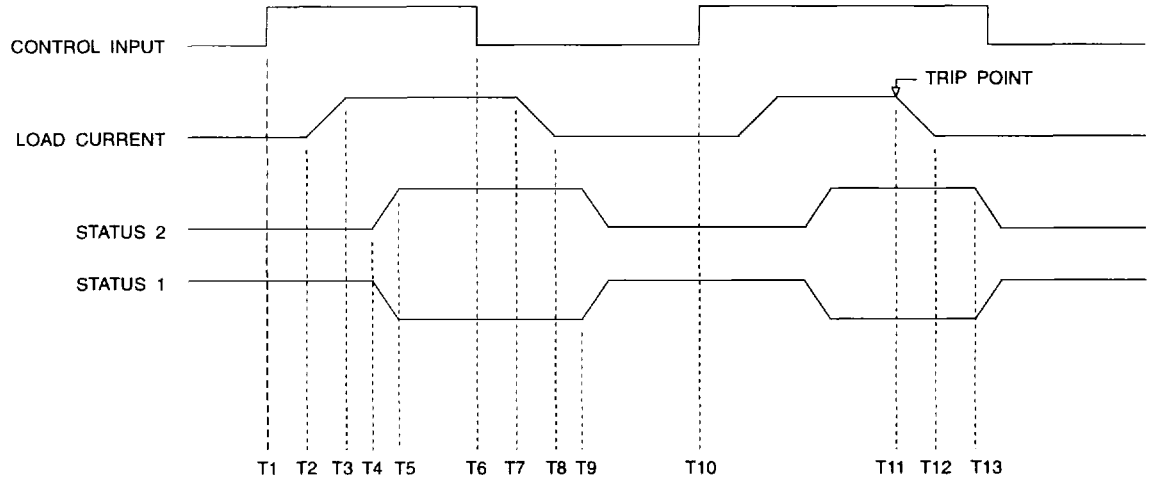
The SSP-21120 has been designed to derive its internal power requirements from the bias supply input (+5 Vdc).

APPLICATIONS INFORMATION

SELECTION

The selection of a proper sized SSPC is essential for protection of the wire and load. This selection should be based on the steady state and transient overload currents.

The shape of the trip curve (I^2T) is selected as optimum to protect the system wiring. The power dissipated in the wire is the wire resistance times the load current squared, and the temperature of the wire is determined by the length of time that this power is being dissipated. This makes the wire temperature proportional to the current squared times the on time. Since the trip curve follows this same characteristic the SSPC can accurately predict the wire temperature rise as a result of overloads and remove load current before the wiring is damaged from overtemperature. Of course, the wire I^2T product should be greater than the SSPC I^2T product for the SSPC to protect the wire.



SOLID-STATE POWER CONTROLLER TIMING AT 28Vdc.				
TIME	DESCRIPTION	MAXIMUM	UNIT	NOTES
T1-T2	TURN-ON DELAY	150	µs	
T2-T3	CURRENT RISE TIME	200	µs	
T1-T4	STATUS 1 & STATUS 2 TURN-ON DELAY	7.5	ms	
T4-T5	STATUS 1 & STATUS 2 RISE AND FALL TIME	350	ns	
T6-T7	TURN-OFF DELAY	130	µs	
T7-T8	CURRENT FALL TIME	200	µs	
T6-T9	STATUS 1 & STATUS 2 TURN-OFF DELAY	5.0	ms	
T10-T11	TRIP TIME AFTER TURN ON	SEE FIG. 2	s	
T11-T12	CURRENT FALL TIME AFTER TRIP	200	µs	LOAD CURRENT < 600%
T11-T12	CURRENT FALL TIME AFTER TRIP	25	µs	LOAD CURRENT > 1000%
T11-T13	TRIP TURN-OFF STATUS 1 DELAY	5.0	ms	

FIGURE 4. SOLID-STATE POWER CONTROLLER TIMING

PRECAUTIONS

When a short circuit causes turn off of the SSPC, precautions have to be taken to limit the transient voltages generated by the wire inductance. The magnitude of this voltage is L*di/dt where "L" is the wire inductance in Henries and "di/dt" is the rate of change of output current. If the SSPC turns off in 10 µsec from a 250 amp overload (300% for 80 amp unit) with a wire inductance of only 10 µH it would generate a spike of 250 volts. This exceeds the voltage rating of the MOSFETs. In order to provide protection from these transients, transient voltage suppressors should be used between the SSPC Neutral and the Power In and between the SSPC Neutral and Power Out terminals. The rating of the transient voltage suppressors should be selected so that at the maximum expected short circuit current, the transient voltage suppressor voltage drop would not exceed the SSPC voltage rating, and the power to be dissipated can be safely absorbed without transient suppressor failure.

While circuit inductance can cause high voltage transients during turn off, lack of circuit inductance can cause current transients prior to turn off. If the output of the SSPC is shorted and there is no circuit inductance, the current from the source can rise instantaneously to a high value. The SSPC will limit the current to about 100 times its rating (10,000%). Circuit inductance will limit the rate of rise of this current. The SSPC can take 25 µs to turn off. The current will always overshoot the 1000% maximum level of the SSPC due to this 25 µs delay. If the current rises slowly due to circuit inductance, the overshoot will be negligible; if the current rises quickly, the overshoot will be more significant. In any case, the current spike will be less than 25 µs.

In most real applications, there will always be significant circuit inductance. The problem to guard against is voltage transients, not current transients.When testing individual SSPCs, be careful to simulate actual system conditions.

POWER-ON RESET

When the POWER IN is first applied, the SSPC will be "off" regardless of the CONTROL CMD input. When the CONTROL CMD input is a logic low, the SSPC can be turned "on" by bringing the CONTROL CMD to a logic high. If the CONTROL CMD input is at a logic high when power is applied, the SSPC may be turned "on" by cycling the CONTROL CMD input to a logic low and then to a logic high. The system controller can be programmed to do this cycling of the CONTROL CMD input. Subsequent loss of the POWER IN causes the SSPC to turn "off." Re-application of the POWER IN again causes a power-on reset. Loss of power to the BIAS SUPPLY INPUT terminals does not turn "off" the SSPC and re-application of this power does not cause a power-on reset.

STATUS CODES

This section contains a fuller explanation of the conditions and meaning of the status codes shown in TABLE 5. Each paragraph number corresponds to the STATE in TABLE 5.

The first four conditions show the control input has commanded the SSPC to be off.

1) The SSPC has failed. STATUS 1 indicates the load is drawing current but the SSPC should be off.

2) The SSPC has failed. STATUS 1 indicates the load is drawing current; STATUS 2 indicates the Power MOSFET switch is on; the SSPC should be off.

3) Normal off condition. STATUS 1 indicates the load is not drawing current; STATUS 2 indicates the Power MOSFET switch is off.

4) The SSPC has failed or STATUS 2 has shorted to the bias supply. STATUS 1 indicates the load is not drawing current; STATUS 2 indicates the Power MOSFET is on; the SSPC should be off. Also this status is generated if POWER IN is lost.

The next four conditions show the control input has commanded the SSPC to be on.

5) The SSPC has failed or there is a short to ground on the STATUS 2 output. STATUS 1 indicates the load is drawing current but STATUS 2 indicates the Power MOSFET switch is off.

6) Normal on condition. STATUS 1 indicates the load is drawing current and STATUS 2 indicates the Power MOSFET switch is on.

7) Tripped condition. STATUS 1 indicates the load is not drawing current and STATUS 2 indicates the Power MOSFET switch if off. The SSPC can be turned back on by cycling the input control to a logic low and then back to a logic high. If the excessive load has not been removed, the SSPC will trip again.

8) No load current. STATUS 1 indicates the load is not drawing current; STATUS 2 indicates the Power MOSFET switch is on. Also this status is generated if POWER IN is lost.

TABLE 5

STATE	INPUT CONTROL CMD	OUTPUT STATUS 1 (see note 2)	OUTPUT STATUS 2 (see note 3)	POWER CONTROLLER AND LOAD STATUS
1	L	L	L	SSPC failure.
2	L	L	H	Load "on"; showing SSPC failure.
3	L	H	L	Load "off"; showing normal "off" condition.
4	L	H	H	SSPC failure or STATUS 2 shorted to bias supply or POWER IN lost.
5	H	L	L	SSPC failure or short to ground on STATUS 2 line.
6	H	L	H	Load "on" showing normal "on" condition.
7	H	H	L	Load "off"; showing "trip" (see note 1).
8	H	H	H	Normal power out with load < 5% of rated SSPC current or POWER IN lost.

Notes:
1) Any trip condition per FIGURE 2.
2) STATUS 1 indicates a logic low.
Less then 5% guarantees a logic low; more then 15% guarantees a logic high.
3) STATUS 2 indicates a logic high when the Power MOSFET switch is on.

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LOADS

The SSP-21120 series can be used with any type of load: any combination of inductive, resistive, and capacitive. In addition, they can be used with dc motors and lamps.

Inductive loads require protecting the SSPC against voltage transients. See the section on Precautions above on page 5.

Capacitive loads require comparing the load inrush current to the trip curve of FIGURE 2. The inrush current must be below the minimum trip curve to avoid tripping on the inrush current.

Capacitive loads can present a discharge problem. The SSPCs use Power MOSFETs as the switching element. The MOSFETs contain a parasitic diode which will be forward biased if the SSPC power output terminal is more positive than the power input terminal. If the 28 Vdc source is turned off while a charge is held on the capacitive load, this diode will turn on and discharge the load through the generator. The SSPC can carry a reverse current equal to its forward current rating; however, the dissipation with reverse current is up to seven times the forward current dissipation for the same current. The user must ensure that the maximum case temperature is not exceeded.

Incandescent lamps must be treated like capacitive loads for inrush current. Since they do not store charge, they do not present a discharge problem.

DC motors also must be treated like capacitive loads for inrush current. If they continue rotating when power is removed, reverse current is a possibility due to back EMF. Voltage transients must also be considered when using dc motors as loads on SSPCs.

HEATSINKING

The SSP-21120 series are designed so that the junction temperature can never exceed its maximum rating if the case temperature is held to +85°C or less. Heatsinking is recommended to keep the case temperature to +85°C when operating at high ambient temperatures. The SSPCs may be operated at room temperature without a heat sink. The maximum ambient temperature, T_A, for operation without a heat sink is 85 - P_d x θ_{CA} (where P_d is the power dissipation from TABLE 4 and θ_{CA} is the thermal resistance from case-to-ambient from TABLE 3).

The same expression is used for finding the maximum ambient temperature with a heat sink except θ_{CA} is now the sum of the thermal resistance from case-to-sink and from sink-to-ambient.

NO OFFSET VOLTAGE

The Power MOSFET used in the DDC SSPCs have no inherent voltage offset. The voltage drop across the Power MOSFET is solely dependent on the current flowing through the device and its "ON" resistance.

Bipolar transistors, on the other hand, have an inherent dc offset voltage to which is added a voltage drop proportional to the devices' "ON" resistance and the current flowing through it. It is this inherent offset voltage that is missing from the power MOSFET. The Power MOSFET in many applications, leads to lower voltage drop and power dissipation as an SSPC switch. In addition the Power MOSFETs driver logic requirements are much simpler, especially when multiple MOSFETs are used, as in the SSPC product.

NO SECONDARY BREAKDOWN, AND PARALLELING SSPCS

A bipolar transistor has a set of current-voltage limits that form an envelope that cannot be exceeded; this is known as the safe operating area of the device. If this envelope is exceeded local hot spots will occur. These hot spots conduct currents more readily then adjacent cool areas and tend to become hotter. This thermal runaway leads to the ultimate destruction of the device; called secondary breakdown.

The Power MOSFETs have the opposite characteristics from that of thermal runaway in bipolar devices. A local hot-spot will steer current away from itself as its resistance in this area goes up. This results in even current sharing throughout the entire device, thereby eliminating hot-spots. The inherent advantage of not having secondary breakdown is that the entire MOSFET has to exceed its temperature limitations before damage results. This characteristic makes the Power MOSFET more rugged when used for power switching then bipolar devices.

Due to the current sharing aspects of the power MOSFET, they can be placed in parallel and share the load equally.

ISOLATION OF CONTROL AND STATUS

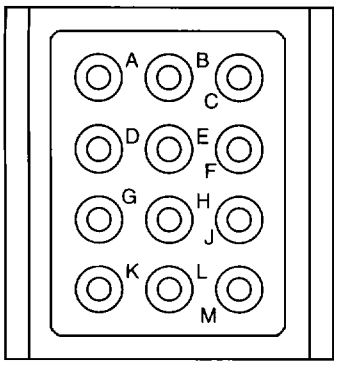
The SSPC was designed with isolation between the load power and the five volt control logic input and the status outputs. This is necessary to prevent noise caused by transients or power spikes on the power line from adversely affecting the operation of the SSPC. Therefore the case, POWER IN, and Control Circuit are all electrically isolated. FIGURE 1, SSPC BLOCK DIAGRAM, shows this isolation as the "ISOLATED CONTROL CIRCUIT"; also notice the separation of the power (neutral) ground and signal (bias supply common) ground.

The electrical isolation is supported by an internal power oscillator that electrically isolates separate internal power supplies that will power the internal analog and digital monolithics. This isolation prevents load or logic ground loops from affecting the proper operation of the SSPC. The isolation also insures that a fault of the switch (MOSFET) could never propagate back into the SSPC logic or cause damage to the logic side.

OPTIONS

The following characteristics can be factory modified on special orders:

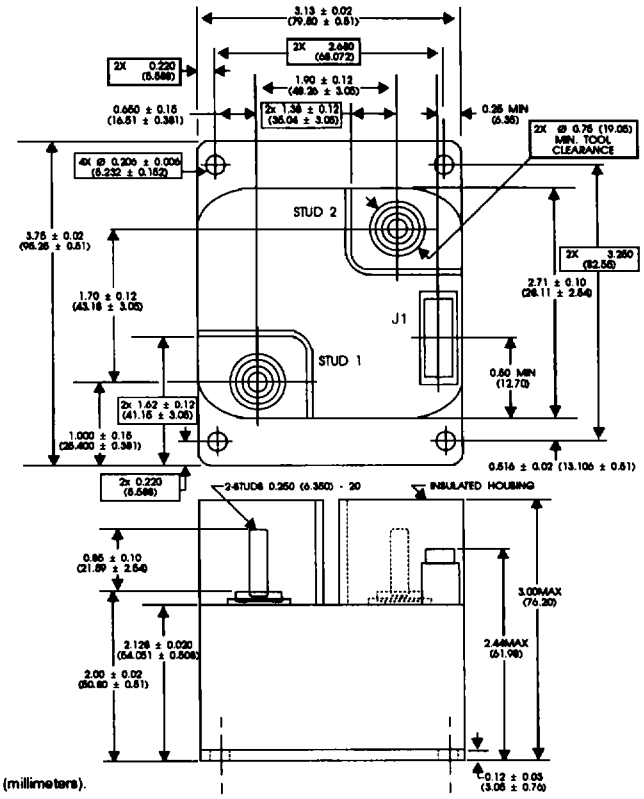
- I^2T TRIP CURVE: K-factor adjustments
- OUTPUT RISE AND FALL TIMES :Turn-Off and Turn-On time can be factory modified. (e.g., capacitive loads.)
- CURRENT RANGE
- CUSTOM PACKAGING



PIN FUNCTIONS	
POWER IN and POWER OUT Terminals	
PIN	**FUNCTION**
STUD 1	POWER IN
STUD 2	POWER OUT
Control Interface Connector - J1	
PIN	**FUNCTION**
A and D	NEUTRAL (POWER GROUND)
B and E	BIAS SUPPLY INPUT
C and F	BIAS SUPPLY COMMON (SIGNAL
G and K	CONTROL COMMAND
H and L	STATUS 1 (STATUS)
J and M	STATUS 2 (BIT/TRIP)

Note: 1. The pairs of pins listed above are electrically connected inside the module.
2. Supplied with Deutsch CTS S20/20 push-in wire pins for the J1 terminal.

FIGURE 4. CONTROL INTERFACE CONNECTOR - J1



Dimensions are in inches (millimeters).

FIGURE 5. MECHANICAL OUTLINE

ORDERING INFORMATION

SSP-21120-080-X

Reliability grade:
B = Hybrids Screened to MIL-PRF-38534 but without QCI testing.
Blank = Standard DDC procedures.

Note: Consult factory for other current ranges.

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