Description

The VE16418165B and VE26418165B are 1M×64-bit and 2M×64-bit dual-in-line dynamic RAM modules(DIMM). It is mounted by 4/8 pieces of 1M×16 DRAM (VG26V18165BB), and each in a standard 42 pin plastic SOJ packages. The VE16418165B and VE26418165B makes high density possible without utilizing the surface mount technology on the printed circuit board. Decoupling capacitors are mounted on power supply line for noise reduction.

Features

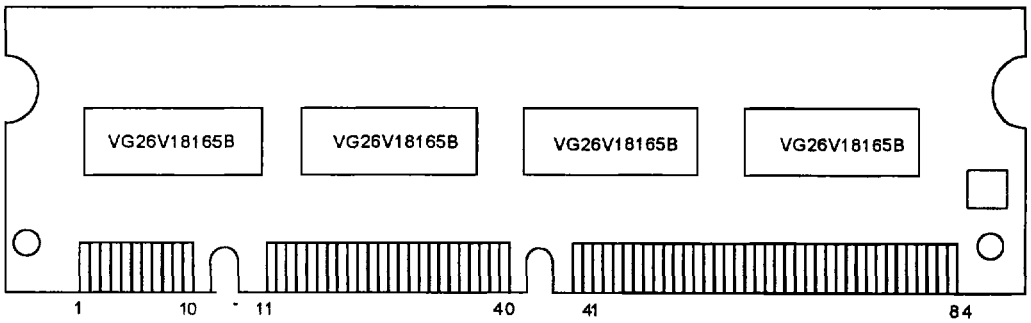
VE16418165B:

- 1,048,576 word by 64 bits organization
- Single 3.3V (±10%) power supply
- High speed t_{RAC} access time : 60/70ns(max)
- Low power dissipation
  - Active mode : 2.59/2.45 W(Max)
  - Standby mode : 7.2mW(Max)
- Extended-data-out (EDO) page mode capability
- LVTTL compatible I/O levels
- 1024 refresh cycles during a 16 ms period
- Multiple refresh modes capability
  $\overline{RAS}$ only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, and hidden refresh
- 168 pin Dual in-line memory module
- JEDEC Standard pinout

VE26418165B:

- 2,097,152 word by 64 bits organization
- Single 3.3V (±10%) power supply
- High speed t_{RAC} access time : 60/70ns(max)
- Low power dissipation
  - Active mode : 2.62/2.48 W(Max)
  - Standby mode : 14.4mW(Max)
- Extended-data-out (EDO) page mode capability
- LVTTL compatible I/O levels (Vcc=3.3V)
- 1024 refresh cycles during a 16 ms period
- Multiple refresh modes capability
  $\overline{RAS}$ only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh and hidden refresh
- 168 pin Dual in-line memory module
- JEDEC Standard pinout

Pin assignment (Front View)

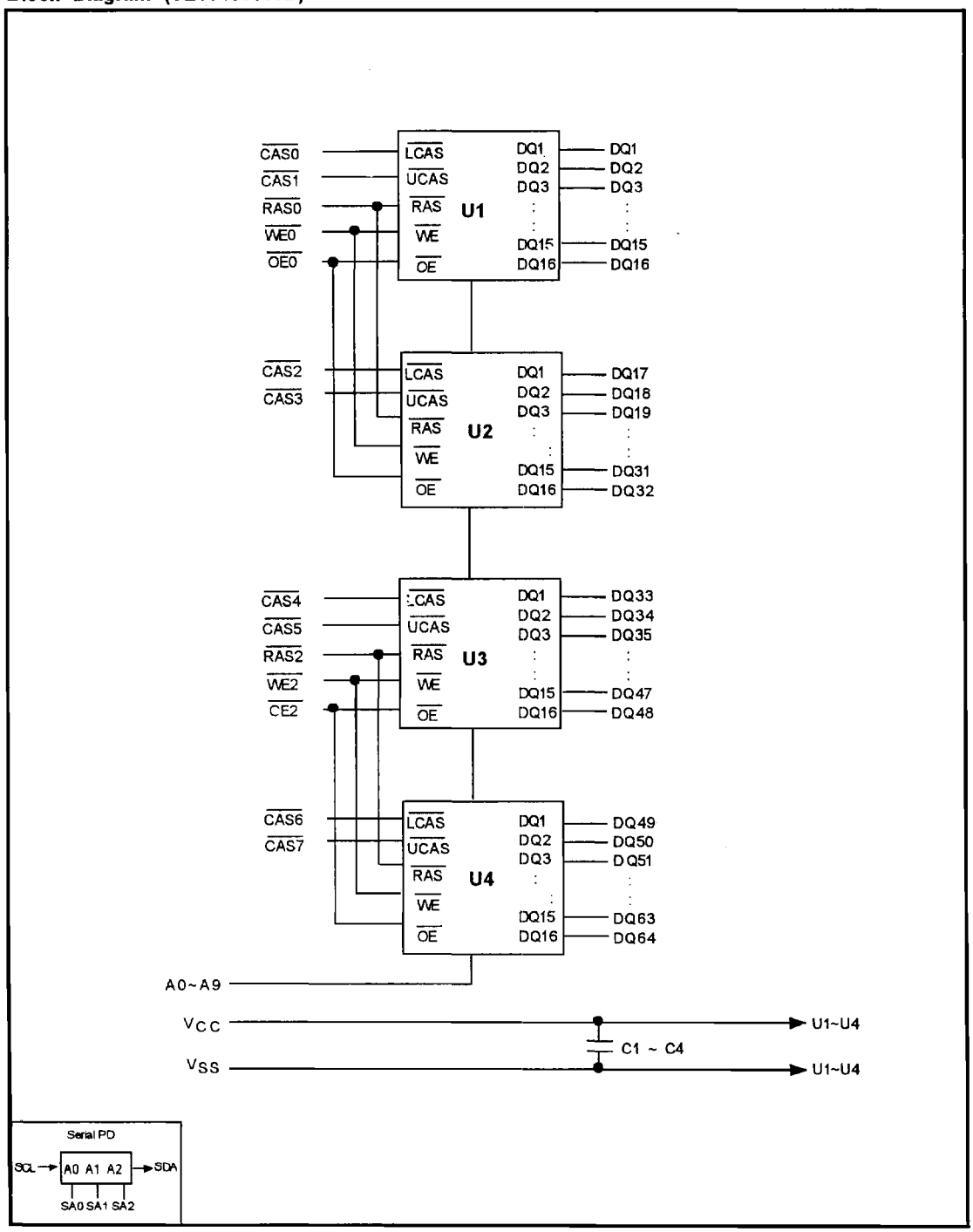


Pin Out

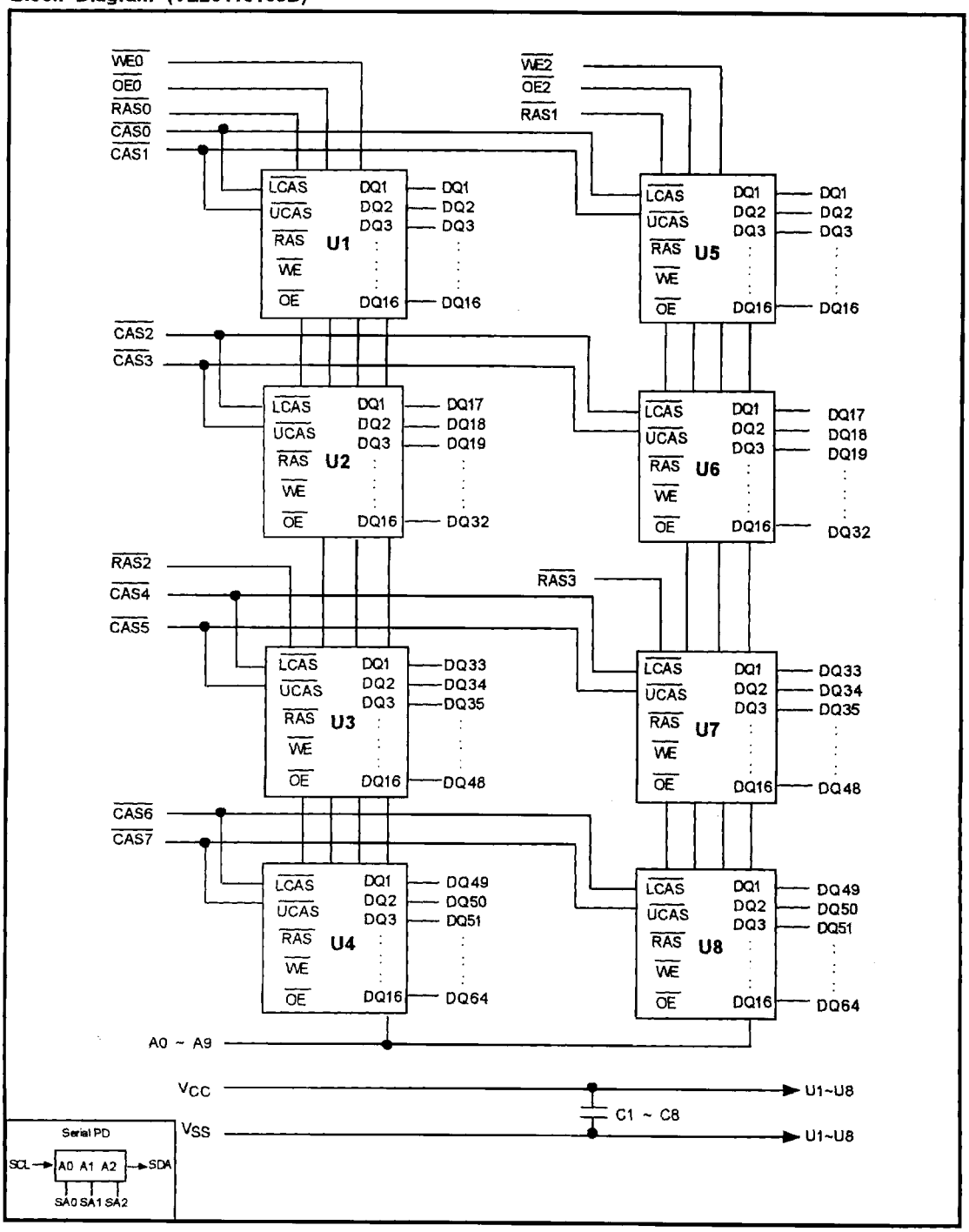
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	22	NC	43	V_{SS}	64	V_{SS}	85	V_{SS}	106	NC	127	V_{SS}	148	V_{SS}
2	DQ1	23	V_{SS}	44	$\overline{OE2}$	65	DQ22	86	DQ33	107	V_{SS}	128	DU	149	DQ54
3	DQ2	24	NC	45	$\overline{RAS2}$	66	DQ23	87	DQ34	108	NC	129	NC/*$\overline{RAS3}$	150	DQ55
4	DQ3	25	NC	46	$\overline{CAS2}$	67	DQ24	88	DQ35	109	NC	130	$\overline{CAS6}$	151	DQ56
5	DQ4	26	V_{CC}	47	$\overline{CAS3}$	68	V_{SS}	89	DQ36	110	V_{CC}	131	$\overline{CAS7}$	152	V_{SS}
6	V_{CC}	27	$\overline{WE0}$	48	$\overline{WE2}$	69	DQ25	90	V_{CC}	11	DU	132	DU	153	DQ57
7	DQ5	28	$\overline{CAS0}$	49	V_{CC}	70	DQ26	91	DQ37	112	$\overline{CAS4}$	133	V_{CC}	154	DQ58
8	DQ6	29	$\overline{CAS1}$	50	NC	71	DQ27	92	DQ38	113	$\overline{CAS5}$	134	NC	155	DQ59
9	DQ7	30	$\overline{RAS0}$	51	NC	72	DQ28	93	DQ39	114	NC/*$\overline{RAS1}$	135	NC	156	DQ60
10	DQ8	31	$\overline{OE0}$	52	NC	73	V_{CC}	94	DQ40	115	DU	136	NC	157	V_{CC}
11	DQ9	32	V_{SS}	53	NC	74	DQ29	95	DQ41	116	V_{SS}	137	NC	158	DQ61
12	V_{SS}	33	A0	54	V_{SS}	75	DQ30	96	V_{SS}	117	A1	138	V_{SS}	159	DQ62
13	DQ10	34	A2	55	DQ17	76	DQ31	97	DQ42	118	A3	139	DQ49	160	DQ63
14	DQ11	35	A4	56	DQ18	77	DQ32	98	DQ43	119	A5	140	DQ50	161	DQ64
15	DQ12	36	A6	57	DQ19	78	V_{SS}	99	DQ44	120	A7	141	DQ51	162	V_{SS}
16	DQ13	37	A8	58	DQ20	79	NC	100	DQ45	121	A9	142	DQ52	163	NC
17	DQ14	38	A10	59	V_{CC}	80	NC	101	DQ46	122	A11	143	V_{CC}	164	NC
18	V_{CC}	39	A12	60	DQ21	81	NC	102	V_{CC}	123	A13	144	DQ53	165B	SA0
19	DQ15	40	V_{CC}	61	NC	82	SDA	103	DQ47	124	V_{CC}	145	NC	166	SA1
20	DQ16	41	V_{CC}	62	DU	83	SCL	104	DQ48	125	DU	146	DU	167	SA2
21	NC	42	DU	63	NC	84	V_{CC}	105	NC	126	DU	147	NC	168	V_{CC}

Note : NC=No connect, DU=Don't Use.* : 2M×64 Version

Block Diagram (VE16418165B)



Block Diagram (VE26418165B)



Truth Table

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES		DQ_S	Notes
						ROW	COL		
STANDBY		H	H→X	X	X	X	X	High-Z	
READ		L	L	H	L	ROW	COL	Data-Out	
WRITE (EARLY WRITE)		L	L	L	X	ROW	COL	Data-In	
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out,Data-In	
EDO PAGE	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out	
MODE READ	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out	
EDO PAGE MODE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In	
WRITE	2nt Cycle	L	H→L	L	X	n/a	COL	Data-In	
EDO PAGE MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out,Data In	
READ WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data In	
HIDDEN	READ	L→H→L	L	H	L	ROW	COL	Data-Out	
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data-In	1
$\overline{RAS}$ ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z	
CBR REFRESH		H→L	L	X	X	X	X	High-Z	

Notes: 1.EARLY WRITE ONLY

Absolute Maximum Ratings

Parameter	Symbol	Value		Unit
Voltage on any pin relative to Vss	V_T	-0.5 to +4.6		V
Supply voltage relative to Vss	V_{CC}	-0.5 to +4.6		V
Short circuit output current	I_{OUT}	50		mA
Power dissipation	P_D	1M×64	4	W
		2M×64	8	
Operating temperature	T_{OPT}	0 to +70		℃
Storage temperature	T_{STG}	-55 to +125		℃

Recommended DC Operating Conditions

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Input High Voltage, all inputs	V_{IH}	2.0	–	Vcc+0.3	V
Input Low Voltage, all inputs	V_{IL}	-0.3	–	0.8	V

Capacitance

Ta=25℃,V_{CC}=3.3V±10% , f=1MHZ

Parameter		Symbol	Size	Typ	Max	Unit	Note
Input capacitance(Address)		C_{I1}	1M×64	-	61	pF	1
			2M×64	-	81		
Input capacitance	($\overline{RAS0}$, $\overline{RAS2}$)	C_{I2}	1M×64	-	51	pF	1
	($\overline{RAS0}$ ~ $\overline{RAS3}$)		2M×64	-	51		
Input capacitance ($\overline{CAS0}$ ~ $\overline{CAS7}$)		C_{I3}	1M×64	-	24	pF	1
			2M×64	-	31		
Input Capacitance ($\overline{WE}$)		C_{I4}	1M×64	-	54	pF	1
			2M×64	-	68		
Input Capacitance ($\overline{OE}$)		C_{I5}	1M×64	-	36	pF	1
			2M×64	-	50		
Output capacitance (Data-in,Data-out)		$C_{I/O}$	1M×64	-	18	pF	1,2
			2M×64	-	25		

Notes : 1. Capacitance measured with effective capacitance measuring method.

2. $\overline{RAS}$, $\overline{CAS}$ = V_{IH} to disable Dout.

DC Characteristics

(Ta=0 to 70°C, V_{CC}=+3.3V±10%, V_{SS}=0V)

Parameter	Symbol	Test Conditions	size	-6		-7		Unit	Notes
				Min	Max	Min	Max		
Operating current	I_{CC1}	$\overline{RAS}$ cycling $\overline{CAS}$ cycling t_{RC}=min.	1M×64 2M×64	-	720 728	-	680 688	mA	1,2
Standby Current	I_{CC2}	TTL interface $\overline{RAS}$, $\overline{CAS}$=V_{IH} Dout=High-Z	1M×64 2M×64	-	8 16	-	8 16	mA	
		CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≧Vcc-0.2V Dout=High-Z	1M×64 2M×64	-	2 4	-	2 4	mA	
$\overline{RAS}$-only refresh current	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH} t_{RC}=min.	1M×64 2M×64	-	720 728	-	680 688	mA	1,2
EDO page mode current	I_{CC4}	t_{PC}=min.	1M×64 2M×64	-	400 408	-	360 368	mA	1,3
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC5}	t_{RC}=min. $\overline{RAS}$, $\overline{CAS}$ cycling	1M×64 2M×64	-	720 728	-	680 688	mA	1,2
Input leakage current	I_{LI}	0V≦Vin≦Vcc+0.3V	1M×64 2M×64	-20 -40	20 40	-20 -40	20 40	μA	
Output leakage current	I_{LO}	0V≦Vout≦Vcc+0.3V Dout=Disable	1M×64 2M×64	-20 -40	20 40	-20 -40	20 40	μA	
Output high voltage	V_{OH}	I_{OH}=-2mA	1M×64 2M×64	2.4 2.4	- -	2.4 2.4	- -	V	
Output low voltage	V_{OL}	I_{OL}=+2mA	1M×64 2M×64	-	0.4 0.4	-	0.4 0.4	V	

Notes :

1. I_{CC} is specified as an average current. It depends on output loading condition and cycle rate when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ =V_{IL}.
3. For I_{CC4} , address can be changed once or less within one EDO page mode cycle time.

AC Characteristics

(Ta =0 to +70°C,V_{CC}=3.3V±10%,V_{SS}=0V)Notes*1,*2,*3

Test conditions

- Input rise and fall times:2ns
- Input timing reference levels :
  V_{IH}=2.0V, V_{IL}=0.8V
- Output timing reference levels :
  V_{OH}=2.0V, V_{OL}=0.8V

Read,Write and Refresh Cycles
(Common Parameters)

Parameter	Symbol	-6		-7		Unit	Notes
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110	-	130	-	ns	
$\overline{RAS}$ precharge time	t_{RP}	40	-	50	-	ns	
$\overline{CAS}$ precharge time in normal mode	t_{CPN}	10	-	10	-	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	ns	4
$\overline{CAS}$ pulse width	t_{CAS}	10	10000	12	10000	ns	5
Row address setup time	t_{ASR}	0	-	0	-	ns	
Row address hold time	t_{RAH}	10	-	10	-	ns	
Column address setup time	t_{ASC}	0	-	0	-	ns	6
Column address hold time	t_{CAH}	10	-	15	-	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	42	20	50	ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	-	35	-	ns	
$\overline{RAS}$ hold time	t_{RSH}	15	-	18	-	ns	
$\overline{CAS}$ hold time	t_{CSH}	50	-	60	-	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	-	5	-	ns	7
Transition time (rise and fall)	t_T	1	50	1	50	ns	8
Refresh period	t_{REF}	-	16	-	16	ms	
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0	-	0	-	ns	
$\overline{OE}$ to Din delay time	tOED	15		18		ns	

Read Cycle

Parameter	Symbol	-6		-7		Unit	Notes
		Min	Max	Min	Max		
Access time from $\overline{RAS}$	t_{RAC}	-	60	-	70	ns	9
Access time from $\overline{CAS}$	t_{CAC}	-	18	-	20	ns	10,11
Access time from column address	t_{AA}	-	30	-	35	ns	11,12
Read command setup time	t_{RCS}	0	-	0	-	ns	4
Read command hold time to $\overline{CAS}$	t_{RCH}	0	-	0	-	ns	7,13
Read command hold time to $\overline{RAS}$	t_{RRH}	10	-	10	-	ns	13
Output buffer turn-off time	t_{OFF}	0	15	0	18	ns	14
Access time from $\overline{OE}$	tOEA	-	15	-	18	ns	
Output buffer turn-off time from $\overline{OE}$	tOEZ	0	15	0	18	ns	14

Write Cycle

Parameter	Symbol	-6		-7		Unit	Notes
		Min	Max	Min	Max		
Write command setup time	t_{WCS}	0	-	0	-	ns	4
Write command hold time	t_{WCH}	10	-	10	-	ns	
Write command pulse width	t_{WP}	10	-	10	-	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15	-	18	-	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15	-	18	-	ns	
Data-in setup time	t_{DS}	0	-	0	-	ns	
Data-in hold time	t_{DH}	10	-	15	-	ns	
$\overline{WE}$ to Data-in delay	t_{WED}	10	-	10	-	ns	

Refresh Cycle

Parameter	Symbol	-6		-7		Unit	Notes
		Min	Max	Min	Max		
$\overline{CAS}$ setup time(CBR refresh)	t_{CSR}	10	-	10	-	ns	
$\overline{CAS}$ hold time (CBR refresh)	t_{CHR}	10	-	10	-	ns	7
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5	-	5	-	ns	4

EDO Page Mode Cycle

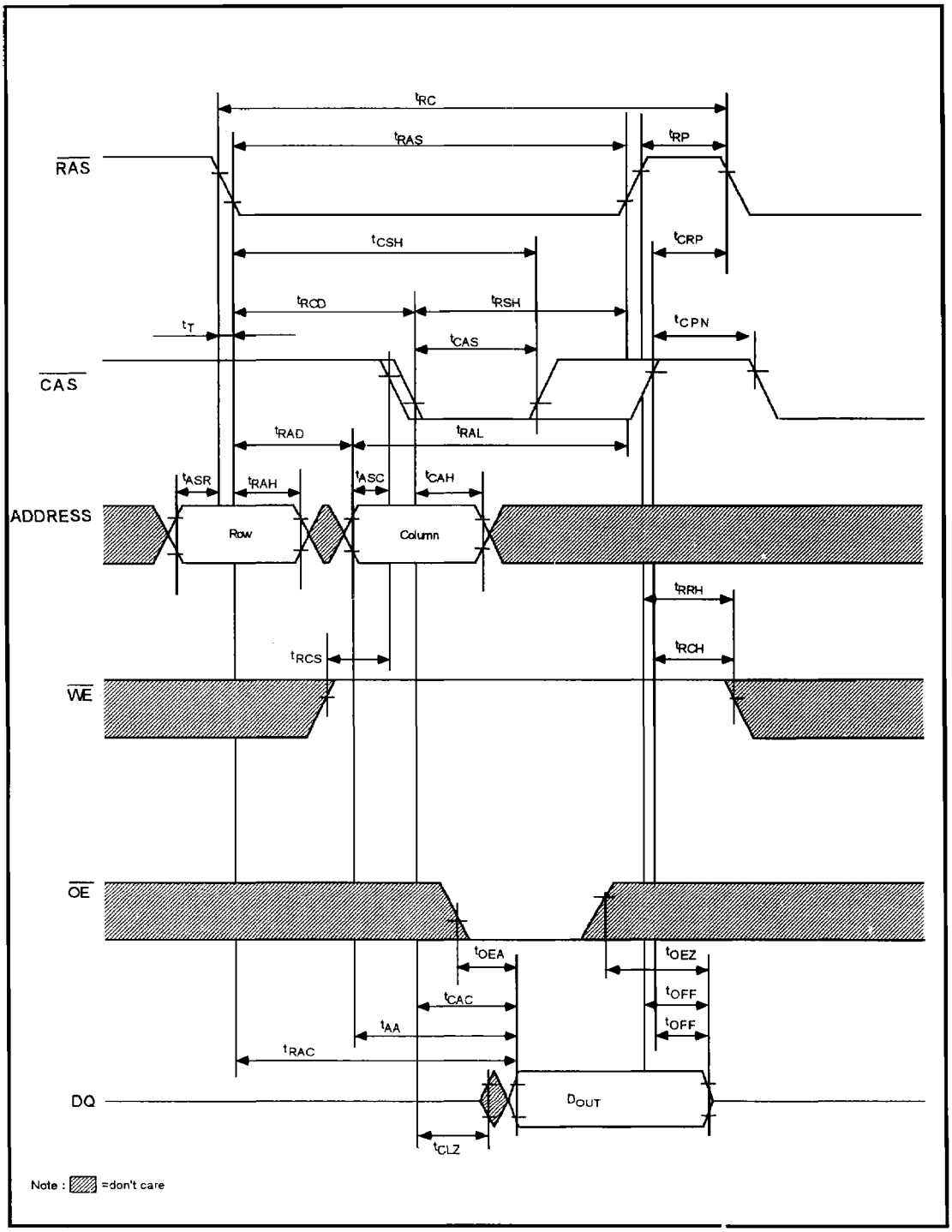
Parameter	Symbol	-6		-7		Unit	Notes
		Min	Max	Min	Max		
EDO page mode cycle time	t_{PC}	25	-	30	-	ns	
EDO page mode $\overline{CAS}$ precharge time	t_{CP}	10	-	10	-	ns	
EDO page mode $\overline{RAS}$ pulse width	t_{RASP}	60	10^5	70	10^5	ns	15
Access time from $\overline{CAS}$ precharge	t_{CPA}	-	35	-	40	ns	7,11
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{CPRH}	35	-	40	-	ns	
$\overline{OE}$ high hold time from $\overline{CAS}$ high	t_{OEHC}	5	-	5	-	ns	
$\overline{OE}$ high pulse width	t_{OEP}	10	-	10	-	ns	
Data Output hold after $\overline{CAS}$ low	t_{COH}	5	-	5	-	ns	
Out disable delay from $\overline{WE}$	t_{WHZ}	3	10	3	10	ns	
$\overline{WE}$ pulse width for output disable when $\overline{CAS}$ high	t_{WPZ}	7	-	7	-	ns	

Notes :

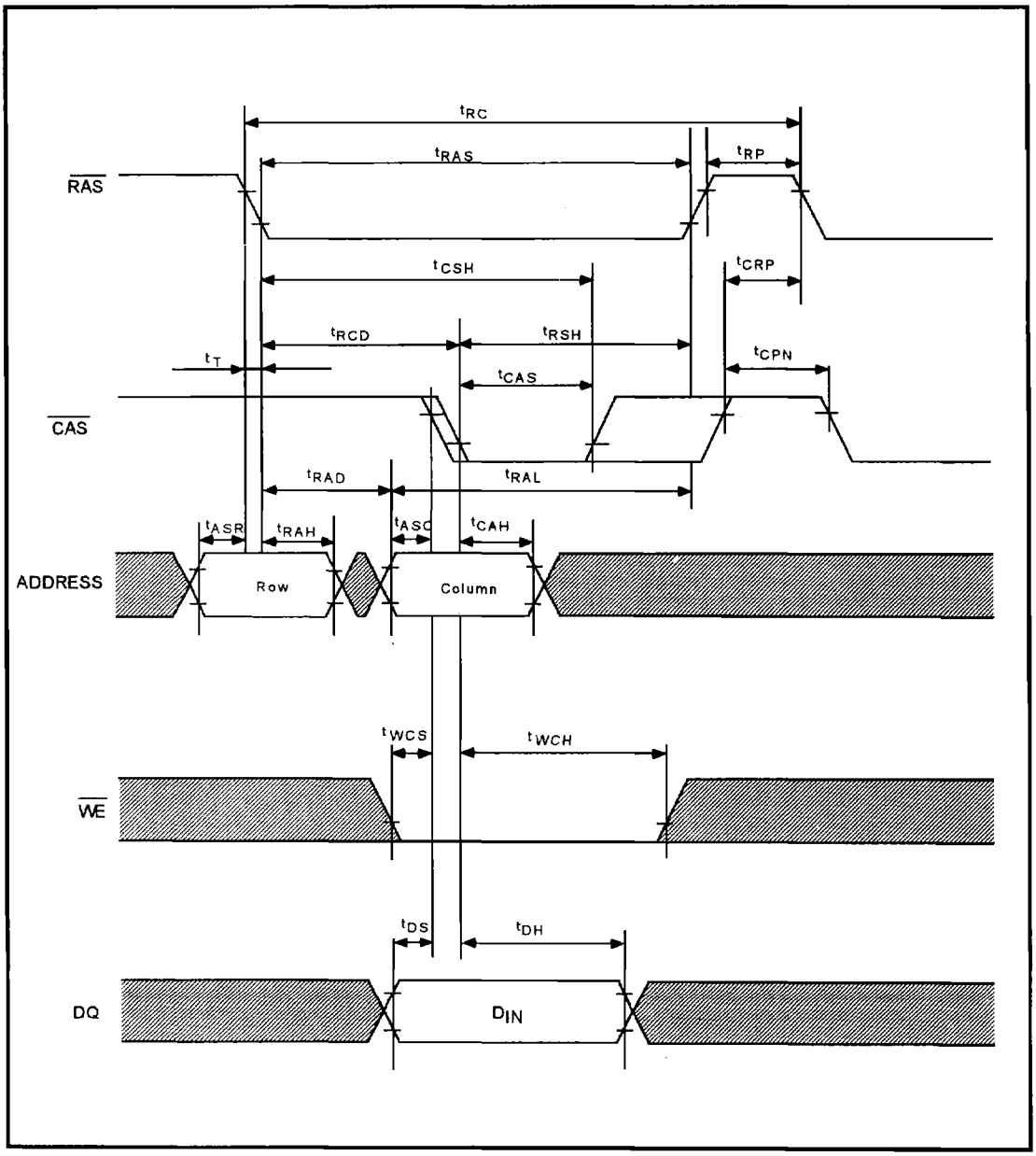
1. AC measurements assume t_T=2ns.
2. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh cycle or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.
3. All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.
4. t_{ASC}(min) , t_{RCS} (min) , t_{WCS}(min) and t_{RPC} are determined by the falling edge of $\overline{CAS}$.
5. Operation with the t_{RCD} (max) limit insures that t_{RAC}(max) can be met, t_{RCD}(max) is specified as a reference point only,if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
6. Operation with the t_{RAD} (max) limit insures that t_{RAC}(max) can be met, t_{RAD}(max) is specified as a reference point only,if t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled exclusively by t_{AA}.
7. t_{CRP}, t_{CHR}, t_{RCH}, t_{CPA} and t_{CPW} are determined by the rising edge of $\overline{CAS}$.
8. V_{IH}(min) and V_{IL} (max) are reference levels for measuring timing or input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Assumes that $t_{RCD} \leq t_{RCD}$(max) and $t_{RAD} \leq t_{RAD}$(max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table,t_{RAC} exceeds the value shown.
10. Assumes that $t_{RCD} \geq t_{RCD}$(max) and $t_{RAD} \leq t_{RAD}$(max).
11. Access time is determined by the longer of t_{AA}, t_{CAC}, t_{CPA}.
12. Assumes that $t_{RCD} \leq t_{RCD}$(max) and $t_{RAD} \geq t_{RAD}$(max).
13. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
14. t_{OFF}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels. t_{OFF} is determined by the later rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. t_{RASP} defines $\overline{RAS}$ pulse width in EDO page mode cycles.

Timing Waveforms

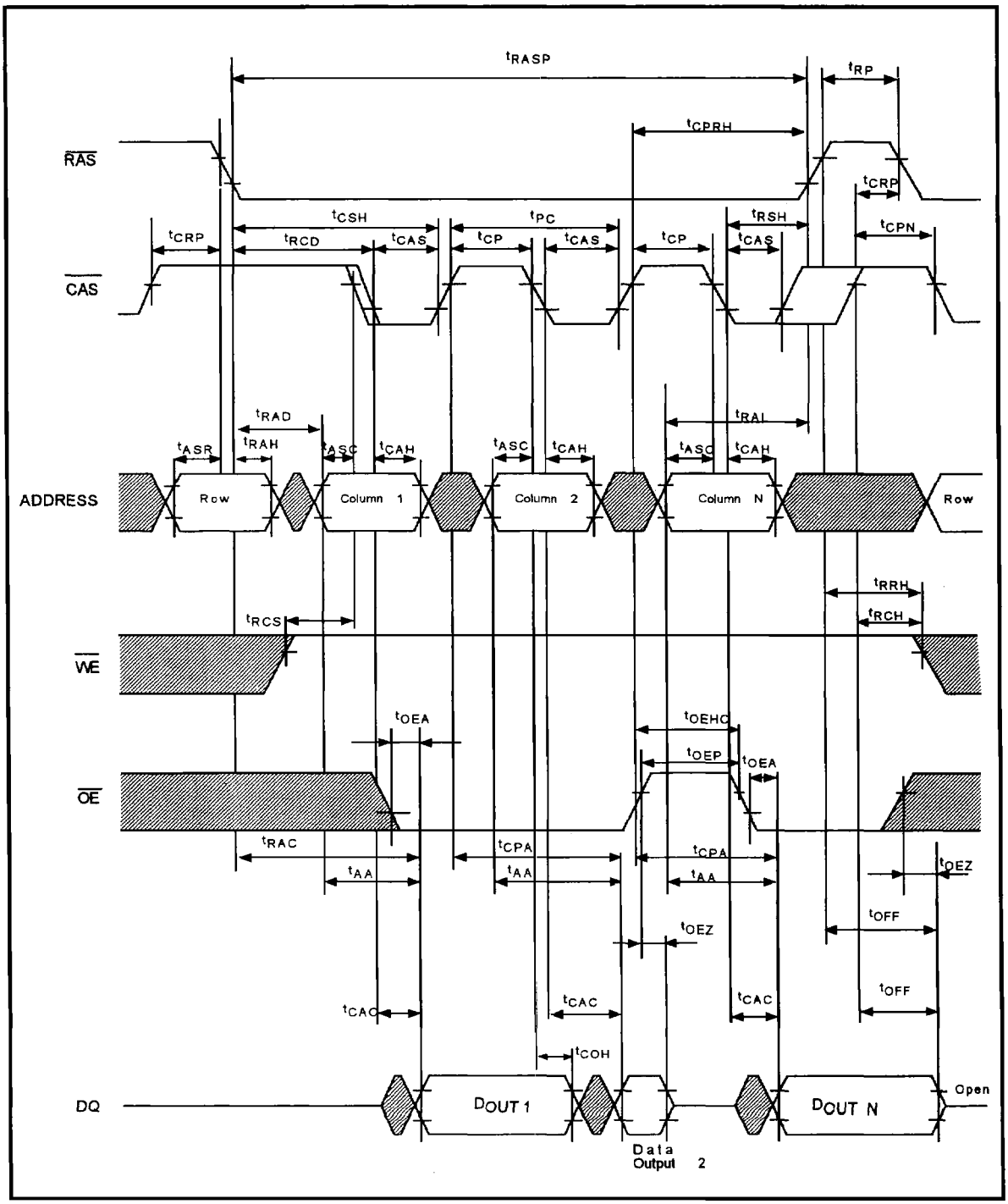
• Read Cycle



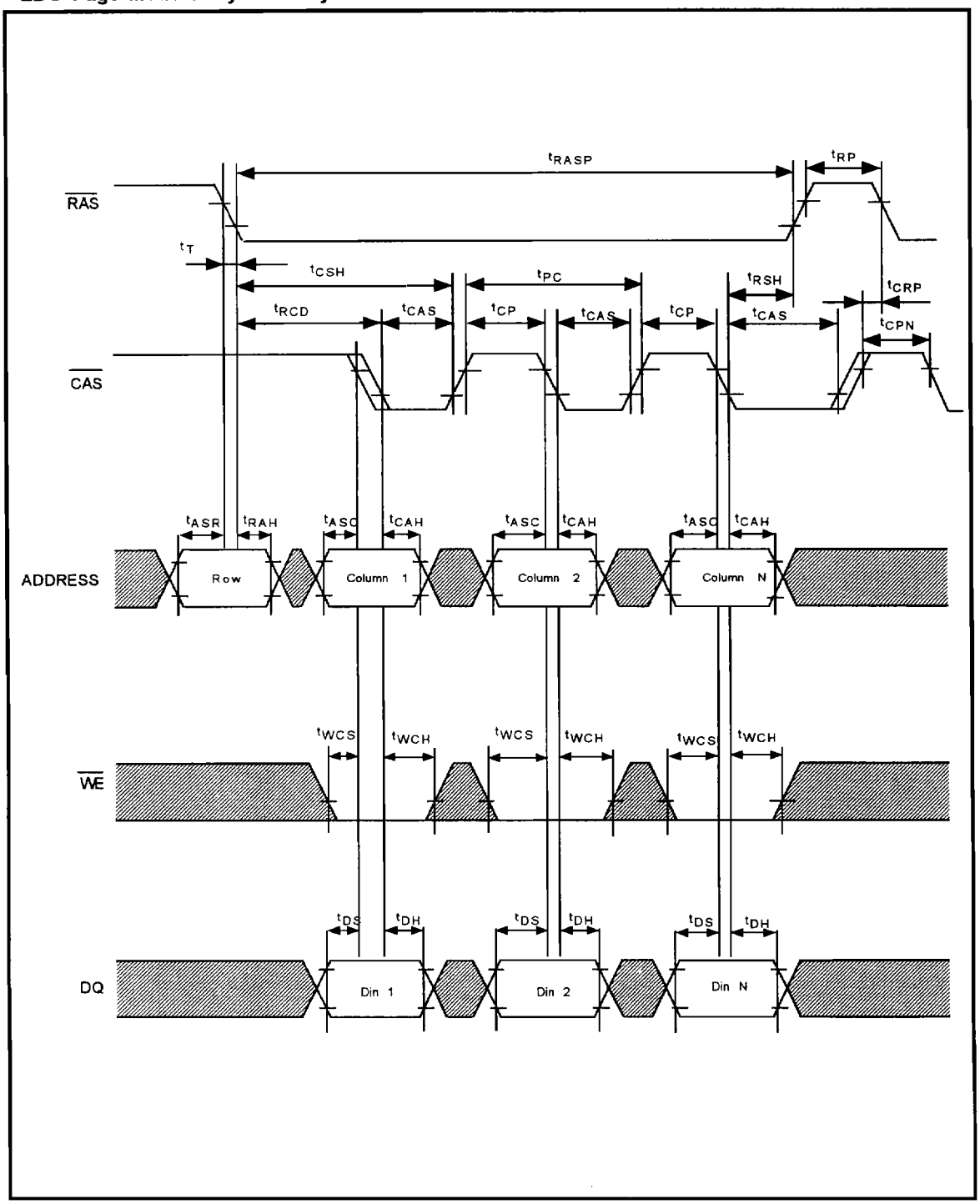
· Early Write Cycle



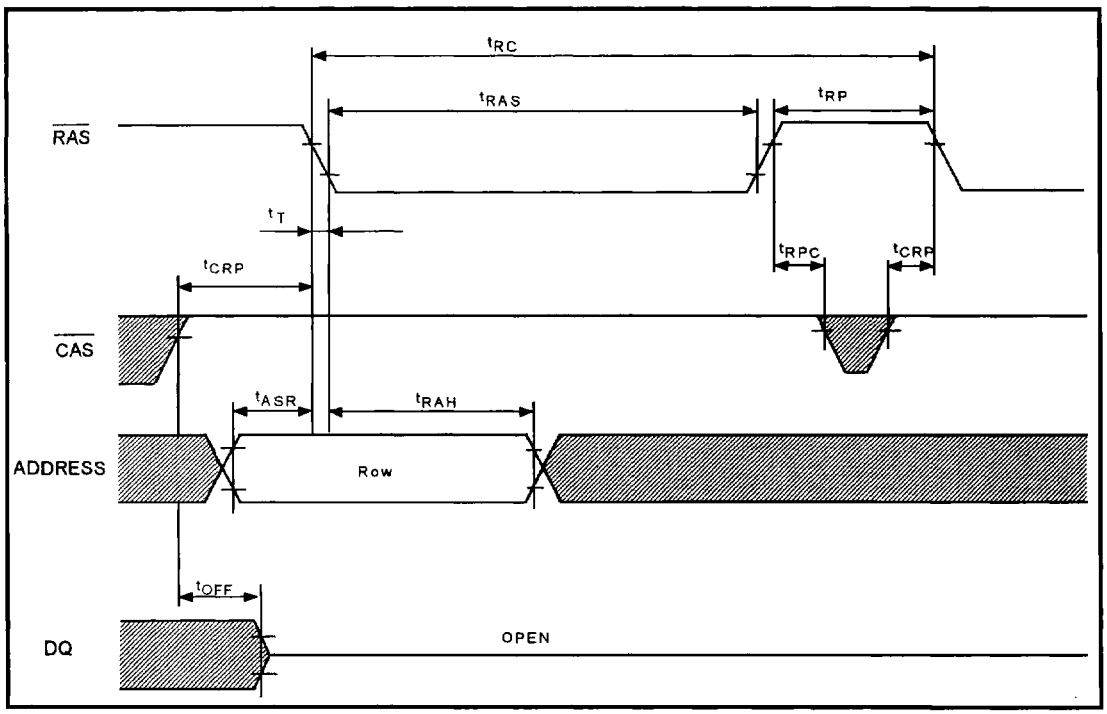
• EDO Page Mode Read Cycle



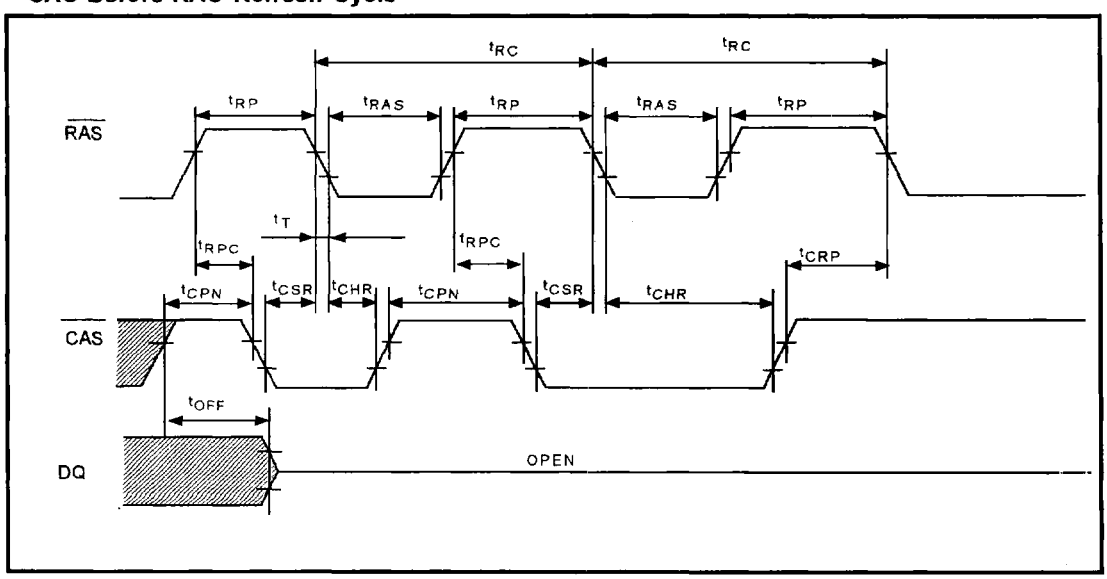
· EDO Page Mode Early Write Cycle



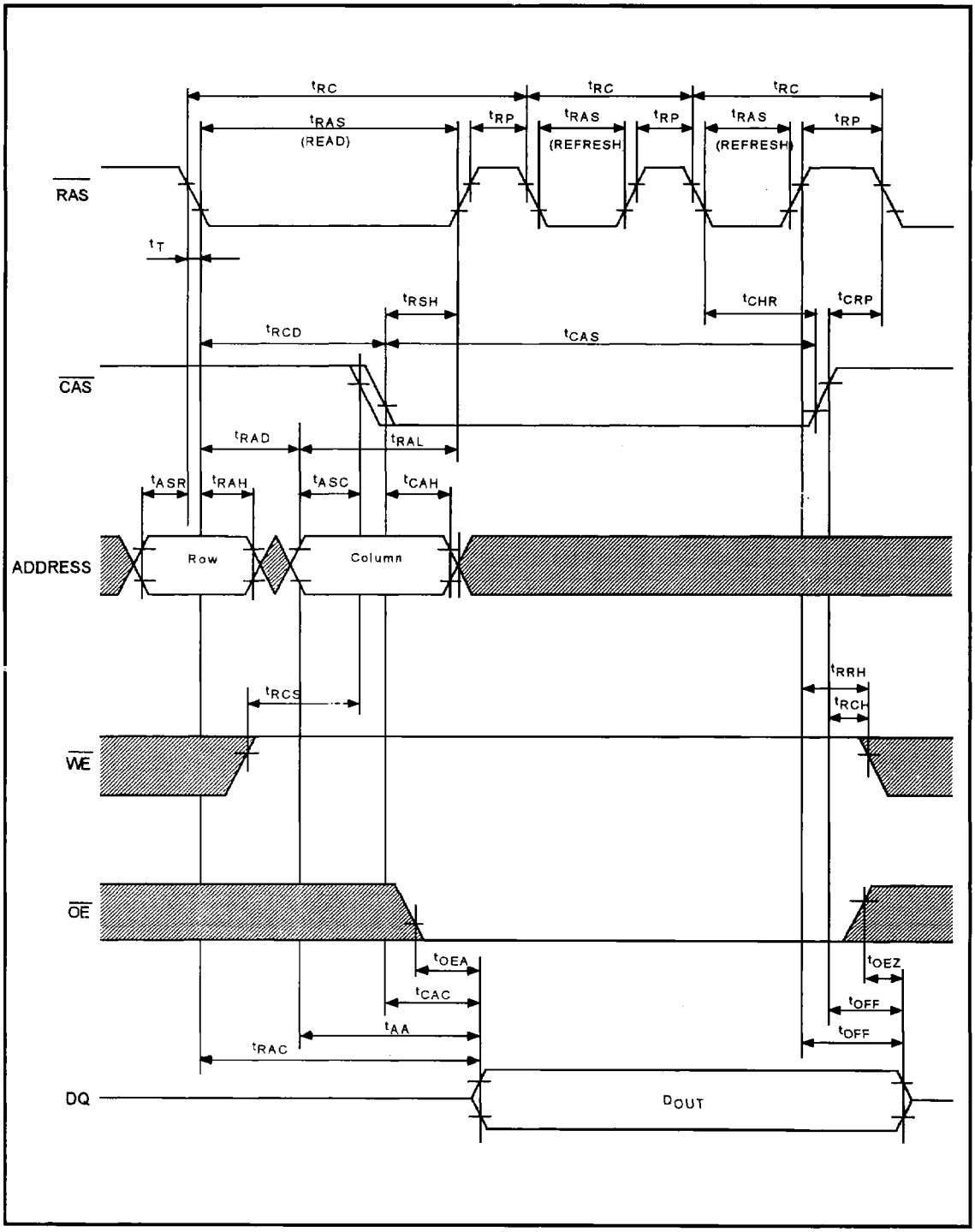
• **$\overline{RAS}$-Only Refresh Cycle**



• **$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle**



· **Hidden Refresh Cycle**



Ordering Information

	1	2	3	4		5	6	7	8	9	10
V	X	X	XX	XXXXX	X	X	X	X	X	-X	

V : VIS Product
1 : RAM Family
M : DRAM SIMM (72pin)
E : DRAM DIMM(168pin)

2 : Memory density (word)
1 : 1M
2 : 2M
4 : 4M

3 : I/O width
32 : x32
64 : x64

4 : Operation mode and refresh with different density
18165B : EDO, 1K ref, 16M DRAM
17805 : EDO, 2K ref, 16M DRAM

5 : Component revision
Blank : None
A : A revision
B : B revision

6 : Component Package
J : SOJ
T : TSOP

7 : PC board finger plating
G : Gold
S : Tin/lead

8 : PC board revision
Blank : none
A : A revision

9 : Customer specific
Blank : none

10 : Speed
-6 : 60 ns
-7 : 70 ns