

### FEATURES

Enhanced Replacement for LF411 and TL081

#### AC PERFORMANCE:

- Settles to  $\pm 0.01\%$  in  $1\mu\text{s}$
- $16\text{V}/\mu\text{s}$  min Slew Rate (AD711J)
- $3\text{MHz}$  min Unity Gain Bandwidth (AD711J)

#### DC PERFORMANCE:

- $0.25\text{mV}$  max Offset Voltage: (AD711C)
- $3\mu\text{V}/^\circ\text{C}$  max Drift: (AD711C)
- $200\text{V}/\text{mV}$  min Open-Loop Gain (AD711K)
- $4\mu\text{V}$  p-p max Noise,  $0.1\text{Hz}$  to  $10\text{Hz}$  (AD711C)

Available in Plastic Mini-DIP, Plastic SO, Hermetic Cerdip, and Hermetic Metal Can Packages

MIL-STD-883B Parts Available

Available in Tape and Reel in Accordance with

- EIA-481A Standard
- Surface Mount (SOIC)
- Dual Version: AD712
- Quad Version: AD713

### PRODUCT DESCRIPTION

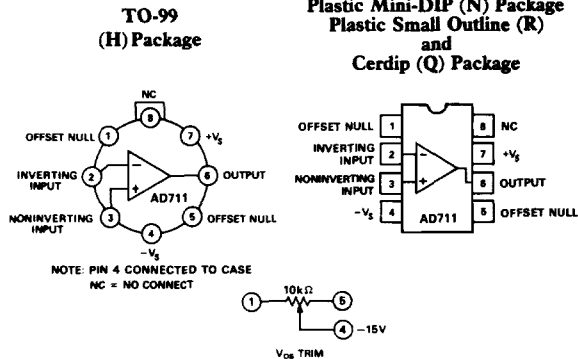
The AD711 is a high speed, precision monolithic operational amplifier offering high performance at very modest prices. Its very low offset voltage and offset voltage drift are the results of advanced laser wafer trimming technology. These performance benefits allow the user to easily upgrade existing designs that use older precision BiFETs and, in many cases, bipolar op amps.

The superior ac and dc performance of this op amp makes it suitable for active filter applications. With a slew rate of  $16\text{V}/\mu\text{s}$  and a settling time of  $1\mu\text{s}$  to  $\pm 0.01\%$ , the AD711 is ideal as a buffer for 12-bit D/A and A/D Converters and as a high-speed integrator. The settling time is unmatched by any similar IC amplifier.

The combination of excellent noise performance and low input current also make the AD711 useful for photo diode preamps. Common-mode rejection of  $88\text{dB}$  and open loop gain of  $400\text{V}/\text{mV}$  ensure 12-bit performance even in high-speed unity gain buffer circuits.

The AD711 is pinned out in a standard op amp configuration and is available in seven performance grades. The AD711J and AD711K are rated over the commercial temperature range of  $0$  to  $+70^\circ\text{C}$ . The AD711A, AD711B and AD711C are rated over the industrial temperature range of  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ . The AD711S and AD711T are rated over the military temperature range of  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$  and are available processed to MIL-STD-883B, Rev. C.

### CONNECTION DIAGRAMS



Extended reliability PLUS screening is available, specified over the commercial and industrial temperature ranges. PLUS screening includes 168-hour burn-in, as well as other environmental and physical tests.

The AD711 is available in an 8-pin plastic mini-DIP, small outline, cerdip, TO-99 metal can or in chip form.

### PRODUCT HIGHLIGHTS

1. The AD711 offers excellent overall performance at very competitive prices.
2. Analog Devices' advanced processing technology and with 100% testing guarantees a low input offset voltage ( $0.25\text{mV}$  max, C grade,  $2\text{mV}$  max, J grade). Input offset voltage is specified in the warmed-up condition. Analog Devices' laser wafer drift trimming process reduces input offset voltage drifts to  $3\mu\text{V}/^\circ\text{C}$  max on the AD711C.
3. Along with precision dc performance, the AD711 offers excellent dynamic response. It settles to  $\pm 0.01\%$  in  $1\mu\text{s}$  and has a 100% tested minimum slew rate of  $16\text{V}/\mu\text{s}$ . Thus this device is ideal for applications such as DAC and ADC buffers which require a combination of superior ac and dc performance.
4. The AD711 has a guaranteed and tested maximum voltage noise of  $4\mu\text{V}$  p-p,  $0.1$  to  $10\text{Hz}$  (AD711C).
5. Analog Devices' well-matched, ion-implanted JFETs ensure a guaranteed input bias current (at either input) of  $25\text{pA}$  max (AD711C) and an input offset current of  $10\text{pA}$  max (AD711C). Both input bias current and input offset current are guaranteed in the warmed-up condition.

# AD711 — SPECIFICATIONS (@ +25°C and $V_S = \pm 15V$ dc, unless otherwise noted)

Model	AD711J/A/S			AD711K/B/T			AD711C			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
<b>INPUT OFFSET VOLTAGE<sup>1</sup></b>										
Initial Offset		0.3	2/1/1		0.2	0.5		0.1	0.25	mV
$T_{min}$ to $T_{max}$			3/2/2			1.0			0.45	mV
vs. Temp.		7	20/20/20		5	10		2	3	$\mu V/^\circ C$
vs. Supply	76	95		80	100		86	110		dB
vs. Supply, $T_{min}$ to $T_{max}$	76/76/76			80			86			dB
Long Term Offset Stability		15			15			15		$\mu V/month$
<b>INPUT BIAS CURRENT<sup>2</sup></b>										
Either Input, $V_{CM} = 0$		15	50		15	50		15	25	pA
Either Input at $T_{max}$			1.1/3.2/51			1.1/3.2/51			1.6	nA
$V_{CM} = 0$ (70°C/85°C/125°C)										
Either Input, $V_{CM} = +10V$		20	100		20	100		20	50	pA
Offset Current, $V_{CM} = 0$		10	25		5	25		5	10	pA
Offset Current at $T_{max}$			0.57/1.6/26			0.57/1.6/26			0.65	nA
(70°C/85°C/125°C)										
<b>FREQUENCY RESPONSE</b>										
Unity Gain, Small Signal	3.0	4		3.4	4		3.4	4		MHz
Full Power Response		200			200			200		kHz
Slew Rate, Unity Gain	16	20		18	20		18	20		V/ $\mu s$
Settling Time to 0.01% <sup>3</sup>		1	1.2		1	1.2		1	1.2	$\mu s$
Total Harmonic Distortion										
$f = 1kHz$										
$R_L \geq 2k\Omega$ , $V_O = 3V_{RMS}$		0.0003			0.0003			0.0003		%
<b>INPUT IMPEDANCE</b>										
Differential		$3 \times 10^{12} \parallel 5.5$			$3 \times 10^{12} \parallel 5.5$			$3 \times 10^{12} \parallel 5.5$		$\Omega \parallel pF$
Common-Mode		$3 \times 10^{12} \parallel 5.5$			$3 \times 10^{12} \parallel 5.5$			$3 \times 10^{12} \parallel 5.5$		$\Omega \parallel pF$
<b>INPUT VOLTAGE RANGE</b>										
Differential <sup>4</sup>		$\pm 20$			$\pm 20$			$\pm 20$		V
Common-Mode Voltage		$+14.5, -11.5$			$+14.5, -11.5$			$+14.5, -11.5$		V
Over Max Operating Range <sup>5</sup>	$-V_S + 4V$		$+V_S - 2V$	$-V_S + 4V$		$+V_S - 2V$	$-V_S + 4V$		$+V_S - 2V$	V
Common-Mode Rejection Ratio										dB
$V_{CM} = \pm 10V$	76	88		80	88		86	94		dB
$T_{min}$ to $T_{max}$	76/76/76	84		80	84		86	90		dB
$V_{CM} = \pm 11V$	70	84		76	84		76	90		dB
$T_{min}$ to $T_{max}$	70/70/70	80		74	80		74	84		dB
<b>INPUT VOLTAGE NOISE</b>										
Voltage 0.1Hz to 10Hz		2			2			2	4.0	$\mu V_{p-p}$
$f = 10Hz$		45			45			45		$nV/\sqrt{Hz}$
$f = 100Hz$		22			22			22		$nV/\sqrt{Hz}$
$f = 1kHz$		18			18			18		$nV/\sqrt{Hz}$
$f = 10kHz$		16			16			16		$nV/\sqrt{Hz}$
<b>INPUT CURRENT NOISE</b>										
$f = 1kHz$		0.01			0.01			0.01		$pA/\sqrt{Hz}$
<b>OPEN LOOP GAIN<sup>6</sup></b>										
$V_O = \pm 10V$ , $R_L \geq 2k\Omega$	150	400		200	400		200	400		V/mV
$V_O = \pm 10V$ , $R_L \geq 2k\Omega$ , $T_{min}$ to $T_{max}$	100/100/100			100			100			V/mV
<b>OUTPUT CHARACTERISTICS</b>										
Voltage @ $R_L \geq 2k\Omega$	$+13, -12.5$	$+13.9, -13.3$		$+13, -12.5$	$+13.9, -13.3$		$+13, -12.5$	$+13.9, -13.3$		V
Voltage @ $R_L \geq 2k\Omega$ , $T_{min}$ to $T_{max}$	$\pm 12/\pm 12/\pm 12$	$+13.8, -13.1$		$\pm 12$	$+13.8, -13.1$		$\pm 12$	$+13.8, -13.1$		V
Short-Circuit Current		25			25			25		mA
<b>POWER SUPPLY</b>										
Rated Performance		$\pm 15$			$\pm 15$			$\pm 15$		V
Operating Range	$\pm 4.5$		$\pm 18$	$\pm 4.5$		$\pm 18$	$\pm 4.5$		$\pm 18$	V
Quiescent Current		2.5	3.4		2.5	3.0		2.5	2.8	mA
<b>TEMPERATURE RANGE</b>										
Operating, Rated Performance										
Commercial (0 to +70°C)		AD711J			AD711K			AD711C		
Industrial (-40°C to +85°C)		AD711A			AD711B					
Military (-55°C to +125°C)		AD711S			AD711T					
<b>PACKAGE OPTIONS<sup>7</sup></b>										
Plastic (N-8)		AD711JN			AD711KN					
SOIC (R-8)		AD711JR			AD711KR					
Cerdip (Q-8)		AD711AQ, AD711SQ			AD711BQ, AD711TQ			AD711CQ		
TO-99 (H-08A)		AD711AH, AD711SH			AD711BH, AD711TH			AD711CH		
Tape and Reel		AD711JR-REEL			AD711KR-REEL					
Chips		AD711J Chips			AD711K Chips			AD711S Chips		
<b>TRANSISTOR COUNT</b>		30			30			30		

NOTES

- <sup>1</sup>Input offset voltage specifications are guaranteed after 5 minutes of operation at  $T_A = +25^\circ\text{C}$ .
- <sup>2</sup>Bias current specifications are guaranteed maximum at either input after 5 minutes of operation at  $T_A = +25^\circ\text{C}$ . For higher temperature, the current doubles every  $10^\circ\text{C}$ .
- <sup>3</sup>Refer to Figure 29.
- <sup>4</sup>Defined as voltage between inputs, such that neither exceeds  $\pm 10\text{V}$  from ground.
- <sup>5</sup>Typically exceeding  $-14.1\text{V}$  negative common-mode voltage on either input results in an output phase reversal.
- <sup>6</sup>Open-Loop Gain is specified with  $V_{OS}$  both nulled and unnullled.
- <sup>7</sup>H = Metal Can; N = Plastic DIP; Q = Cerdip; R = SOIC. For outline information see Package Information section.

Specifications subject to change without notice.

All min and max specifications are guaranteed. Specifications in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

**ABSOLUTE MAXIMUM RATINGS<sup>1</sup>**

Supply Voltage	$\pm 18\text{V}$
Internal Power Dissipation <sup>2</sup>	500mW
Input Voltage <sup>3</sup>	$\pm 18\text{V}$
Output Short Circuit Duration	Indefinite
Differential Input Voltage	$+V_S$ and $-V_S$
Storage Temperature Range (Q, H)	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Storage Temperature Range (N)	$-65^\circ\text{C}$ to $+125^\circ\text{C}$
Operating Temperature Range	
AD711J/K	0 to $+70^\circ\text{C}$
AD711A/B/C	$-40^\circ\text{C}$ to $+85^\circ\text{C}$
AD711S/T	$-55^\circ\text{C}$ to $+125^\circ\text{C}$
Lead Temperature Range (Soldering 60 seconds)	$300^\circ\text{C}$

NOTES

<sup>1</sup>Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

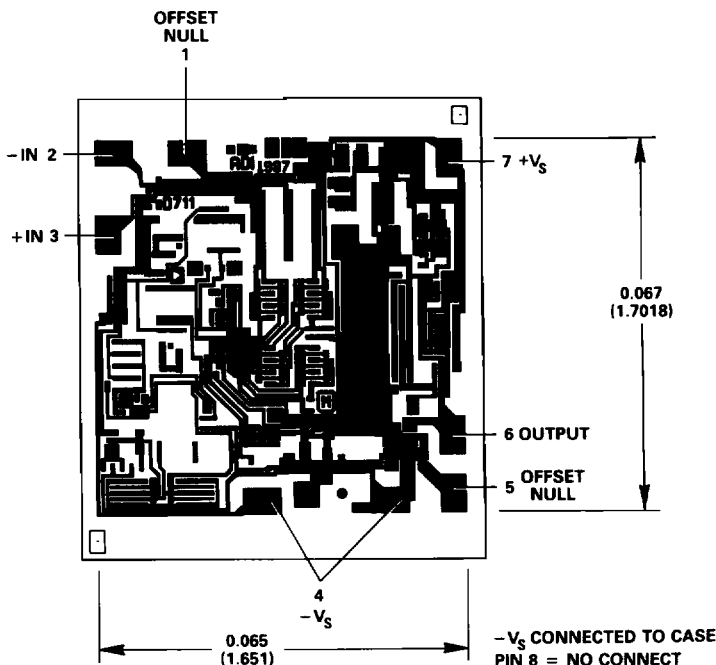
<sup>2</sup>Thermal Characteristics:

- 8-Pin Plastic Package:  $\theta_{JC} = 33^\circ\text{C}/\text{W}$ ;  $\theta_{JA} = 100^\circ\text{C}/\text{W}$
- 8-Pin Cerdip Package:  $\theta_{JC} = 22^\circ\text{C}/\text{W}$ ;  $\theta_{JA} = 110^\circ\text{C}/\text{W}$
- 8-Pin Metal Can Package:  $\theta_{JC} = 65^\circ\text{C}/\text{W}$ ;  $\theta_{JA} = 150^\circ\text{C}/\text{W}$

<sup>3</sup>For supply voltages less than  $\pm 18\text{V}$ , the absolute maximum input voltage is equal to the supply voltage.

**METALLIZATION PHOTOGRAPH**

Dimensions shown in inches and (mm).  
Contact factory for latest dimensions.



# AD711—Typical Characteristics

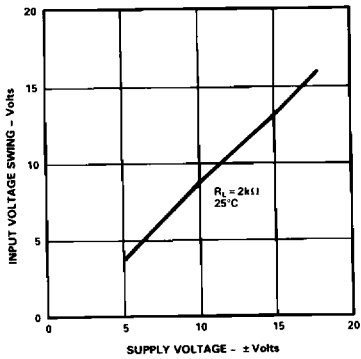


Figure 1. Input Voltage Swing vs. Supply Voltage

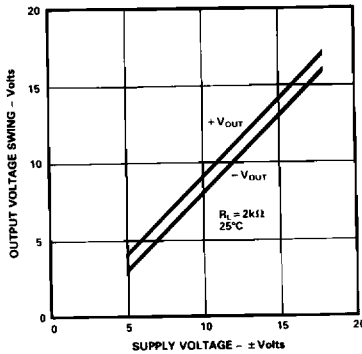


Figure 2. Output Voltage Swing vs. Supply Voltage

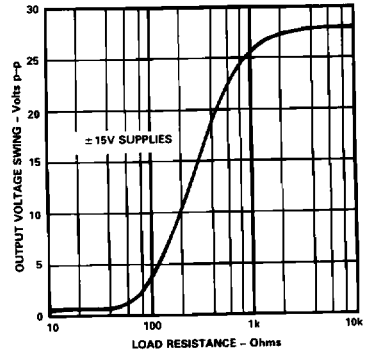


Figure 3. Output Voltage Swing vs. Load Resistance

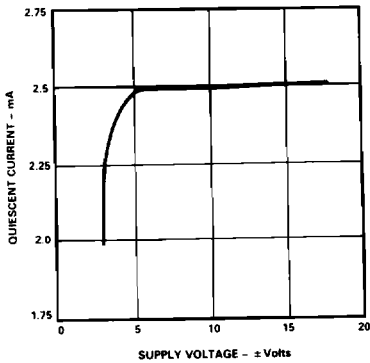


Figure 4. Quiescent Current vs. Supply Voltage

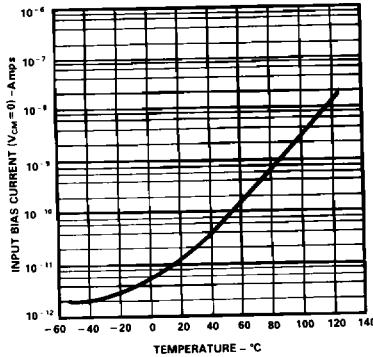


Figure 5. Input Bias Current vs. Temperature

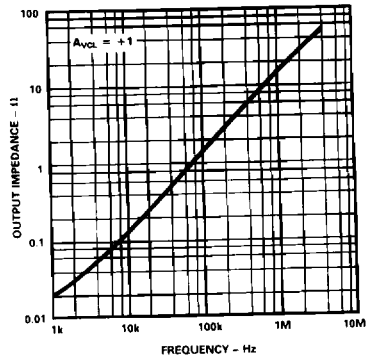


Figure 6. Output Impedance vs. Frequency

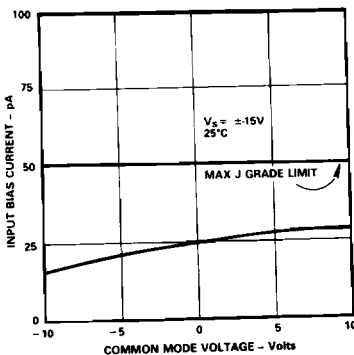


Figure 7. Input Bias Current vs. Common Mode Voltage

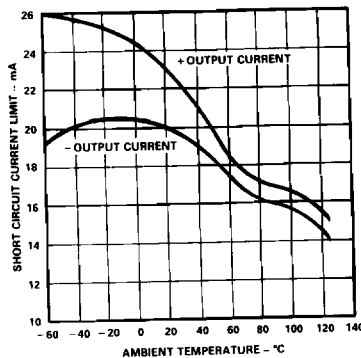


Figure 8. Short Circuit Current Limit vs. Temperature

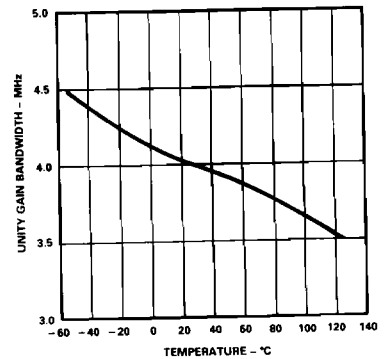


Figure 9. Unity Gain Bandwidth vs. Temperature

# Typical Characteristics—AD711

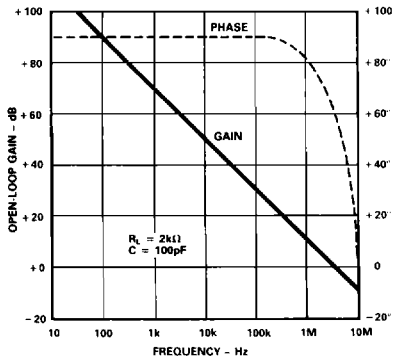


Figure 10. Open-Loop Gain and Phase Margin vs. Frequency

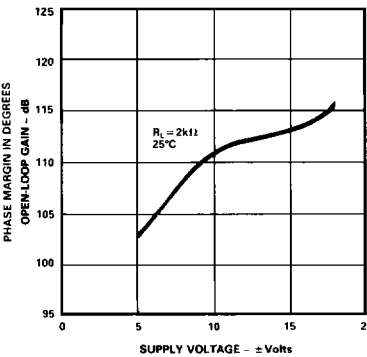


Figure 11. Open-Loop Gain vs. Supply Voltage

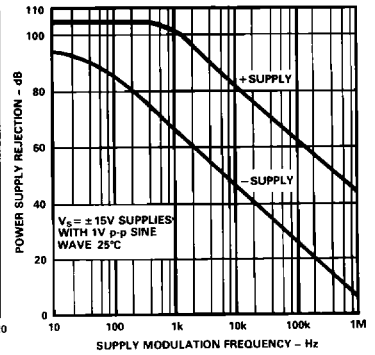


Figure 12. Power Supply Rejection vs. Frequency

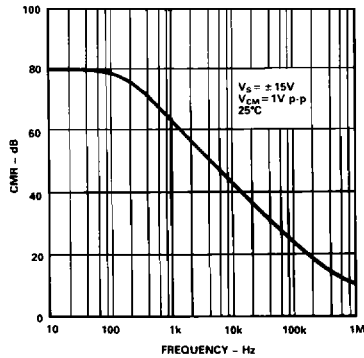


Figure 13. Common Mode Rejection vs. Frequency

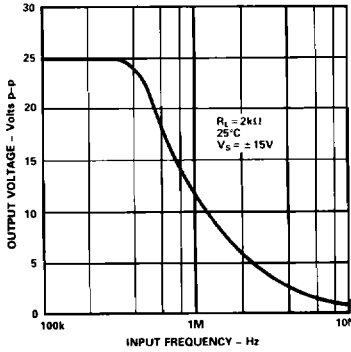


Figure 14. Large Signal Frequency Response

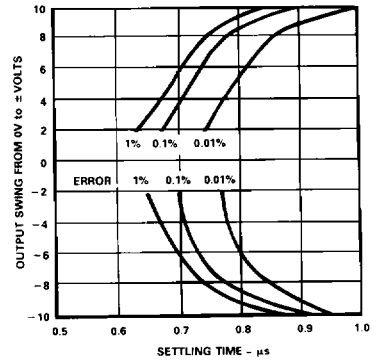


Figure 15. Output Swing and Error vs. Settling Time

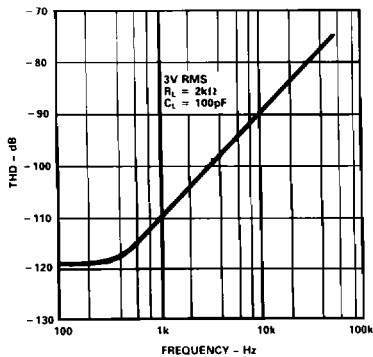


Figure 16. Total Harmonic Distortion vs. Frequency

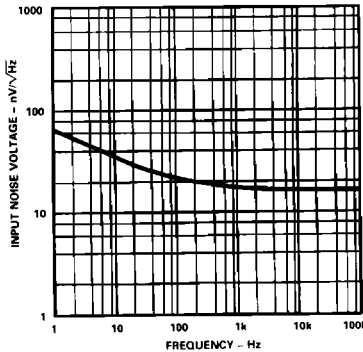


Figure 17. Input Noise Voltage Spectral Density

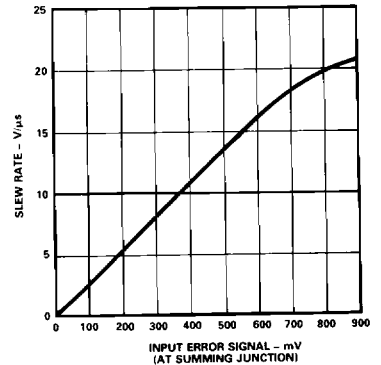


Figure 18. Slew Rate vs. Input Error Signal

# AD711

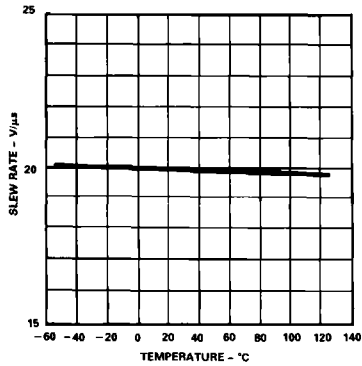


Figure 19. Slew Rate vs. Temperature

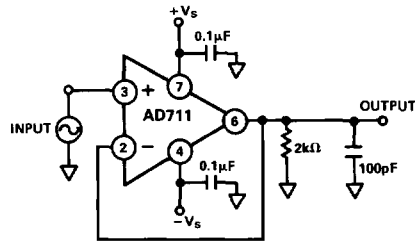


Figure 20. T.H.D. Test Circuit

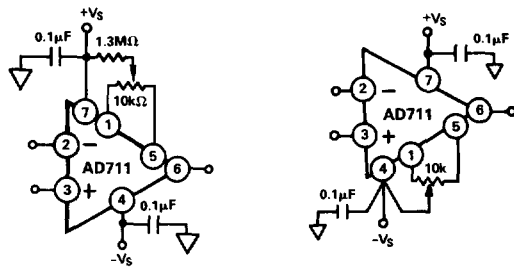


Figure 21. Offset Null Configurations

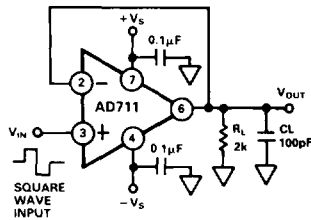


Figure 22a. Unity Gain Follower

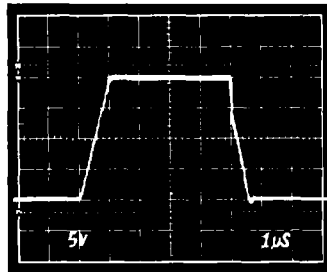


Figure 22b. Unity Gain Follower Pulse Response (Large Signal)

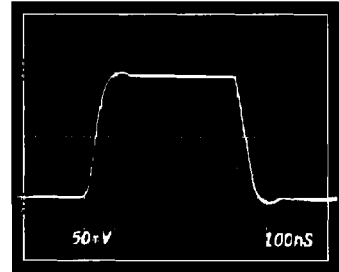


Figure 22c. Unity Gain Follower Pulse Response (Small Signal)

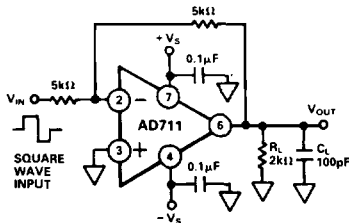


Figure 23a. Unity Gain Inverter

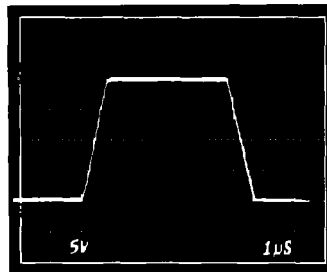


Figure 23b. Unity Gain Inverter Pulse Response (Large Signal)

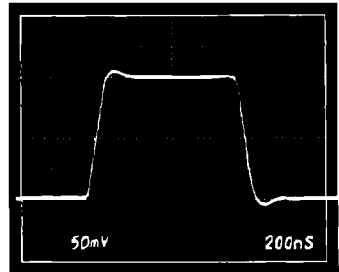


Figure 23c. Unity Gain Inverter Pulse Response (Small Signal)

### OPTIMIZING SETTling TIME

Most bipolar high-speed D/A converters have current outputs; therefore, for most applications, an external op amp is required for current-to-voltage conversion. The settling time of the converter/op amp combination depends on the settling time of the DAC and output amplifier. A good approximation is:

$$\tau_{\text{Total}} = \sqrt{(\tau_{\text{DAC}})^2 + (\tau_{\text{AMP}})^2}$$

The settling time of an op amp DAC buffer will vary with the noise gain of the circuit, the DAC output capacitance, and with the amount of external compensation capacitance across the DAC output scaling resistor.

Settling time for a bipolar DAC is typically 100 to 500ns. Previously, conventional op amps have required much longer settling times than have typical state-of-the-art DACs; therefore, the amplifier settling time has been the major limitation to a high-speed voltage-output D-to-A function. The introduction of the AD711/712 family of op amps with their 1 $\mu$ s (to  $\pm 0.01\%$  of final value) settling time now permits the full high-speed capabilities of most modern DACs to be realized.

In addition to a significant improvement in settling time, the low offset voltage, low offset voltage drift, and high open-loop gain of the AD711 family assures 12-bit accuracy over the full operating temperature range.

The excellent high-speed performance of the AD711 is shown in the oscilloscope photos of Figure 25. Measurements were taken using a low input capacitance amplifier connected directly to the summing junction of the AD711 – both photos show the worst case situation: a full-scale input transition. The DAC's 4k $\Omega$  [10k $\Omega$ ||8k $\Omega$  = 4.4k $\Omega$ ] output impedance together with a 10k $\Omega$  feedback resistor produce an op amp noise gain of 3.25. The current output from the DAC produces a 10V step at the op amp output (0 to -10V Figure 25a, -10V to 0V Figure 25b.)

Therefore, with an ideal op amp, settling to  $\pm 1/2\text{LSB}$  ( $\pm 0.01\%$ ) requires that 375 $\mu$ V or less appears at the summing junction. This means that the error between the input and output (that voltage which appears at the AD711 summing junction) must be less than 375 $\mu$ V. As shown in Figure 25, the total settling time for the AD711/AD565 combination is 1.2 microseconds.

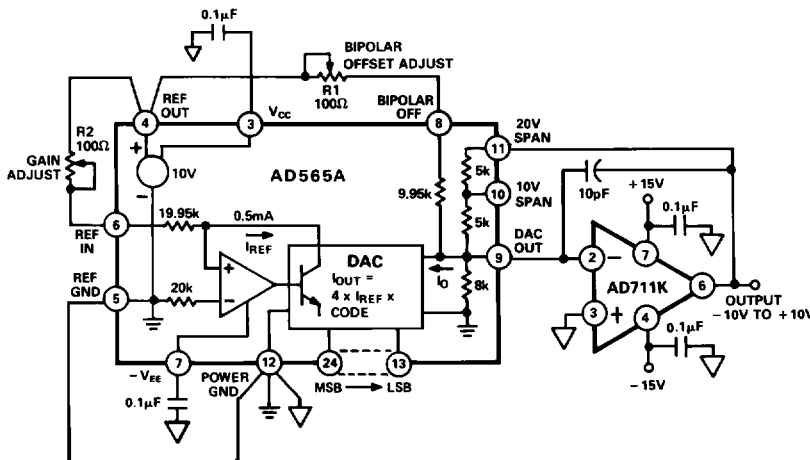


Figure 24.  $\pm 10\text{V}$  Voltage Output Bipolar DAC

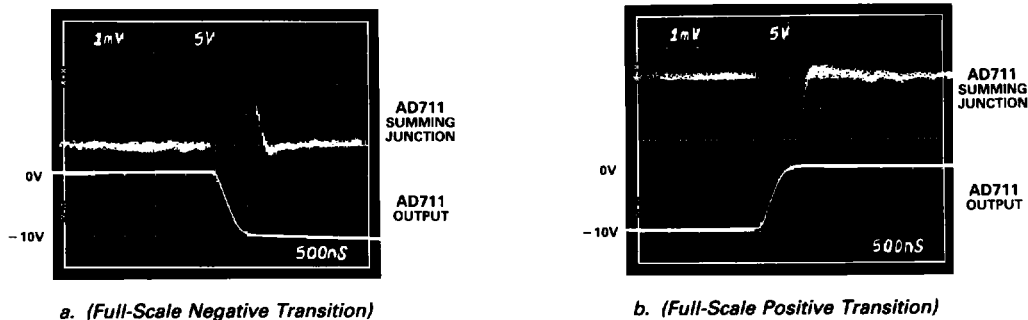


Figure 25. Settling Characteristics for AD711 with AD565A

# AD711

## OP AMP SETTLING TIME – A MATHEMATICAL MODEL

The design of the AD711 gives careful attention to optimizing individual circuit components; in addition, a careful tradeoff was made: the gain bandwidth product (4MHz) and slew rate (20V/μs) were chosen to be high enough to provide very fast settling time but not too high to cause a significant reduction in phase margin (and therefore stability). Thus designed, the AD711 settles to ±0.01%, with a 10V output step, in under 1μs, while retaining the ability to drive a 100pF load capacitance when operating as a unity gain follower.

If an op amp is modeled as an ideal integrator with a unity gain crossover frequency of  $\omega_o/2\pi$ , Equation 1 will accurately describe the small signal behavior of the circuit of Figure 26a, consisting of an op amp connected as an I-to-V converter at the output of a bipolar or CMOS DAC. This equation would completely describe the output of the system if not for the op amp's finite slew rate and other nonlinear effects.

Equation 1.

$$\frac{V_o}{I_{IN}} = \frac{-R}{\frac{R(C_f + C_X)}{\omega_o} s^2 + \left(\frac{G_N}{\omega_o} + RC_f\right) s + 1}$$

where  $\frac{\omega_o}{2\pi}$  = op amp's unity gain frequency

$G_N$  = "noise" gain of circuit  $\left(1 + \frac{R}{R_o}\right)$

This equation may then be solved for  $C_f$ :

Equation 2.

$$C_f = \frac{2 - G_N}{R\omega_o} + \frac{2\sqrt{RC_X\omega_o + (1 - G_N)}}{R\omega_o}$$

In these equations, capacitor  $C_X$  is the total capacitance appearing at the inverting terminal of the op amp. When modeling a DAC buffer application, the Norton equivalent circuit of Figure 26a can be used directly; capacitance  $C_X$  is the total capacitance of the output of the DAC plus the input capacitance of the op amp (since the two are in parallel).

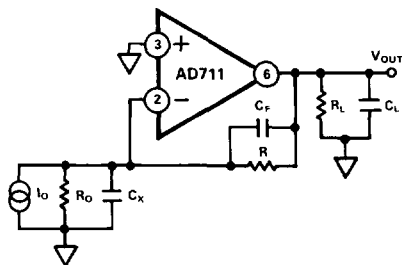


Figure 26a. Simplified Model of the AD711 Used as a Current-Out DAC Buffer

When  $R_o$  and  $I_o$  are replaced with their Thevenin  $V_{IN}$  and  $R_{IN}$  equivalents, the general purpose inverting amplifier of Figure 26b is created. Note that when using this general model, capacitance  $C_X$  is EITHER the input capacitance of the op amp if a simple inverting op amp is being simulated OR it is the combined capacitance of the DAC output and the op amp input if the DAC buffer is being modeled.

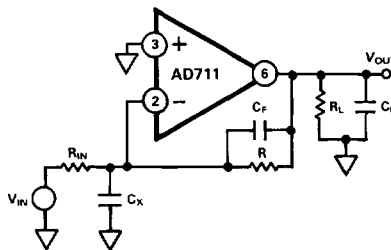


Figure 26b. Simplified Model of the AD711 Used as an Inverter

In either case, the capacitance  $C_X$  causes the system to go from a one-pole to a two-pole response; this additional pole increases settling time by introducing peaking or ringing in the op amp output. Since the value of  $C_X$  can be estimated with reasonable accuracy, Equation 2 can be used to choose a small capacitor,  $C_f$ , to cancel the input pole and optimize amplifier response. Figure 27 is a graphical solution of Equation 2 for the AD711 with  $R = 4k\Omega$ .

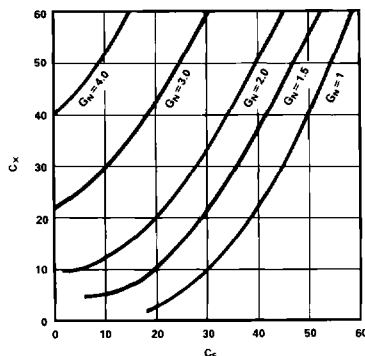


Figure 27. Value of Capacitor  $C_f$  vs. Value of  $C_X$

The photos of Figures 28a and 28b show the dynamic response of the AD711 in the settling test circuit of Figure 29.

The input of the settling time fixture is driven by a flat-top pulse generator. The error signal output from the false summing node of A1 is clamped, amplified by A2 and then clamped again. The error signal is thus clamped twice: once to prevent overloading amplifier A2 and then a second time to avoid overloading the oscilloscope preamp. The Tektronix oscilloscope preamp type 7A26 was carefully chosen because it does not overload with these input levels. Amplifier A2 needs to be a very high speed FET-input op amp; it provides a gain of 10, amplifying the error signal output of A1.



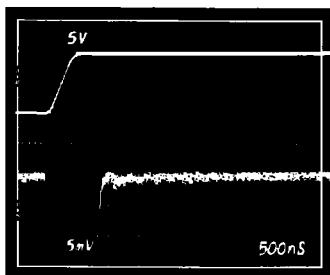


Figure 28a. Settling Characteristics 0 to +10V Step  
Upper Trace: Output of AD711 Under Test (5V/Div)  
Lower Trace: Amplified Error Voltage (0.01%/Div)

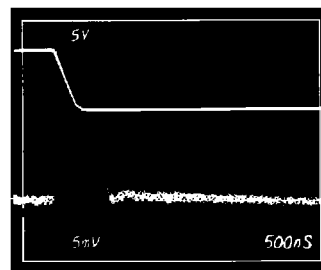


Figure 28b. Settling Characteristics 0 to -10V Step  
Upper Trace: Output of AD711 Under Test (5V/Div)  
Lower Trace: Amplified Error Voltage (0.01%/Div)

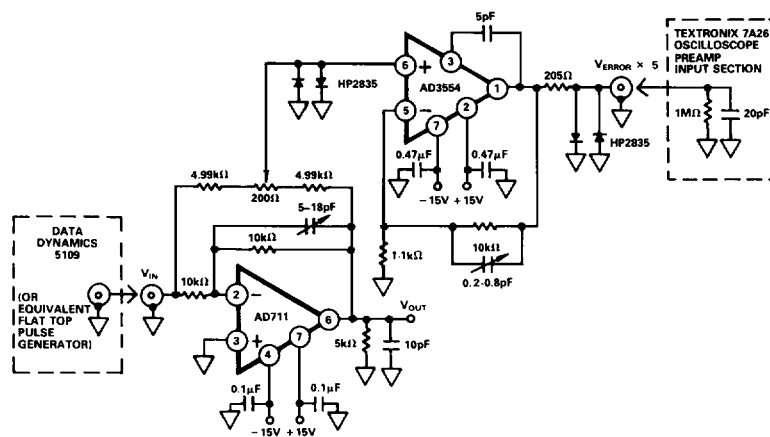


Figure 29. Settling Time Test Circuit

## GUARDING

The low input bias current (15pA) and low noise characteristics of the AD711 BiFET op amp make it suitable for electrometer applications such as photo diode preamplifiers and picoampere current-to-voltage converters. The use of a guarding technique such as that shown in Figure 30, in printed circuit board layout and construction is critical to minimize leakage currents. The guard ring is connected to a low impedance potential at the same level as the inputs. High impedance signal lines should not be extended for any unnecessary length on the printed circuit board.

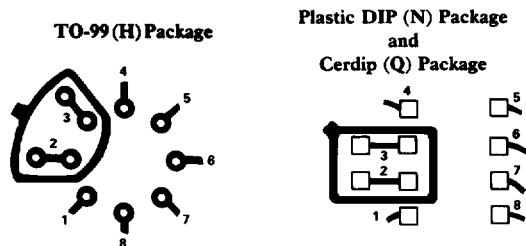


Figure 30. Board Layout for Guarding Inputs

## D/A CONVERTER APPLICATIONS

The AD711 is an excellent output amplifier for CMOS DACs. It can be used to perform both 2 quadrant and 4 quadrant operation. The output impedance of a DAC using an inverted R-2R ladder approaches R for codes containing many 1s, 3R for codes containing a single 1, and for codes containing all zero, the output impedance is infinite.

For example, the output resistance of the AD7545 will modulate between 11kΩ and 33kΩ. Therefore, with the DAC's internal feedback resistance of 11kΩ, the noise gain will vary from 2 to 4/3. This changing noise gain modulates the effect of the input offset voltage of the amplifier, resulting in nonlinear DAC-amplifier performance.

The AD711K with guaranteed 500μV offset voltage minimizes this effect to achieve 12-bit performance.

Figures 31 and 32 show the AD711 and AD7545 (12-bit CMOS DAC) configured for unipolar binary (2-quadrant multiplication) or bipolar (4-quadrant multiplication) operation. Capacitor C1 provides phase compensation to reduce overshoot and ringing.

# AD711

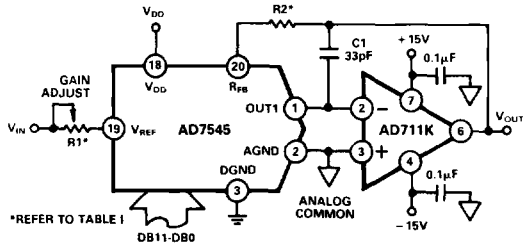


Figure 31. Unipolar Binary Operation

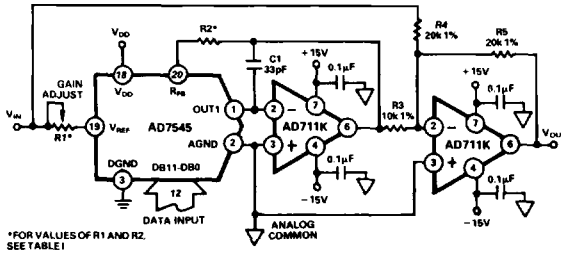


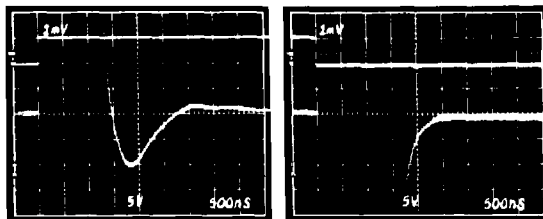
Figure 32. Bipolar Operation

R1 and R2 calibrate the zero offset and gain error of the DAC. Specific values for these resistors depend upon the grade of AD7545 and are shown below.

TRIM RESISTOR	JN/AQ/SD	KN/BQ/TD	LN/CQ/UD	GLN/GCQ/GUD
R1	500Ω	200Ω	100Ω	20Ω
R2	150Ω	68Ω	33Ω	6.8Ω

Table 1. Recommended Trim Resistor Values vs. Grades of the AD7545 for  $V_{DD} = +5V$

Figures 33a and 33b show the settling time characteristics of the AD711 when used as a DAC output buffer for the AD7545.



a. Full-Scale Positive Transition

b. Full-Scale Negative Transition

Figure 33. Settling Characteristics for AD711 with AD7545

## NOISE CHARACTERISTICS

The random nature of noise, particularly in the  $1/f$  region, makes it difficult to specify in practical terms. At the same time, designers of precision instrumentation require certain guaranteed maximum noise levels to realize the full accuracy of their equipment.

The AD711C grade is specified at a maximum level of  $4.0\mu V$  p-p, in a 0.1 to 10Hz bandwidth. Each AD711C receives a 100% noise test for two 10-second intervals; devices with any excursion in excess of  $4.0\mu V$  are rejected. The screened lot is then submitted to Quality Control for verification on an AQL basis.

All other grades of the AD711 are sample-tested on an AQL basis to a limit of  $6\mu V$  p-p, 0.1 to 10Hz.

## DRIVING THE ANALOG INPUT OF AN A/D CONVERTER

An op amp driving the analog input of an A/D converter, such as that shown in Figure 34, must be capable of maintaining a constant output voltage under dynamically changing load conditions. In successive-approximation converters, the input current is compared to a series of switched trial currents. The comparison point is diode clamped but may deviate several hundred millivolts resulting in high frequency modulation of A/D input current. The output impedance of a feedback amplifier is made artificially low by the loop gain. At high frequencies, where the loop gain is low, the amplifier output impedance can approach its open loop value. Most IC amplifiers exhibit a minimum open loop output impedance of  $25\Omega$  due to current limiting resistors. A few hundred microamps reflected from the change in converter

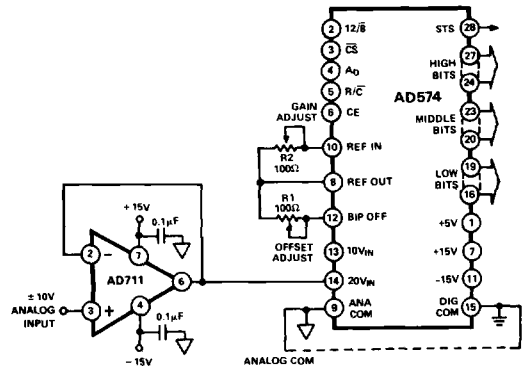
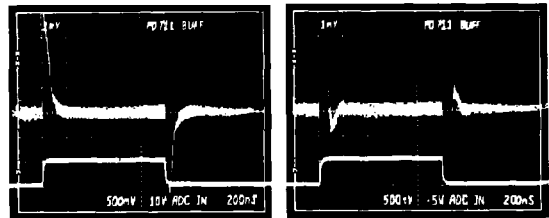


Figure 34. AD711 as ADC Unity Gain Buffer



a. Source Current = 2mA

b. Sink Current = 1mA

Figure 35. ADC Input Unity Gain Buffer Recovery Times

loading can introduce errors in instantaneous input voltage. If the A/D conversion speed is not excessive and the bandwidth of the amplifier is sufficient, the amplifier's output will return to the nominal value before the converter makes its comparison. However, many amplifiers have relatively narrow bandwidth yielding slow recovery from output transients. The AD711 is ideally suited to drive high speed A/D converters since it offers both wide bandwidth and high open-loop gain.

### DRIVING A LARGE CAPACITIVE LOAD

The circuit in Figure 36 employs a 100Ω isolation resistor which enables the amplifier to drive capacitive loads exceeding 1500pF; the resistor effectively isolates the high frequency feedback from the load and stabilizes the circuit. Low frequency feedback is returned to the amplifier summing junction via the low pass filter formed by the 100Ω series resistor and the load capacitance,  $C_L$ . Figure 37 shows a typical transient response for this connection.

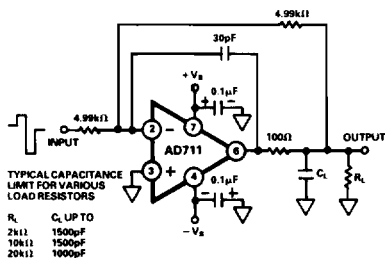


Figure 36. Circuit for Driving a Large Capacitive Load

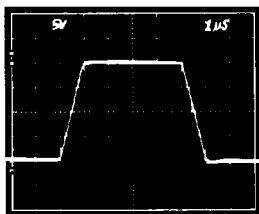


Figure 37. Transient Response  $R_L = 2k\Omega$ ,  $C_L = 500pF$

### ACTIVE FILTER APPLICATIONS

In active filter applications using op amps, the dc accuracy of the amplifier is critical to optimal filter performance. The amplifier's offset voltage and bias current contribute to output error. Offset voltage will be passed by the filter and may be amplified to produce excessive output offset. For low frequency applications requiring large value input resistors, bias currents flowing through these resistors will also generate an offset voltage.

In addition, at higher frequencies, an op amp's dynamics must be carefully considered. Here, slew rate, bandwidth, and open-loop gain play a major role in op amp selection. The slew rate must be fast as well as symmetrical to minimize distortion. The amplifier's bandwidth in conjunction with the filter's gain will dictate the frequency response of the filter.

The use of a high performance amplifier such as the AD711 will minimize both dc and ac errors in all active filter applications.

### SECOND ORDER LOW PASS FILTER

Figure 38 depicts the AD711 configured as a second order Butterworth low pass filter. With the values as shown, the corner frequency will be 20kHz; however, the wide bandwidth of the AD711 permits a corner frequency as high as several hundred kilohertz. Equations for component selection are shown below.

$$R1 = R2 = \text{user selected (typical values: } 10k\Omega - 100k\Omega)$$

$$C1 = \frac{1.414}{(2\pi)(f_{\text{cutoff}})(R1)}, \quad C2 = \frac{0.707}{(2\pi)(f_{\text{cutoff}})(R1)}$$

Where  $C1$  and  $C2$  are in farads.

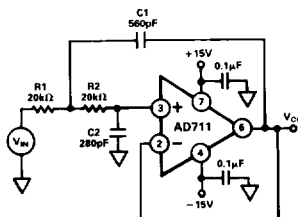


Figure 38. Second Order Low Pass Filter

An important property of filters is their out-of-band rejection. The simple 20kHz low pass filter shown in Figure 38, might be used to condition a signal contaminated with clock pulses or sampling glitches which have considerable energy content at high frequencies.

The low output impedance and high bandwidth of the AD711 minimize high frequency feedthrough as shown in Figure 39.

The upper trace is that of another low cost BiFET op amp showing 17dB more feedthrough at 5MHz.

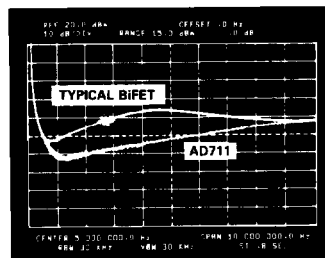


Figure 39.

# AD711

## 9 POLE CHEBYCHEV FILTER

Figure 40 shows the AD711 and its dual counterpart, the AD712, as a 9 pole Chebychev filter using active frequency dependent negative resistors (FDNR). With a cutoff frequency of 50kHz and better than 90dB rejection, it may be used as an anti-aliasing filter for a 12-bit Data Acquisition System with 100kHz throughput.

As shown in Figure 40, the filter is comprised of four FDNRs

(A, B, C, D) having values of  $4.9395 \times 10^{-15}$  and  $5.9276 \times 10^{-15}$  farad-seconds. Each FDNR active network provides a two-pole response; for a total of 8 poles. The 9th pole consists of a  $0.001\mu\text{F}$  capacitor and a  $124\text{k}\Omega$  resistor at Pin 3 of amplifier A2. Figure 41 depicts the circuits for each FDNR with the proper selection of R. To achieve optimal performance, the  $0.001\mu\text{F}$  capacitors must be selected for 1% or better matching and all resistors should have 1% or better tolerance.

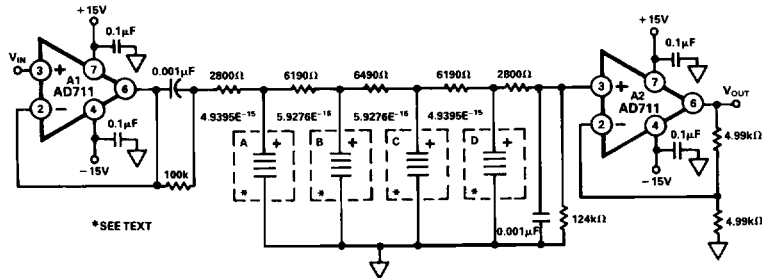


Figure 40. 9 Pole Chebychev Filter

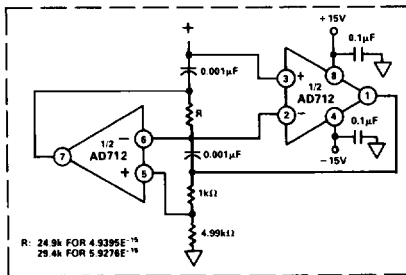


Figure 41. FDNR for 9 Pole Chebychev Filter

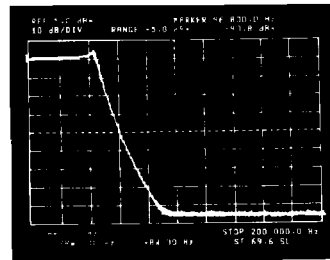


Figure 42. High Frequency Response for 9 Pole Chebychev Filter