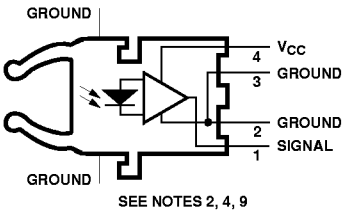
125 Megabaud Versatile Link Receiver

HFBR-25X6 Series

Description

The HFBR-25X6 receivers contain a PIN photodiode and transimpedance pre-amplifier circuit in a horizontal (HFBR-2526) or vertical (HFBR-2536) blue housing, and are designed to interface to 1mm diameter plastic optical fiber or 200 µm hard clad silica glass optical fiber. The receivers convert a received optical signal to an analog output voltage. Follow-on circuitry can optimize link performance for a variety of distance and data rate requirements. Electrical bandwidth greater than 65 MHz allows design of high speed data links with plastic or hard clad silica optical fiber. Refer to Application Note 1066 for details for recommended interface circuits.



Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Reference
Storage Temperature	T_S	-40	+75	°C	
Operating Temperature	T_A	0	+70	°C	
Lead Soldering Temperature			260	°C	Note 1
Cycle Time			10	s	
Signal Pin Voltage	V_O	-0.5	V_{CC}	V	
Supply Voltage	V_{CC}	-0.5	6.0	V	
Output Current	I_O		25	mA	

CAUTION: The small junction sizes inherent to the design of this component increase the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Electrical/Optical Characteristics 0 to 70°C; 5.25 V ≥ V_{CC} ≥ 4.75 V; power supply must be filtered (see Figure 1, Note 2).

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition	Note
AC Responsivity 1 mm POF	$R_{P,APF}$	1.7	3.9	6.5	mV/μW	650 nm	Note 4
AC Responsivity 200 μm HCS	$R_{P,HCS}$	4.5	7.9	11.5	mV/μW		
RMS Output Noise	V_{NO}		0.46	0.69	mV_{RMS}		Note 5
Equivalent Optical Noise Input Power, RMS - 1 mm POF	$P_{N,RMS}$		- 39	-36	dBm		Note 5
Equivalent Optical Noise Input Power, RMS - 200 μm HCS	$P_{N,RMS}$		-42	-40	dBm		Note 5
Peak Input Optical Power - 1 mm POF	P_R			-5.8 -6.4	dBm dBm	5 ns PWD 2 ns PWD	Note 6
Peak Input Optical Power - 200 μm HCS	P_R			-8.8 -9.4	dBm dBm	5 ns PWD 2 ns PWD	Note 6
Output Impedance	Z_O		30		Ω	50 MHz	Note 4
DC Output Voltage	V_O	0.8	1.8	2.6	V	P_R = 0 μW	
Supply Current	I_{CC}		9	15	mA		
Electrical Bandwidth	BW_E	65	125		MHz	-3 dB electrical	
Bandwidth * Rise Time			0.41		Hz * s		
Electrical Rise Time, 10-90%	t_r		3.3	6.3	ns	P_R = -10 dBm peak	
Electrical Fall Time, 90-10%	t_f		3.3	6.3	ns	P_R = -10 dBm peak	
Pulse Width Distortion	PWD		0.4	1.0	ns	P_R = -10 dBm peak	Note 7
Overshoot			4		%	P_R = -10 dBm peak	Note 8

Notes:

1. 1.6 mm below seating plane.
2. The signal output is an emitter follower, which does not reject noise in the power supply. The power supply must be filtered as in Figure 1.
3. Typical data are at 25°C and V_{CC} = +5 Vdc.
4. Pin 1 should be ac coupled to a load ≥ 510 Ω with load capacitance less than 5 pF.
5. Measured with a 3 pole Bessel filter with a 75 MHz, -3dB bandwidth.
6. The maximum Peak Input Optical Power is the level at which the Pulse Width Distortion is guaranteed to be less than the PWD listed under Test Condition. $P_{R,Max}$ is given for PWD = 5 ns for designing links at ≤ 50 MBd operation, and also for PWD = 2 ns for designing links up to 125 MBd (for both POF and HCS input conditions).
7. 10 ns pulse width, 50% duty cycle, at the 50% amplitude point of the waveform.
8. Percent overshoot is defined at:

$$\frac{(V_{PK} - V_{100\%})}{V_{100\%}} \times 100\%$$

9. Pins 5 and 8 are primarily for mounting and retaining purposes, but are electrically connected. It is recommended that these pins be connected to ground to reduce coupling of electrical noise.
10. If there is no input optical power to the receiver (no transmitted signal) electrical noise can result in false triggering of the receiver. In typical applications, data encoding and error detection prevent random triggering from being interpreted as valid data. Refer to Application Note 1066 for design guidelines.

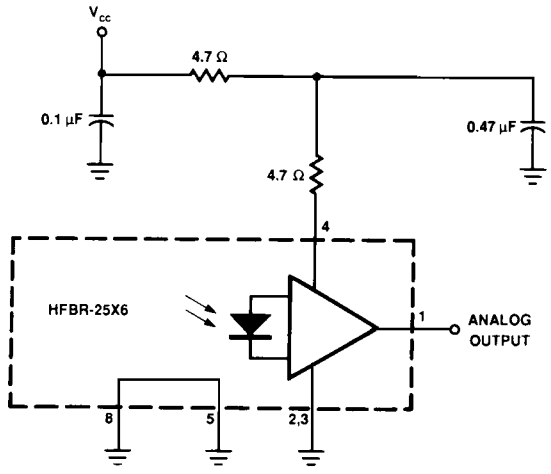


Figure 1. Recommended Power Supply Filter Circuit.

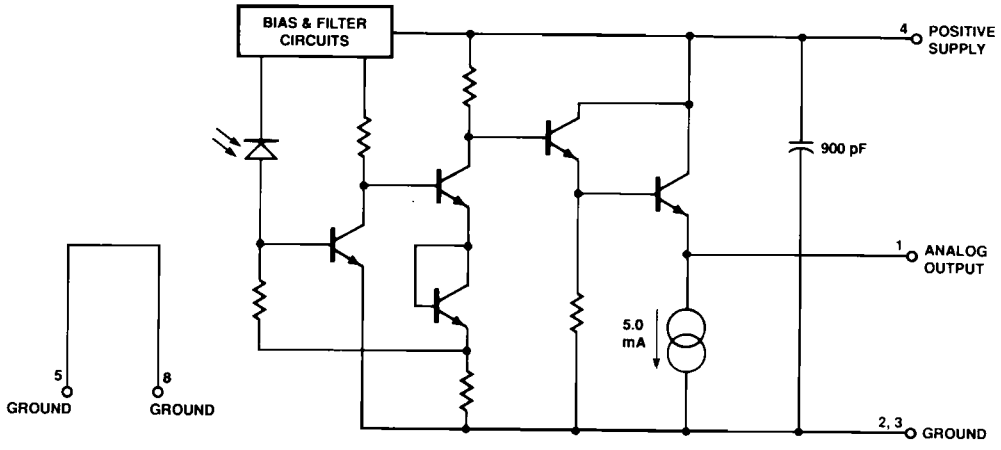


Figure 2. Simplified Receiver Schematic.

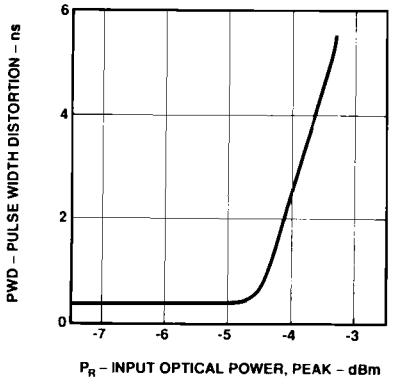


Figure 3. Typical Pulse Width Distortion vs. Peak Input Power.

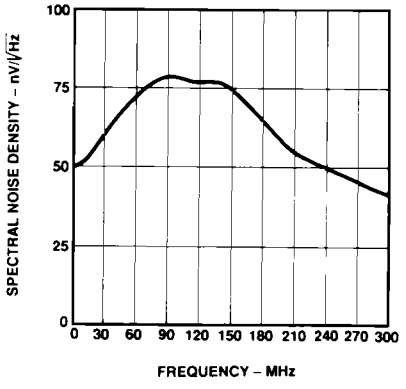


Figure 4. Typical Output Spectral Noise Density vs. Frequency.

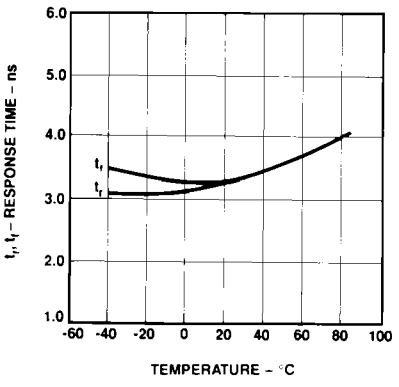
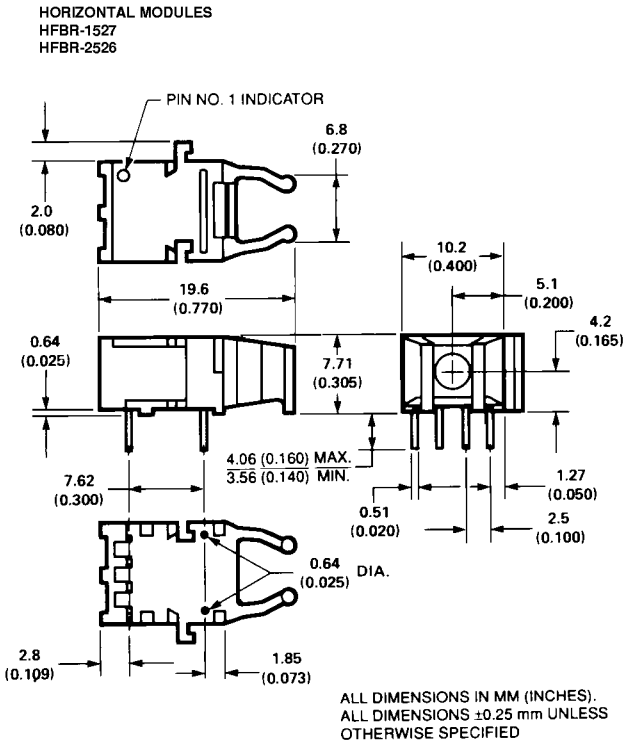
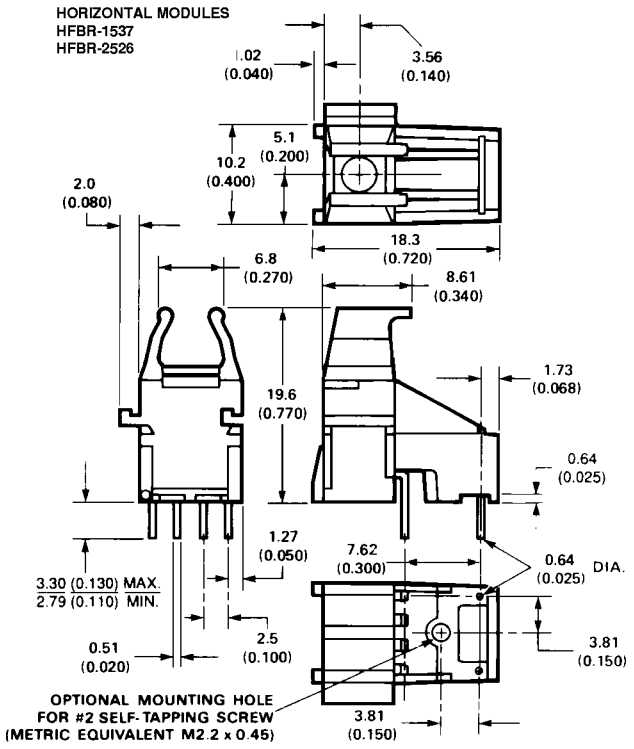


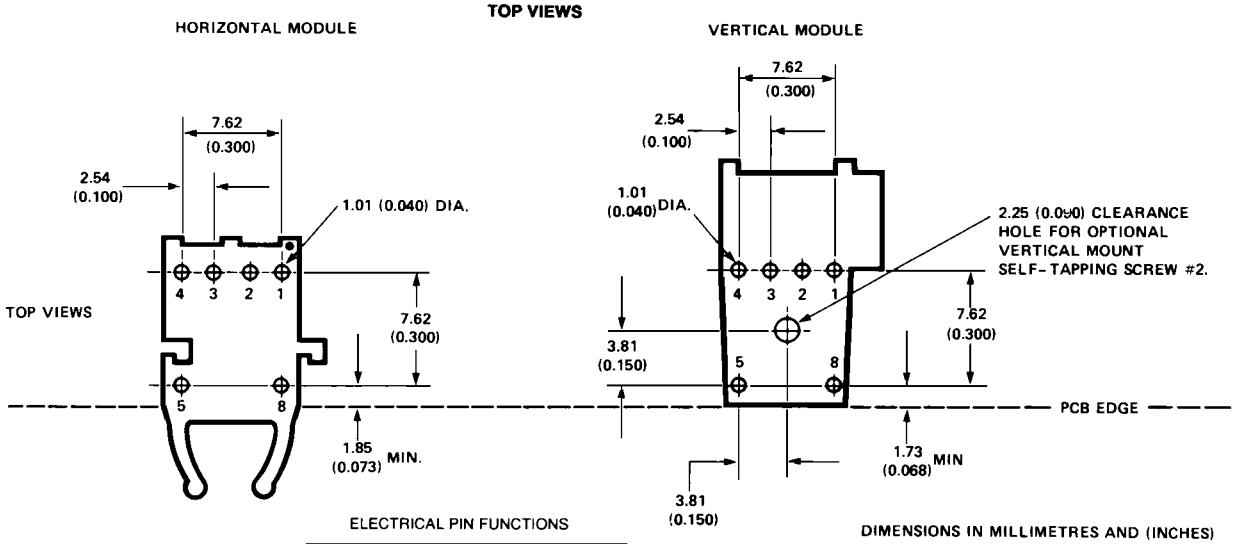
Figure 5. Typical Rise and Fall Time vs. Temperature..

Versatile Link Mechanical Dimensions





Versatile Link Printed Circuit Board Layout Dimensions



ELECTRICAL PIN FUNCTIONS

PIN NO.	TRANSMITTERS HFBR-15X7	RECEIVERS HFBR-25X6
1	ANODE	SIGNAL
2	CATHODE	GROUND
3	GROUND*	GROUND
4	GROUND*	V_{CC} (+5 V)
5	GROUND**	GROUND**
8	GROUND**	GROUND**

*NO INTERNAL CONNECTION.
**PINS 5 AND 8 CONNECTED INTERNALLY TO EACH OTHER ONLY.

DIMENSIONS IN MILLIMETRES AND (INCHES)