# HN62428 Series

## 524,288-word x 16-bit / 1,048,576-word x 8-bit CMOS Programmable Mask ROM

# HITACHI

The HN62428 Series is a 8-Mbit CMOS Programmable Mask ROM organized either as 524,288 words by 16 bits or as 1,048,576 words by 8 bits. It can be operated with a battery because of low power consumption.

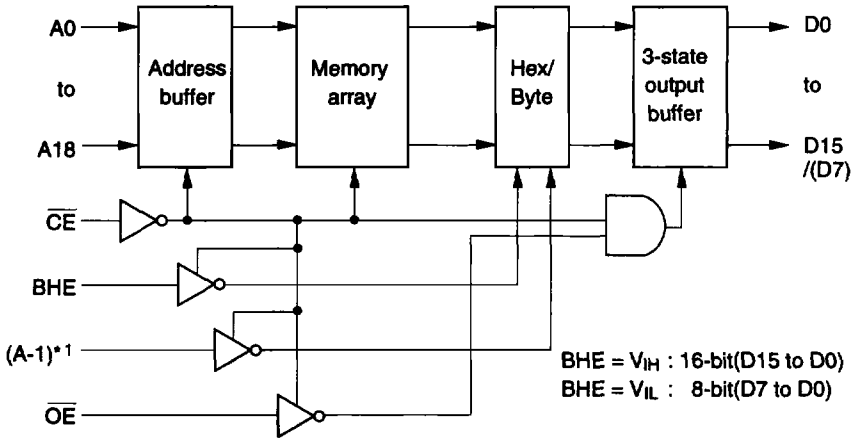
### Features

- Single 5 V
- Wired OR is permitted for the output in three states.
- TTL compatible
- Address access time: 150/200 ns (max)
- Low power consumption: 100 mW (typ) active
  5 µW (typ) standby
- Byte-wide or word-wide data organization (switched by BHE terminal)

### Ordering Information

| Type No. | Access time | Package |
|---|---|---|
| HN62428P-15/-20 | 150/200 ns | 600 mil 42-pin plastic DIP (DP-42) |
| HN62428TT-15/-20 | 150/200 ns | 44-pin plastic TSOP-II (TTP-44D) |
| HN62428FB-15/-20 | 150/200 ns | 44-pin plastic SOP (FP-44D) |

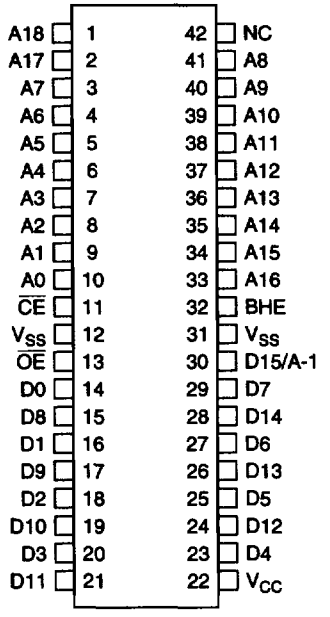
## Block Diagram




Note: 1. A-1 is least significant address. When BHE is 'low', D14 to D8 goes the high impedance state.

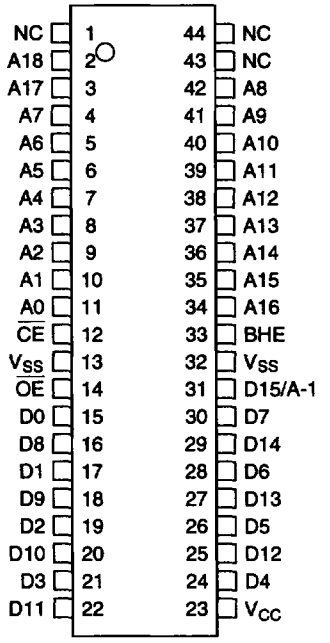
## Pin Arrangement

HN62428P



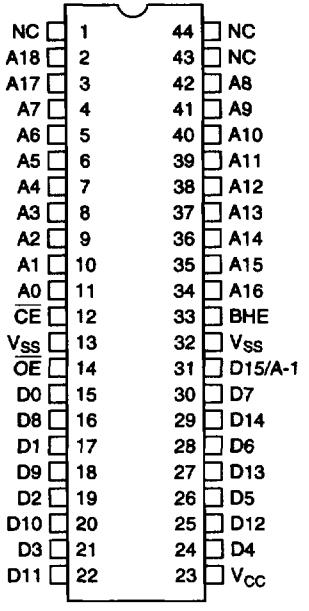

(Top View)

HN62428TT




(Top View)

HN62428FB




(Top View)

## Absolute Maximum Ratings

| Item | Symbol | Rating | Unit |
|---|---|---|---|
| Power supply voltage | $V_{CC}$ | –0.3 to +7.0 | V |
| Terminal voltage | Vin, Vout | –0.3 to $V_{CC}$ + 0.3 | V |
| Operating temperature | Topr | 0 to +70 | °C |
| Storage temperature | Tstg | –55 to +125 | °C |
| Bias temperature | Tbias | –20 to +85 | °C |

Note: With respect to $V_{SS}$.

## Recommended DC Operating Conditions ($V_{SS}$ = 0 V, Ta = 0 to +70°C)

| Item | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Power supply voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| Input voltage | $V_{IH}$ | 2.2 | — | $V_{CC}$ + 0.3 | V |
| | $V_{IL}$ | –0.3 | — | 0.8 | V |

## DC Characteristics ($V_{CC}$ = 5 V ± 10%, $V_{SS}$ = 0 V, Ta = 0 to +70°C)

| Item | | Symbol | Min | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Power supply current | Active | $I_{CC}$ | — | 50 | mA | $V_{CC}$ = 5.5 V, $I_{DOUT}$ = 0 mA, $t_{RC}$ = min |
| | Standby | $I_{SB}$ | — | 30 | µA | $V_{CC}$ = 5.5 V, $\overline{CE} \geq V_{CC} - 0.2$ V |
| Input leak current | | $\|I_{LI}\|$ | — | 10 | µA | Vin = 0 to $V_{CC}$ |
| Output leak current | | $\|I_{LO}\|$ | — | 10 | µA | $\overline{CE}$ = 2.2 V, Vout = 0 to $V_{CC}$ |
| Output voltage | | $V_{OH}$ | 2.4 | — | V | $I_{OH}$ = –205 µA |
| | | $V_{OL}$ | — | 0.4 | V | $I_{OL}$ = 1.6 mA |

## Capacitance ($V_{CC}$ = 5 V ± 10%, $V_{SS}$ = 0 V, Ta = 25°C, $V_{IN}$ = 0 V, f = 1 MHz)

| Item | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input capacitance | Cin | — | 15 | pF |
| Output capacitance | Cout | — | 15 | pF |

Note: This parameter is sampled and not 100% tested.

## AC Operating Characteristics ($V_{CC}$ = 5 V ± 10%, $V_{SS}$ = 0 V, Ta = 0 to +70°C)

**Test Conditions**

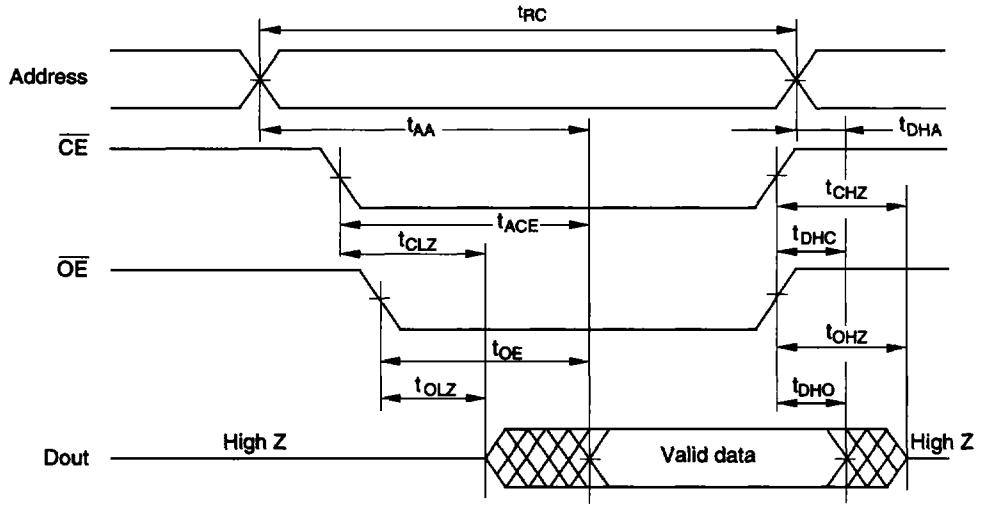
- Input pulse level: 0.8 to 2.4 V
- I/O timing reference level: 1.5 V
- Input rise/fall time: 10 ns
- Output load: 1 TTL gate + $C_L$ = 100 pF (including jig capacitance)

| Item | Symbol | HN62428-15 | | HN62428-20 | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| Cycle time | $t_{RC}$ | 150 | — | 200 | — | ns |
| Address access time | $t_{AA}$ | — | 150 | — | 200 | ns |
| $\overline{CE}$ access time | $t_{ACE}$ | — | 150 | — | 200 | ns |
| $\overline{OE}$ access time | $t_{OE}$ | — | 70 | — | 100 | ns |
| BHE access time | $t_{BHE}$ | — | 150 | — | 200 | ns |
| Output hold time from address change | $t_{DHA}$ | 0 | — | 0 | — | ns |
| Output hold time from $\overline{CE}$ | $t_{DHC}$ | 0 | — | 0 | — | ns |
| Output hold time from $\overline{OE}$ | $t_{DHO}$ | 0 | — | 0 | — | ns |
| Output hold time from BHE | $t_{DHB}$ | 0 | — | 0 | — | ns |
| $\overline{CE}$ to output in high-Z | $t_{CHZ}$*1 | — | 70 | — | 70 | ns |
| $\overline{OE}$ to output in high-Z | $t_{OHZ}$*1 | — | 70 | — | 70 | ns |
| BHE to output in high-Z | $t_{BHZ}$*1 | — | 70 | — | 70 | ns |
| $\overline{CE}$ to output in low-Z | $t_{CLZ}$ | 10 | — | 10 | — | ns |
| $\overline{OE}$ to output in low-Z | $t_{OLZ}$ | 10 | — | 10 | — | ns |
| BHE to output in low-Z | $t_{BLZ}$ | 10 | — | 10 | — | ns |

Note: *1 $t_{CHZ}$, $t_{OHZ}$ and $t_{BHZ}$ define the time at which the output goes to the high impedance state and is not referenced to output voltage level.

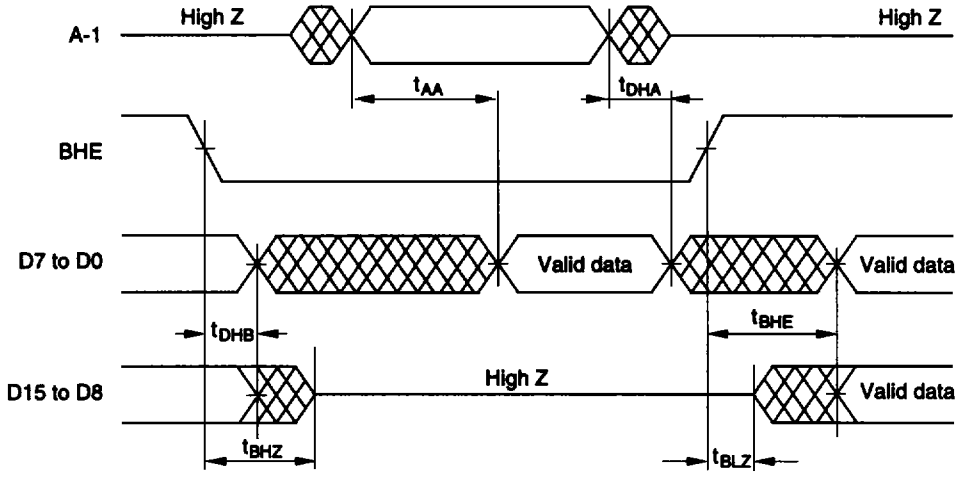
## Timing Waveform

**Word Mode (BHE = "$V_{IH}$") or Byte Mode (BHE = "$V_{IL}$")**



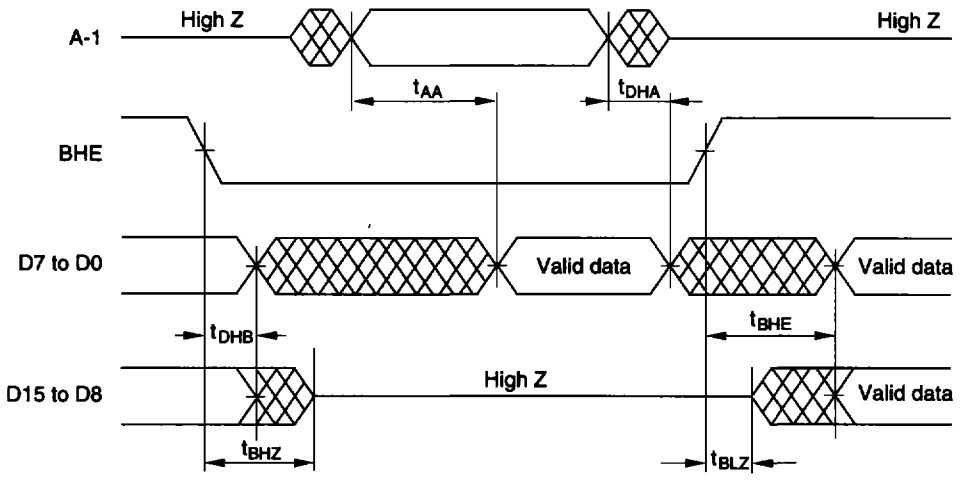

Notes: 1. $t_{DHA}$, $t_{DHC}$, $t_{DHO}$ : Determined by whichever is faster.
2. $t_{AA}$, $t_{ACE}$, $t_{OE}$ : Determined by whichever is slower.
3. $t_{CLZ}$, $t_{OLZ}$ : Determined by whichever is slower.

**Switching between Word Mode and Byte Mode**




Notes: 1. $\overline{CE}$, $\overline{OE}$ are of selected status. A18 – A0 are fixed.
2. D15/A-1 terminal is of output state when BHE = $V_{IH}$, $\overline{CE}$ and $\overline{OE}$ are of selected state. At this time, an input signal that is of the inverse phase to the output should not be impressed.

**Switching between Word Mode and Byte Mode**

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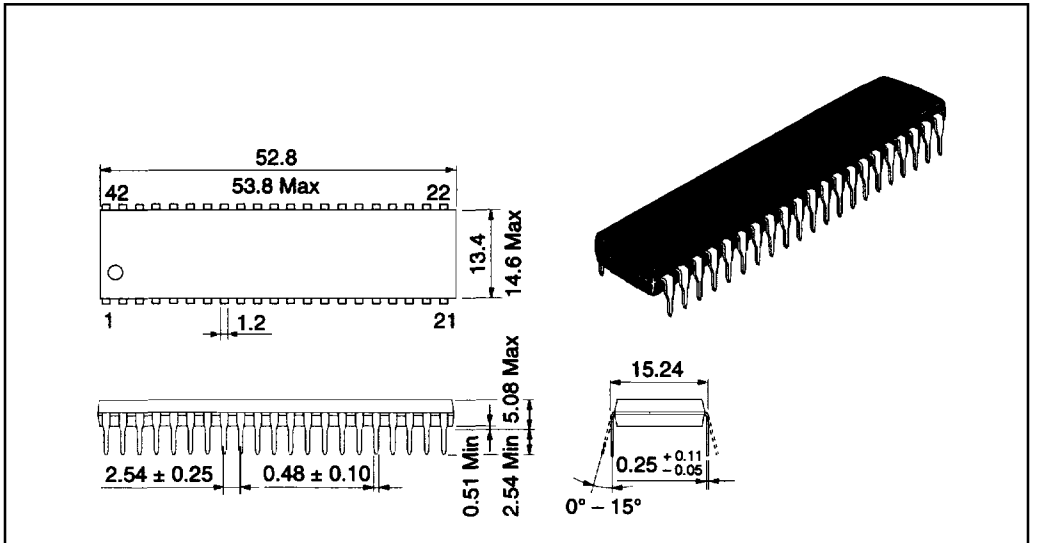
2. D15/A-1 terminal is of output state when BHE = $V_{IH}$, $\overline{CE}$ and $\overline{OE}$ are of selected state. At this time, an input signal that is of the inverse phase to the output should not be impressed.

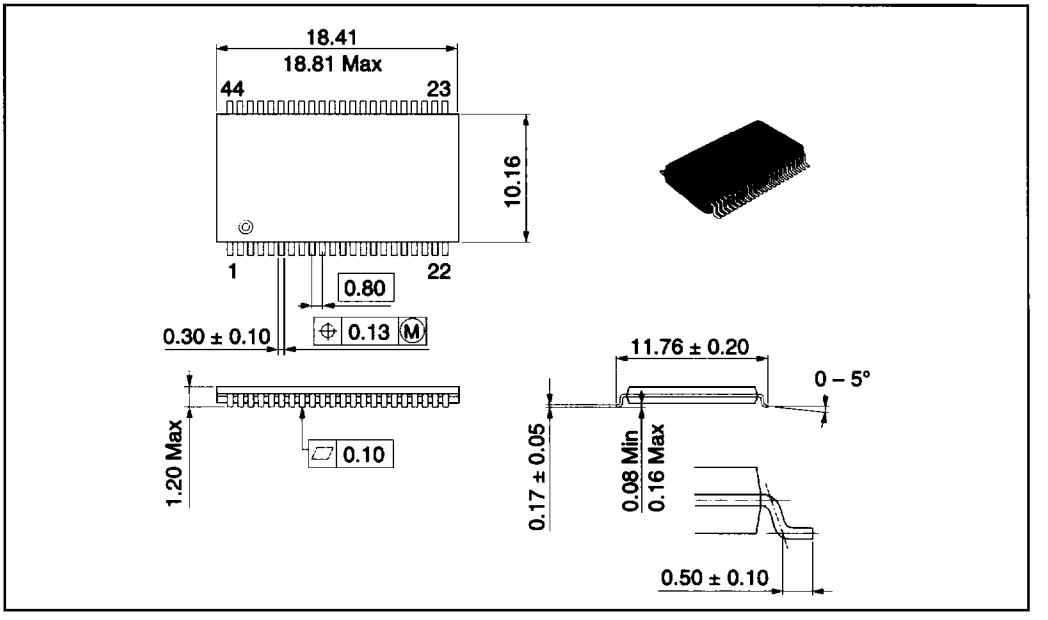
## Package Dimensions

**HN62428P Series (DP-42)** **Unit : mm**



## Package Dimensions (cont)

**HN62428TT Series (TTP-44D)** **Unit : mm**




**HN62428FB Series (FP-44D)** **Unit : mm**