ADVANCED INFORMATION

Integrated Circuit Systems, Inc.

ICS8733-01

FORWARD ERROR CORRECTION CLOCK GENERATOR

GENERAL DESCRIPTION

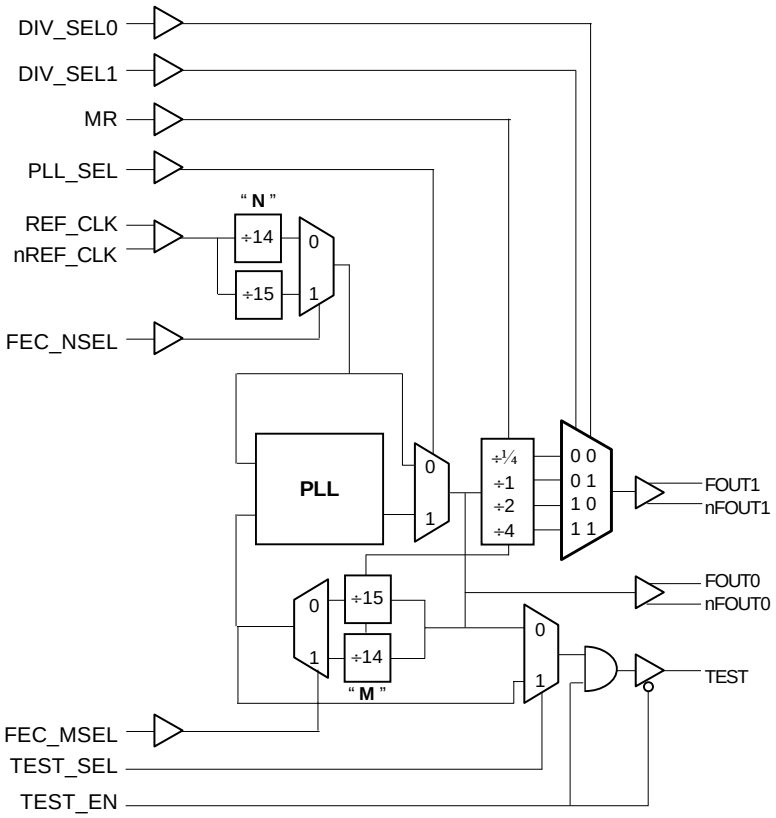
The ICS8733-01 is a dual output clock generator and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8733-01 is designed to be used for applications utilizing Forward Error Correction (FEC) designs. The ICS8733-01 generates a 14/15 or a 15/14 output clock based upon the input reference clock in order to incorporate the FEC capability required by the application.

Clock generator is performed by a fully integrated and low-jitter phase-locked loop. The ICS8733-01 accepts any differential signal as its input with an input reference frequency range of 36.27MHz to 750MHz. There are two LVPECL outputs which can generate output frequencies of 38.88MHz to 700MHz.

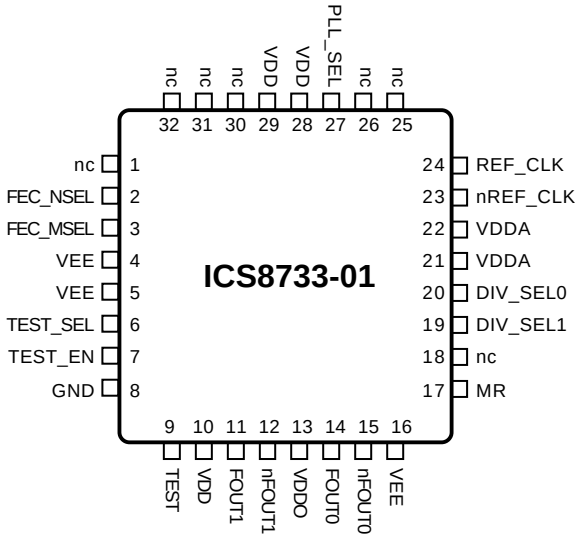
FEATURES

- Clock synthesis of 14/15 or 15/14 of the input reference clock to be utilized in Forward Error Correction (FEC) applications
- Fully integrated PLL
- Accepts any differential input signal (PECL, HSTL, LVDS, SSTL, etc.)
- Dual differential 3.3V LVPECL outputs
- 38.88MHz to 700MHz output frequency
- PLL bypass and test modes that support in-circuit testing and on-chip functional block characterization
- LVTTL / LVCMOS control inputs
- 3.3V supply voltage
- 32 lead low profile QFB (LQFP), 7mm x 7mm x 1.4mm package body, 0.8mm package lead pitch
- 0°C to 70°C ambient operating temperature

BLOCK DIAGRAM



PIN ASSIGNMENT



32-Lead LQFP
Y Package
Top View

The Advance Information presented herein represents a product currently in design or being considered for design. The noted characteristics are design targets. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

FUNCTIONAL DESCRIPTION

The ICS8733-01 features a fully integrated PLL and therefore requires no external component for setting the loop bandwidth.

The ICS8733-01 will generate an output having a frequency as follows:

$$fFOUT0 = fREF\_CLK \times \frac{M}{N}$$

The M and N bits are controlled by the FEC_NSEL and FEC_MSEL control pins as shown in *Table 3A and Table 3B.*

As a result, FOUT0 can be configured to have an output frequency equal to 14/15, 15/14, 14/14, or 15/15 of the reference input frequency.

The second output clock (FOUT1) is configured to produce a frequency equal to FOUT0, FOUT/2, FOUT0/4, or FOUT0x4, dependent upon the DIV_SEL0 and DIV_SEL1 bits as shown in *Table 3C.*

The reference input frequency range is dependent upon not only the M and N bits, but also upon the FOUT1 output configuration which is determined by the DIV_SEL0 and DIV_SEL1 bits. *Table 3B* shows the possible FOUT0 and FOUT1 output configurations as well as the reference input frequency range for each of these configurations.

The ICS8733-01 also supports in-circuit testing and on-chip functional block characterization via two test inputs and one test output. With the ICS8733-01 in PLL bypass mode (PLL_SEL = 0), the reference input bypasses the PLL and in-circuit testing of the N, M, and output dividers can take place. *Table 3D* shows the output configurations for the different combinations of the DIV_SEL1 and DIV_SEL0 pins.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 18, 25, 26, 30, 31, 32	nc	Unused		Unused pin.
2	FEC_NSEL	Input	Pulldown	Selects the N divide value. LVCMOS / LVTTL interface levels.
3	FEC_MSEL	Input	Pulldown	Selects the M divide value. LVCMOS / LVTTL interface levels.
4, 5, 8, 16	VEE	Power		Ground pin. Connect to ground.
6	TEST_SEL	Input	Pulldown	Configures the TEST output pin to one of two different test modes. LVCMOS / LVTTL interface levels.
7	TEST_EN	Input	Pulldown	Enables the TEST output pin. LVCMOS / LVTTL interface levels.
9	TEST	Output		Output test pin. Programmed using TEST_SEL pin as shown in Table 3D.
10, 28, 29	VDD	Power		Power supply pin for core and test output.
11, 12	FOUT1, nFOUT1	Output		Differential output for the generator. 3.3V LVPECL interface levels.
13	VDDO	Power		Output power supply pins. Connect to 3.3V.
14, 15	FOUT0, nFOUT0	Output		Differential ouput for the generator. 3.3V LVPECL interface levels.
17	MR	Input	Pulldown	Resets the M, N, and output divider. Forces FOUT0 and FOUT1 low. LVCMOS / LVTTL interface levels.
19, 20	DIV_SEL1, DIV_SEL0	Input	Pulldown	Determines the output divide value for FOUT1. LVCMOS / LVTTL interface levels.
21, 22	VDDA	Power		PLL power supply pin. Connect to 3.3V.
23	nREF_CLK,	Input	Pullup	Inverting differential clock input. Accepts any differential levels.
24	REF_CLK	Input	Pulldown	Non-inverting differential clock input. Accepts any differential levels.
27	PLL_SEL	Input	Pullup	Determines whether generator is in PLL or bypass mode. LVCMOS / LVTTL interface levels.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
CIN	Input Capacitance	REF_CLK, nREF_CLK			TBD		pF
		MR, PLL_SEL, TEST_EN, TEST_SEL, DIV_SEL0, DIV_SEL1, FEC_NSEL, FEC_MSEL			TBD		pF
RPULLUP	Input Pullup Resistor				51		KΩ
RPULLDOWN	Input Pulldown Resistor				51		KΩ

TABLE 3A. FEC_NSEL TRUTH TABLE

FEC_NSEL	N
0	14
1	15

TABLE 3B. FEC-MSEL TRUTH TABLE

FEC_MSEL	M
0	15
1	14

TABLE 3C. OUTPUT CONFIGURATION AND INPUT FREQUENCY RANGE TABLE

DIV_SEL1	DIV_SEL0	FOUT0	FOUT1	Reference Input Frequency Range (MHz)			
				FEC_NSEL: FEC_MSEL = 00	FEC_NSEL: FEC_MSEL = 01	FEC_NSEL: FEC_MSEL = 10	FEC_NSEL: FEC_MSEL = 11
0	0	fREFxM/N	fREFx4M/N	36.27 - 81.67	36.27 - 87.50	38.88 - 87.50	38.88 - 93.75
0	1	fREFxM/N	fREFxM/N	93.3 - 326.67	100 - 350	100 - 350	107.1 - 375
1	0	fREFxM/N	fREFxM/2N	186.7 - 653.33	200 - 700	200 - 700	214.3 - 750
1	1	fREFxM/N	fREFxM/4N	186.7 - 653.33	200 - 700	200 - 700	214.3 - 750

TABLE 3D. OUTPUT CONFIGURATION TABLE FOR TEST MODE OPERATION (PLL_SEL = 0 AND TEST_EN = 1)

DIV_SEL1	DIV_SEL0	FOUT0	FOUT1	Test	
				TEST_SEL = 0	TEST_SEL = 1
0	0	fREF/4N	fREF/N	2fREF/N	fREF/2MN
0	1	fREF/N	fREF/N	2fREF/N	2fREF/MN
1	0	fREF/N	fREF/2N	fREF/N	fREF/MN
1	1	fREF/N	fREF/4N	fREF/N	fREF/MN

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	4.6V
Inputs	-0.5V to VDD+0.5 V
Outputs	-0.5V to VDD+0.5V
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, VDD=VDDA=VDDO=3.3V±5%, T_A=0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
VDD	Input Power Supply Voltage		3.135	3.3	3.465	V
VDDA	Analog Power Supply Voltage		3.135	3.3	3.465	V
VDDO	Output Power Supply Voltage		3.135	3.3	3.465	V
IEE	Power Supply Current					mA

TABLE 4B. DIFFERENTIAL DC CHARACTERISTICS, VDD=VDDA=VDDO=3.3V±5%, T_A=0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
IIH	Input High Current	REF_CLK	VIN = 3.465V			150	µA
		nREF_CLK	VIN = 3.465V			5	µA
IIL	Input Low Current	REF_CLK	VIN = 0V	-5			µA
		nREF_CLK	VIN = 0V	-150			µA

NOTE: For REF_CLK, nREF_CLK input levels, see VPP and VCMR in AC Characteristics table.

TABLE 4C. LVCMOS/LVTTL DC CHARACTERISTICS, VDD=VDDA=VDDO=3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
VIH	Input High Voltage	DIV_SEL0, DIV_SEL1, PLL_SEL, MR, FEC_NSEL, FEC_MSEL, TEST_SEL, TEST_EN	VDDI = 3.465V	2		3.765	V
VIL	Input Low Voltage	DIV_SEL0, DIV_SEL1, PLL_SEL, MR, FEC_NSEL, FEC_MSEL, TEST_SEL, TEST_EN	VDDI = 3.465V	-0.3		0.8	V
IIH	Input High Current	DIV_SEL0, DIV_SEL1, FEC_NSEL, FEC_MSEL, TEST_SEL, TEST_EN, MR	VDDx = VIN = 3.465V			150	µA
		PLL_SEL	VDDx = VIN = 3.465V			5	µA
IIL	Input Low Current	DIV_SEL0, DIV_SEL1, FEC_NSEL, FEC_MSEL, TEST_SEL, TEST_EN, MR	VDDx = 3.465V, VIN = 0V	-5			µA
		PLL_SEL	VDDx = 3.465V, VIN = 0V	-150			µA
VOH	Output High Voltage	TEST	VDDx = 3.135V, IOH = -36mA	2.6			V
VOL	Output Low Voltage	TEST	VDDx = 3.135V, IOL = 36mA			0.5	V

TABLE 4D. LVPECL DC CHARACTERISTICS, VDD=VDDA=VDDO=3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
VOH	Output High Voltage; NOTE 1, 2	FOUT0, nFOUT0, FOUT1, nFOUT1	VDDx = 3.3V	2.1			V
VOL	Output Low Voltage; NOTE 1, 2	FOUT0, nFOUT0, FOUT1, nFOUT1	VDDx = 3.3V			1.6	V
VSWING	Peak-to-Peak Output Voltage Swing	FOUT0, nFOUT0, FOUT1, nFOUT1					

NOTE 1: FOUT0, nFOUT0, FOUT1, nFOUT1 outputs terminated with 50 Ω to VDDO - 2V.
NOTE 2: These levels are specified for VDDO - 3.3V. Output levels will vary 1:1 with VDDO.

TABLE 5. INPUT FREQUENCY CHARACTERISTICS, VDD=VDDA=VDDO=3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
fIN	Maximum Input Frequency	REF_CLK		36.27		750	MHz
tR	Input Rise Time	REF_CLK	Measured at 20% to 80% points			TBD	ns
tF	Input Fall Time	REF_CLK	Measured at 20% to 80% points			TBD	ns
tDC	Input Reference Duty Cycle	REF_CLK		TBD		TBD	%

TABLE 6. AC CHARACTERISTICS, VDD=VDDA=VDDO=3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
FOUT	Output Frequency		3.135 ≤ VDDx ≤ 3.465V	31.25		700	MHz
VPP	Peak-to-Peak Input Voltage	REF_CLK, nREF_CLK		0.15		1.3	V
VCMR	Common Mode Input Voltage	REF_CLK, nREF_CLK	LVPECL Levels	1.8		2.4	V
			DCM, HSTL, LVDS, SSTL Levels	0.31		1.3	V
tsk(o)	Output Skew					10	ps
tjit(cc)	Peak Cycle-to-Cycle Jitter					50	ps
tDC	Output Duty Cycle			47		53	%
tR	Output Rise Time	FOUT0, nFOUT0, FOUT1, nFOUT1	20% to 80%	300		800	ps
tF	Output Fall Time	FOUT0, nFOUT0, FOUT1, nFOUT1	20% to 80%	300		800	ps
tLOCK	PLL Lock Time					TBD	ns

PACKAGE OUTLINE - Y SUFFIX

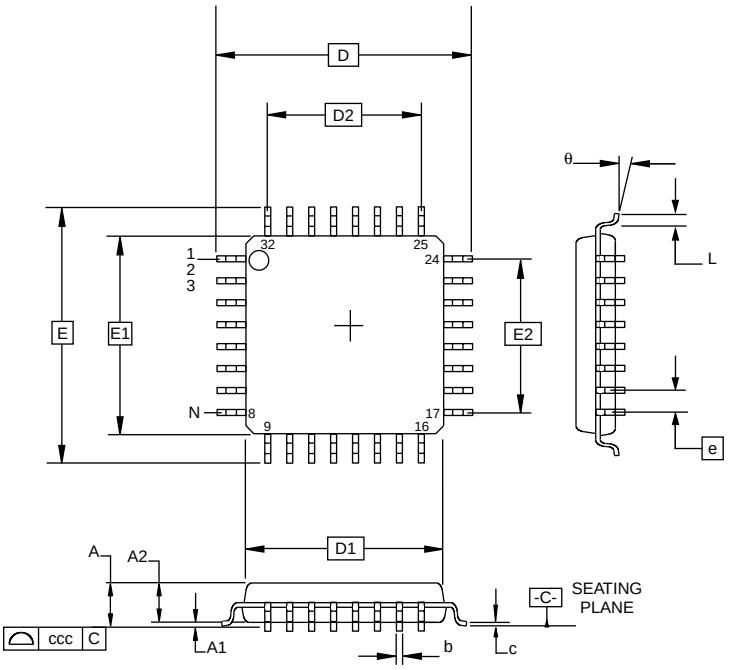


TABLE 7. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09		0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.60	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.60	
e		0.80 BASIC	
L	0.45	0.60	0.75
θ	0°		7°
ccc			0.10

Reference Document: JEDEC Publication 95, MS-026

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8733Y-01	ICS8733-01	32 Lead LQFP	250 per tray	0°C to 70°C
ICS8733YT-01	ICS8733-01	32 Lead LQFP on Tape and Reel	2000	0°C to 70°C