40V Precision Single Supply Rail-to-Rail Output Low Power Operational Amplifiers

ISL28118, ISL28218

The ISL28118 and ISL28218 are single and dual precision, single supply rail-to-rail output amplifiers with a common mode input voltage range extending to 0.5V below the V- rail. These op amps feature low power, low offset voltage, and low temperature drift, making them the ideal choice for applications requiring both high DC accuracy and AC performance. The devices can operate from single (3V to 40V) or dual (±1.5V to ±20V) supplies. The combination of precision and small footprint provides the user with outstanding value and flexibility relative to similar competitive parts.

Applications for these amplifiers include precision instrumentation, data acquisition, precision power supply controls, and industrial controls.

Both parts are offered in 8 Ld TDFN, 8 Ld SOIC and 8 Ld MSOP packages. All devices are offered in standard pin configurations and operate over the extended temperature range of -40°C to +125°C.

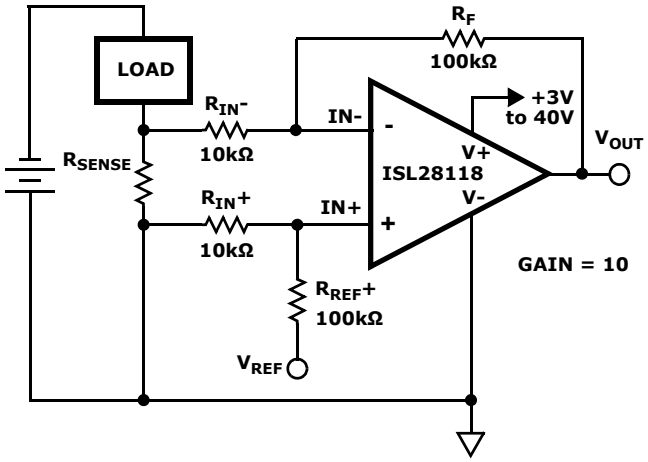
Features

- Rail-to-Rail Output
- Below-Ground (V-) Input Capability to -0.5V
- Single Supply Range . . . . . .3V to 40V
- Low Current Consumption 850µA
- Low Noise Voltage . . . . . 5.6nV/√Hz
- Low Noise Current . . . . . 355fA/√Hz
- Low Input Offset Voltage
  - ISL28118 . . . . . 150µV Max.
  - ISL28218 . . . . . 230µV Max.
- Superb Offset Voltage Temperature Drift
  - ISL28118 . . . . . .1.2µV/°C, Max.
  - ISL28218 . . . . . .1.4µV/°C, Max.
- Operating Temperature Range . . . .-40°C to +125°C
- No Phase Reversal

Applications

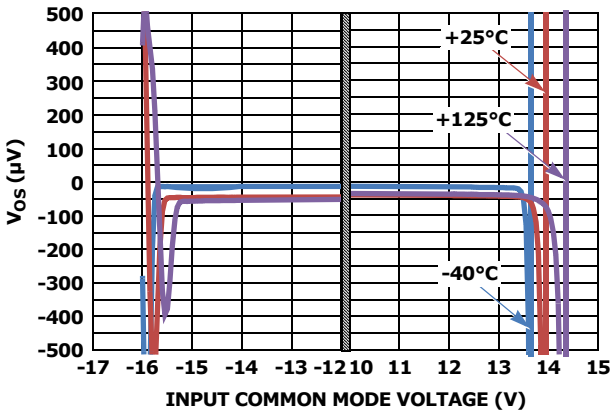
- Precision Instruments
- Medical Instrumentation
- Data Acquisition
- Power Supply Control
- Industrial Process Control

Typical Application

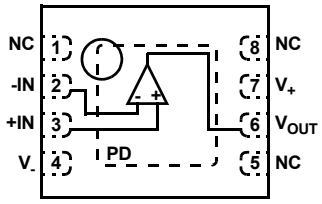


SINGLE-SUPPLY, LOW-SIDE CURRENT SENSE AMPLIFIER

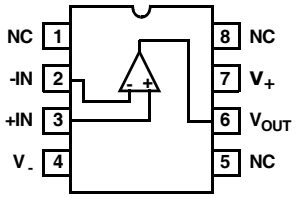
Input Offset Voltage vs Input Common Mode Voltage, V_S = ±15V



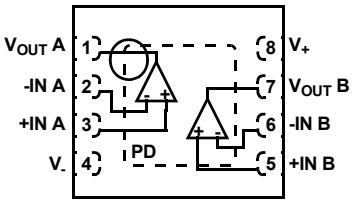
ISL28118
(8 LD TDFN)
TOP VIEW



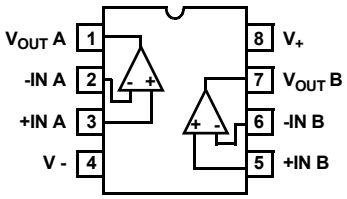
ISL28118
(8 LD SOIC, 8 LD MSOP)
TOP VIEW



ISL28218
(8 LD TDFN)
TOP VIEW

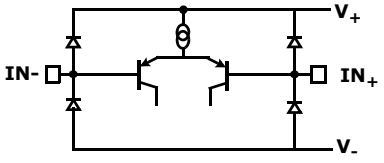


ISL28218
(8 LD SOIC, 8 LD MSOP)
TOP VIEW

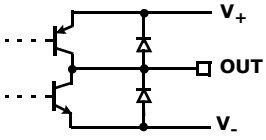


Pin Descriptions

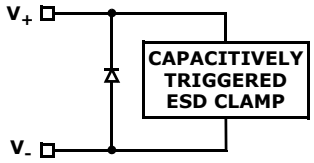
ISL28118 (8 LD TDFN)	ISL28118 (8 LD SOIC, MSOP)	ISL28218 (8 LD TDFN)	ISL28218 (8 LD SOIC, MSOP)	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
3	3	3	3	+IN_A	Circuit 1	Amplifier A non-inverting input
2	2	2	2	-IN_A	Circuit 1	Amplifier A inverting input
6	6	1	1	V_{OUT}_A	Circuit 2	Amplifier A output
4	4	4	4	V_-	Circuit 3	Negative power supply
		5	5	+IN_B	Circuit 1	Amplifier B non-inverting input
		6	6	-IN_B	Circuit 1	Amplifier B inverting input
		7	7	V_{OUT}_B	Circuit 2	Amplifier B output
7	7	8	8	V_+	Circuit 3	Positive power supply
PAD		PAD		PAD		Thermal Pad is electrically isolated from active circuitry. Pad can float, connect to Ground or to a potential source that is free from signals or noise sources.



CIRCUIT 1



CIRCUIT 2



CIRCUIT 3

Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	TEMPERATURE RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL28118FBZ	28118 FBZ	-40 to +125	8 Ld SOIC	M8.15E
Coming Soon ISL28118FRTZ	118Z	-40 to +125	8 Ld TDFN	L8.3x3A
Coming Soon ISL28118FUZ	8118Z	-40 to +125	8 Ld MSOP	M8.118
ISL28218FBZ (Note 1)	28218 FBZ	-40 to +125	8 Ld SOIC	M8.15E
ISL28218FRTZ	218Z	-40 to +125	8 Ld TDFN	L8.3x3A
ISL28218FUZ	8218Z	-40 to +125	8 Ld MSOP	M8.118

NOTES:

1. Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL28118, ISL28218. For more information on MSL, please see Technical Brief TB363.

Absolute Maximum Ratings

Maximum Supply Voltage 42V
Maximum Differential Input Current 20mA
Maximum Differential Input
Voltage. . . . . 42V or V_- - 0.5V to V_+ + 0.5V
Min/Max Input Voltage . . . . . 42V or V_- - 0.5V to V_+ + 0.5V
Max/Min Input Current for Input Voltage . . >V+ or <V- ±20mA
Output Short-Circuit Duration (1 output at a time) . . Indefinite
ESD Tolerance
Human Body Model (Tested per JESD22-A114F) 3kV
Machine Model (Tested per JESD22-A115-A) 300V
Charged Device Model (Tested per CDM-22CI0ID) 2kV

Operating Conditions

Ambient Operating Temperature Range . . . . -40°C to +125°C
Maximum Operating Junction Temperature . . . . . +150°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
ISL28118		
8 Ld TDFN Package (Notes 5, 6) . . .	50	9
8 Ld SOIC Package (Notes 4, 7) . . .	120	60
8 Ld MSOP Package (Notes 4, 7) . .	165	57
ISL28218		
8 Ld TDFN Package (Notes 5, 6) . . .	48	5.5
8 Ld SOIC Package (Notes 4, 7) . . .	120	55
8 Ld MSOP Package (Notes 4, 7) . .	150	45

Storage Temperature Range . . . . . -65°C to +150°C
Pb-free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
6. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.
7. For θ_{JC}, the “case temp” location is taken at the package top center.

Electrical Specifications

V_S ±15V, V_{CM} = 0, V_O = 0V, R_L = Open, T_A= +25°C, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +125°C. Temperature data established by characterization**.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
V_{OS}	Input Offset Voltage	ISL28118	-150	25	150	µV
			-270		**270**	µV
		ISL28218	-230	40	230	µV
			-290		**290**	µV
TCV_{OS}	Input Offset Voltage Temperature Coefficient	ISL28118	**-1.2**	**0.2**	**1.2**	µV/°C
		ISL28218	**-1.4**	**0.3**	**1.4**	µV/°C
ΔV_{OS}	Input Offset Voltage Match (ISL28218 only)		-280	44	280	µV
			-365		**365**	µV
I_B	Input Bias Current		-575	-230		nA
			-800			nA
TCI_B	Input Bias Current Temperature Coefficient			**-0.8**		nA/°C
I_{OS}	Input Offset Current		-50	4	50	nA
			-75		**75**	nA
CMRR	Common-Mode Rejection Ratio	V_{CM} = V_- - 0.5V to V_+ - 1.8V		118		dB
		V_{CM} = V_- - 0.2V to V_+ -1.8V		118		dB
	ISL28118	V_{CM} = V_- to V_+ -1.8V	102	118		dB
			98			dB
	ISL28218	V_{CM} = V_- to V_+ -1.8V	103	118		dB
			99			dB

Electrical Specifications V_S ±15V, V_{CM} = 0, V_O = 0V, R_L = Open, T_A= +25°C, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +125°C. Temperature data established by characterization. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
V_{CMIR}	Common Mode Input Voltage Range	Guaranteed by CMRR test	V_- - 0.5		V_+ - 1.8	V
			V_-		**V_+ - 1.8**	V
PSRR	Power Supply Rejection Ratio	V_S = 3V to 40V, V_{CMIR} = Valid Input Voltage	109	124		dB
			105			dB
A_{VOL}	Open-Loop Gain	V_O = -13V to +13V, R_L = 10kΩ to ground	125	136		dB
		ISL28118	**120**			dB
		ISL28218	**122**			dB
V_{OL}	Output Voltage Low, V_{OUT} to V_-	R_L = 10kΩ			70	mV
		ISL28118			**85**	mV
		ISL28218			**73**	mV
V_{OH}	Output Voltage High, V_+ to V_{OUT}	R_L = 10kΩ			110	mV
					120	mV
I_S	Supply Current/Amplifier	ISL28118; R_L = Open		0.85	1.2	mA
					1.6	mA
		ISL28218; R_L = Open		0.85	1.1	mA
					1.4	mA
I_{SC+}	Output Short Circuit Source Current	R_L = 10Ω to V_-		16		mA
I_{SC-}	Output Short Circuit Sink Current	R_L = 10Ω to V_+		28		mA
V_{SUPPLY}	Supply Voltage Range	Guaranteed by PSRR	**3**		**40**	V
AC SPECIFICATIONS						
GBWP	Gain Bandwidth Product	A_{CL} = 101, V_{OUT} = 100mV_{P-P}; R_L = 2k		4		MHz
e_{np-p}	Voltage Noise	0.1Hz to 10Hz, V_S = ±18V		300		nV_{P-P}
e_n	Voltage Noise Density	f = 10Hz, V_S = ±18V		8.5		nV/√Hz
e_n	Voltage Noise Density	f = 100Hz, V_S = ±18V		5.8		nV/√Hz
e_n	Voltage Noise Density	f = 1kHz, V_S = ±18V		5.6		nV/√Hz
e_n	Voltage Noise Density	f = 10kHz, V_S = ±18V		5.6		nV/√Hz
in	Current Noise Density	f = 1kHz, V_S = ±18V		355		fA/√Hz
THD + N	Total Harmonic Distortion + Noise	1kHz, G = 1, V_O = 3.5V_{RMS}, R_L = 10kΩ		0.0003		%
TRANSIENT RESPONSE						
SR	Slew Rate	A_V = 1, R_L = 2kΩ, V_O = 10V_{P-P}		±1.2		V/µs
t_r, t_f, Small Signal	Rise Time 10% to 90% of V_{OUT}	A_V = 1, V_{OUT} = 100mV_{P-P} , R_f = 0Ω, R_L = 2kΩ to V_{CM}		100		ns
	Fall Time 90% to 10% of V_{OUT}	A_V = 1, V_{OUT} = 100mV_{P-P} , R_f = 0Ω, R_L = 2kΩ to V_{CM}		100		ns
t_s	Settling Time to 0.01% 10V Step; 10% to V_{OUT}	A_V = 1, V_{OUT} = 10V_{P-P} , R_f = 0Ω R_L = 2kΩ to V_{CM}		8.5		µs

Electrical Specifications

V_S ±5V, V_{CM} = 0, V_O = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +125°C. Temperature data established by characterization**.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
V_{OS}	Input Offset Voltage	ISL28118	-150	25	150	µV
			-270		**270**	µV
		ISL28218	-230	40	230	µV
			-290		**290**	µV
TCV_{OS}	Input Offset Voltage Temperature Coefficient	ISL28118	**-1.2**	**0.2**	**1.2**	µV/°C
		ISL28218	**-1.4**	**0.3**	**1.4**	µV/°C
ΔV_{OS}	Input Offset Voltage Match (ISL28218 only)		-280	44	280	µV
			-365		**365**	µV
I_B	Input Bias Current		-575	-230		nA
			-800			nA
TCI_B	Input Bias Current Temperature Coefficient			**-0.8**		nA/°C
I_{OS}	Input Offset Current		-50	4	50	nA
			-75		**75**	nA
CMRR	Common-Mode Rejection Ratio	V_{CM} = V_- - 0.5V to V_+ - 1.8V		119		dB
		V_{CM} = V_- - 0.2V to V_+ -1.8V		119		dB
		V_{CM} = V_- to V_+ -1.8V	101	117		dB
			97			dB
V_{CMIR}	Common Mode Input Voltage Range	Guaranteed by CMRR test	V_- - 0.5		V_+ - 1.8	V
			V_-		**V_+ - 1.8**	V
PSRR	Power Supply Rejection Ratio	V_S = 3V to 40V, V_{CMIR} = Valid Input Voltage	109	124		dB
			105			dB
A_{VOL}	Open-Loop Gain	V_O = -3V to +3V, R_L = 10kΩ to ground	122	132		dB
			117			dB
V_{OL}	Output Voltage Low, V_{OUT} to V_-	R_L = 10kΩ			38	mV
					45	mV
V_{OH}	Output Voltage High, V_+ to V_{OUT}	R_L = 10kΩ			65	mV
					70	mV
I_S	Supply Current/Amplifier	R_L = Open		0.85	1.1	mA
					1.4	µA
I_{SC+}	Output Short Circuit Source Current	R_L = 10Ω to V_-		13		mA
I_{SC-}	Output Short Circuit Sink Current	R_L = 10Ω to V_+		20		mA
AC SPECIFICATIONS						
GBWP	Gain Bandwidth Product	A_{CL} = 101, V_{OUT} = 100mV_{P-P}; R_L = 2k		3.2		MHz
e_{np-p}	Voltage Noise	0.1Hz to 10Hz		320		nV_{P-P}
e_n	Voltage Noise Density	f = 10Hz		9		nV/√Hz
e_n	Voltage Noise Density	f = 100Hz		5.7		nV/√Hz

Electrical Specifications V_S ±5V, V_{CM} = 0, V_O = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +125°C. Temperature data established by characterization. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
e_n	Voltage Noise Density	f = 1kHz		5.5		nV/√Hz
e_n	Voltage Noise Density	f = 10kHz		5.5		nV/√Hz
in	Current Noise Density	f = 1kHz		380		fA/√Hz
THD + N	Total Harmonic Distortion + Noise	1kHz, G = 1, V_O = 1.25V_{RMS}, R_L = 10kΩ		0.0003		%
TRANSIENT RESPONSE						
SR	Slew Rate	A_V = 1, R_L = 2kΩ, V_O = 4V_{P-P}		±1		V/µs
t_r, t_f, Small Signal	Rise Time 10% to 90% of V_{OUT}	A_V = 1, V_{OUT} = 100mV_{P-P}, R_f = 0Ω, R_L = 2kΩ to V_{CM}		100		ns
	Fall Time 90% to 10% of V_{OUT}	A_V = 1, V_{OUT} = 100mV_{P-P}, R_f = 0Ω, R_L = 2kΩ to V_{CM}		100		ns
t_s	Settling Time to 0.01% 4V Step; 10% to V_{OUT}	A_V = 1, V_{OUT} = 4V_{P-P} , R_f = 0Ω R_L = 2kΩ to V_{CM}		4		µs

NOTE:

8. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified.

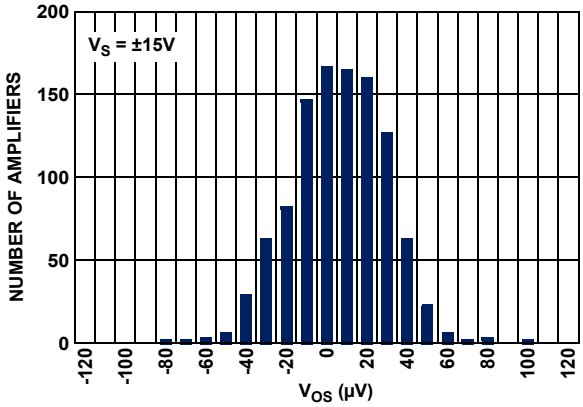


FIGURE 1. ISL28118 INPUT OFFSET VOLTAGE DISTRIBUTION

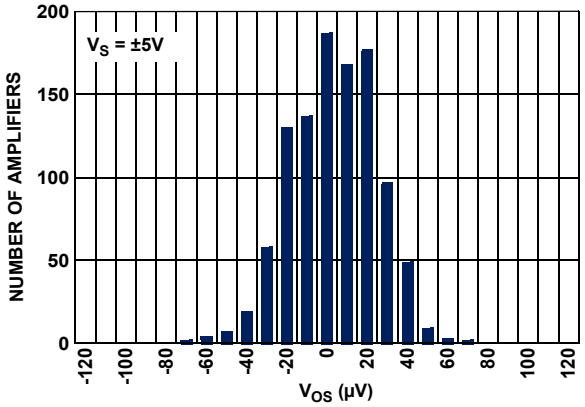


FIGURE 2. ISL28118 INPUT OFFSET VOLTAGE DISTRIBUTION

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. **(Continued)**

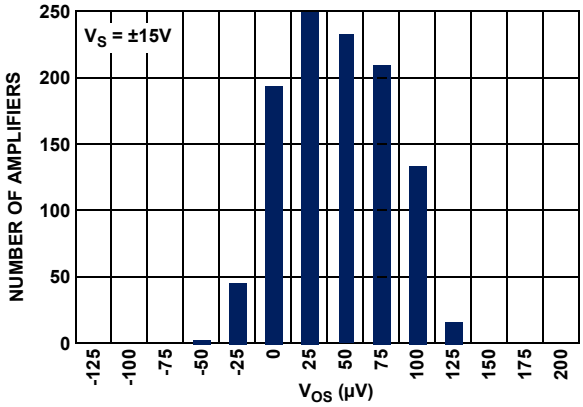


FIGURE 3. ISL28218 INPUT OFFSET VOLTAGE DISTRIBUTION

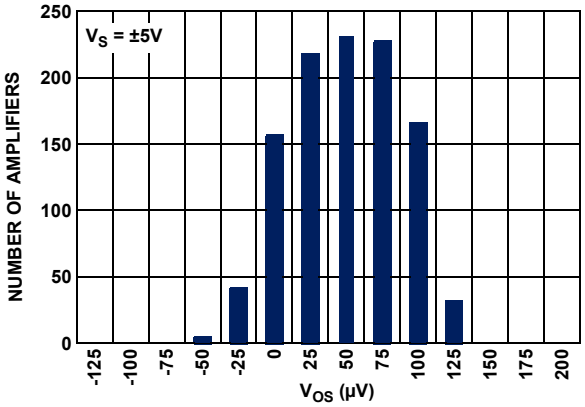


FIGURE 4. ISL28218 INPUT OFFSET VOLTAGE DISTRIBUTION

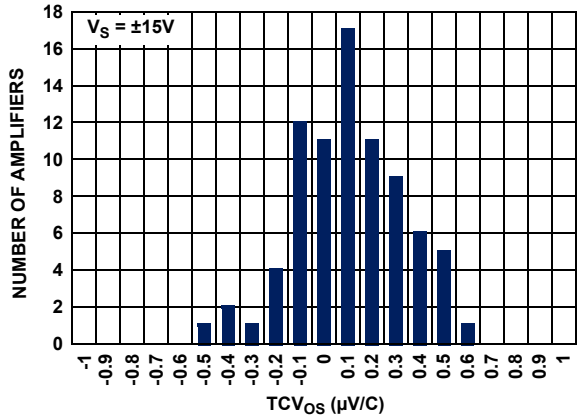


FIGURE 5. ISL28118 TCV_{OS} vs NUMBER OF AMPLIFIERS ±15V

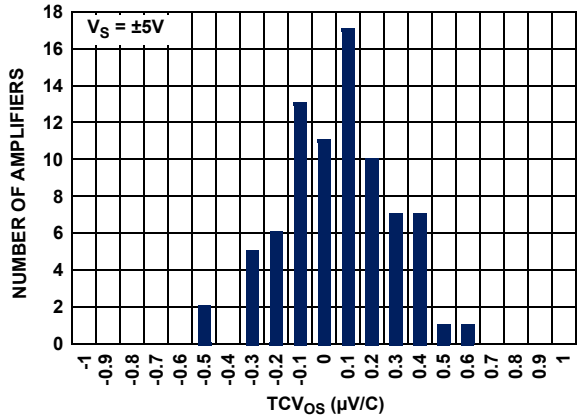


FIGURE 6. ISL28118 TCV_{OS} vs NUMBER OF AMPLIFIERS ±5V

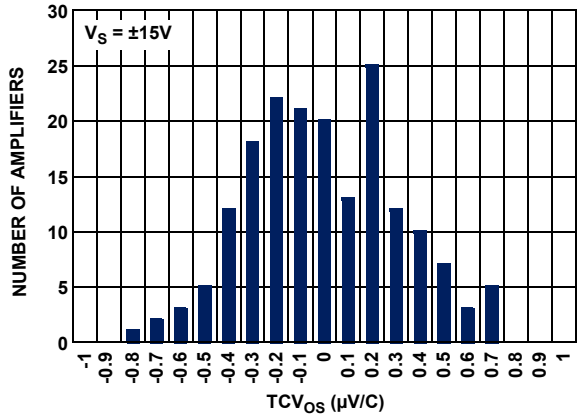


FIGURE 7. ISL28218 TCV_{OS} vs NUMBER OF AMPLIFIERS ±15V

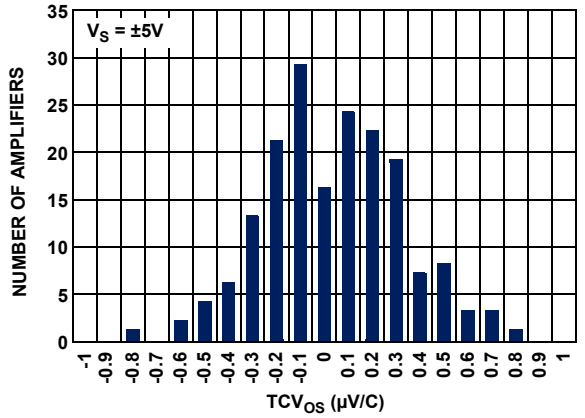


FIGURE 8. ISL28218 TCV_{OS} vs NUMBER OF AMPLIFIERS ±5V

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. **(Continued)**

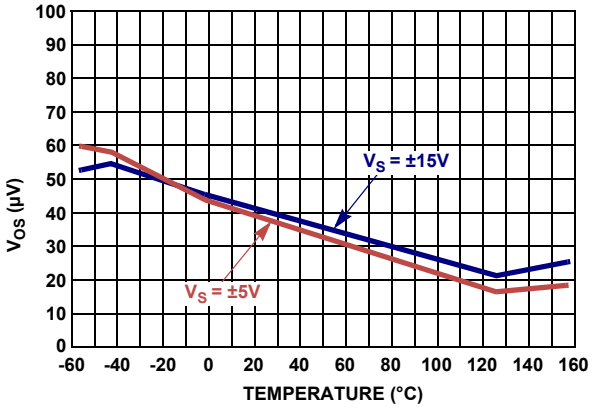


FIGURE 9. V_{OS} vs TEMPERATURE

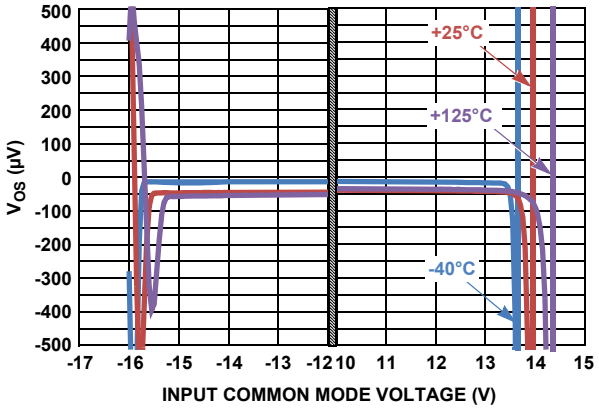


FIGURE 10. INPUT OFFSET VOLTAGE vs INPUT COMMON MODE VOLTAGE, V_S = ±15V

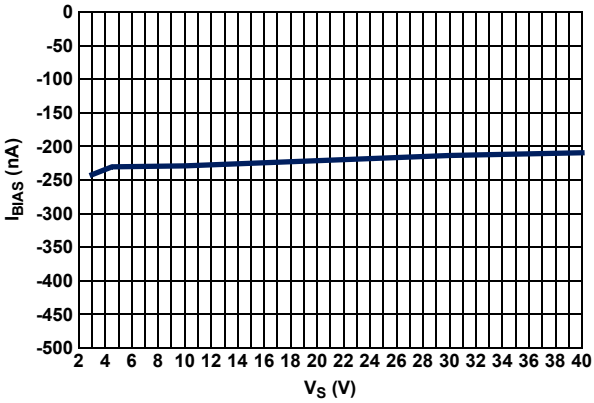


FIGURE 11. I_{BIAS} vs V_S

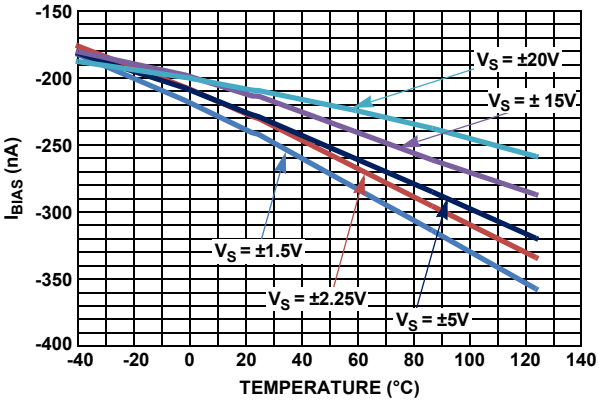


FIGURE 12. I_{BIAS} vs TEMPERATURE vs SUPPLY

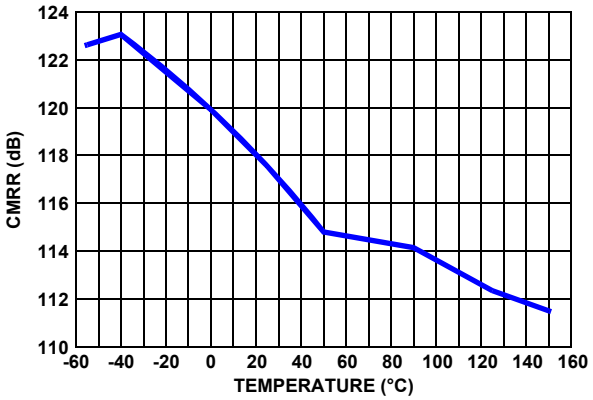


FIGURE 13. ISL28118 CMRR vs TEMPERATURE, V_S = ±15V

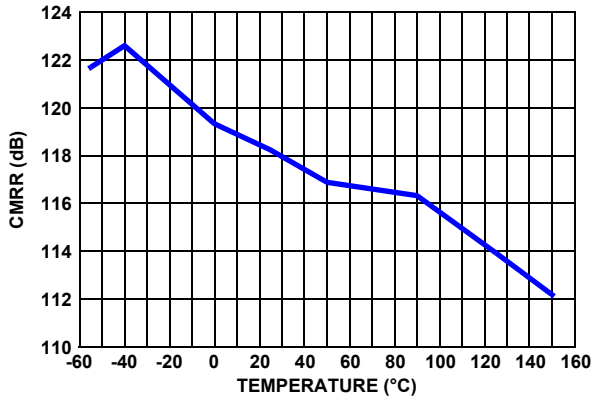


FIGURE 14. ISL28118 CMRR vs TEMPERATURE, V_S = ±5V

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. **(Continued)**

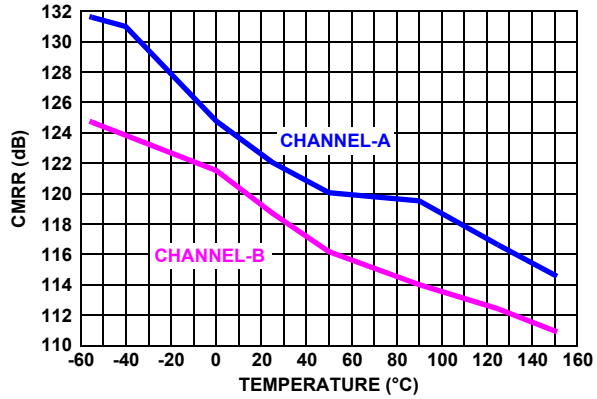


FIGURE 15. ISL28218 CMRR vs TEMPERATURE, V_S = ±15V

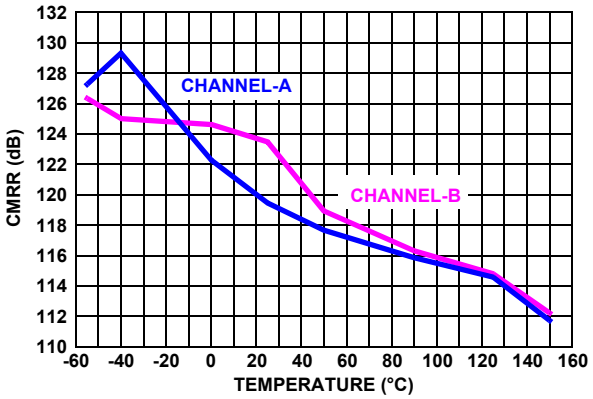


FIGURE 16. ISL28218 CMRR vs TEMPERATURE, V_S = ±5V

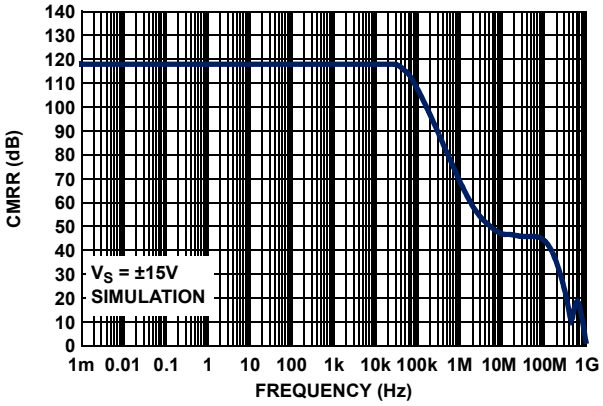


FIGURE 17. CMRR vs FREQUENCY, V_S = ±15V

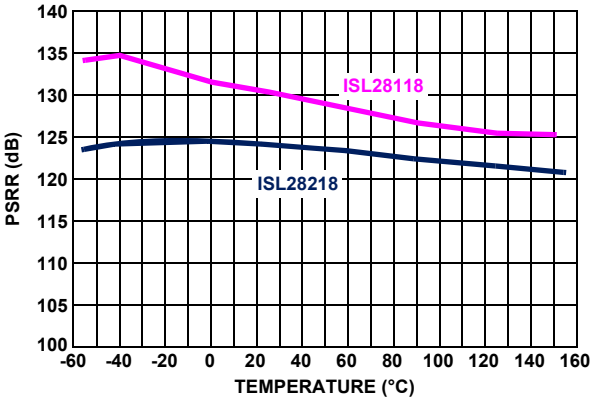


FIGURE 18. PSRR vs TEMPERATURE, V_S = ±15V

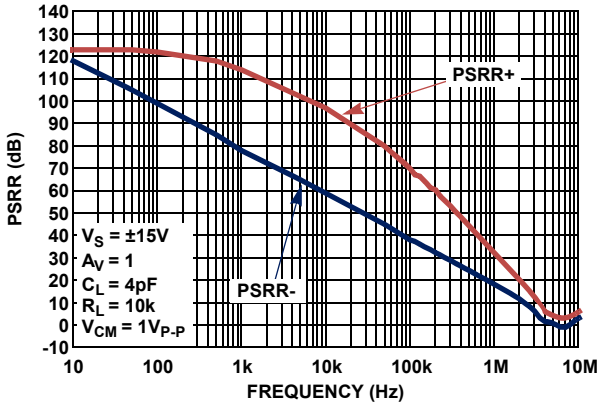


FIGURE 19. PSRR vs FREQUENCY, V_S = ±15V

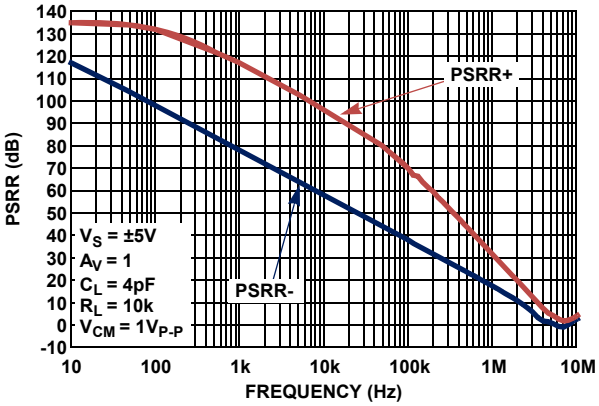


FIGURE 20. PSRR vs FREQUENCY, V_S = ±5V

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. **(Continued)**

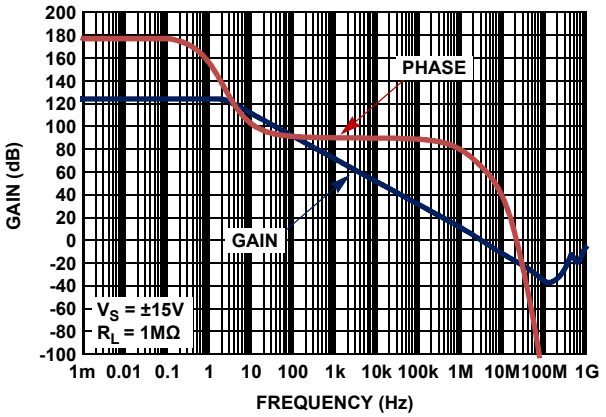


FIGURE 21. OPEN-LOOP GAIN, PHASE vs FREQUENCY, V_S = ±15V

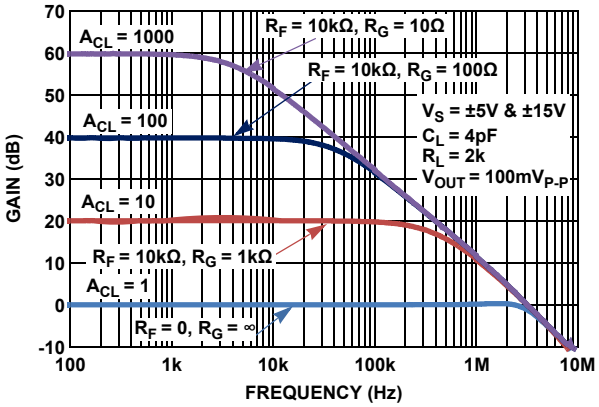


FIGURE 22. FREQUENCY RESPONSE vs CLOSED LOOP GAIN

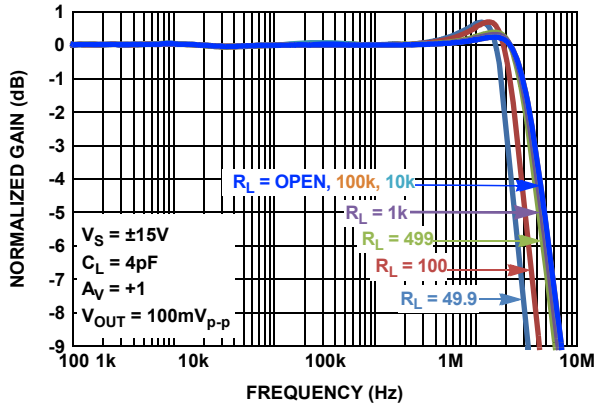


FIGURE 23. GAIN vs FREQUENCY vs R_L, V_S = ±15V

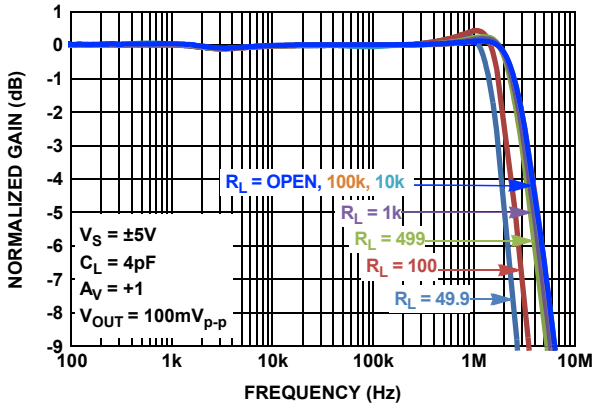


FIGURE 24. GAIN vs FREQUENCY vs R_L, V_S = ±5V

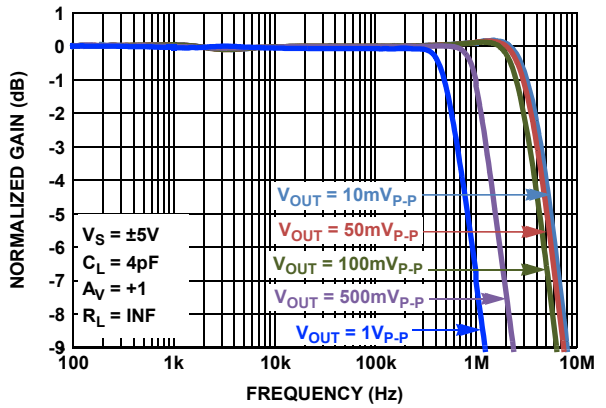


FIGURE 25. GAIN vs FREQUENCY vs OUTPUT VOLTAGE

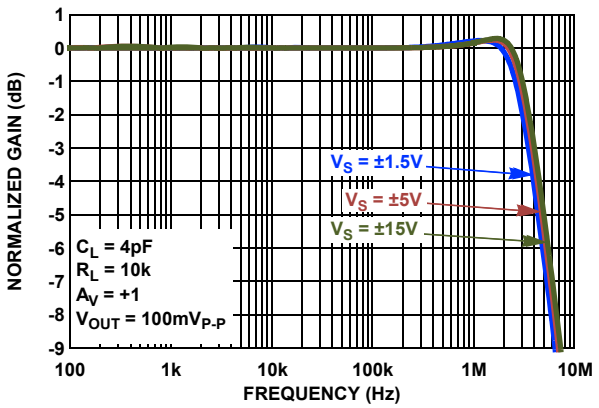


FIGURE 26. GAIN vs FREQUENCY vs SUPPLY VOLTAGE

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. **(Continued)**

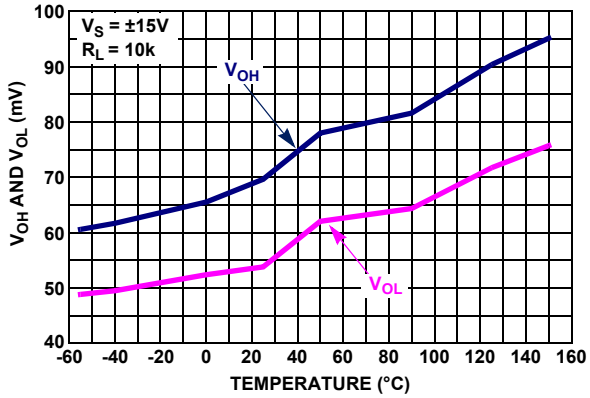


FIGURE 27. ISL28118 V_{OUT} HIGH & LOW vs TEMPERATURE, V_S = ±15V, R_L = 10k

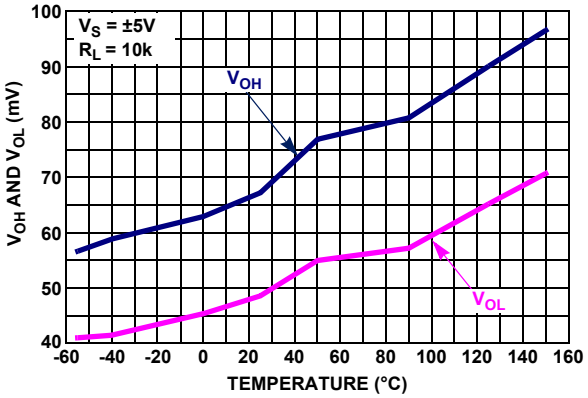


FIGURE 28. ISL28118 V_{OUT} HIGH AND LOW vs TEMPERATURE, V_S = ±5V, R_L = 10k

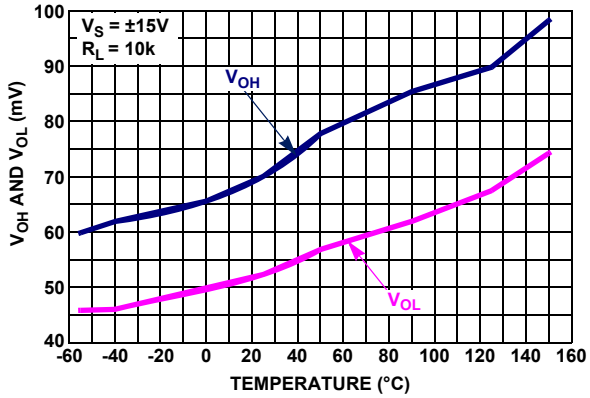


FIGURE 29. ISL28218 V_{OUT} HIGH & LOW vs TEMPERATURE, V_S = ±15V, R_L = 10k

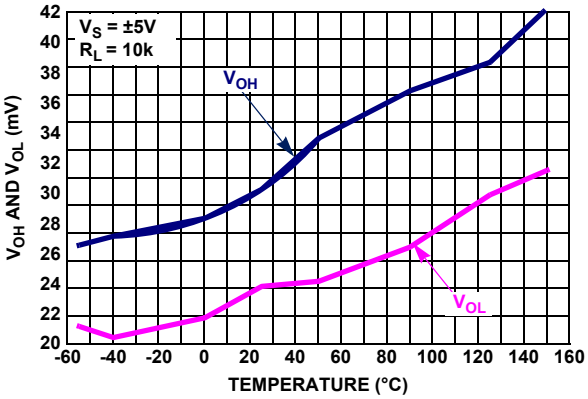


FIGURE 30. ISL28218 V_{OUT} HIGH AND LOW vs TEMPERATURE, V_S = ±5V, R_L = 10k

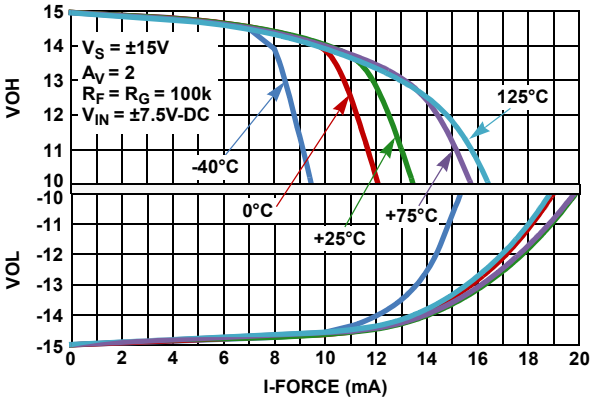


FIGURE 31. ISL28118 OUTPUT VOLTAGE SWING vs LOAD CURRENT V_S = ±15V

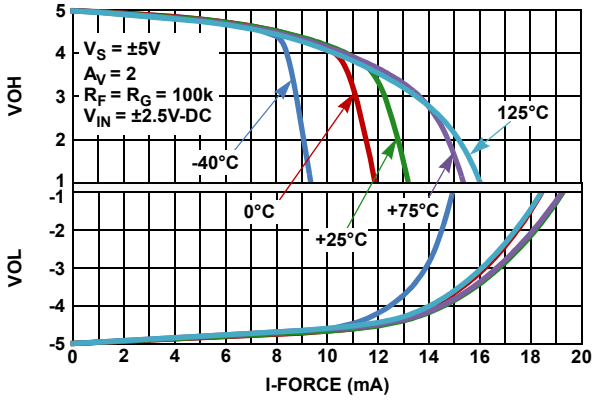


FIGURE 32. ISL28118 OUTPUT VOLTAGE SWING vs LOAD CURRENT V_S = ±5V

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. **(Continued)**

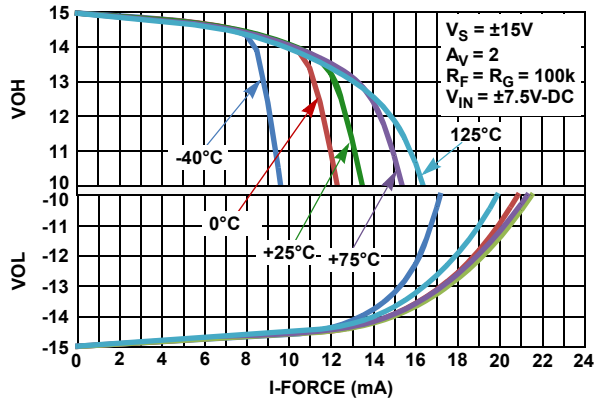


FIGURE 33. ISL28218 OUTPUT VOLTAGE SWING vs LOAD CURRENT V_S = ±15V

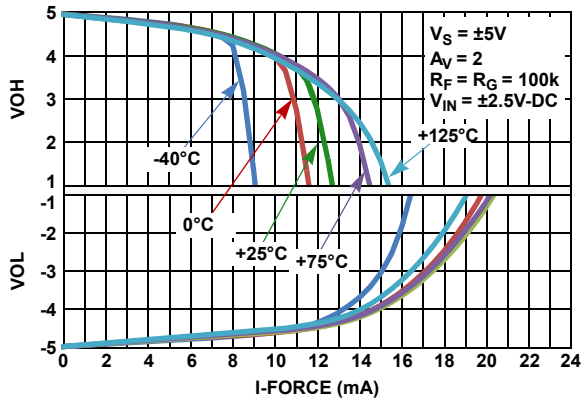


FIGURE 34. ISL28218 OUTPUT VOLTAGE SWING vs LOAD CURRENT V_S = ±5V

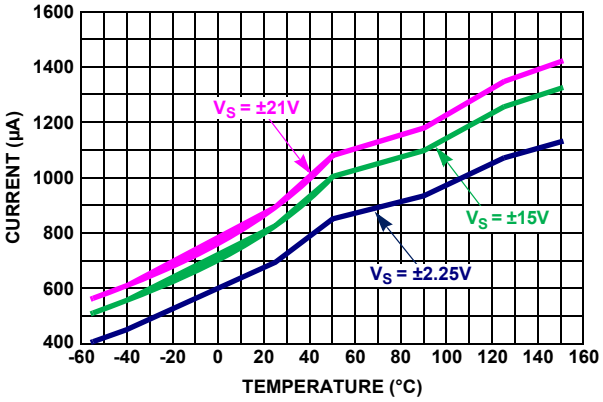


FIGURE 35. ISL28118 SUPPLY CURRENT vs TEMPERATURE vs SUPPLY VOLTAGE

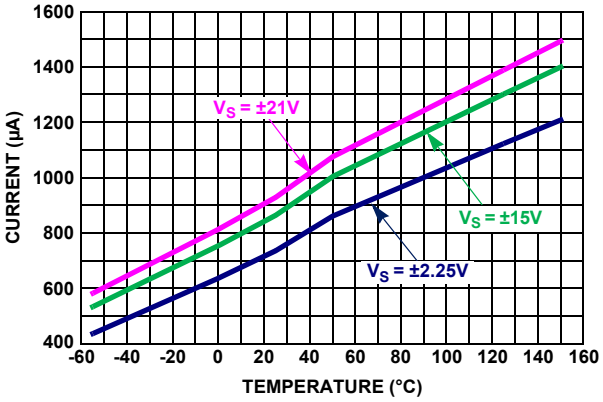


FIGURE 36. ISL28218 SUPPLY CURRENT vs TEMPERATURE vs SUPPLY VOLTAGE

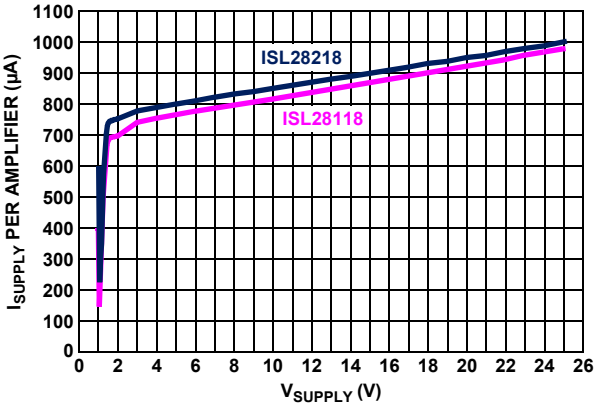


FIGURE 37. SUPPLY CURRENT vs SUPPLY VOLTAGE

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. **(Continued)**

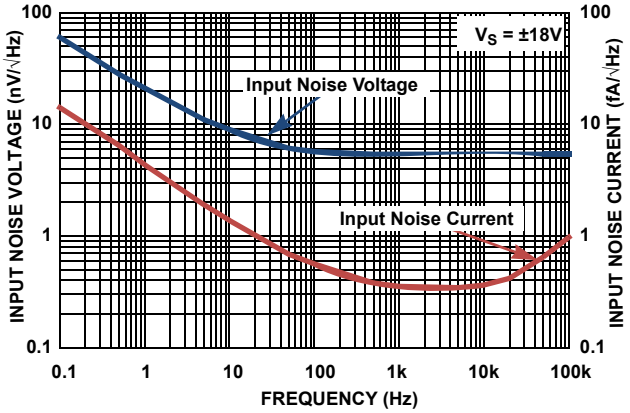


FIGURE 38. INPUT NOISE VOLTAGE (en) AND CURRENT (in) vs FREQUENCY, V_S = ±18V

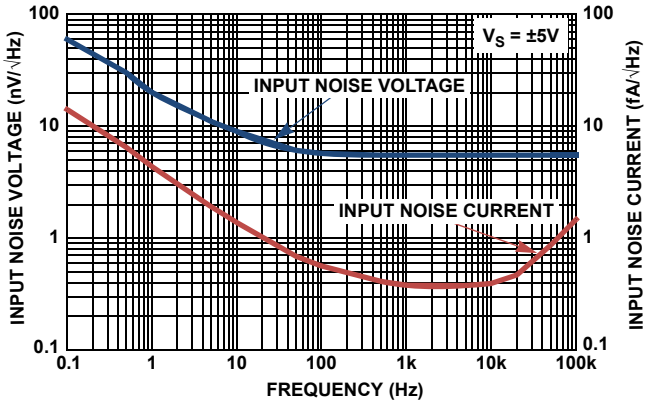


FIGURE 39. INPUT NOISE VOLTAGE (en) AND CURRENT (in) vs FREQUENCY, V_S = ±5V

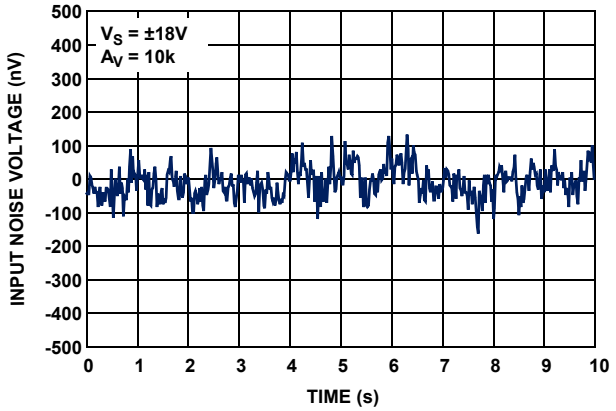


FIGURE 40. INPUT NOISE VOLTAGE 0.1Hz TO 10Hz, V_S = ±18V

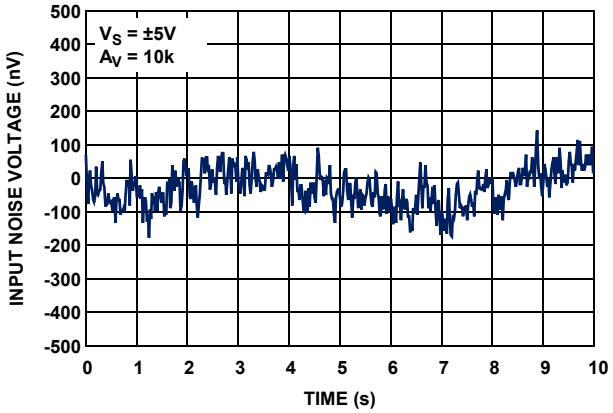


FIGURE 41. INPUT NOISE VOLTAGE 0.1Hz TO 10Hz, V_S = ±5V

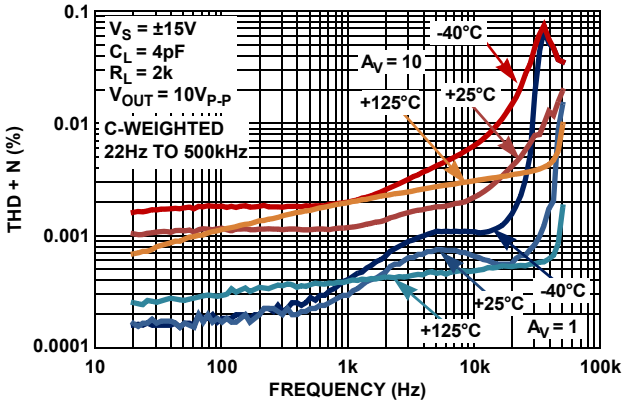


FIGURE 42. THD+N vs FREQUENCY vs TEMPERATURE, A_V = 1, 10, R_L = 2k

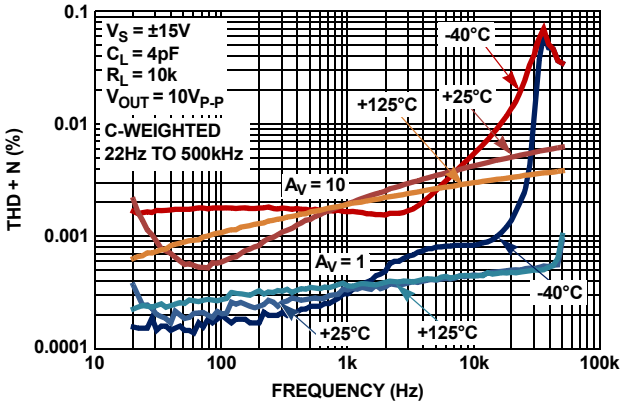


FIGURE 43. THD+N vs FREQUENCY vs TEMPERATURE, A_V = 1, 10, R_L = 10k

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. **(Continued)**

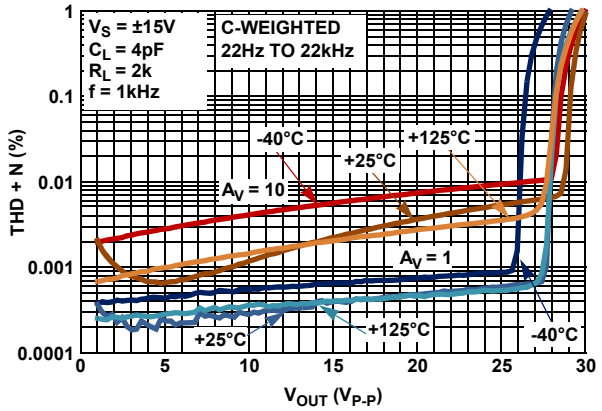


FIGURE 44. THD+N vs OUTPUT VOLTAGE (V_{OUT}) vs TEMPERATURE, A_V = 1, 10, R_L = 2k

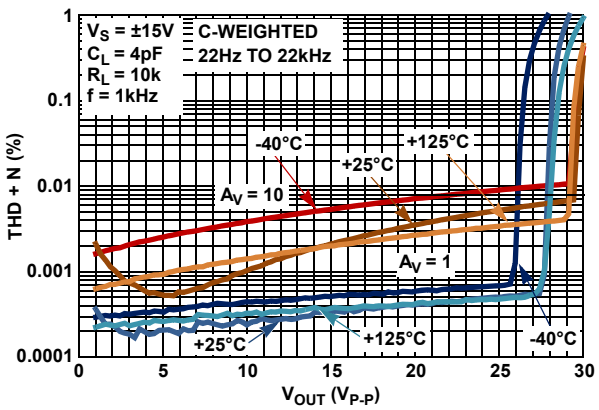


FIGURE 45. THD+N vs OUTPUT VOLTAGE (V_{OUT}) vs TEMPERATURE, A_V = 1, 10, R_L = 10k

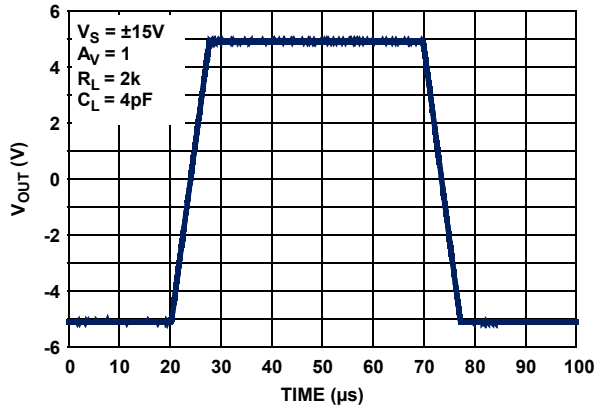


FIGURE 46. LARGE SIGNAL 10V STEP RESPONSE, V_S = ±15V

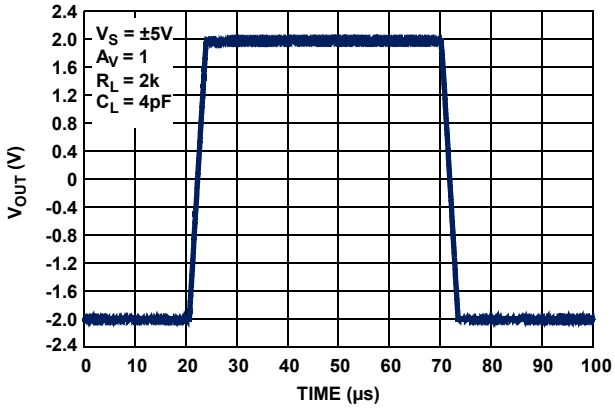


FIGURE 47. LARGE SIGNAL 4V STEP RESPONSE, V_S = ±5V

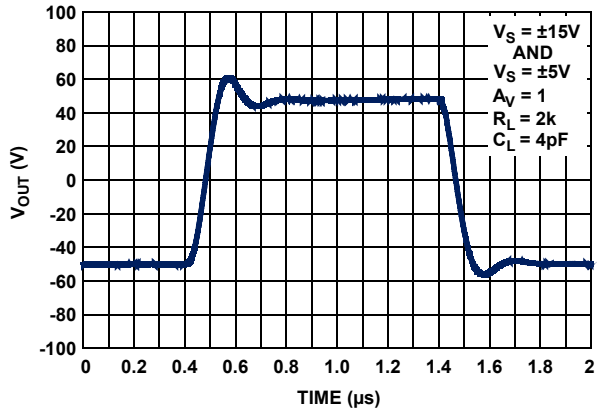


FIGURE 48. SMALL SIGNAL TRANSIENT RESPONSE V_S = ±5V, ±15V

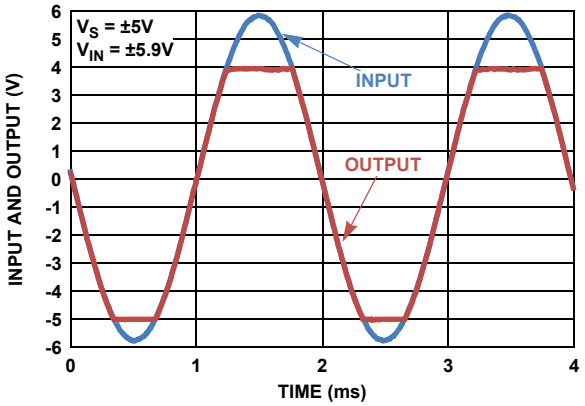


FIGURE 49. NO PHASE REVERSAL

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. **(Continued)**

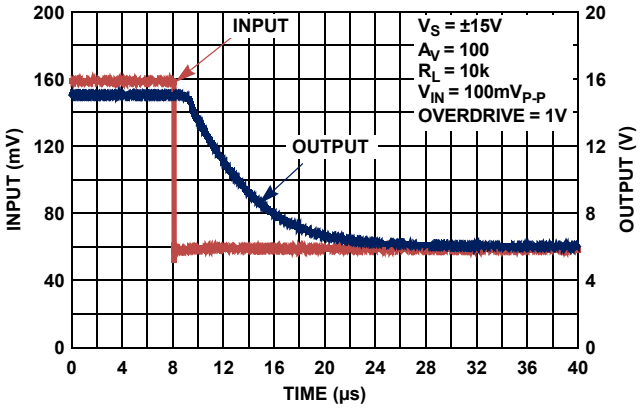


FIGURE 50. POSITIVE OUTPUT OVERLOAD RESPONSE TIME, V_S = ±15V

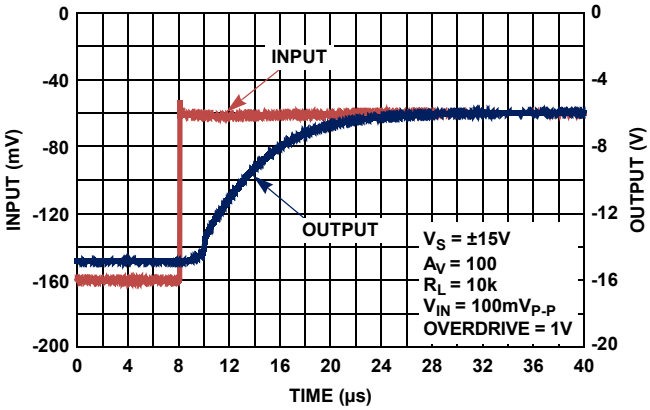


FIGURE 51. NEGATIVE OUTPUT OVERLOAD RESPONSE TIME, V_S = ±15V

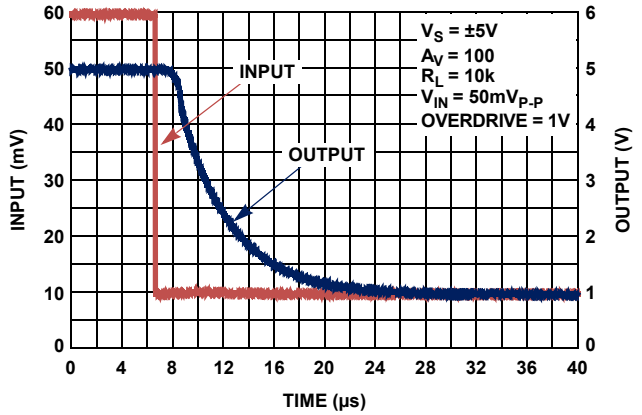


FIGURE 52. POSITIVE OUTPUT OVERLOAD RESPONSE TIME, V_S = ±5V

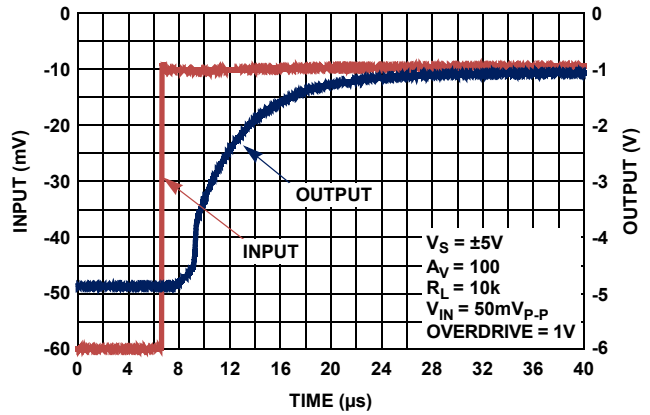


FIGURE 53. NEGATIVE OUTPUT OVERLOAD RESPONSE TIME, V_S = ±5V

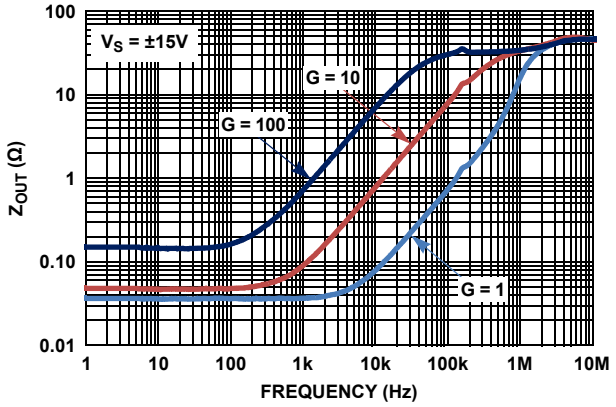


FIGURE 54. OUTPUT IMPEDANCE vs FREQUENCY, V_S = ±15V

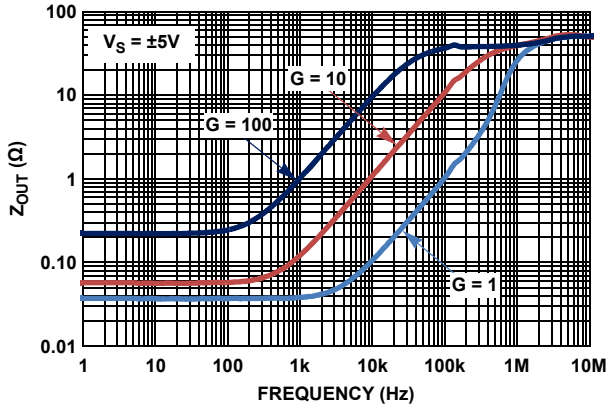


FIGURE 55. OUTPUT IMPEDANCE vs FREQUENCY, V_S = ±5V

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. **(Continued)**

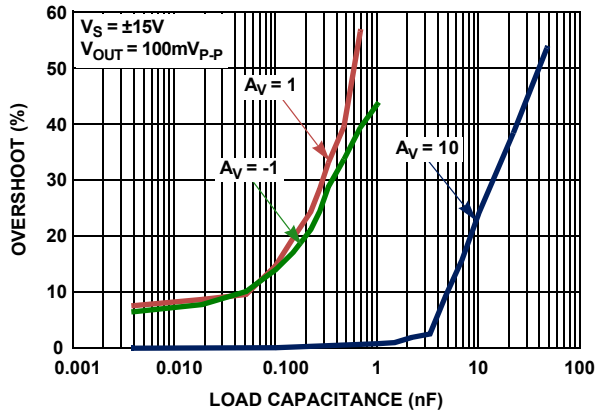


FIGURE 56. OVERSHOOT vs CAPACITIVE LOAD, V_S = ±15V

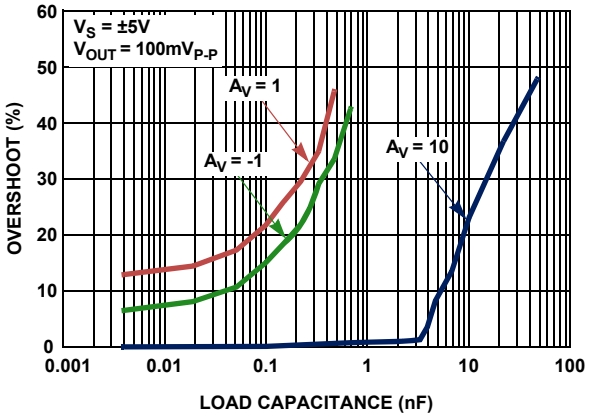


FIGURE 57. OVERSHOOT vs CAPACITIVE LOAD, V_S = ±5V

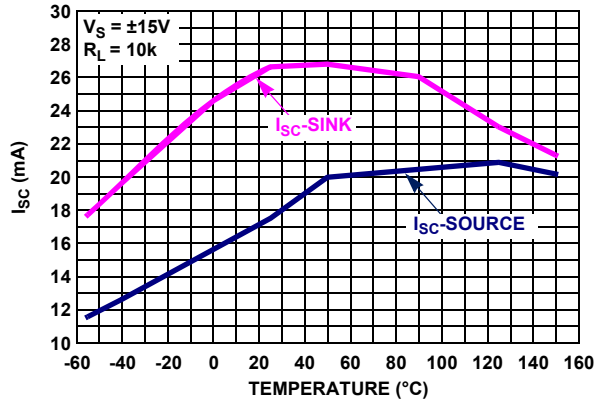


FIGURE 58. ISL28118 SHORT CIRCUIT CURRENT vs TEMPERATURE, V_S = ±15V

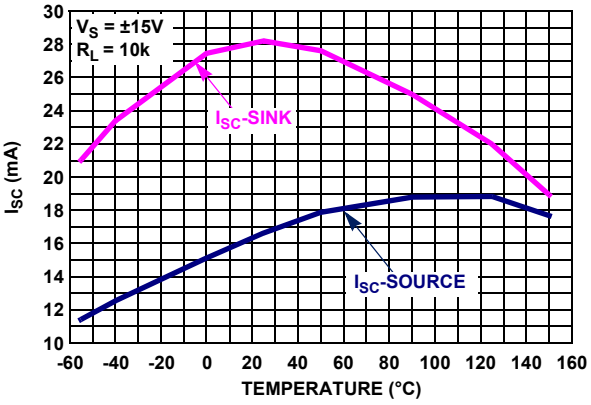


FIGURE 59. ISL28218 SHORT CIRCUIT CURRENT vs TEMPERATURE, V_S = ±15V

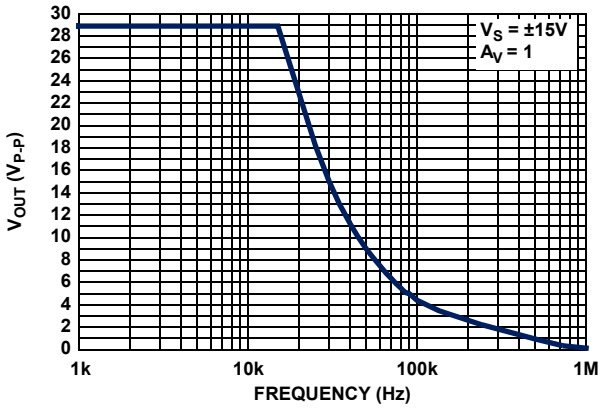


FIGURE 60. MAX OUTPUT VOLTAGE vs FREQUENCY

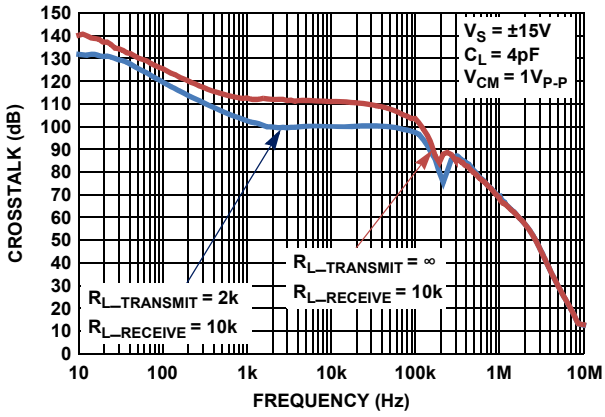


FIGURE 61. CHANNEL SEPARATION vs FREQUENCY, R_L = inf , V_S = ±15V

Applications Information

Functional Description

The ISL28118 and ISL28218 are single and dual, single supply rail-to-rail output amplifiers with a common mode input voltage range extending to 0.5V below the V- rail. These op amps feature very low quiescent current of 850µV, and low temperature drift. Both devices are fabricated in a new precision 40V complementary bipolar DI process and immune from latch-up.

Operating Voltage Range

The devices are designed to operate over the 3V (±1.5V) to 40V (±20V) range and are characterized at 10V (±5V) and 30V (±15V). Both DC and AC performance remain virtually unchanged over the complete operating voltage range. Parameter variation with operating voltage is shown in the "Typical Performance Curves" beginning on page 7.

Input Stage Performance

The ISL28118 and ISL28218 PNP input stage provides a maximum input differential voltage of 42V. The input stage is capable of below ground sensing. The device is fully characterized down to half a volt below the V- rail at +25°C. The input common mode voltage range sensitivity to temperature is shown in Figure 10 (±15V). These features provide excellent CMRR, AC performance and extremely low input distortion over a wide temperature range.

Input ESD Diode Protection

The PNP input stage has a max input differential voltage equal to a diode drop greater than the supply voltage (max 42V). This feature enables the device to function reliably in large signal pulse applications without the need for anti-parallel clamp diodes required on MOSFET and most bipolar input stage op amps. Thus, input signal distortion caused by nonlinear clamps under high slew rate conditions are avoided.

In applications where one or both amplifier input terminals are at risk of exposure to voltages beyond the supply rails, current limiting resistors may be needed at each input terminal (see Figure 62 $R_{IN}+$, $R_{IN}-$) to limit current through the power supply ESD diodes to 20mA.

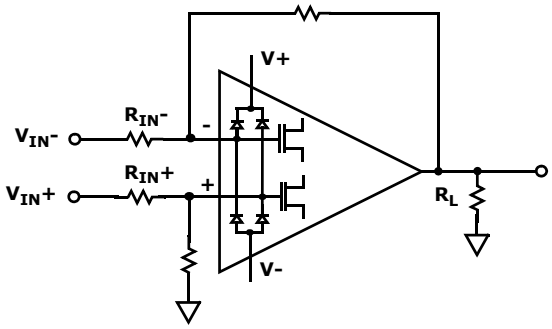


FIGURE 62. INPUT ESD DIODE CURRENT LIMITING

Output Drive Capability

The bipolar rail-to-rail output stage features rail-to-rail output swing at moderate levels of output current (Figures 31 through 34).

The output current is internally limited. Output current limit over-temperature is shown in Figures 31 through 34. The amplifiers can withstand a short circuit to either rail as long as the power dissipation limits are not exceeded. This applies to only 1 amplifier at a time for the dual op amp. Continuous operation under these conditions may degrade long term reliability.

Output Phase Reversal

Output phase reversal is a change of polarity in the amplifier transfer function when the input voltage exceeds the supply voltage. The ISL28118 and ISL28218 are immune to output phase reversal, out to 0.5V beyond the rail ($V_{ABS\ MAX}$) limit (Figure 49).

Using Only One Channel

The ISL28218 is a dual op-amp. If the application only requires one channel, the user must configure the unused channel to prevent it from oscillating. The unused channel will oscillate if the input and output pins are floating. This will result in higher than expected supply currents and possible noise injection into the channel being used. The proper way to prevent this oscillation is to short the output to the inverting input and ground the positive input (as shown in Figure 63).

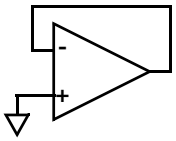


FIGURE 63. PREVENTING OSCILLATIONS IN UNUSED CHANNELS

Power Dissipation

It is possible to exceed the +150°C maximum junction temperatures under certain load and power supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related using Equation 1:

$$T_{JMAX} = T_{MAX} + \theta_{JA} x PD_{MAXTOTAL} \quad \text{(EQ. 1)}$$

where:

- $P_{DMAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PD_{MAX})
- PD_{MAX} for each amplifier can be calculated using Equation 2:

$$PD_{MAX} = V_S \times I_{qMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad \text{(EQ.2)}$$

where:

- T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- PD_{MAX} = Maximum power dissipation of 1 amplifier
- V_S = Total supply voltage
- I_{qMAX} = Maximum quiescent supply current of 1 amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application
- R_L = Load resistance

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
11/12/10	FN7532.1	On page 1: Features Section, added Low input offset voltage and superb offset voltage temperature drift for ISL28118. Updated Intersil trademark statement (bottom of page) On page 3: Removed "coming soon" from ISL28118FBZ. Updated tape & reel note. On page 4: Change ISL28118 Theta JA value from 158 to 165. Added ISL28118 min/max specs to VOS (input offset voltage), TCVOS and min specs to CMRR. On page 5: Added AVOL MIN spec for ISL28118 in dB. Changed existing AVOL spec from V/mV to dB. Added VOL max spec for ISL28118, IS Typ and Max spec for ISL28118. Changed TS from 18µs to 8.5µs. On page 6: Added Min Max VOS spec, TCVOS spec for ISL28118. Changed AVOL specs from V/mV to dB. On page 7: Changed Slew Rate TYP from ±1.2V/µs to ±1V/µs. Added for TS TYP spec = 4µs. Changed min/max note 8 to “Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.” Added Figs 1 & 2 for ISL28118. Figures 3 & 4 moved to page 8. On page 8: Added Figures 5 & 6 On page 9: Added Figures 13 & 14 for ISL28118 On page 10, in Figure 17, changed VS from ±5V to ±15V On page 12: Added Figures 27, 28, 31 & 32 for ISL28118 On page 13: Added Figure 35 for ISL28118 On page 14: Figure 41 changed VS from ±18V to ±5V, Figure 42 added RL = 2k, Figure 43 added RL = 10k and corrected "HD+N" to "THD+N" On page 15, Figure 44 added RL = 2k, Figure 45 RL = 10k. On page 17: Added Figure 58 for ISL28118 On page 17, Figure 58 and 59, graph upper left corner changed VS = ±5V to VS = ±15V On page 17, Figure 61, deleted VS = ±5V
9/16/10	FN7532.0	Initial Release

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL28118, ISL28218.

To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

FITs are available from our website at: http://rel.intersil.com/reports/sear

For additional products, see www.intersil.com/product_tree

Intersil products are manufactured, assembled and tested utilizing ISO9000 quality systems as noted in the quality certifications found at www.intersil.com/design/quality

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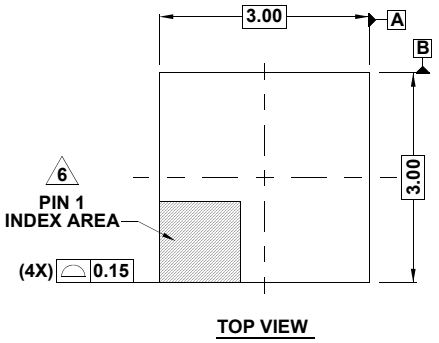
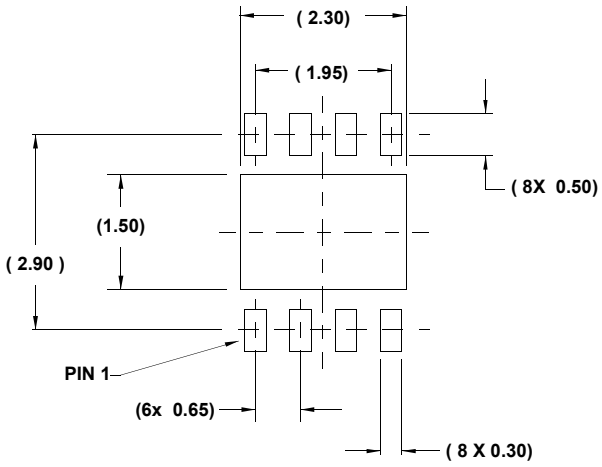
Package Outline Drawing

L8.3x3A

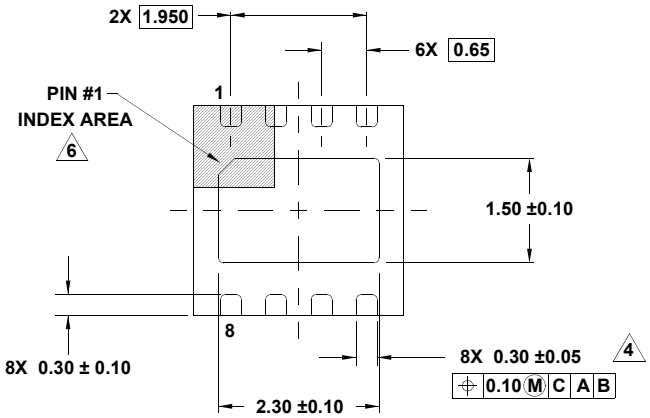
8 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE
Rev 4, 2/10



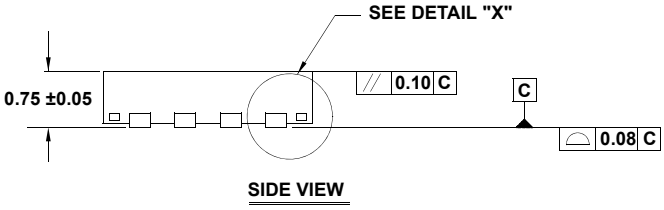
TOP VIEW



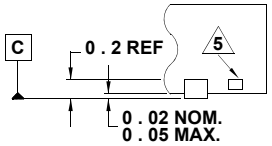
TYPICAL RECOMMENDED LAND PATTERN



BOTTOM VIEW



SIDE VIEW



DETAIL "X"

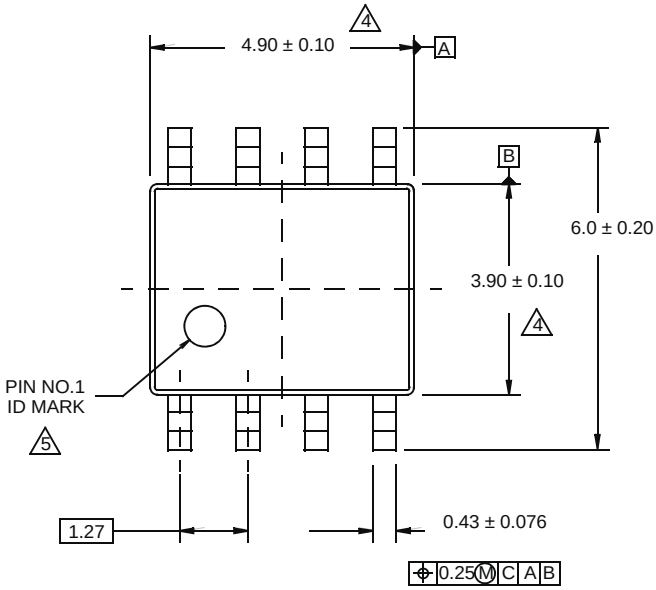
NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.20mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Compliant to JEDEC MO-229 WEEC-2 except for the foot length.

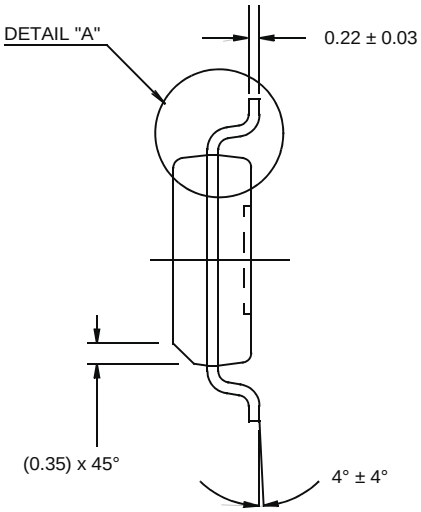
Package Outline Drawing

M8.15E

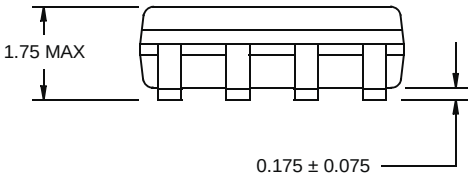
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE
Rev 0, 08/09



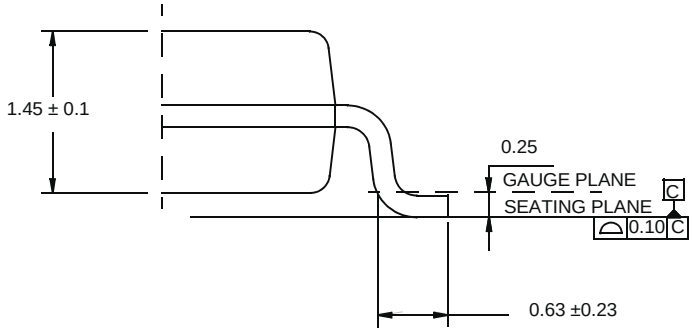
TOP VIEW



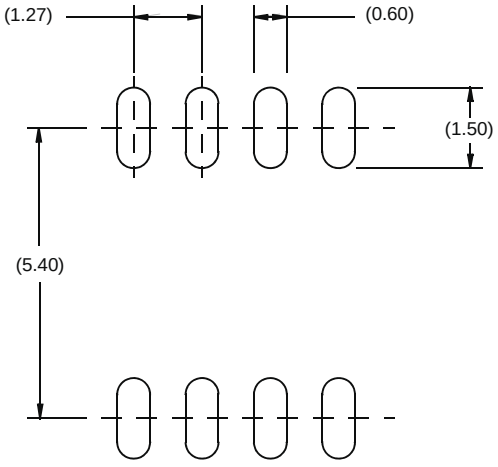
SIDE VIEW "B"



SIDE VIEW "A"



DETAIL "A"



TYPICAL RECOMMENDED LAND PATTERN

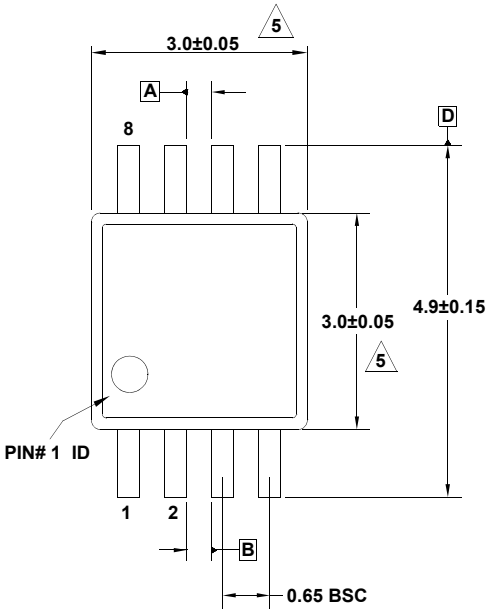
NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Reference to JEDEC MS-012.

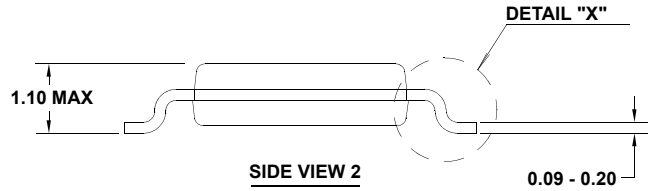
Package Outline Drawing

M8.118

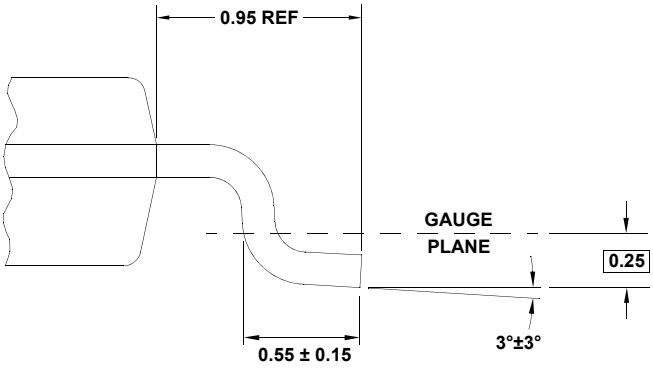
8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE
Rev 3, 3/10



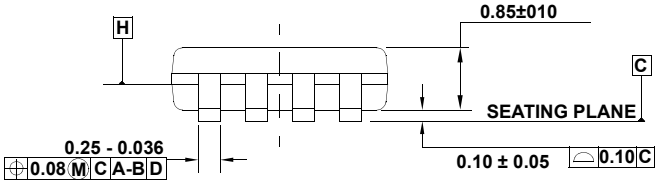
TOP VIEW



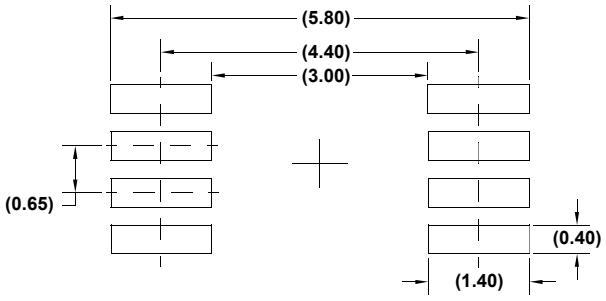
SIDE VIEW 2



DETAIL "X"



SIDE VIEW 1



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.