October 1989
Edition 1.0

FUJITSU

DATA SHEET

MB8431/32-90/-90L/-90LL/-12/-12L/-12LL
CMOS 16K-BIT DUAL-PORT SRAM

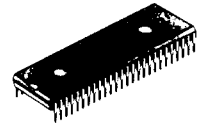
2K x 8 Bits CMOS Dual-Port Static Random Access Memory

The Fujitsu MB8431 and MB8432 are 2,048 words x 8 bits dual-port static high performance, random access memories fabricated with CMOS technology. MB8431 and MB8432 provide the user with two separately controlled I/O ports with independent addresses, Chip Select ($\overline{CS}$), Write Enable ($\overline{WE}$), Output Enable ($\overline{OE}$), and I/O functions. This arrangement permits independent access to any memory location for either a Read or Write operation – a useful feature for shared data processing applications. These devices have an automatic power-down feature controlled by $\overline{CS}$.

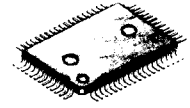
To avoid data contention on the same address, a $\overline{BUSY}$ input is provided for address arbitration; in addition, MB8431 utilizes an interrupt ($\overline{INT}$) flag which allows communication between systems on either side of the RAM. Both devices use a single +5 V power supply and all pins are TTL-compatible. A simplified block diagram of the SRAM is shown in Figure 1.

Some typical applications for these memory devices are multiprocessing systems, distributed networks, external register files, and peripheral controllers.

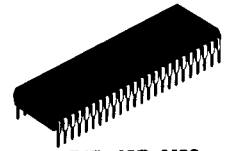
- Organization: 2,048 words x 8 bits
- Static operation: no clocks or timing strobe required
- Access time: $t_{AA} = t_{ACS} = 90$ ns max. (MB8431/32-90)
  (MB8431/32-90L/-90LL)
  $t_{AA} = t_{ACS} = 120$ ns max. (MB8431/32-12)
  (MB8431/32-12L/-12LL)
- Power consumption for the standard version:
  660 mW max. (Both ports active)
  385 mW max. (One port active)
  38.5 mW max. (Both ports standby, TTL)
  11 mW max. (Both ports standby, CMOS)
- Power consumption for the L and LL-versions:
  495 mW max. (Both ports active)
  275 mW max. (One port active)
  27.5 mW max. (Both ports standby, TTL)
  1.1 mW max. (Both ports standby, CMOS)
- Single +5 V supply ±10% tolerance
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capacity
- Electrostatic protection for all inputs and outputs
- Data retention voltage: 2 V min.
- Address arbitration function: $\overline{BUSY}$ input
- Interrupt function for communication between systems (*MB8431 only*): $\overline{INT}$ flag
- Expansion capability using MB8421/22 (Master) and MB8431/32 (Slave)
- Standard Plastic Packages:
  48-pin DIP MB8432-xx(L/LL)P
  52-pin DIP MB8431-xx(L/LL)P
  64-pin QFP MB8431-xx(L/LL)PFQ



DIP–52P–M01
(MB8431)



FPT–64P–M01
(MB8431)



DIP–48P–M02
(MB8432)

Pin Assignment

See page 4–81

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7	V
Input Voltage on any pin with respect to V_{SS}	V_{IN}	−0.5 to V_{CC} +0.5	V
Output Voltage on any I/O pin with respect to V_{SS}	V_{OUT}	−0.5 to V_{CC} +0.5	V
Output Current	I_{OUT}	±20	mA
Power dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature	T_{STG}	−40 to +125	°C

Note: Permanent device damage may occur if **ABSOLUTE MAXIMUM RATINGS** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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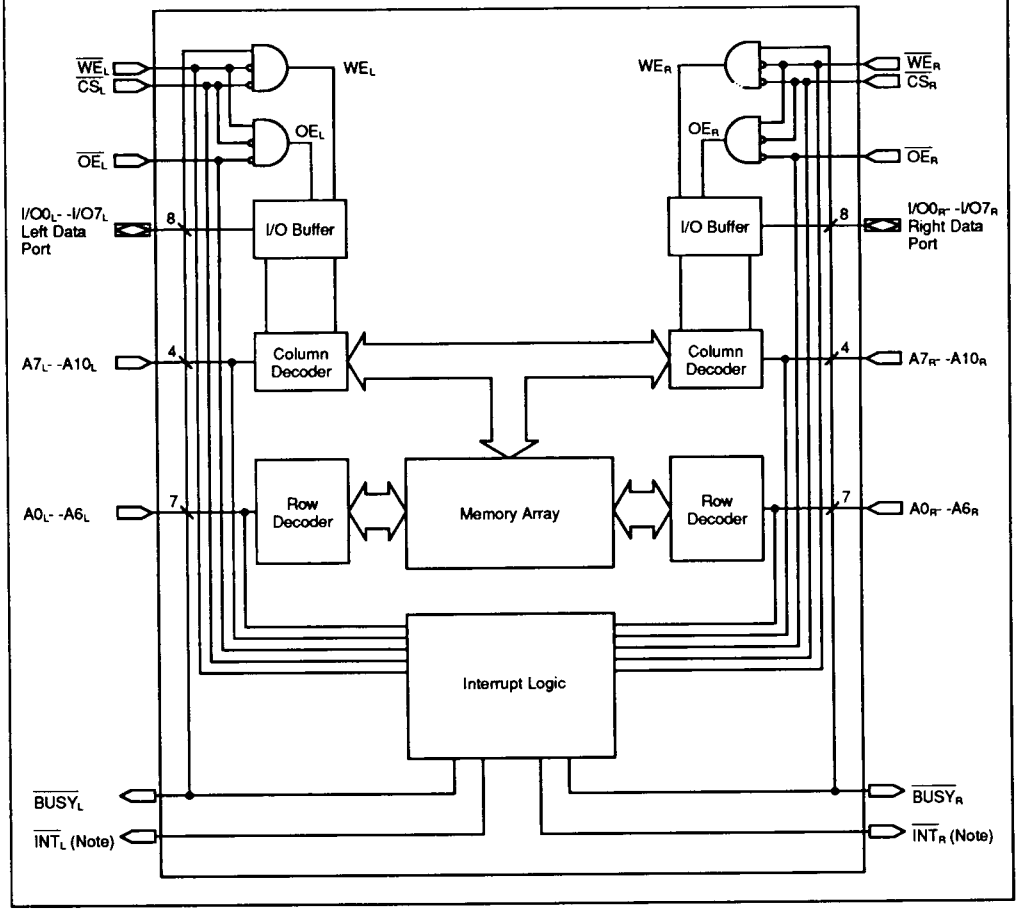
PIN NAMES

LEFT PORT	RIGHT PORT	NAMES
$\overline{CS_L}$	$\overline{CS_R}$	Chip Select Input
$\overline{WE_L}$	$\overline{WE_R}$	Write Enable Input
$\overline{OE_L}$	$\overline{OE_R}$	Output Enable Input
$\overline{INT_L}$	$\overline{INT_R}$	Interrupt * Flag Output
$\overline{BUSY_L}$	$\overline{BUSY_R}$	Busy Flag Input
$A0_L$ to $A10_L$	$A0_R$ to $A10_R$	Address Input
$I/O0_L$ to $I/O7_L$	$I/O0_R$ to $I/O7_R$	Data Input/Output
V_{CC}		Power
GND		Ground

*: Applies to MB8431 only.

Fig. 1 — MB8431/32/31L/32L BLOCK DIAGRAM



Note: MB8431 only.

CAPACITANCE (T_A = 25° C, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (VIN=0V)	C_{IN}		10	pF
I/O Capacitance (VI/O=0V)	$C_{I/O}$		10	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to VSS)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Operating Temperature	T_A	0		70	°C

DC CHARACTERISTICS

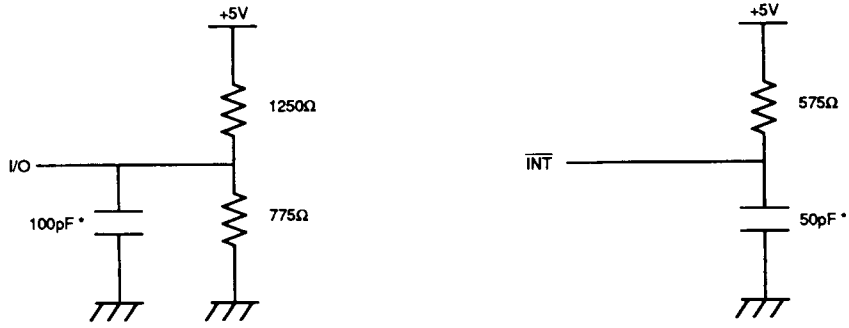
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Condition	MB8431/ MB8432-90/12		MB8431/ MB8432-90L/90LL/12L/12LL		Unit
			Min	Max	Min	Max	
Operating Supply Current (Both ports Active)	I_{CC}	Cycle=Min. Duty=100% I_{OUT}=0mA		120		90	mA
Standby Supply Current	I_{SB1}	Both ports=Standby $\overline{CS_L}$ & $\overline{CS_R}$=V_{IH}		7		5	mA
	I_{SB2}	One port=Standby $\overline{CS_L}$ or $\overline{CS_R}$=V_{IH}, I_{OUT}=0mA		70		50	mA
	I_{SB3}	Both ports=Full standby $\overline{CS_L}$ & $\overline{CS_R}$≥V_{CC}–0.2V		2		0.2	mA
	I_{SB4}	One port=Full standby $\overline{CS_L}$ or $\overline{CS_R}$≥V_{CC}–0.2V, I_{OUT}=0mA		70		50	mA
Input Leakage Current	I_{LI}	V_{IN}=0V to V_{CC}	–10	10	–10	10	µA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH}, I/O=0V to V_{CC}	–10	10	–10	10	µA
Input High Voltage	V_{IH}		2.2	V_{CC}+0.3	2.2	V_{CC}+0.3	V
Input Low Voltage	V_{IL}		–0.3 *1	0.8	–0.3 *1	0.8	V
Output High Voltage	V_{OH} *2	I_{OUT}=–1.0mA	2.4		2.4		V
Output Low Voltage	V_{OL}	I_{OUT}=3.2mA		0.4		0.4	V
Output Low Voltage for Open-Drain	V_{OL}	I_{OUT}=8mA		0.4		0.4	V

*1 Undershoot –3.0V min at less than 20ns pulse width.
*2 The $\overline{INT}$ pins require pull-up resistors because they are open-drain outputs.

AC TEST CONDITIONS

- Input Pulse Levels: 0V to 3.0V
- Input Pulse Rise & Fall Times: tR, tF=5ns
- Timing Reference Levels: 1.5V
- Output Load



* Including Jig and stray capacitance

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AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

READ CYCLE

Parameter	Symbol	MB8431-90/90L/90LL MB8432-90/90L/90LL		MB8431-12/12L/12LL MB8432-12/12L/12LL		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	90		120		ns
Address Access Time	t_{AA}		90		120	ns
Chip Select Access Time	t_{ACS}		90		120	ns
Output Enable Access Time	t_{AOE}		40		50	ns
Output Hold from Address Change	t_{OH}	10		10		ns
Chip Select to Output Low-Z *2	t_{CLZ}	5		5		ns
Output Enable to Output Low-Z *2	t_{OLZ}	5		5		ns
Chip Select to Output High-Z *2	t_{CHZ}		40		50	ns
Output Enable to Output High-Z *2	t_{OHZ}		40		50	ns
Power up from Chip Select	t_{PU}	0		0		ns
Power down from Chip Select	t_{PD}		50		60	ns

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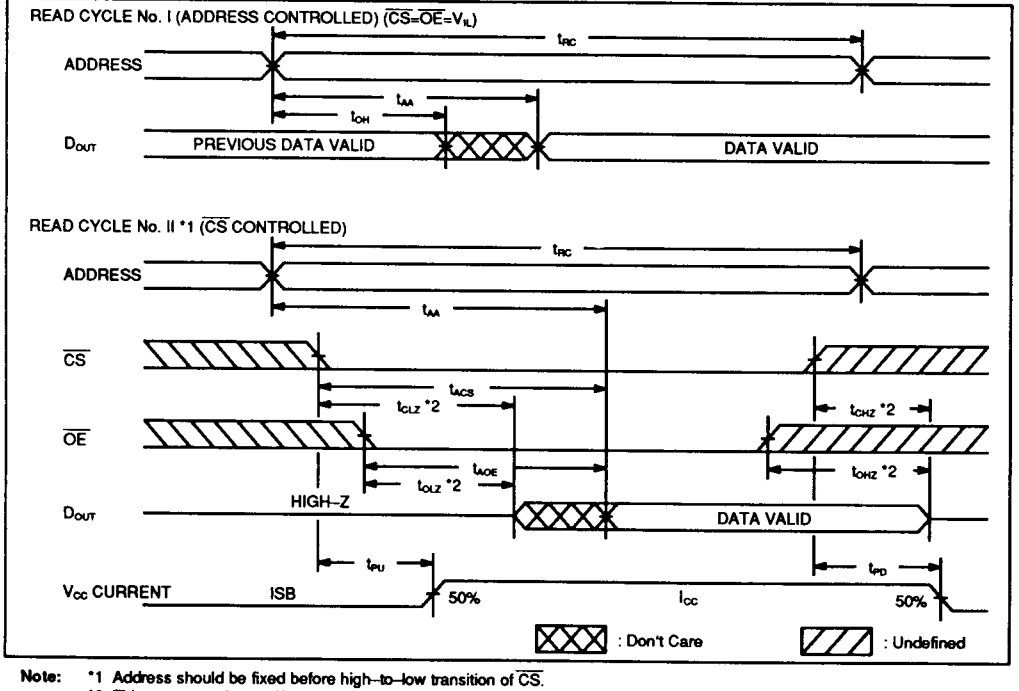
READ CYCLE TIMING DIAGRAMS ($\overline{WE}$=V_{IH})

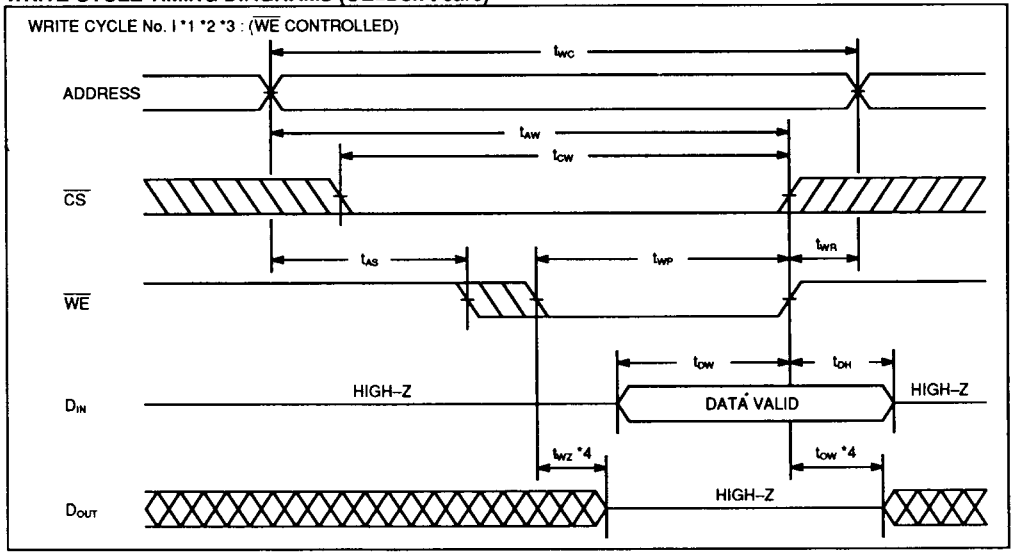


Note: *1 Address should be fixed before high-to-low transition of $\overline{CS}$.
*2 This parameter is specified at the point of ±500mV from steady state voltage with output capacitance 5pF.

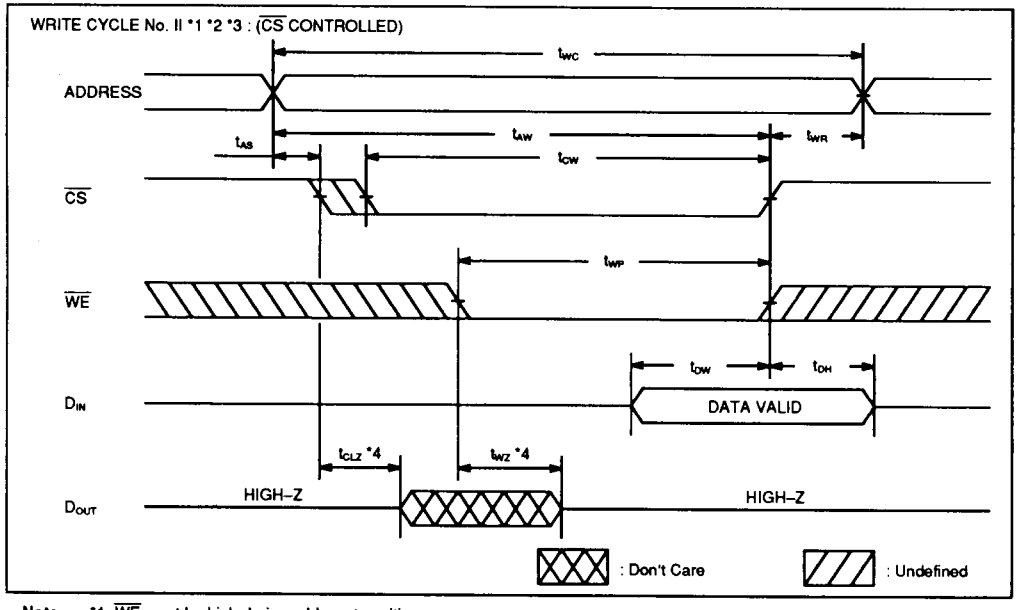
WRITE CYCLE

Parameter	Symbol	MB8431-90/90L/90LL MB8432-90/90L/90LL		MB8431-12/12L/12LL MB8432-12/12L/12LL		Unit
		Min	Max	Min	Max	
Write Cycle Time	t_{WC}	90		120		ns
Address Valid to End of Write	t_{AW}	85		100		ns
Chip Select to End of Write	t_{CW}	85		100		ns
Address Setup Time	t_{AS}	0		0		ns
Write Pulse Width	t_{WP}	60		70		ns
Write Recovery Time	t_{WR}	0		0		ns
Data Valid to End of Write	t_{DW}	40		40		ns
Data Hold Time	t_{DH}	0		0		ns
Write Enable to Output Low-Z *4	t_{OW}	0		0		ns
Write Enable to Output High-Z *4	t_{WZ}		40		50	ns

WRITE CYCLE TIMING DIAGRAMS ($\overline{OE}$=Don't care)



Note: *1 $\overline{WE}$ must be high during address transition.
*2 If $\overline{OE}$, $\overline{CS}$ are in the READ Mode, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*3 If $\overline{CS}$ goes high prior to or coincident with $\overline{WE}$ transition to high, the output remains in high impedance state.
*4 Transition is measured at the point of ±500mV from steady state voltage with C_L=5pF.



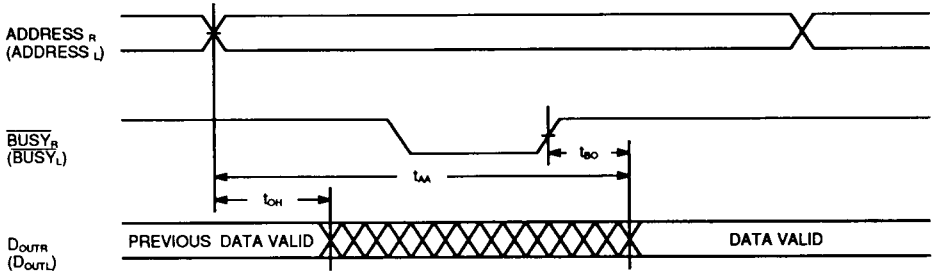
Note: *1 $\overline{WE}$ must be high during address transition.
*2 If $\overline{OE}$, $\overline{CS}$ are in the READ Mode, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*3 If $\overline{CS}$ goes high prior to or coincident with $\overline{WE}$ transition to high, the output remains in high impedance state.
*4 This parameter is specified at the point of ±500mV from steady state voltage with output capacitance 5pF.

SLAVE BUSY TIMING

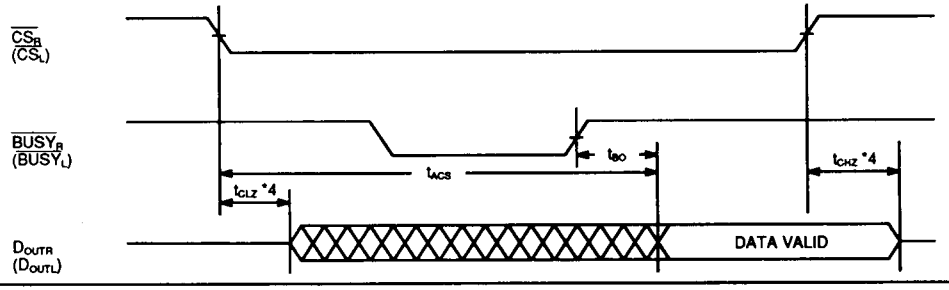
Parameter	Symbol	MB8431-90/90L/90LL MB8432-90/90L/90LL		MB8431-12/12L/12LL MB8432-12/12L/12LL		Unit
		Min	Max	Min	Max	
Busy Access Time	t_{BO}		0		0	ns
Write Set Up Time To Busy	t_{WS}	−10		−10		ns
Write Hold Time From Busy	t_{WH}	20		25		ns

CONTENTION CYCLE TIMING DIAGRAMS ($\overline{WE}$=V_{IH})

CONTENTION READ CYCLE No. I *1 *2 : (ADDRESS CONTROLLED) ($\overline{CS}$=$\overline{OE}$=V_{IL})



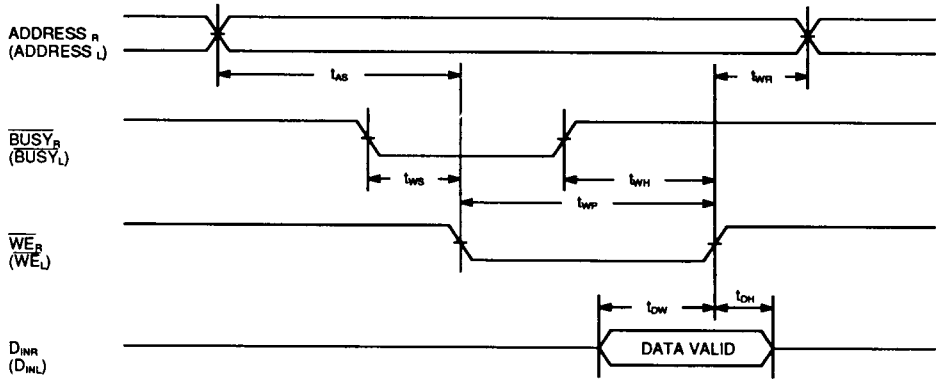
CONTENTION READ CYCLE No. II *1 *3 : ($\overline{CS}$ CONTROLLED)



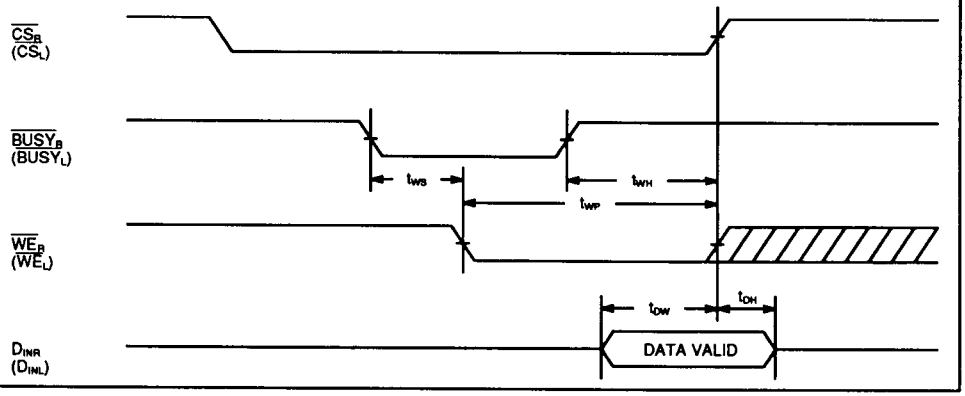
Note: *1 In case of dualaccess at the same memory location, the port that access the RAM first sets the $\overline{BUSY}$ flag high.
*2 $\overline{CS}$ must be low before or coincident with transition of address.
*3 Address is valid prior to cincident with high-to-low transition of $\overline{CS}$.
*4 This parameter is specified at the point of ±500mV from steady state voltage with output capacitance 5pF.

CONTENTION CYCLE TIMING DIAGRAMS

CONTENTION WRITE CYCLE No. I *1 *2 *3 ($\overline{WE}$ CONTROLLED)



CONTENTION WRITE CYCLE No. II *3 : *1 *2 *3 ($\overline{CS}$ CONTROLLED)

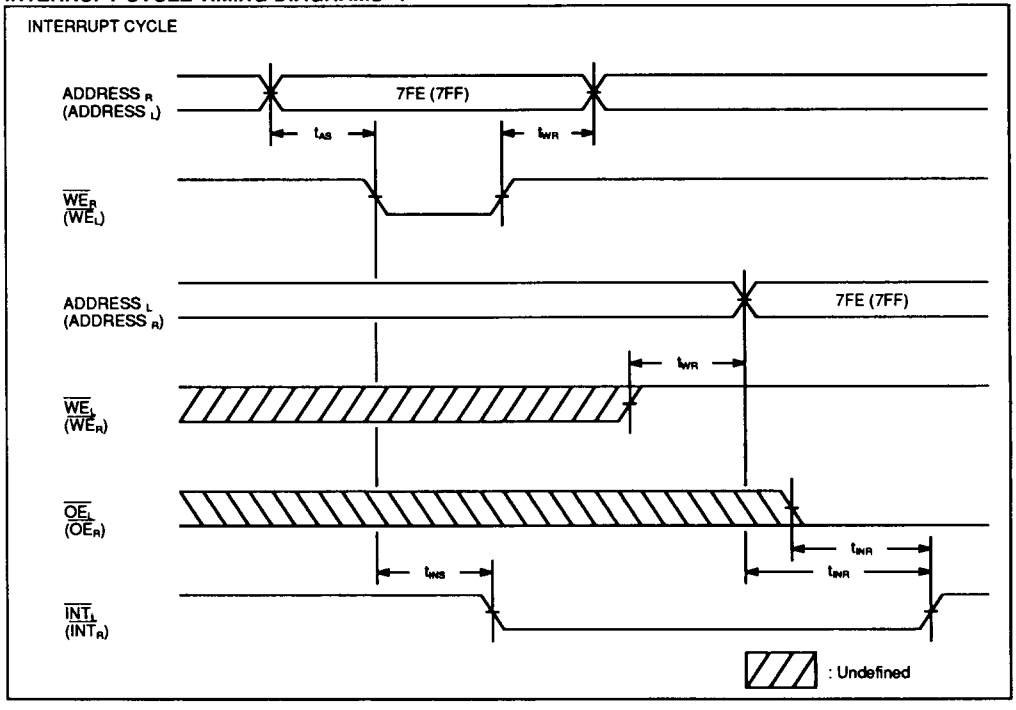


Note: *1 $\overline{WE}$ must be high during address transition.
*2 I/O pins are in the output state, so the input signals of opposite phase must not be applied.
*3 During $\overline{BUSY}$ input is low, write operation can not be excuted even if $\overline{WE}$ is low.

INTERRUPT TIMING *1

Parameter	Symbol	MB8431-90/90L/90LL MB8432-90/90L/90LL		MB8431-12/12L/12LL MB8432-12/12L/12LL		Unit
		Min	Max	Min	Max	
INT Set Time	t_{INS}		80		100	ns
INT Reset Time	t_{INR}		80		100	ns

INTERRUPT CYCLE TIMING DIAGRAMS *1



Note: *1 Applies to MB8431 only.

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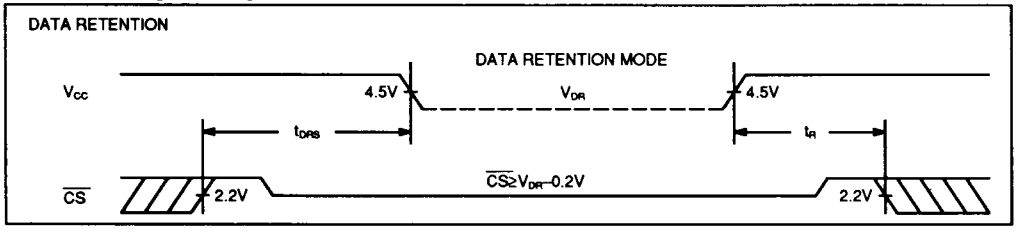
DATA RETENTION CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Data Retention Supply Voltage		V_{DR}	2.0		5.5	V
Data Retention Supply Current *1	Standard	I_{DR}			0.2	mA
	L-Version				20	µA
	LL-Version *2				2	µA
Data Retention Setup Time		t_{DRS}	0			ns
Operation Recovery Time		t_R	t_{RC}			ns

Note: *1 V_{CC}=V_{DR}=3V, $\overline{CS_L}$ & $\overline{CS_H}$≥V_{CC}-0.2V
*2 V_{DR}=3V, T_A=0°C to 40°C

DATA RETENTION TIMING



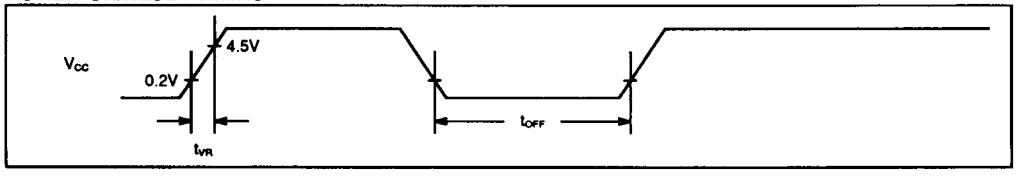
POWER ON/RESET CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB8431-90/90L/90LL MB8432-90/90L/90LL		MB8431-12/12L/12LL MB8432-12/12L/12LL		Unit
		Min	Max	Min	Max	
Power Up Time *1	t_{VR}	0.05	50	0.05	50	ms
Power Off Time *2	t_{OFF}	1		1		S

*1 This is required to keep normal operation for power on/reset circuit which initialize $\overline{INT}$ output to "H" automatically when V_{CC} is applied.
*2 This is required to keep normal operation for power on/reset circuit which V_{CC} is repeatly turn on/off.

POWER ON/RESET TIMING

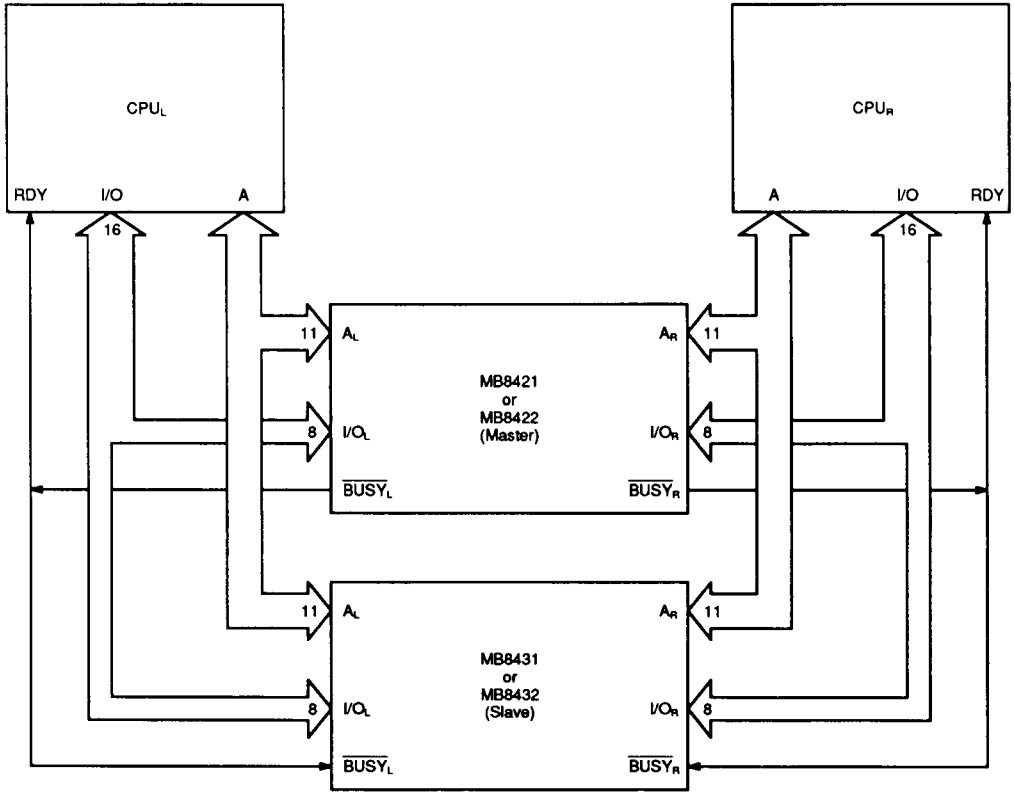


Function Description:

1. ORGANIZATION:
   MB8431/32 are 2K words x 8 bit Dual port Static Random Access Memory.
   Each port has independent addresses, chip select ($\overline{CS}$), write enable ($\overline{WE}$), output enable ($\overline{OE}$) and data input/output (I/O) functions.

2. SLAVE BUSY FUNCTION:
   In order to do bit expansion using 8 bit width dual port RAM such as MB8421/22, two or more parts should be connected paralel. But such case, there is a possibility, which depends on arbitration timing, of outputting $\overline{BUSY}$ signal to different ports and put both CPUs in waiting state. This causes a trouble. Using MB8431/32 which have slave busy function (busy input) is one of the solutaion for such trouble. Bit expansion is easily achievable to pair–use slave type dual port RAM such as MB8431/32 and master type dual port RAM such as MB8421/22.

(Example)
As an example, Fig1 shows 16 bit dual port memory system.
In this system, master type Dual port RAM (MB8421/22) judge arbitration for address contention and output result of the judgement from $\overline{BUSY}$ pin. This output returned to CPU and make the CPU in waiting state and also the output is applied to slave type dual port RAM (MB8431/32).
Though slave type dual port RAM (MB8431/32) do not judge for arbitration, they have $\overline{BUSY}$ input pin and inhibit write operation of the correspondent port during "L" signal form $\overline{BUSY}$ output of master type dual port RAM (MB8421/22) is applied to the $\overline{BUSY}$ input.
A system consists of one master dual port RAM (MB8421/22) and three slave dual port RAMs (MB8431/32) is harmonized for 32 bit application.



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3. INTERRUPT FUNCTION:
The interrupt function ($\overline{INT}$) is provided to allow communication between the systems on either sides of the dual–port RAM. $\overline{INT}_L$ is set to low, when the processor on the right port writes to address 7FE (A0=L and A1 to A10=H). $\overline{INT}_L$ is then reset to High, when the left port acknowledges by reading the same address 7FE. Thus the address 7FE is like a 8 bit word mail–box transferring information from the right–port to the left–port.

$\overline{INT}_R$ on the other hand is set to low, when processor on the left port writes to the address 7FF (A=0 to A10=H). $\overline{INT}_R$ is reset to High, when the right port acknowledges by reading this address. Hence, the address 7FF is a second 8 bit word mail–box transferring information form the left port to the right port.

The $\overline{INT}_L$ and $\overline{INT}_R$ are set to High on power–up. If the port is in the standby mode, it can still get interrupted by the processor on the other side.

In case he $\overline{BUSY}$ flag is set to low, then the pertinent port can not set or reset the $\overline{INT}$ flag.

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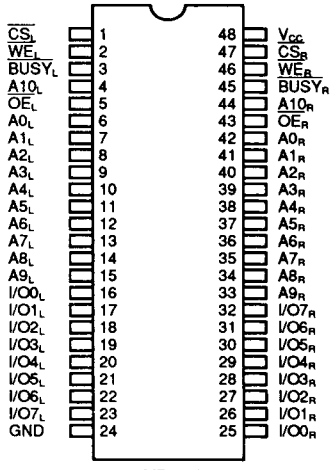
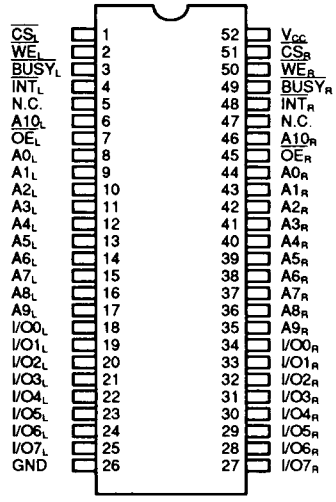
TOP VIEW

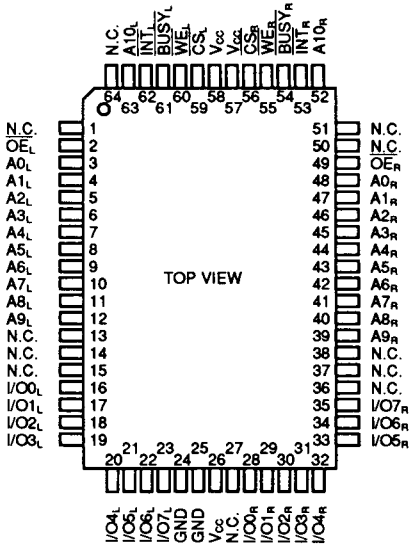


MB8432

TOP VIEW



MB8431



MB8431

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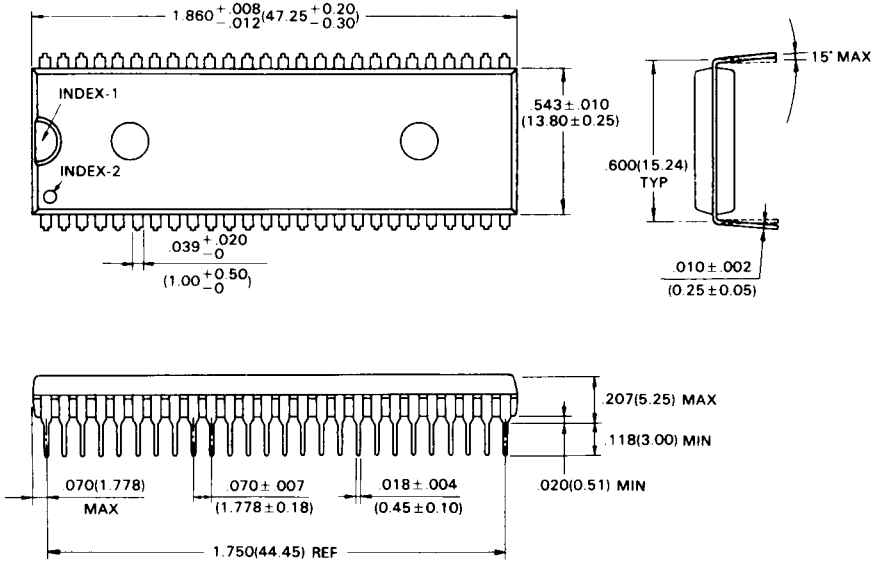
52-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-52P-M01)



Dimensions in
inches (millimeters)

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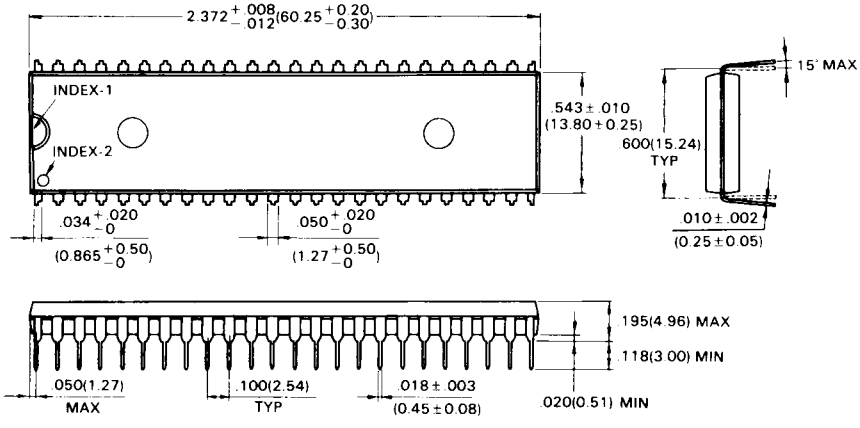
48-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-48P-M02)

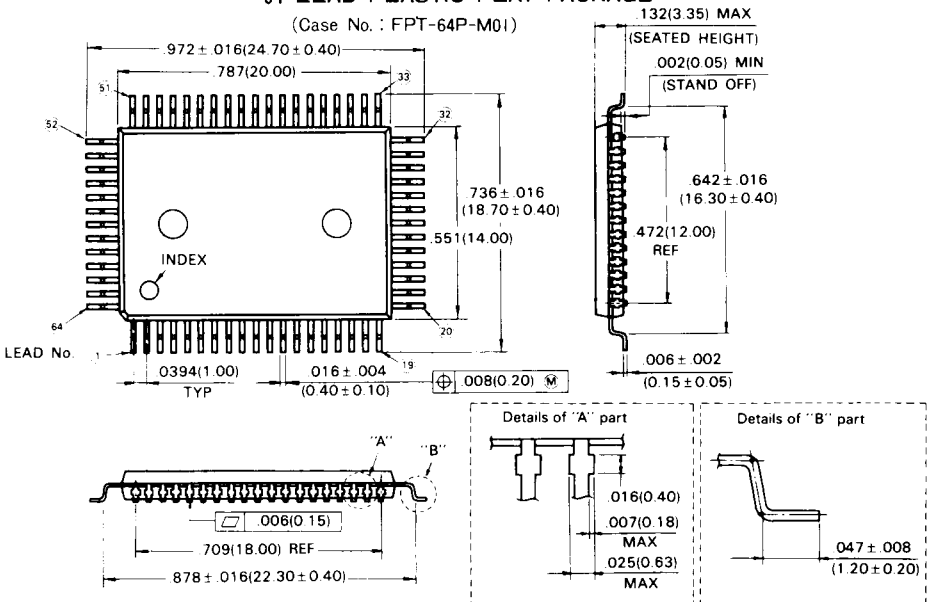


Dimensions in
inches (millimeters)

4

64-LEAD PLASTIC FLAT PACKAGE

(Case No. : FPT-64P-M01)



Dimensions in
inches (millimeters)

4