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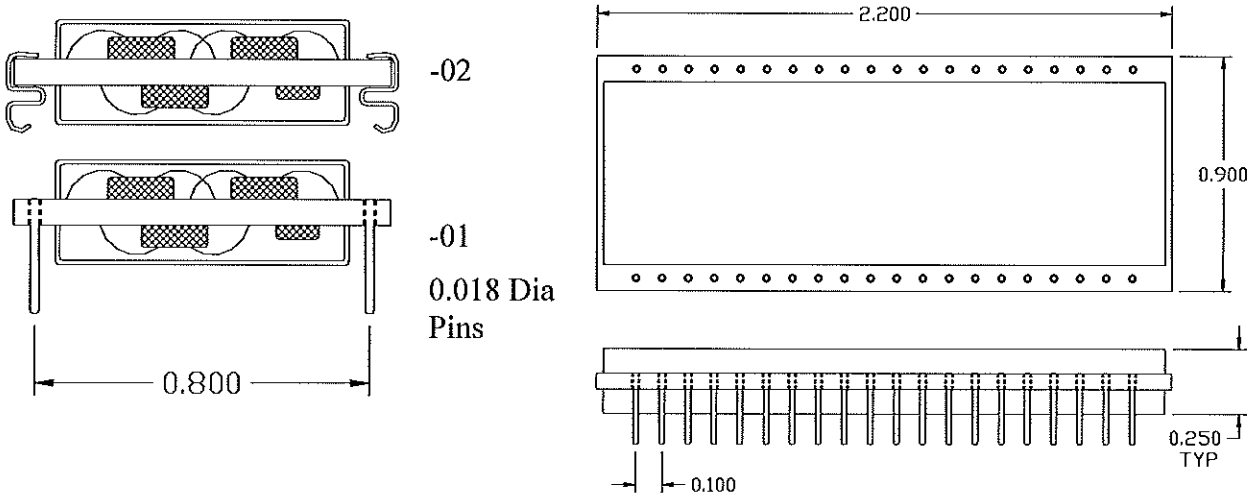
HIGH TEMPERATURE

32MB FLASH MEMORY MODULE

PART NUMBER 32MB08F-01/02 REV M

CMOS 5.0 Volt-only 8-bit



DISTINCTIVE CHARACTERISTICS

- 5.0 Volt +/- 10% for Read and Write Operations
- Sector Erase Architecture
- Supports Full Chip Erase
- Embedded Erase Algorithms
- Embedded Program Algorithms
- Data Polling and Toggle Bit Feature for Detection Of Program or Erase Cycle Completion
- Ready/Busy output (FLASHRDY) Hardware Detection Of Program or Erase Cycle Completion
- Erase Suspend/Resume Supports Reading or Programming Data to a Sector not Being Erased
- Low Power Consumption
- Hardware Reset Pin to Set Internal State Machine to the Read Mode
- Designed for High Temperature Applications

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PIN DESCRIPTION

1	FLASHRDY_H	40	VCC - 5.0 VOLTS
2	A_H13	39	A_H4
3	A_H14	38	A_H5
4	A_H15	37	A_H6
5	A_H16	36	A_H7
6	A_H17	35	A_H8
7	A_H18	34	A_H9
8	A_H19	33	A_H10
9	A_H20	32	A_H11
10	A_H21	31	A_H12
11	A_H22	30	RSTFLASH_L
12	A_H23	29	D_H0
13	A_H24	28	D_H1
14	WE_L	27	D_H2
15	CE_L	26	D_H3
16	A_H0	25	D_H4
17	A_H1	24	D_H5
18	A_H2	23	D_H6
19	A_H3	22	D_H7
20	GND	21	RE_L

Table 1

SIGNAL DESCRIPTION

VCC	Power Supply
WE_L	Write Enable Asserted Low Input
CE_L	Chip Enable Asserted Low Input
RSTFLASH_L	Reset Flash Asserted Low Input
RE_L	Read/Output Enable Asserted Low Input
FLASHRDY_H	Flash Ready Output (Tristate - Internal Pull-up Resistor)
A_H[24..21]	Select Line Inputs for Individual Flash Memory Chips
A_H[20..0]	Address Inputs
D_H[7..0]	Data Input/Outputs
GND	Ground

Table 2

GENERAL DESCRIPTION

The Flash Memory Module 32MB08F contains 16 Flash Memory chips along with the associated buffers and chip select logic. The 32MB08F module functionally appears as a 32MB by 8 bit Flash memory device. Figure 1 shows the functional layout. Address, data, and chip select buffers are built-in. This feature eliminates the need for these buffer devices on the user hardware. These HCMOS devices increase the Max Access Time and other CE, and RE access times from using a single flash memory device, but were added to facilitate the user design.

Figure 1 shows the address, data, and control paths to each of the 16 individual flash memory elements. The top three address lines, A_H[24..21] select the individual flash chip which will be used in the access and routes the Chip Enable (CE_L) signal to the selected part. The CE_L signal also enables the data buffer device. The data direction is selected by the Read Enable (RE_L) signal. When this signal is at a low level, the data direction is from the 32MB08F to the user's data bus. The Write Enable (WE_L), Reset Flash (RSTFLASH_L), and RE_L signals are routed through a buffer directly to the flash chip. The circuit designer should use the WE_L signal to control data writes to the 32MB08F rather than use the alternate CE_L controlled write operations. The Address, RE_L, and CE_L signals should meet the setup specifications before the WE_L signal is asserted.

Each flash memory device can be read in a random access manner. Writes, however, are done on a byte-by-byte basis and strict write procedures need to be followed. Before writing to a location in memory, that memory must first be erased. This can be done on a 64K byte sector basis, or it can be done on a chip wide basis. The memory chips draw up to 60 milliamps during the erase cycle. It is possible to program the individual memory chips to enter erase cycles at the same time. Care should be taken that the thermal limits of the device are not exceeded and that the power supply can provide the necessary current. It is recommended that the chips be individually

erased. It is also possible to have more than one chip in a write mode at the same time. The write state can also draw up to 50 milliamps so care should be taken when causing more than one chip to be in the write state.

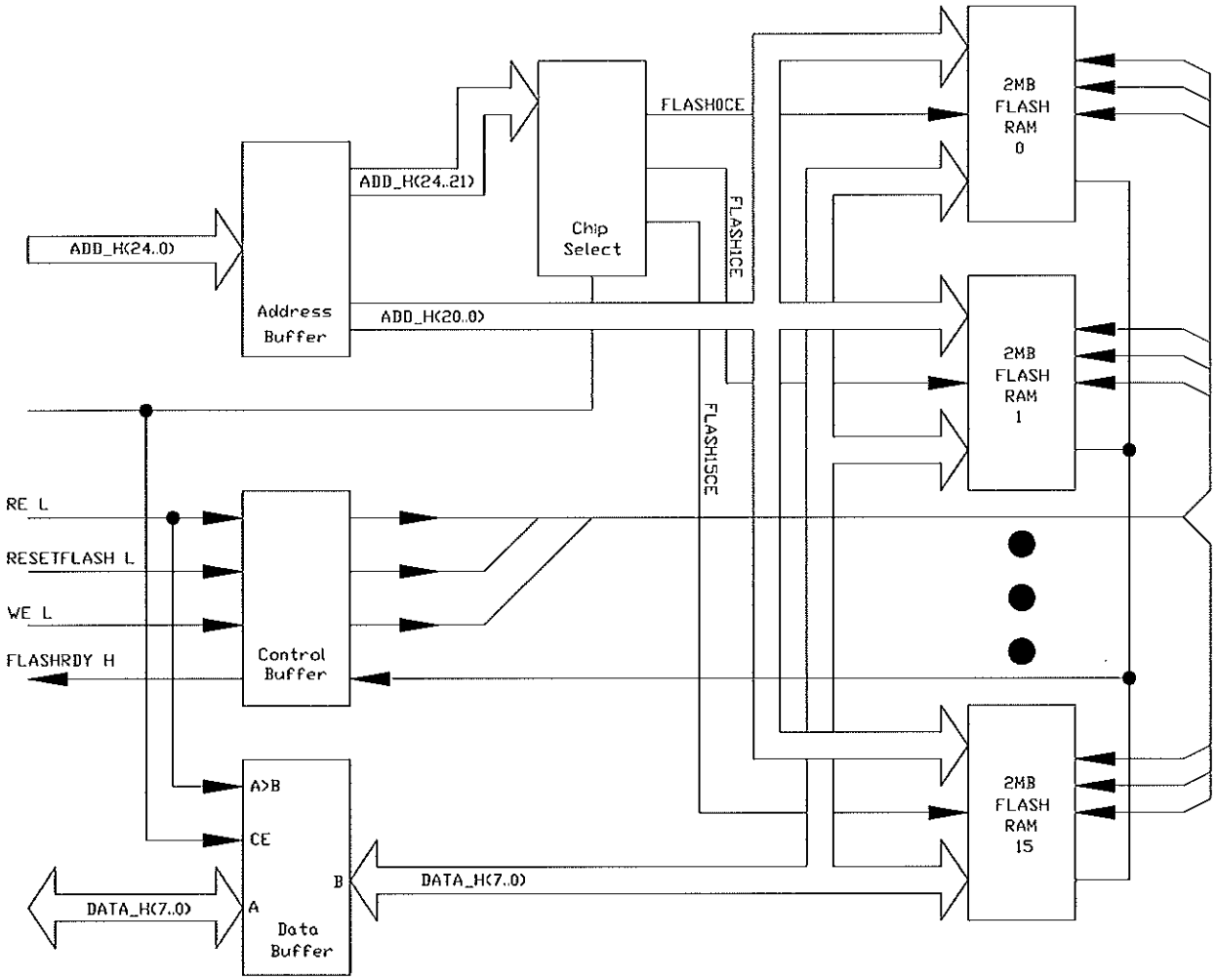

Figure 1

AUTOMATIC PROGRAMMING

Each Flash chip in the 32MB08F is byte programmable using the Automatic Programming algorithm. The Automatic Programming algorithm avoids a time out sequence requirement for the programming. The typical chip programming time at room temperature is less than 15 seconds.

AUTOMATIC CHIP ERASE

Each Flash chip in the 32MB08F is bulk erased using 10 ms erase pulses according to an Automatic Chip Erase algorithm. Typical erasure at room temperature is accomplished in less than 19 seconds. The Automatic Erase algorithm automatically programs the entire array prior to electrical erase. The timing and verification of electrical erase are controlled internally within the device.

AUTOMATIC SECTOR ERASE

Each Flash chip in the 32MB08F is sector(s) erasable using an Auto Sector Erase algorithm. Sector erase modes allow sectors of the array to be erased in one erase cycle. The Automatic Sector Erase algorithm automatically programs the specified sector(s) prior to electrical erase. The timing and verification of electrical erase are controlled internally within the device.

AUTOMATIC PROGRAMMING ALGORITHM

The Automatic Programming algorithm requires the user to only write program set-up commands (including 2 unlock write cycle and A0H) and a program command (program data and address). The device automatically times the programming pulse width, provides the program verification, and counts the number of sequences. A status bit similar to DATA polling and a status bit toggling between consecutive read cycles, provide feedback to the user as to the status of the programming operation.

AUTOMATIC ERASE ALGORITHM

The Automatic Erase algorithm requires the user to write commands to the command register using standard microprocessor write timings. The device will automatically pre-program and verify the entire array. Then the device automatically times the erase pulse width, provides the erase verification, and counts the number of sequences. A status bit toggling between consecutive read cycles provides feedback to the user as to the status of the programming operation.

Register contents serve as inputs to an internal state machine, which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. During a system write cycle, addresses are latched on the falling edge, and data are latched on the rising edge of WE.

Each Flash chip in the 32MB08F electrically erases all bits simultaneously using Fowler-Nordheim tunneling. Using the EPROM programming mechanism of hot electron injection programs the bytes.

During a program cycle, the state-machine will control the program sequences and command register will not respond to any command set. During a Sector Erase cycle, the command register will only respond to Erase Suspend command. After Erase Suspend is completed, the device stays in read mode. After the state machine has completed its task, it will allow the command register to respond to its full command set.

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32MB08F COMMAND DEFINITIONS

Command Sequence	Bus Write Cycles Required	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		ADDR	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Reset	1	xxxxH	F0H										
Read	1	RA	RD										
Byte Program	4	555H	AAH	2AAH	55H	555H	A0H	PA	PD				
Chip Erase	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	10H
Sector Erase	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	SA	30H
Erase Suspend	1	xxxxH	B0H										
Erase Resume	1	xxxxH	30H										

Table 3

NOTES:

1. RA = Address of the memory location to be read.
2. PA = Address of the memory location to be programmed. Address is latched on the falling edge of the WE_L pulse.
3. SA = Address of the sector to be erased. The combination of A[20..16] will uniquely select any 64K byte Sector.
4. RD = Data read from location RA during Read operation.
5. PD = Data to be programmed at location PA. Data is latched on the rising edge of WE_L.
6. Read and Byte program functions to non-erasing sectors are allowed in the Erase Suspend Mode.
7. The above table defines individual states of the sixteen Flash chips. Each chip is individually selected by address lines A[24..21].

Each Flash Chip in the device can be read, written and erased. Device erasure and programming are accomplished via the command register within each flash chip. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device.

The command register itself does not occupy any addressable memory location. The register is a latch used to store the command along with the address and data information needed to execute the command. The command register is written by bringing WE_L to a low level while CE_L is at a low level and RE_L is high. Addresses are latched on the falling edge of WE_L.

COMMAND DEFINITIONS

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in the improper sequence will force the device to the read mode. Table 4 defines the valid register command sequences. Note that the Erase Suspend (BOH) and Erase Resume (30H) commands are valid only while the Sector Erase operation is in progress.

USER BUS OPERATIONS

Operation	CE_L	RE_L	WE_L	A[24..21]	D[7..0]	Reset
Read	L	L	H	Select	Dout	H
Standby	H	H	X	X	High Z	H
Output Disable	L	H	H	Select	High Z	H
Write	L	H	L	Select	Din	H
Hardware Reset/Standby	H	H	H	X	High Z	L

Table 4

STANDBY MODE

There are two ways to implement a Standby Mode. One is to set CE_L to the high state, and the other is to assert the Hardware Reset pin RSTFLASH_L to a Low State. When using both signals to implement the Standby mode CE_L in the High State, and RSTFLASH_L in the low state the current drawn by the device is lowest and is typically <50 micro Amps. RE_L should be in the high state when implementing the Standby Mode.

OUTPUT DISABLE

With the RE_L input at a logic high level, output from the device is disabled.

READ MODE

The 32MB08F has two control functions, which must be satisfied in order to obtain data at the outputs. CE_L is the master select and will select one of the 16 flash chips corresponding to address lines A[24..21]. WE_L should be in the high state. The data associated with the address A[20..0] will be gated to the outputs when RE_L goes low. RE_L should be used to gate data to the output pins if the device is selected.

Address access time (Tacc) is equal to the delay from stable addresses to valid output data. The chip enable access time (Tcs) is the delay from stable addresses and stable CE_L to valid data at the output pins. The output enable access time is the delay from the falling edge of RE_L to valid data at the output pins assuming the addresses have been stable for at least Tacc-Tce time.

READ/RESET COMMAND

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data. The device remains enabled for reads until the command register contents are altered.

If program-fail or erase-fail happen, the write of F0H will reset the device to abort the operation. A valid command must then be written to place the device in the desired state.

SET-UP AUTOMATIC CHIP/SECTOR ERASE

Chip erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command 80H. Two more "unlock" write cycles are then followed by the chip erase command 10H.

The Automatic Chip Erase does not require the device to be entirely pre-programmed prior to executing the Automatic Chip Erase. Upon executing the Automatic Chip Erase, the device will automatically program and verify the entire memory for an all-zero data pattern. When the device is automatically verified to contain an all-zero pattern, a self-timed chip erase and verify begin. The erase and verify operations are completed when the data on Q7 is "1" at which time the device returns to the Read mode. The system is not required to provide any control or timing during these operations.

When using the Automatic Chip Erase algorithm, note that the erase automatically terminates when adequate erase margin has been achieved for the memory array (no erase verification command is required).

If the Erase operation was unsuccessful, the data on Q5 is "1"(see Table 5), indicating the erase operation exceed internal timing limit.

The automatic erase begins on the rising edge of the last WE pulse in the command sequence and terminates when the data on Q7 is "1" and the data on Q6 stops toggling for two consecutive read cycles, at which time the device returns to the Read mode.

SECTOR ERASE

The Automatic Sector Erase does not require the device to be entirely pre-programmed prior to executing the Automatic Set-up Sector Erase command and Automatic Sector Erase command. Upon executing the Automatic Sector Erase command, the device will automatically program and verify the sector(s) memory for an all-zero data pattern. The system is not required to provide any control or timing during these operations.

When the sector(s) is automatically verified to contain an all-zero pattern, a self-timed sector erase and verify begin. The erase and verify operations are complete when the data on Q7 is "1" and the data on Q6 stops toggling for two consecutive read cycles, at which time the device returns to the Read mode. The system is not required to provide any control or timing during these operations.

When using the Automatic Sector Erase algorithm, note that the erase automatically terminates when adequate erase margin has been achieved for the memory array (no erase verification command is required). Sector erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the set-up command 80H. Two more "unlock" write cycles are then followed by the sector erase command 30H. The sector address is latched on the falling edge of WE, while the command (data) is latched on the rising edge of WE. Sector addresses selected are loaded into internal register on the sixth falling edge of WE. Each successive sector load cycle started by the falling edge of WE must begin within 80ms from the rising edge of the preceding WE. Otherwise, the loading period ends and internal auto sector erase cycle starts. (Monitor Q3 to determine if the sector erase timer window is still open, see section Q3, Sector Erase Timer.) Any command other than Sector Erase (30H) or Erase Suspend (B0H) during the timeout period resets the device to read mode.

	Status	Q7	Q6	Q5	Q3	Q2
In Progress	Byte Program in Auto Program Algorithm	#Q7	Toggle	0	0	1
In Progress	Auto Erase Algorithm	0	Toggle	0	1	Toggle
In Progress	Erase Suspended Mode, Erase Suspend Read (Erase Suspended Sector)	1	1	0	0	Toggle (Note 1)
In Progress	Erase Suspended Mode, Erase Suspend Read (Non-Erase Suspended Sector)	Data	Data	Data	Data	Data
In Progress	Erase Suspended Mode, Erase Suspend Program (Non-Erase Suspended Sector)	#Q7	Toggle (Note 2)	0	0	1 (Note 3)
Exceeded Time Limits	Byte Program in Auto Program Algorithm	#Q7	Toggle	0	0	1
Exceeded Time Limits	Program/Erase in Auto Erase Algorithm	0	Toggle	1	1	N/A
Exceeded Time Limits	Erase Suspended Mode, Erase Suspend Program (Non-Erase Suspended Sector)	#Q7	Toggle	0	0	N/A

Table 5. Write Operation Status

Notes:

1.Performing successive read operations from the erase-suspended sector will cause Q2 to toggle.
2.Performing successive read operations from any address will cause Q6 to toggle.
3.Reading the byte address being programmed while in the erase-suspend program mode will indicate logic "1" at the Q2 bit. However, successive reads from the erase-suspended sector will cause Q2 to toggle.

ERASE SUSPEND

This command only has meaning while the state machine is executing Automatic Sector Erase operation, and therefore will only be responded during Automatic Sector Erase operation. However, When the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation. After this command has been executed, the command register will initiate erase suspend mode. The state machine will return to read mode automatically after suspend is ready. At this time, state machine only allows the command register to respond to the Read Memory Array, Erase Resume and program commands.

The system can determine the status of the program operation using the Q7 or Q6 status bits, just as in the standard program operation. After an erase-suspend program operation is complete, the system can once again read array data within non-suspended blocks.

ERASE RESUME

This command will cause the command register to clear the suspend state and return back to Sector Erase mode but only if an Erase Suspend command was previously issued. Erase Resume will not have any effect in all other conditions. Another Erase Suspend command can be written after the chip has resumed erasing.

SET-UP AUTOMATIC PROGRAM COMMANDS

The device is programmed on a byte-by-byte basis within each of the 16 flash memory chips. Each chip is selected by the high order address lines A[24..21]. To initiate Automatic Program mode, A three-cycle command sequence is required. There are two "unlock" write cycles. These are followed by writing the Automatic Program command A0H.

Once the Automatic Program command is initiated, the next WE pulse causes a transition to an active programming operation. Addresses are latched on the falling edge, and data are internally latched on the rising edge of the WE pulse. The rising edge of WE also begins the programming operation. The system is not required to provide further controls or timings. The device will automatically provide an adequate internally generated program pulse and verify margin.

If the program operation was unsuccessful, the data on Q5 is "1"(see Table 5), indicating the program operation exceed internal timing limit. The automatic programming operation is completed when the data read on Q6 stops toggling for two consecutive read cycles and the data on Q7 and Q6 are equivalent to data written to these two bits, at which time the device returns to the Read mode (no program verify command is required).

DATA POLLING

Q7

Each Flash chip in the 32MB08F device features Data Polling as a method to indicate to the host system that the Automatic Program or Erase algorithms are either in progress or completed.

While the Automatic Programming algorithm is in operation, an attempt to read the device will produce the complement data of the data last written to Q7. Upon completion of the Automatic Program Algorithm an attempt to read the device will produce the true data last written to Q7. The Data Polling feature is valid after the rising edge of the fourth WE pulse of the four write pulse sequences for automatic program.

While the Automatic Erase algorithm is in operation, Q7 will read "0" until the erase operation is competed. Upon completion of the erase operation, the data on Q7 will read "1". The Data Polling feature is valid after the rising edge of the sixth WE pulse of six-write pulse sequences for automatic chip/sector erase.

The Data Polling feature is active during Automatic Program/Erase algorithm or sector erase time-out. (see section Q3 Sector Erase Timer)

TOGGLE BIT I
Q6

Each flash chip in the 32MB08F also features the Toggle Bit I on Q6 as a method to indicate to the host system whether an Automatic Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE pulse in the command sequence (prior to the program or erase operation), and during the sector time-out.

During an Automatic Program or Erase algorithm operation, successive read cycles to any address cause Q6 to toggle. The system may use either OE or CE to control the read cycles. When the operation is complete, Q6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, Q6 toggles and returns to reading array data. If not all selected sectors are protected, the Automatic Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use Q6 and Q2 together to determine whether a sector is actively erasing or is erase suspended. When the device is actively erasing (that is, the Automatic Erase algorithm is in progress), Q6 toggling. When the device enters the Erase Suspend mode, Q6 stops toggling. However, the system must also use Q2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use Q7.

If a program address falls within a protected sector, Q6 toggles for approximately 2us after the program command sequence is written, then returns to reading array data.

Q6 also toggles during the erase-suspend-program mode, and stops toggling once the Automatic Program algorithm is complete.

Table 5 shows the outputs for Toggle Bit I on Q6.

TOGGLE BIT II
Q2

The "Toggle Bit II" on Q2, when used with Q6, indicates whether a particular sector is actively erasing (that is, the Automatic Erase algorithm is in process), or whether that sector is erase-suspended. Toggle Bit I is valid after the rising edge of the final WE pulse in the command sequence.

Q2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE or CE to control the read cycles.) But Q2 cannot distinguish whether the sector is actively erasing or is erase-suspended. Q6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sectors and mode information. Refer to Table 5 to compare outputs for Q2 and Q6.

READING TOGGLE BITS Q6/ Q2

Whenever the system initially begins reading toggle bit status, it must read Q7-Q0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on Q7-Q0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of Q5 is high (see the section on Q5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as Q5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that system initially determines that the toggle bit is toggling and Q5 has not gone high. The system may continue to monitor the toggle bit and Q5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation.

EXCEEDED TIMING LIMIT

Q5

Q5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions Q5 will produce a "1". This time-out condition indicates that the program or erase cycle was not successfully completed. Data Polling and Toggle Bit are the only operating functions of the device under this condition.

If this time-out condition occurs during sector erase operation, it specifies that a particular sector is bad and it may not be reused. However, other sectors are still functional and may be used for the program or erase operation. The device must be reset to use other sectors. Write the Reset command sequence to the device, and then execute program or erase command sequence. This allows the system to continue to use the other active sectors in the device.

If this time-out condition occurs during the chip erase operation, it specifies that the entire chip is bad or combination of sectors is bad.

If this time-out condition occurs during the byte programming operation, it specifies that the entire sector containing that byte is bad and this sector may not be reused, (other sectors are still functional and can be reused).

The time-out condition may also appear if a user tries to program a non-blank location without erasing. In this case the device locks out and never completes the Automatic Algorithm operation. Hence, the system never reads a valid data on Q7 bit and Q6 never stops toggling. Once the Device has exceeded timing limits, the Q5 bit will indicate a "1". Please note that this is not a device failure condition since the device was incorrectly used.

DATA PROTECTION

Each Flash chip in the 32MB08F is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transition.

During power up the device automatically resets the state machine in the Read mode. In addition, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting from VCC power-up and power-down transition or system noise.

TEMPORARY SECTOR UNPROTECT

This feature allows temporary unprotection of previously protected sector to change data in-system. The Temporary Sector Unprotect mode is activated by setting the RESET pin to VID (11.5V-12.5V). During this mode, formerly protected sectors can be programmed or erased as unprotected sector. Once VID is remove from the RESET pin, all the previously protected sectors are protected again.

SECTOR ERASE TIMER

Q3

After the completion of the initial sector erase command sequence, the sector erase time-out will begin. Q3 will remain low until the time-out is complete. Data Polling and Toggle Bit are valid after the initial sector erase command sequence.

If Data Polling or the Toggle Bit indicates the device has been written with a valid erase command, Q3 may be used to determine if the sector erase timer window is still open. If Q3 is high ("1") the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by Data Polling or Toggle Bit. If Q3 is low ("0"), the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of Q3 prior to and following each subsequent sector erase command. If Q3 were high on the second status check, the command may not have been accepted.

WRITE PULSE "GLITCH" PROTECTION

Noise pulses of less than 5ns (typical) on RE_L, CE_L or WE_L will not initiate a write cycle.

LOGICAL INHIBIT

Writing is inhibited by holding any one of OE = VIL, CE = VIH or WE = VIH. To initiate a write cycle CE and WE must be a logical zero while OE is a logical one.

POWER-UP SEQUENCE

Each Flash chip in the 32MB08F powers up in the Read only mode. In addition, the memory contents may only be altered after successful completion of the predefined command sequences

FLASHRDY_H

This signal on the 32MB08F is the wired-or of the tri-state Ready/Busy signal from each of the 16 Flash chips. Each Ready/Busy output on the Flash chips indicate to the host system that the Embedded Algorithms are either in progress or have been completed. If the output is low, the device is busy with either a program or an erase operation. If the output is high, the device is ready to accept any read/write or erase operation. When the FLASHRDY_H pin is low, the individual flash chip device will not accept any additional program or erase commands with the exception of the Erase Suspend command. If the chip is placed in an Erase Suspend mode, the FLASHRDY_H output will be high. Note that because of the wired-or nature, the status of each individual chip is not reflected. It is not recommended that more than one chip at a time be placed in a write or erase condition due to excessive currents and heat.

During programming, the FLASHRDY_H pin is driven low after the rising edge of the fourth WE_L pulse. During an erase operation the FLASHRDY_H pin is driven low after the rising edge of the sixth WE_L pulse. The FLASHRDY_H pin will indicate a busy condition during the RSTFLASH pulse. This pin is electrically pulled high by a 4.7K ohm resister internal to the device.

RSTFLASH - HARDWARE RESET

Driving the RSTFLASH pin low will reset each flash chip in the 32MB08F device. The RSTFLASH pin must be kept low for at least 500 ns. Any operation in progress will be terminated and the internal state machine will be reset to the read mode 20 microseconds after the RSTFLASH pin is driven low. If a hardware reset occurs during a program on erase operation. the data at that particular location will be indeterminate.

When the RSTFLASH pin is low and the internal reset is complete, the device goes to standby mode and cannot be accessed. Also, note that all the data output pins are tri-stated for the duration of the RSTFLASH pulse. Once the RSFLASH pin is taken high, the device requires 500 ns of wake-up time until outputs are valid for read access.

The RSTFLASH pin may be tied to the system reset input. Therefore, if a system reset occurs during the Embedded Program or Erase Algorithm, the device will be automatically reset to read mode and this will enable the systems microprocessor to read the boot-up firmware from the Flash memory.

ABSOLUTE MAXIMUM RATINGS

Parameter	Range	Unit
Voltage on Any Pin with Respect to GND (except Vcc)	- 0.5 to Vcc + 0.5	Volts
Vcc Supply Voltage with Respect to GND	- 0.5 to + 7.0	Volts

Table 6

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage (@ 25 deg C)	Vcc	+ 4.5	+ 5.5	Volts
Supply Voltage (@ 175 deg C)	Vcc	+ 4.75	+ 5.25	Volts
Input High Voltage	Vih	+ 3.15	+ 3.85	Volts
Input Low Voltage	Vil	+ 0.8	+ 0.8	Volts
Operating Temperature	Ta	- 55	+ 175	Degrees C

Table 7

DC CHARACTERISTICS- READ OPERATION

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
ILI	Input Leakage Current	-------	-------	1	uA	VIN = GND to VCC
ILO	Output Leakage Current	-------	-------	+/-1	uA	VOUT = GND to VCC
ISB1	Standby VCC Current	-------	-------	1	mA	#CE = VIH
ISB2	Standby VCC Current	-------	0.2	5	uA	#CE = VCC + 0.3V
ICC1	Operating VCC Current	-------	-------	30	mA	IOUT = 0mA, f = 1 MHz
ICC2	Operating VCC Current	-------	-------	50	mA	IOUT = 0mA, f = 10MHz
VIL	Input Low Voltage	-0.3 (Note 1)	-------	0.8	V	
VIH	Input High Voltage	2.0	-------	VCC + 0.3	V	
VOL	Output Low Voltage	-------	--------	0.45	V	IOL = 2.1 mA
VOH	Output High Voltage	2.4	-------	--------	V	IOH = 2 mA

Table 8

Notes:

1. VIL min = -1.0V for pulse width is equal to or less than 50 ns. VIL min = -2.0V for pulse width is equal to or less than 20 ns.
2. VIH max = VCC + 1.5V for pulse width
3. DC Characteristics are applicable to a single flash chip.

AC CHARACTERISTICS - READ-ONLY OPERATIONS

Symbol	Parameter	MIN.	MAX.	UNIT	CONDITIONS
tACC	Address to Output Delay		120	ns	CE=OE=VIL
TCE	CE to Output Delay		120	ns	OE=VIL
tOE	OE to Output Delay		50	ns	CE=VIL
TDF	OE High to Output Float (see note)	0	30	ns	CE=VIL
tOH	Address to Output hold	0		ns	CE=OE=VIL

Table 9

TEST CONDITIONS:

Input pluse levels 0.45V/2.4V
Input rise and fall times is equal to or less that 20 ns
Output load 1 TTL gate + 100 pF (including scope and jig)
Reference levels for measuring timing 0.8V,2.0V

NOTE:

tDF is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

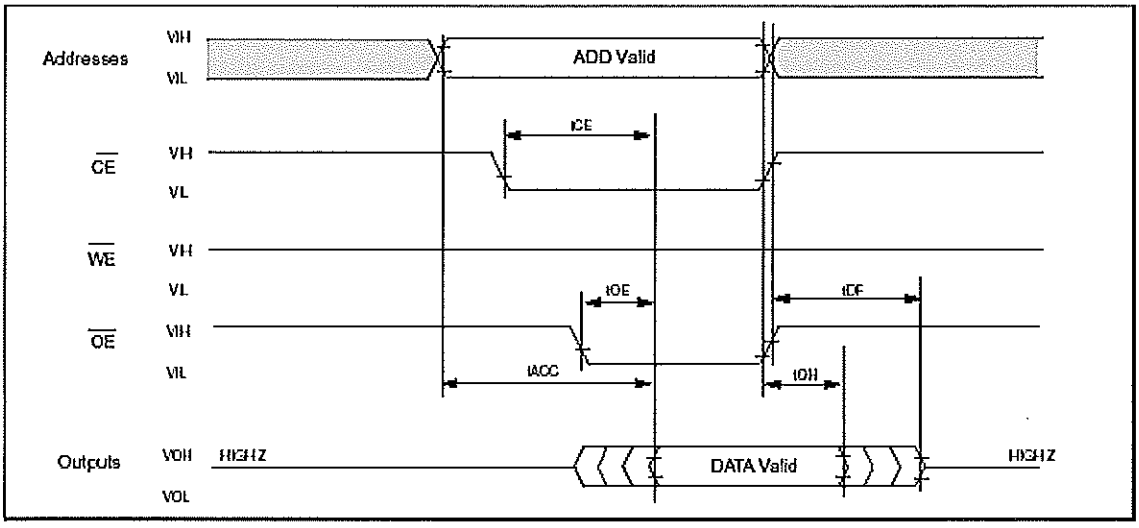

Figure 2: AC Waveforms for Read Operations

DC CHARACTERISTICS

WRITE / ERASE / PROGRAM OPERATIONS – WE_L

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
ICC1(Read)	Operating VCC Current			30	mA	IOUT=0mA,f=1MHz
ICC2				50	mA	IOUT=0mA,F=10MHz
ICC3(Program)				50	mA	In Programming
ICC4(Program)				50	mA	In Erase
ICCES	VCC Erase Suspend Current		2		mA	CE=VIH, Erase Suspended

Table 10

Notes:

1. DC Characteristics are applicable to a single flash chip.

AC Characteristics
WRITE / ERASE / PROGRAM OPERATIONS - WE_L

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
tOES	OE setup time	50		ns
tCWC	Command Programming cycle	120		ns
tCEP	WE programming width pulse width	50		ns
tCEPH1	WE programming pulse width High	20		ns
TtCEPH2	WE programming pulse width High	20		ns
tAS	Address setup time	0		ns
tAH	Address hold time	50		ns
tDS	Data setup time	50		ns
tDH	Data hold time	0		ns
tCESC	CE setup time before command write	0		ns
tDF	Output disable time (note1)		30	ns
tAETC	Total erase time in auto chip erase (note2,3)	32(TYP)	256	s
tAETB	Total erase tine in auto sector erase (note2,3)	4(TYP)	30	s
tAVT	Byte programmingtime in auto verify (note2,3)	7(TYP)	300	us
tBAL	Block address load time	80		us
tCH	CE Hold Time	0		ns
tCS	CE setup to WE going low	0		ns
tVLHT	Voltage transition time	4		us
tOESP	OE setup time to WE Active	4		us
tWPP1	Write pulse width for sector protect	10		us
tWPP2	Write pulse width for sector unprotect	12		ms

Table 11

Notes:
1. tDF defined as the time which the output achieves the open circuit condition and data is no longer driven.
2. Numbers are sampled, not 100% tested.
3. Typical values are measured at 25C,VCC=5.OV.

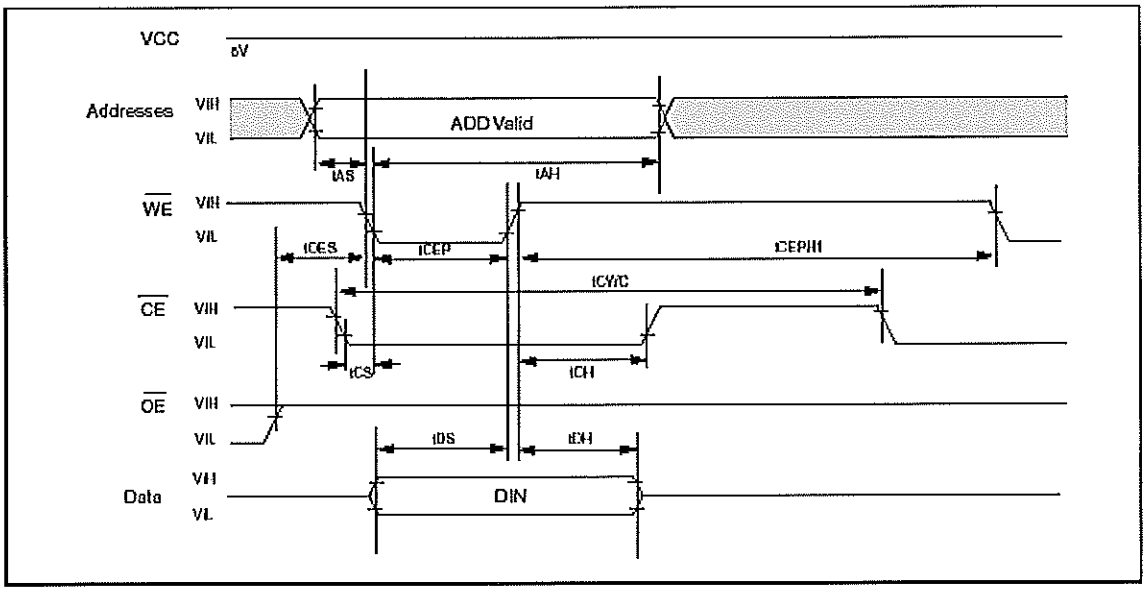

Figure 3: AC Waveforms for Write/Erase Operation Timings

CAPACITANCE

Parameter	Symbol	Conditions	Typical	Units
RE_L	Cre	Vin = 0.2V, F = 1.0 KHz	5.5	pF
WE_L	Cwe	Vin = 0.2V, F = 1.0 KHz	6.0	pF
CE_L	Cce	Vin = 0.2V, F = 1.0 KHz	110	pF
FLASHRDY_H	Cfr	Vin = 0.2V, F = 1.0 KHz	165	pF
RSTFLASH_L	Crf	Vin = 0.2V, F = 1.0 KHz	6.0	pF
A_H[24..0]	Cad	Vin = 0.2V, F = 1.0 KHz	5.0	pF
D_H[7..0]	Cio	Vin = 0.2V, F = 1.0 KHz	10	pF

Table 12 (Ta = +25 Deg C)

AUTOMATIC PROGRAMMING TIMING WAVEFORM

One byte data is programmed. Verify in fast algorithm and additional programming by external control are not required because these operations are executed automatically by internal control circuit. Programming completion can be verified by DATA polling and toggle bit checking after automatic verification starts. Device outputs DATA during programming and DATA after programming on Q7.(Q6 is for toggle bit; see toggle bit, DATA polling, timing waveform)

AUTOMATIC PROGRAMMING TIMING WAVEFORM

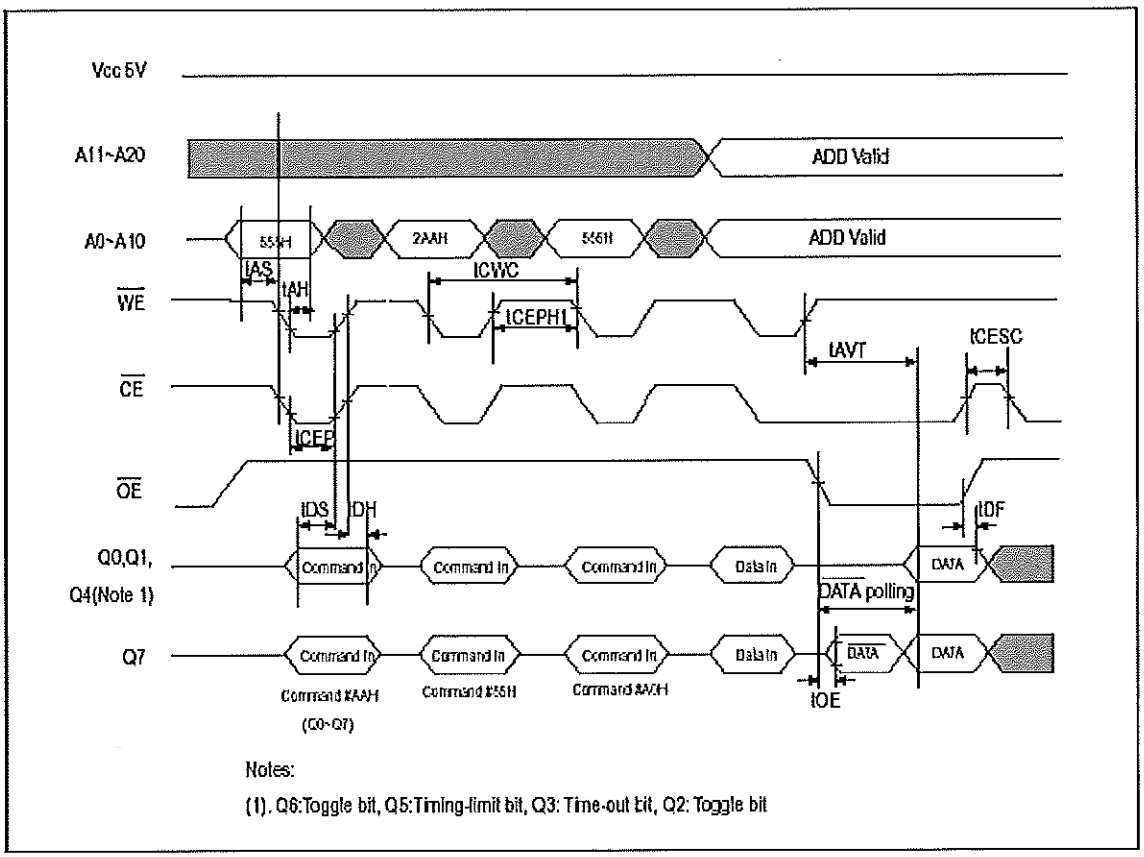

Figure 4

AUTOMATIC CHIP ERASE ALGORITHM FLOWCHART

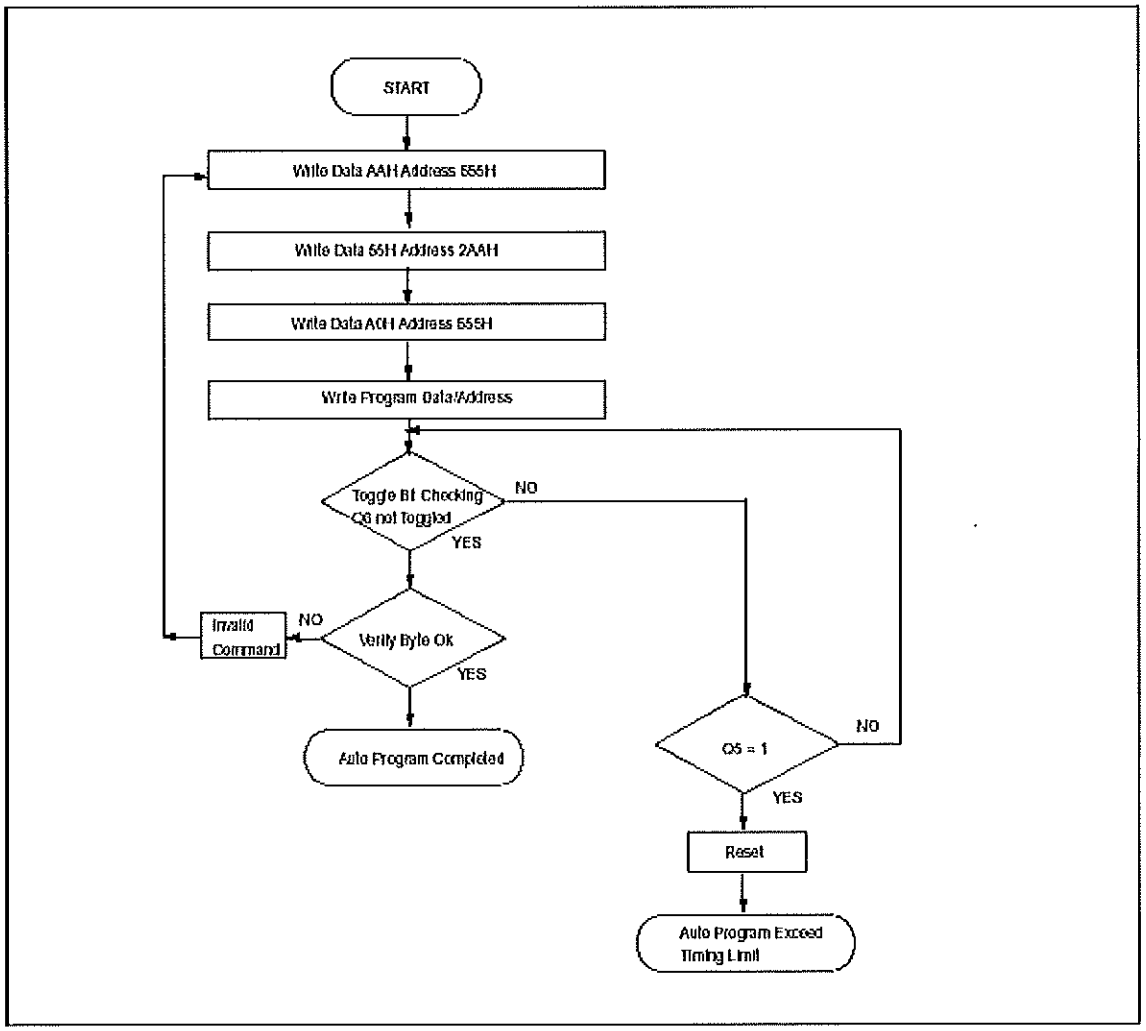

Figure 5

AUTOMATIC CHIP ERASE TIMING WAVEFORM

All data in chip are erased. External erase verification is Not required because data is erased automatically by internal control circuit. Erasure completion can be verified by DATA polling and toggle bit checking after automatic erase starts. Device outputs 0 during erasure and 1 after erasure on Q7.(Q6 is for toggle bit; see toggle bit, DATA polling, timing waveform)

AUTOMATIC CHIP ERASE TIMING WAVEFORM

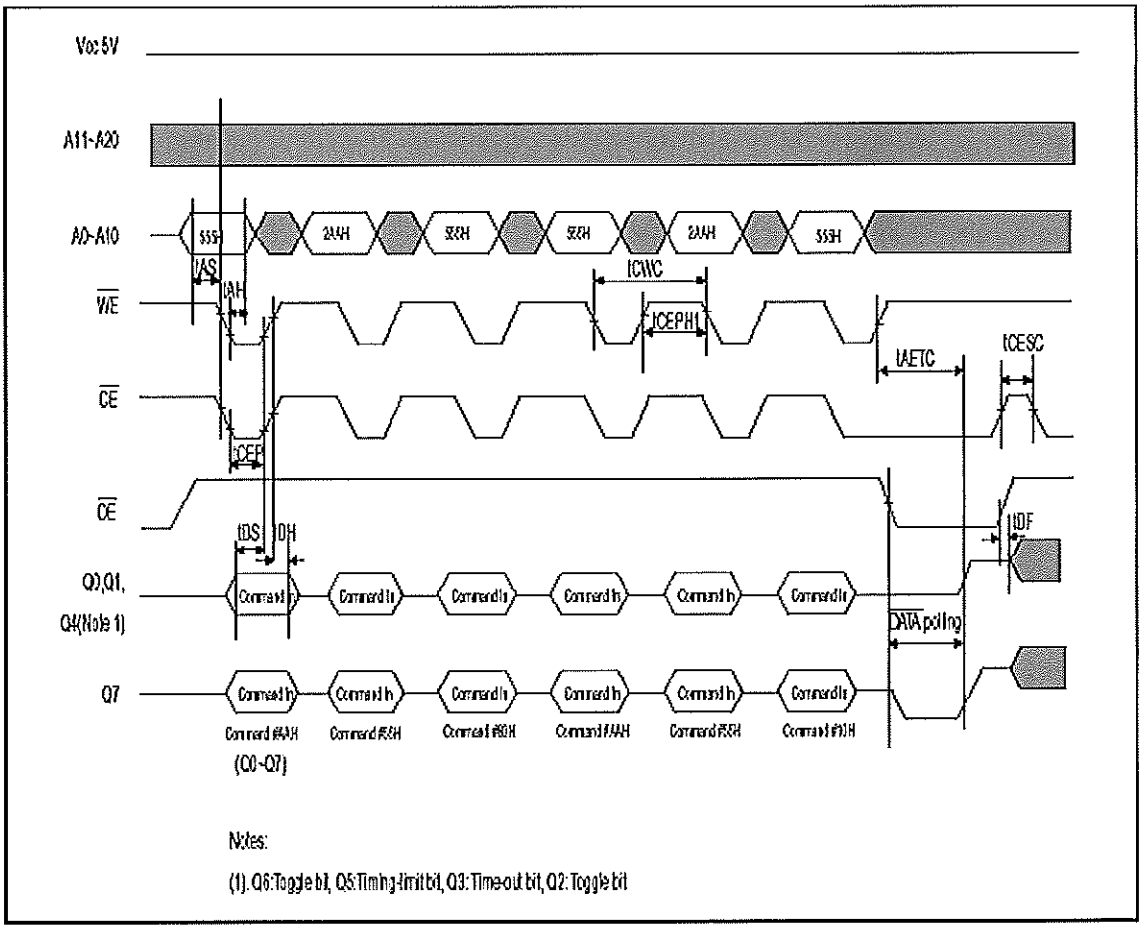

Figure 6

AUTOMATIC CHIP ERASE ALGORITHM FLOWCHART

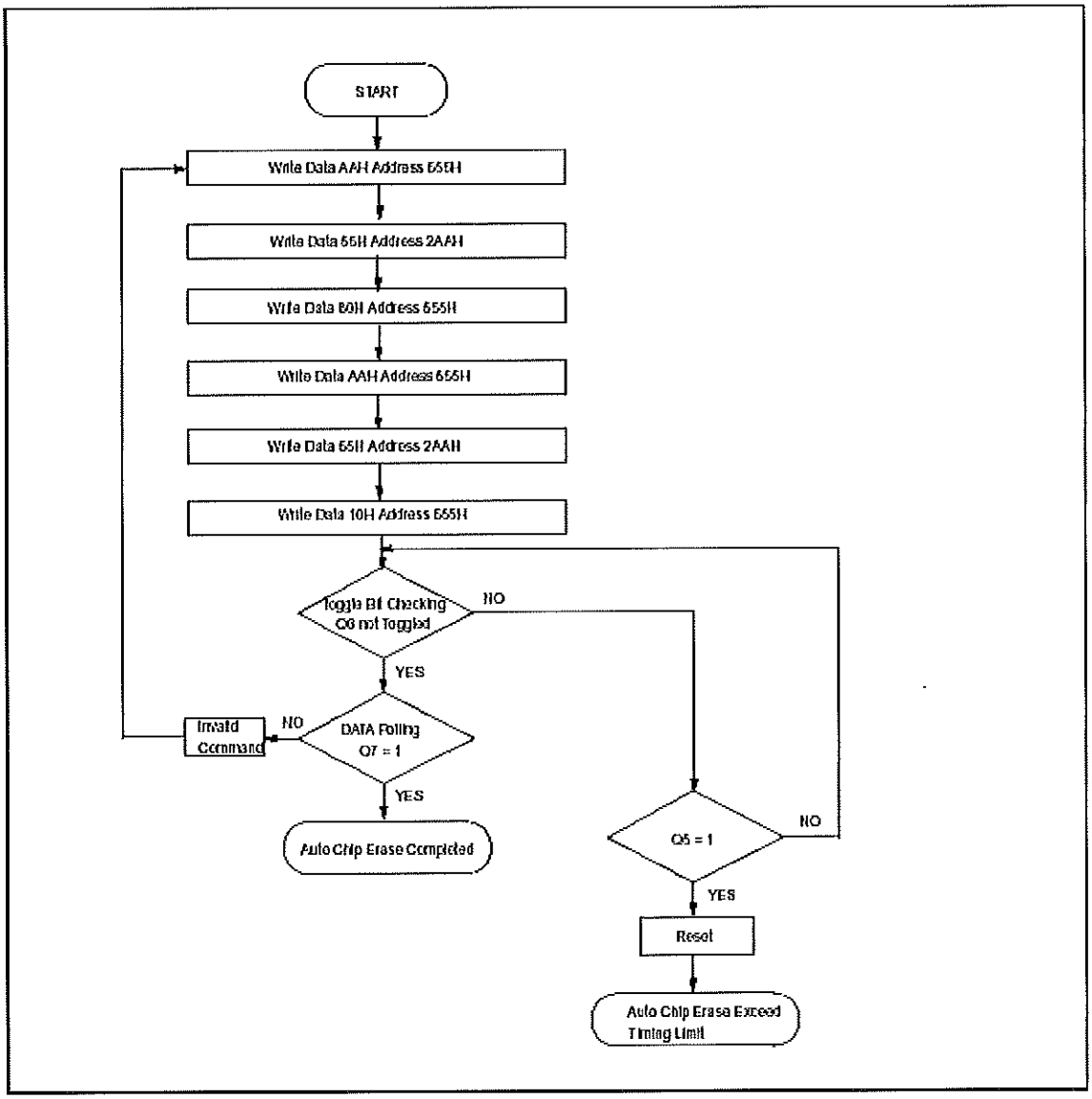

Figure 7

AUTOMATIC SECTOR ERASE TIMING WAVEFORM

Block data indicated by A16 to A20 are erased. External erase verify is not required because data are erased automatically by internal control circuit. Erasure completion can be verified by DATA polling and toggle bit checking after automatic erase starts. Device outputs 0 during erasure and 1 after erasure on Q7.(Q6 is for toggle bit; see toggle bit, DATA polling, timing waveform)

AUTOMATIC SECTOR ERASE TIMING WAVEFORM

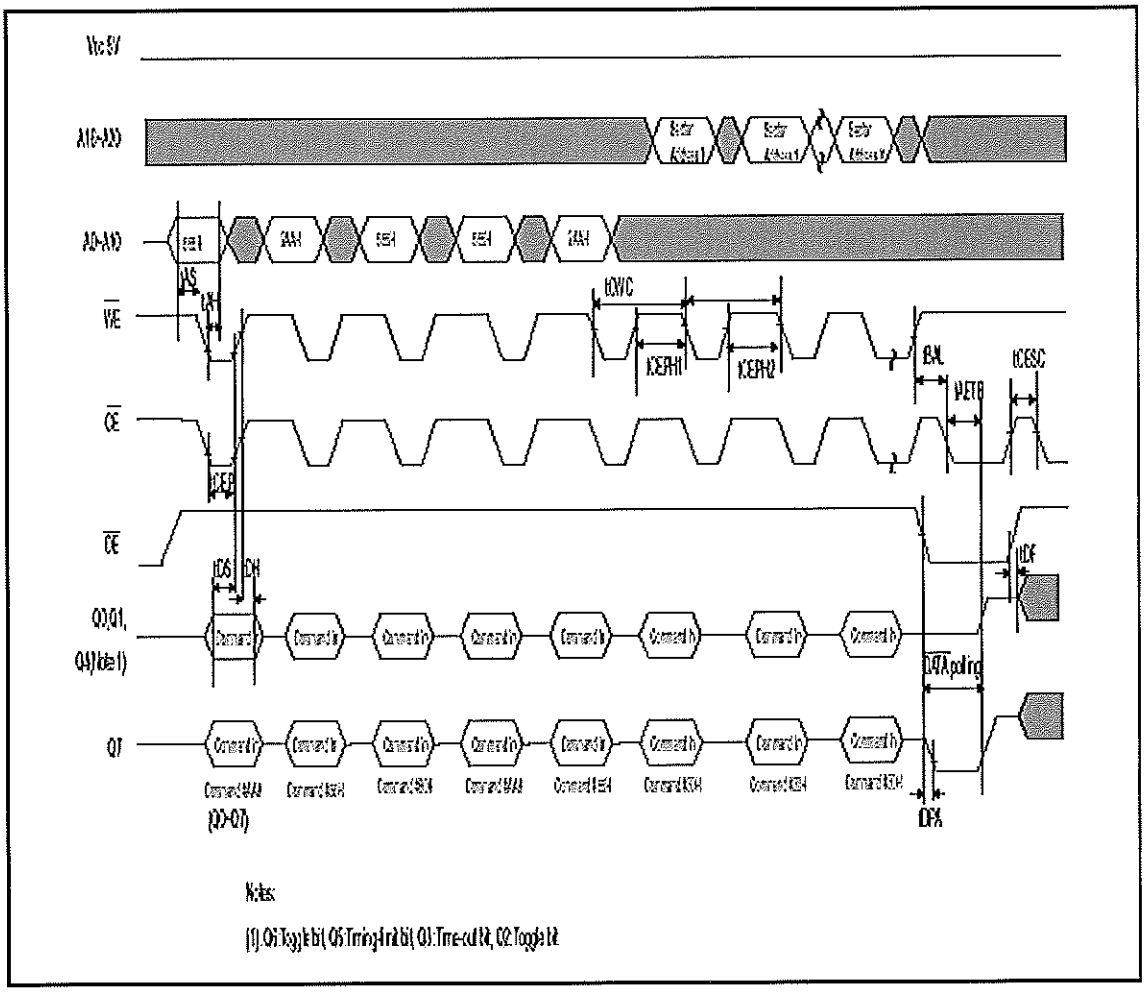

Figure 8

AUTOMATIC SECTOR ERASE ALGORITHM FLOWCHART

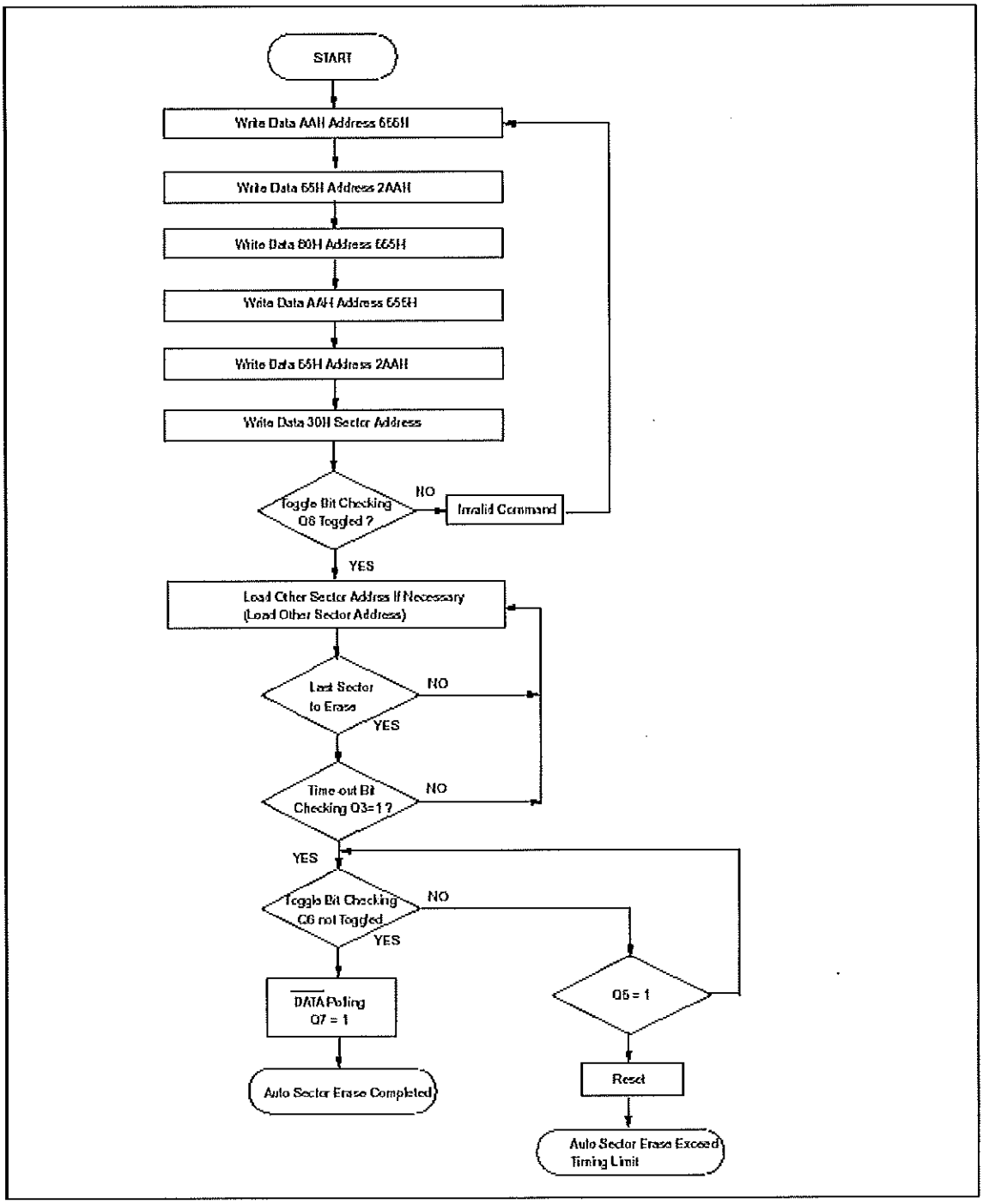

Figure 9

ERASE SUSPEND/ERASE RESUME FLOWCHART

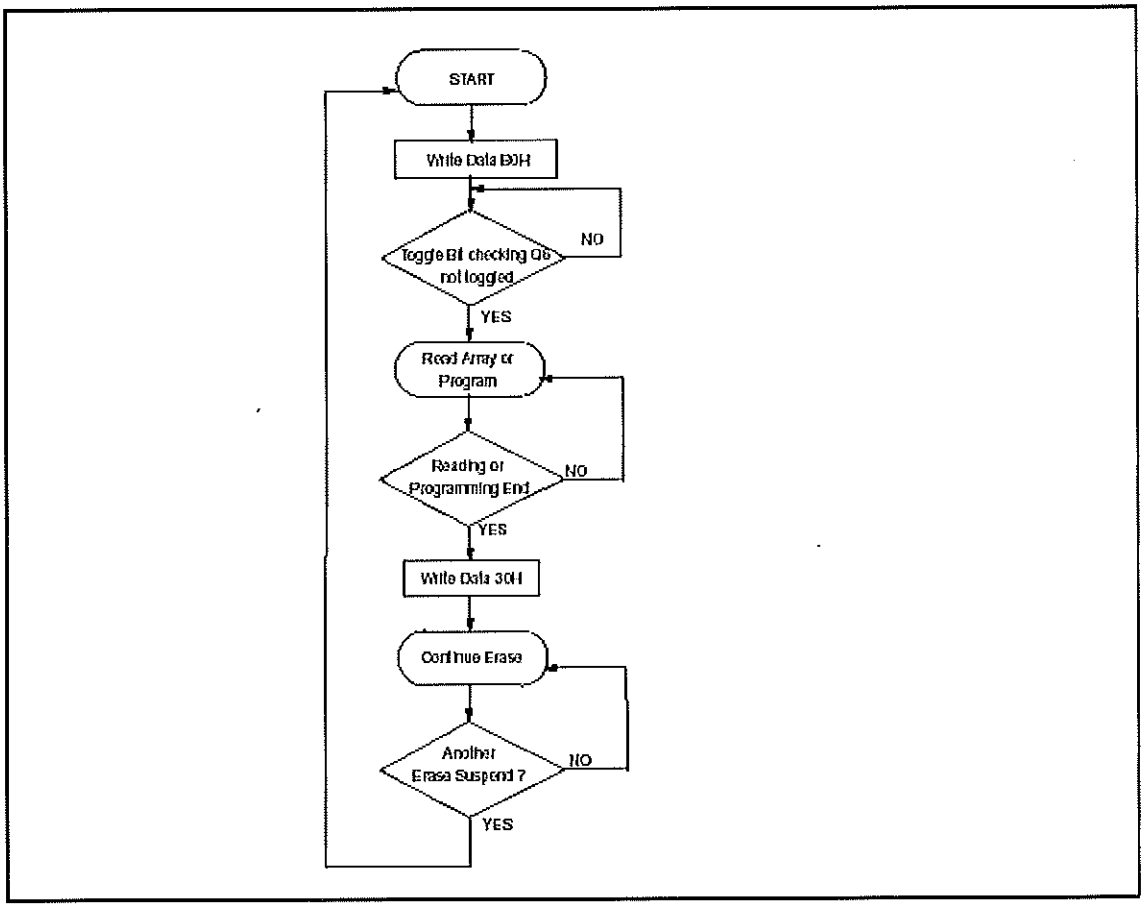

Figure 10

TIMING WAVEFORM FOR GROUP SECTOR PROTECTION FOR SYSTEM WITH 12V

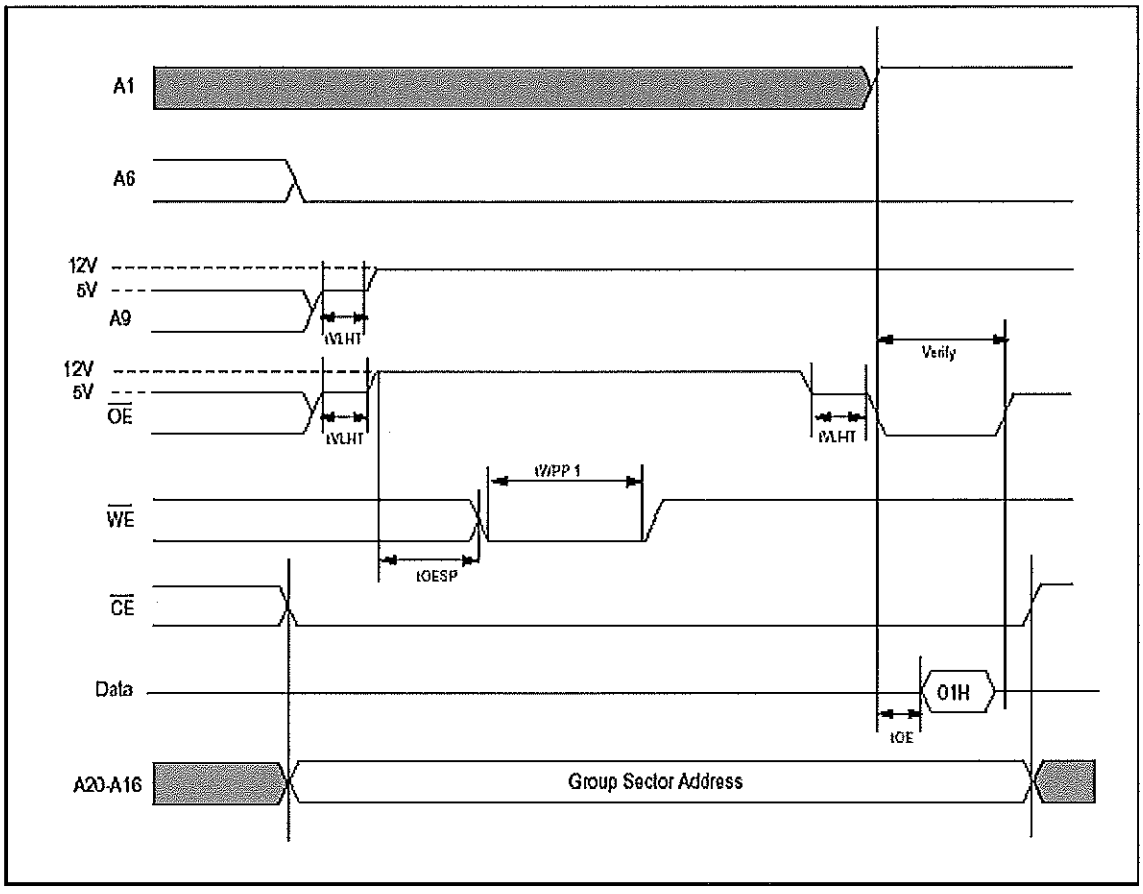

Figure 11

SECTOR GROUP PROTECTION ALGORITHM FOR SYSTEM WITH 12V

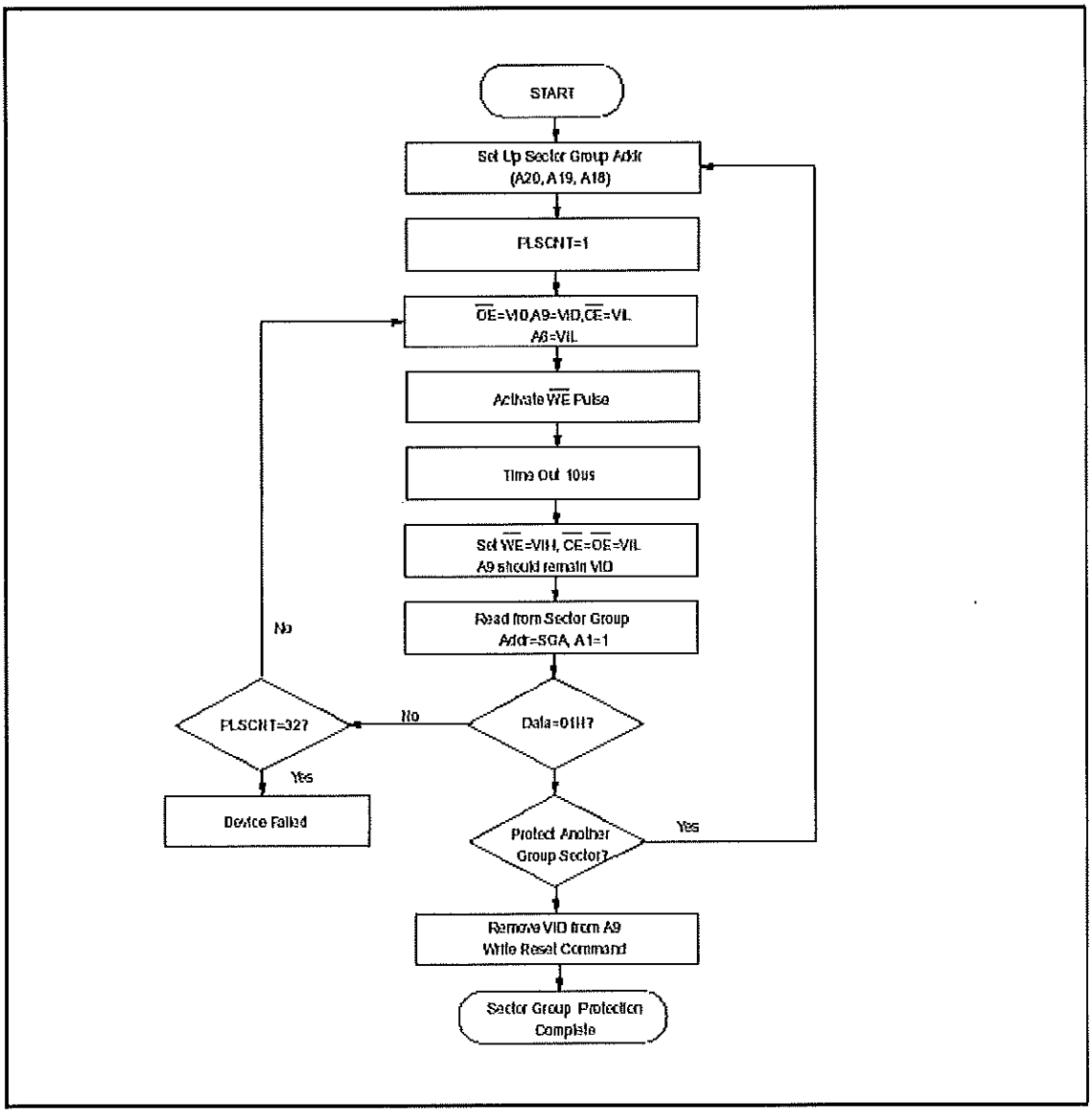

Figure 12

TIMING WAVEFORM FOR CHIP UNPROTECTION FOR SYSTEM WITH 12V

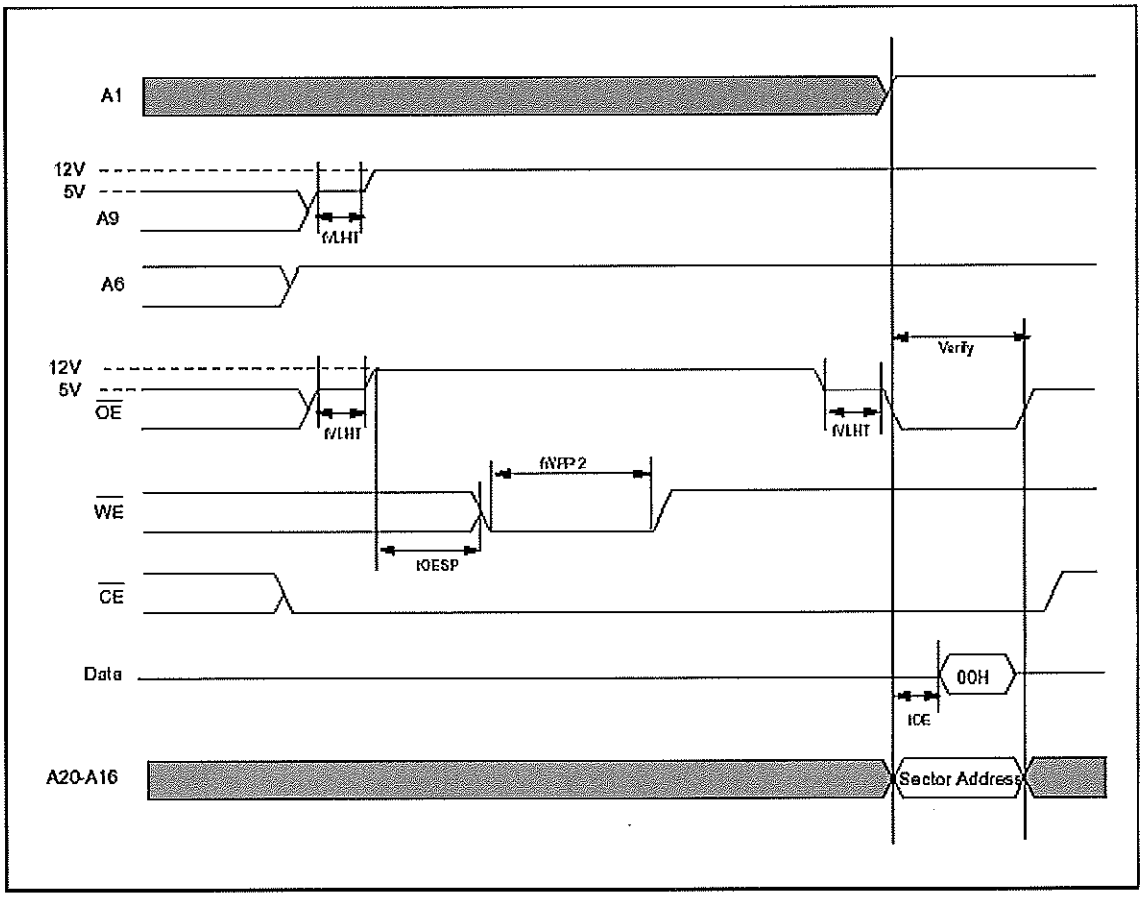

Figure 13

SECTOR GROUP PROTECTION ALGORITHM FOR SYSTEM WITH 12V

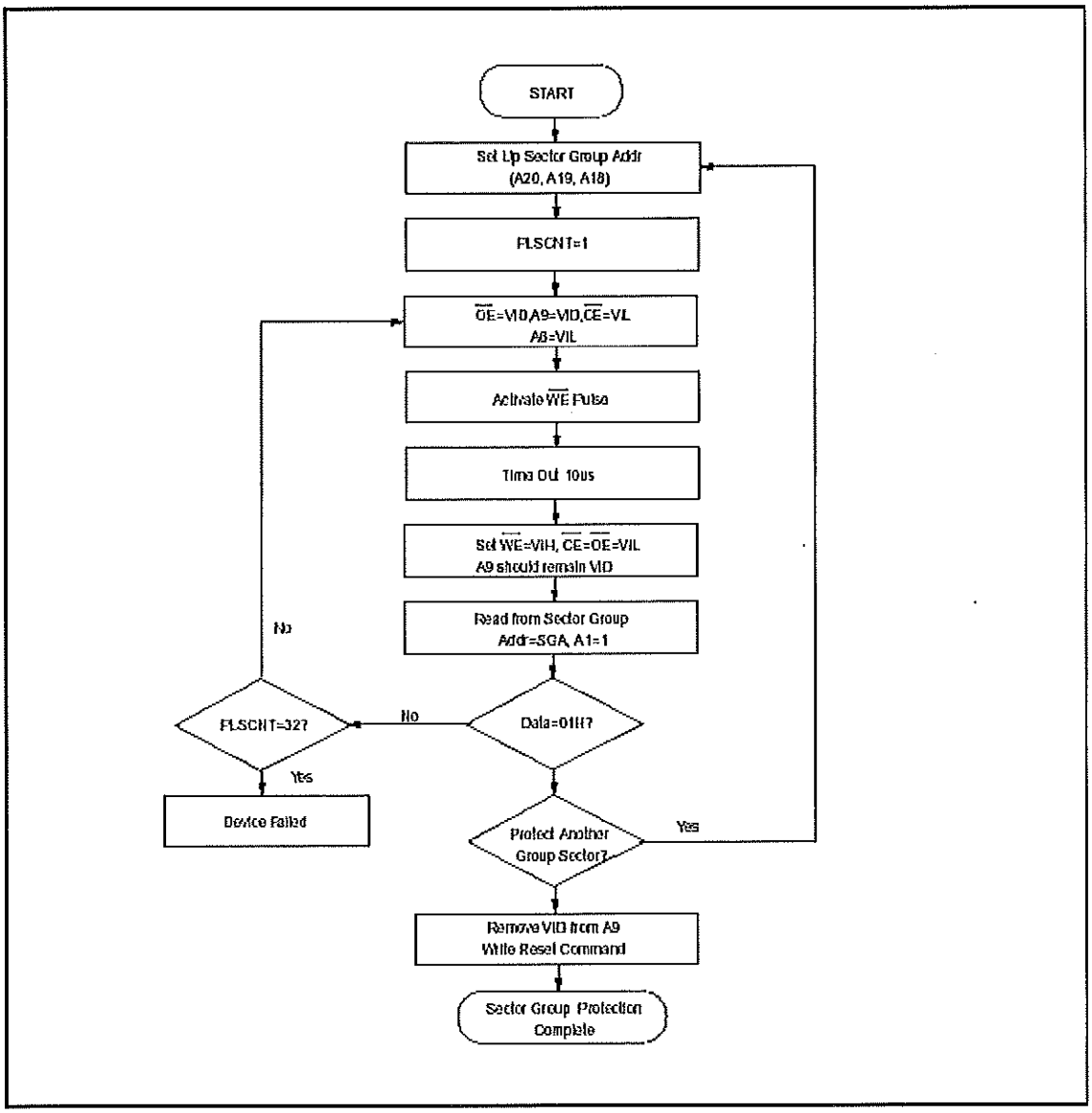

Figure 14

CHIP UNPROTECTION ALGORITHM FOR SYSTEM WITH 12V

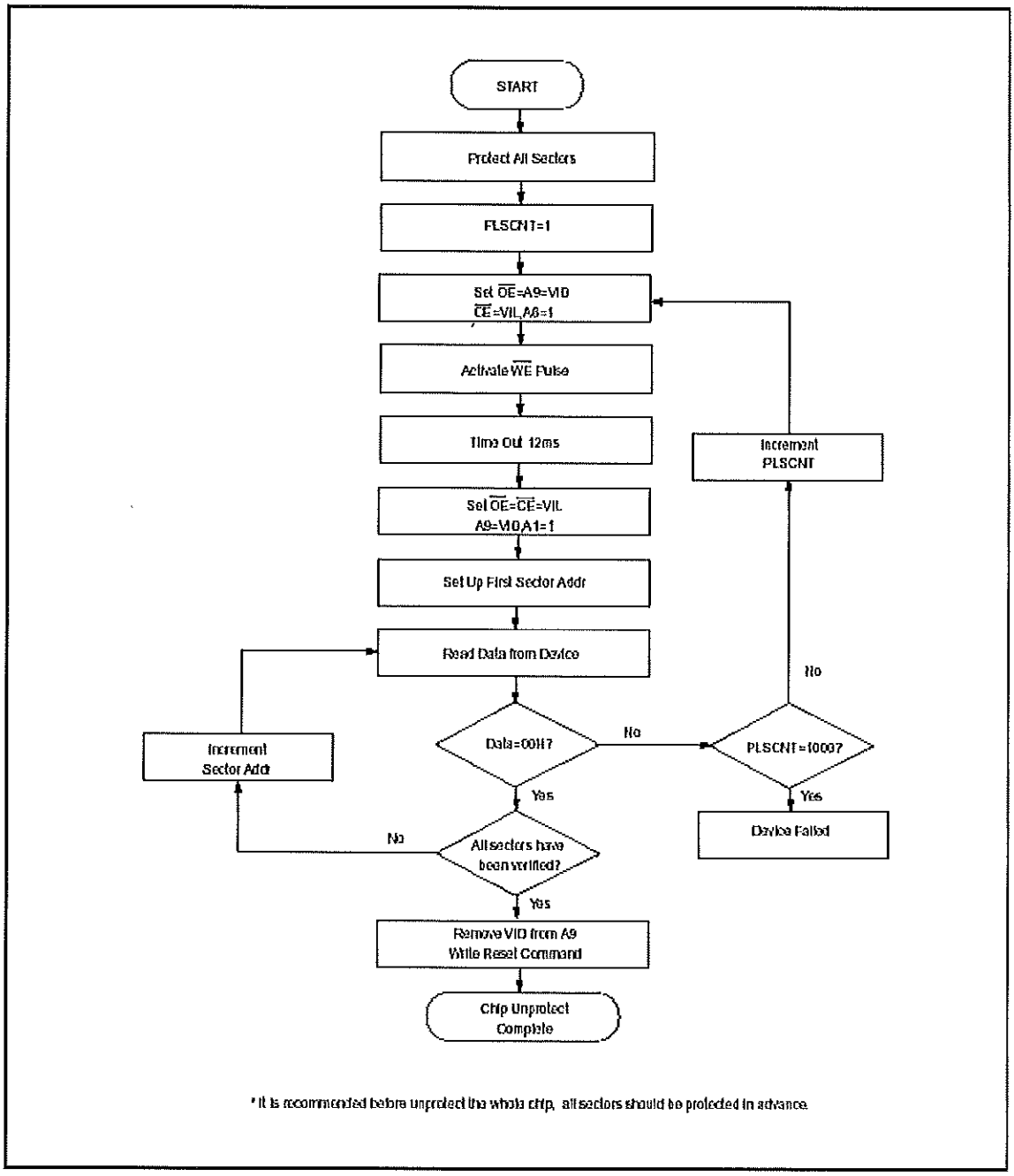

Figure 15

TEMPORARY SECTOR UNPROTECT ALGORITHM

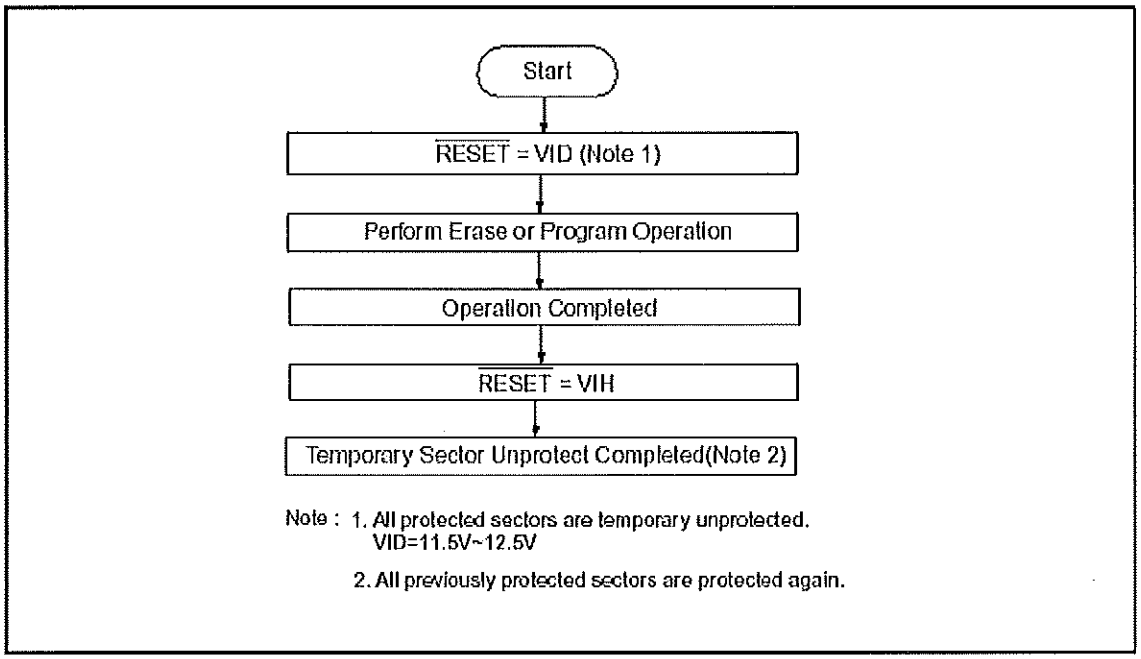

Figure 16

ID CODE READ TIMING WAVEFORM

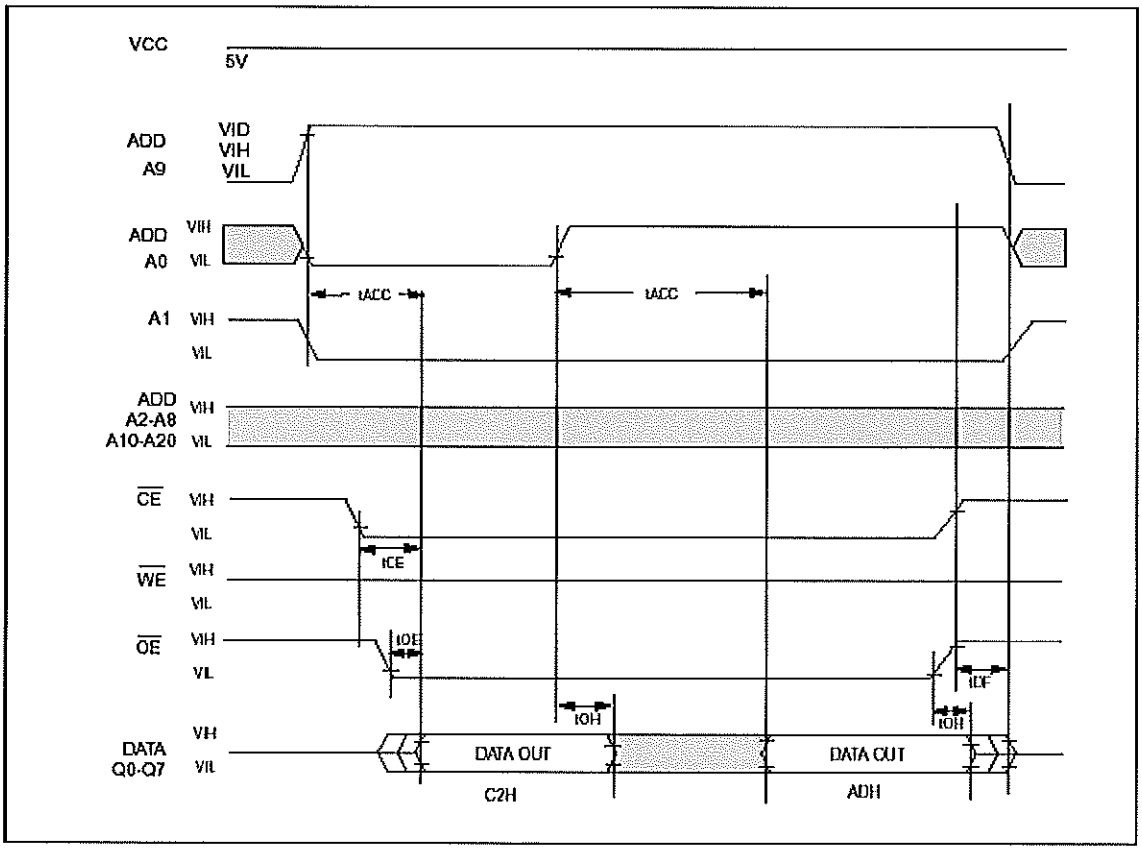

Figure 17

ERASE AND PROGRAMMING PERFORMANCE (1)

PARAMETER	LIMITS			UNITS
	MIN.	TYP.(2)	MAX. (3)	
Sector Erase Time		4	30	sec
Chip Erase Time		32	256	sec
Byte programming Time		7	300	sec
Chip Programming Time		15	45	sec
Erase/Program Cycles	100,000			Cycles

Table 13

Notes:

1. Not 100% Tested, Excludes external system level overhead.
2. Typical values measured at 25C, 4.5V.
3. Maximum values measured at 25C, 4.5V.

LATCH-UP CHARACTERISTICS

	MIN.	MAX.
Input Voltage with respect to GND on all pins except I/O pins	-1.0V	13.5V
Input Voltage with respect to GND on all I/O pins	-1.0V	Vcc+1.0V
Current	-10mA	+100mA
Includes all pins except Vcc=5.0V, one pin at a time.		

Table 14

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ORDERING INFORMATION

32MB08F-01 Rev M **Through Hole 40 Pin DIP**

32MB08F-02 Rev M **40 J-Lead Surface Mount Package**

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Document
Revision History

Revision No.	Description	Date
1.0	Initial Release	27 Oct 2005
2.0	Table data corrections were made.	9 Jan 2009