

# AS3560

## Class-G Stereo Headphone Amplifier

### 1 General Description

The AS3560 is a Class-G stereo headphone amplifier optimized for usage within portable devices. The Class-G supply rail adaptation is implemented by an integrated DCDC buck converter that takes its input directly from the battery. The continuous adoption of supply rails is done according to the input signal swing and load conditions. This architecture implements significant power savings compared to traditional Class-AB amplifiers.

An I2C control interface is implemented for a 32-step volume control including a mute function for each channel separately.

The integrated charge pump generates a symmetric negative supply for true ground output signal levels without the need of output coupling capacitors. In addition it helps to lower the overall pop noise of the amplifier.

A supervisory circuit is included for overtemperature and short-circuit protection.

Differential inputs together with output ground sensing guarantees very low noise sensitivity.

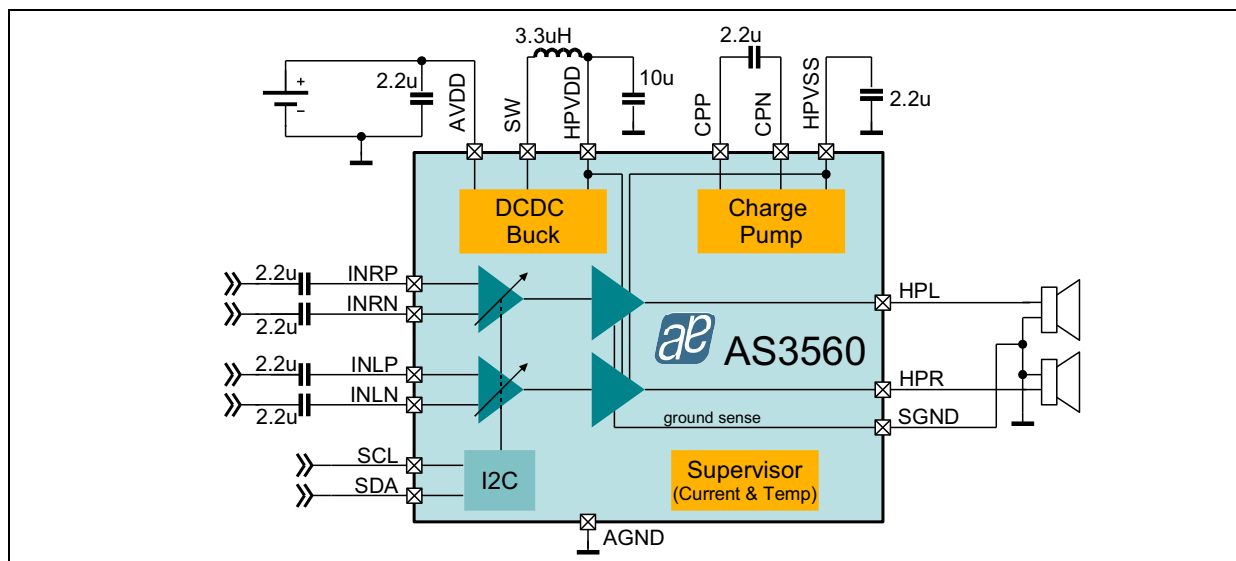
### 2 Key Features

- G-Class amplifier with integrated DCDC buck converter
  - 2x30mW, 0.02% THD @16Ω
  - >100dB SNR @0.9V<sub>rms</sub>
- Popless startup and mute/unmute feature
- Charge pump for true ground output without coupling capacitors
- Direct battery connection with wide supply range: 2.3V to 5.5V
- Low power consumption optimized for battery operation
  - 1 mA quiescent current with both channels enabled
  - <5 μA shutdown current
- Fully Differential Inputs reduce system noise
  - Also configurable as Single-Ended Inputs
- SGND pin for ground sensing and ground feedback minimizes sensitivity to interference
- I2C control interface
  - volume control with 32 gain steps, -59 to +4dB, <-80dB mute
  - Channel independent enable control
- Current and Temperature Supervisor
- Package: 0.4 mm Pitch WL-CSP (1.615x1.615mm)

### 3 Applications

- Mobile Phones
- Portable Navigation Devices, Media Devices
- Media Devices

Figure 1. AS3560 Block Diagram

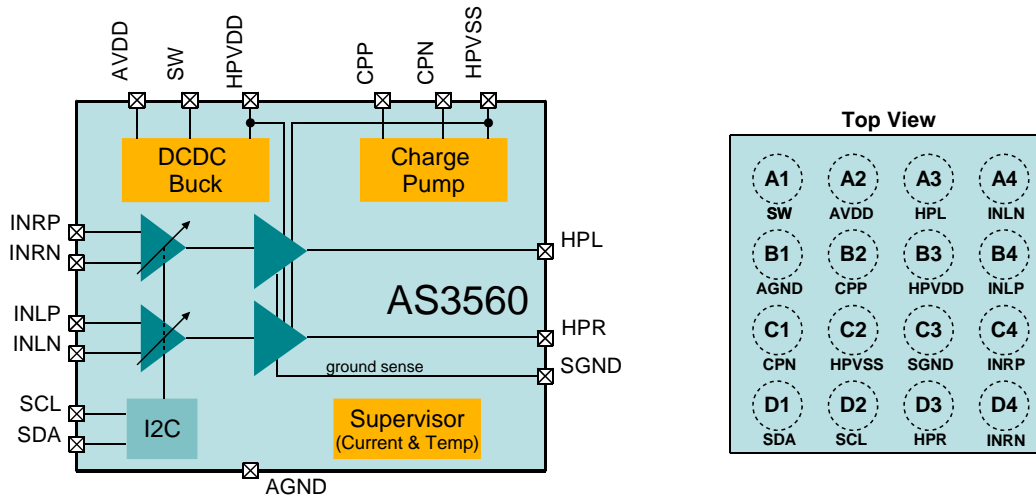


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## 4 Pin Assignments

Figure 2. Pin Assignments (Top View)



### 4.1 Pin Descriptions

Table 1. Pin Descriptions

Pin Name	Pin Number	Description
SW	A1	Buck converter switching node
AVDD	A2	Primary power supply for device
HPL	A3	Left channel headphone amplifier output
INLN	A4	Inverting left input for differential signals; connect to left input signal through 2.2 $\mu$ F capacitor for single-ended input applications
AGND	B1	Main Ground for headphone amplifiers, DC/DC converter, and charge pump
CPP	B2	Charge pump positive flying cap; connect to 2.2 $\mu$ F flying capacitor
HPVDD	B3	Power supply for headphone amplifier (DC/DC output node)
INLP	B4	Non-inverting left input for differential signals; connect to ground through 2.2 $\mu$ F capacitor for single-ended input applications
CPN	C1	Charge pump negative flying cap; connect to 2.2 $\mu$ F flying capacitor
HPVSS	C2	Charge pump output; connect 2.2 $\mu$ F capacitor to GND
SGND	C3	Ground sense; connect to headphone jack ground
INRP	C4	Non-Inverting right input for differential signals; connect to right input signal through 2.2 $\mu$ F capacitor for single-ended input applications
SDA	D1	I <sup>2</sup> C Data; 1.8V logic compliant
SCL	D2	I <sup>2</sup> C Clock; 1.8V logic compliant
HPR	D3	Right channel headphone amplifier output
INRN	D4	Inverting right input for differential signals; connect to ground through 2.2 $\mu$ F capacitor for single-ended input applications

## 5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Operating Conditions on page 5 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
Supply voltage, AVDD	-0.3	7	V	for 1 ms peaks
Amplifier supply voltage, HPVDD	-0.3	2.0	V	
SGND	-0.3	0.3	V	
Differential Input voltage	HPVSS -0.3V	HPVDD +0.3V	V	
Input voltage at SCL, SDA	-0.3	7.0	V	
Breakdown voltage at amplifier outputs	HPVSS -0.5	HPVDD +0.5	V	
Input current (latchup immunity)		±200	mA	Norm: JEDEC 78
<b>Continuous Power Dissipation</b>				
Continuous power dissipation		TBD	mW	$P_T^1$
Continuous power dissipation derating factor		TBD	mW/°C	$P_{DERATE}^2$
<b>Electrostatic Discharge</b>				
ESD HBM		±2	KV	Norm: MIL 883 E Method 3015
ESD MM		±100	V	Norm: JEDEC JESD 22-A115-A level A
ESD CDM		±500	V	Norm: JEDEC JESD 22-C101C
<b>Temperature Range and Storage Conditions</b>				
Junction Temperature		+150	°C	internally limited (overtemperature protection) auto shutdown at 140 °C
Storage Temperature Range	-55	+125	°C	
Package Body Temperature		+260	°C	The reflow peak soldering temperature (body temperature) specified is in accordance with IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".
Humidity non-condensing	5	85	%	
Moisture Sensitive Level		1		Represents a max. floor life time of unlimited

1. Depending on actual PCB layout and PCB used
2.  $P_{DERATE}$  derating factor changes the total continuous power dissipation ( $P_T$ ) if the ambient temperature is not 70 °C.  
Therefore for e.g.  $T_{AMB}=85\text{ }^{\circ}\text{C}$  calculate  $P_T$  at 85°C =  $P_T - P_{DERATE} * (85\text{ }^{\circ}\text{C} - 70\text{ }^{\circ}\text{C})$

## 6 Electrical Characteristics

AVDD=3.6V, T<sub>A</sub>=25 °C, R<sub>load</sub> = 32 Ω unless otherwise specified.

Table 3. Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>General Operating Conditions</b>						
AVDD	Supply Voltage		2.3		5.5	V
	Rail Voltages HPVDD, HPVSS (Buck and CP output)		0.8	0.9	1.0	V
			1.15	1.25	1.35	V
			1.7	1.8	1.9	V
I <sub>DD</sub>	Quiescent Current	both channels enabled, no audio signal		1.1	1.5	mA
I <sub>SD</sub>	Shutdown Current	SW shutdown		1	5	µA
I <sub>S</sub>	Supply Current	Output: 2x100µW @ 3dB Crest Factor		2.0	3.5	mA
		Output: 2x500µW @ 3dB Crest Factor		3.1	5.5	mA
		Output: 2x1mW @ 3dB Crest Factor		4.0	7.5	mA
T <sub>A</sub>	Operating Temperature Range		-30	25	+85	°C
t <sub>WAKEUP</sub>	Wakeup Time			10	15	ms
<b>Input Interfaces</b>						
V <sub>IL</sub>	Low-level input voltage (SCL, SDA)	AVDD 2.9V to 4.5V			0.6	V
V <sub>IH</sub>	High-level input voltage (SCL, SDA)	AVDD 2.9V to 4.5V	1.2			V
V <sub>HYST</sub>	Hysteresis (SCL, SDA)		50	100	200	mV
Z <sub>IN</sub>	Input Impedance Line Inputs	Differential	20			kΩ
		Single Ended	10			kΩ
<b>HPA Output</b>						
V <sub>OUT</sub>	Output Voltage	R <sub>load</sub> =16Ω, THD+N=1%, L+R out of phase	0.7			V <sub>rms</sub>
		R <sub>load</sub> =32Ω, THD+N=1%, L+R in phase	0.9			V <sub>rms</sub>
	Output DC Offset	Both channels enabled			500	µV
Z <sub>OUT</sub>	Output Impedance	In HiZ mode <40 KHz		10		kΩ
		In HiZ mode 6 MHz		500		Ω
		In HiZ mode 36 MHz		75		Ω
	Voltage applied to Output; HPR, HPL	when SWS = 0, HiZ_L = HiZ_R = 1, device in Hi-Z mode	-1.8		1.8	V
C <sub>LOAD</sub>	Capacitive Load	ext. cap, 15Ω series resistor	0.8	5	100	nF
		ext cap, directly connected			100	pF
Z <sub>OUT,SD</sub>	Output impedance in shutdown	SWS = 1		8		kΩ
	Voltage applied to Output; HPR, HPL	when SWS = 1, device disabled	-0.3		3.6	V
<b>Audio Parameters</b>						
THD+N	Total Harmonic Distortion + Noise	700mV <sub>rms</sub> , 1KHz		0.01	0.02	%
PSRR	Power Supply Rejection Ratio	Gain 0dB @217 Hz		90		dB
SNR	Signal-to-Noise Ratio	900mV <sub>rms</sub> , 1KHz		104		dB
	Channel Separation	>16Ω (Headset)		60		dB
		>10kΩ (Lineout)		80		dB

Table 3. Operating Conditions (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_N$	Output Noise	Gain 0dB, A-weighted		5.3	9	$\mu V_{rms}$
<b>Other Parameters</b>						
	Thermal Shutdown	Threshold		140		°C
		Hysteresis		20		

## 7 Detailed Operating Characteristics

$T_A = 25^\circ\text{C}$ ,  $AV_{DD} (V_{DD}) = 3.6\text{ V}$ ,  $GAIN = 0\text{ dB}$ ,  $C_{HPVDD} = 10\text{ }\mu\text{F}$ ,  $C_{HPVSS} = 2.2\text{ }\mu\text{F}$ ,  $C_{INPUT} = C_{FLYING} = 2.2\text{ }\mu\text{F}$ ,  $R_L = 32\text{ }\Omega$  unless otherwise specified.

Figure 3. THD+N versus output power for  $AV_{DD}=2.5\text{ V}$ ,  $R_L=32\text{ }\Omega$

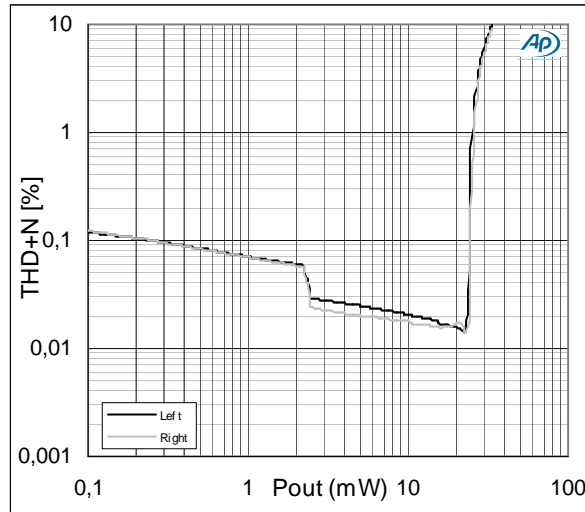


Figure 4. THD+N versus output power for  $AV_{DD}2.5\text{ V}$ ,  $R_L=16\text{ }\Omega$

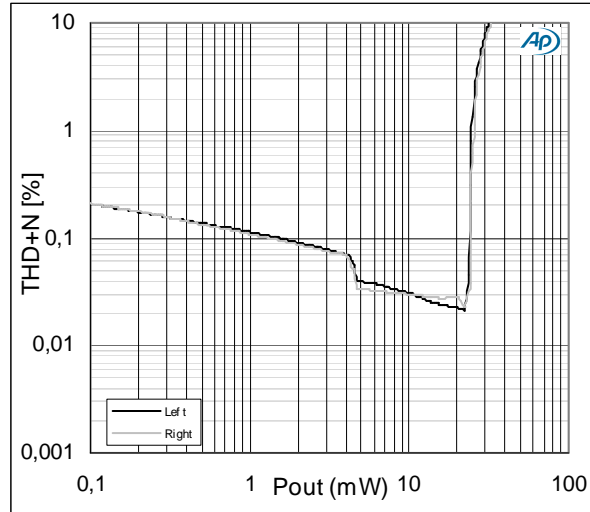


Figure 5. THD+N versus output power for  $AV_{DD}=3.6\text{ V}$ ,  $R_L=32\text{ }\Omega$

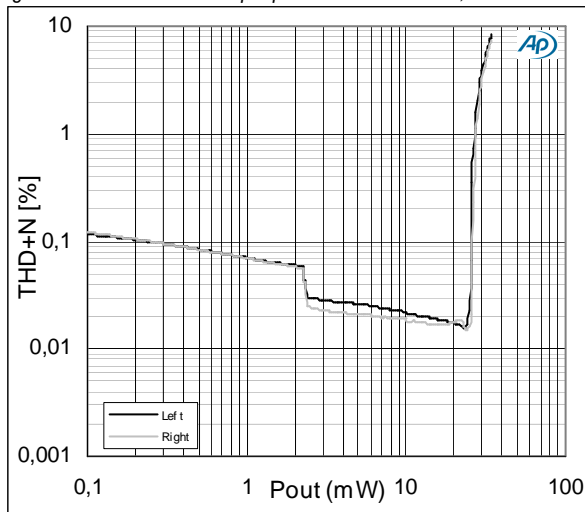


Figure 6. THD+N versus output power for  $AV_{DD}=3.6\text{ V}$ ,  $R_L=16\text{ }\Omega$

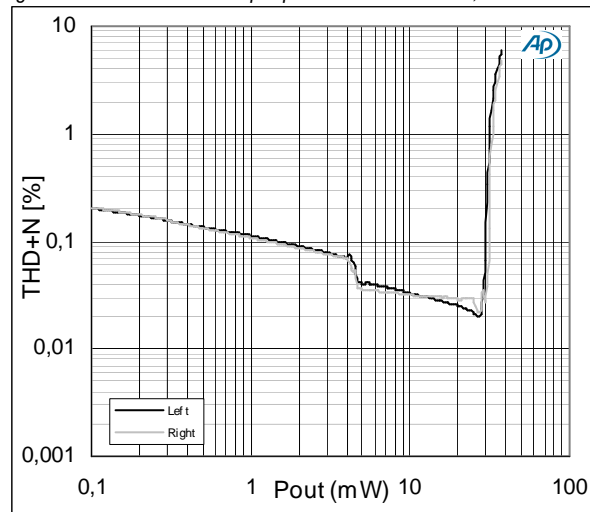


Figure 7. THD+N versus output power for  $AV_{DD}=5.5\text{ V}$ ,  $R_L=32\text{ }\Omega$

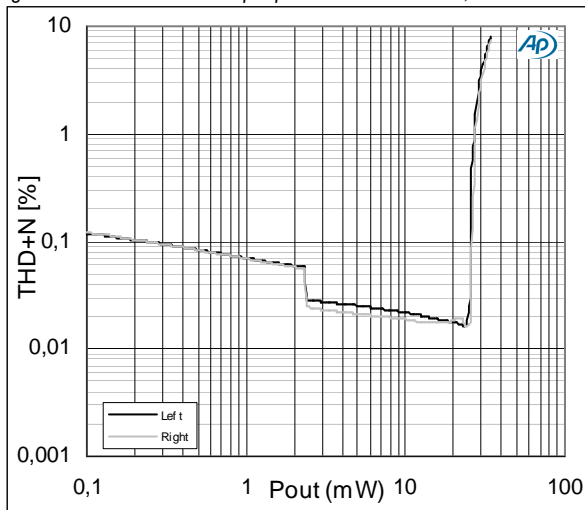


Figure 8. THD+N versus output power for  $AV_{DD}=5.5\text{ V}$ ,  $R_L=16\text{ }\Omega$

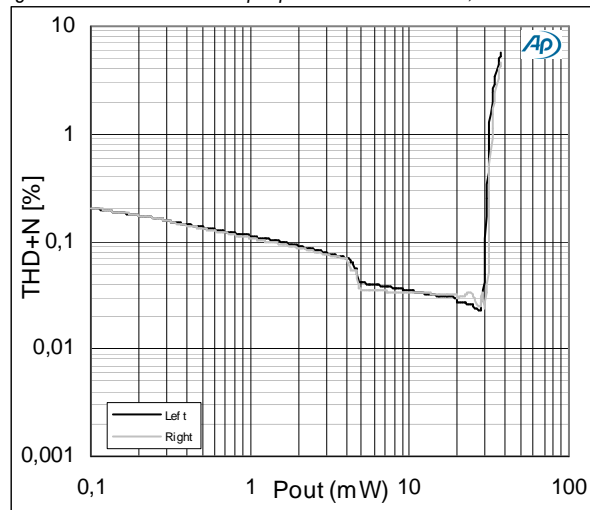


Figure 9. THD+N versus frequency for AVDD=2.5V, RL=32 Ω

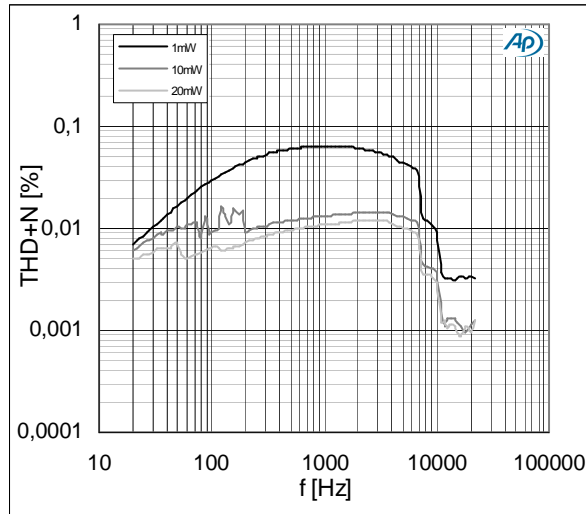


Figure 10. THD+N versus frequency for AVDD=2.5V, RL=16 Ω

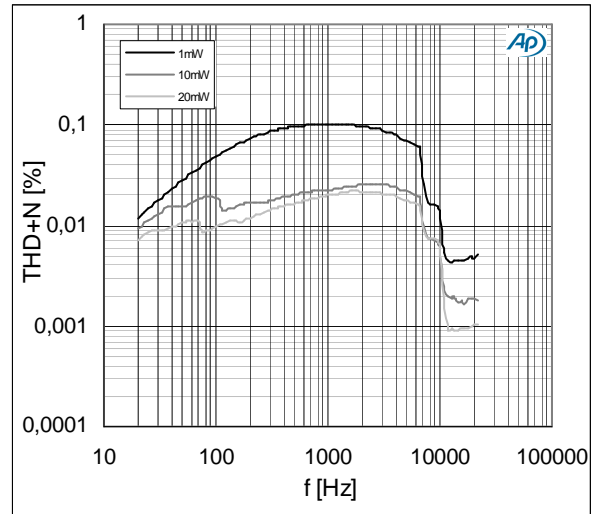


Figure 11. THD+N versus frequency for AVDD=3.6V, RL=32 Ω

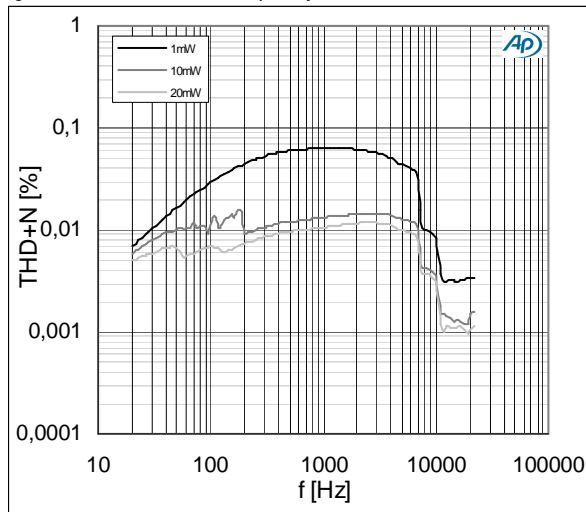


Figure 12. THD+N versus frequency for AVDD=3.6V, RL=16 Ω

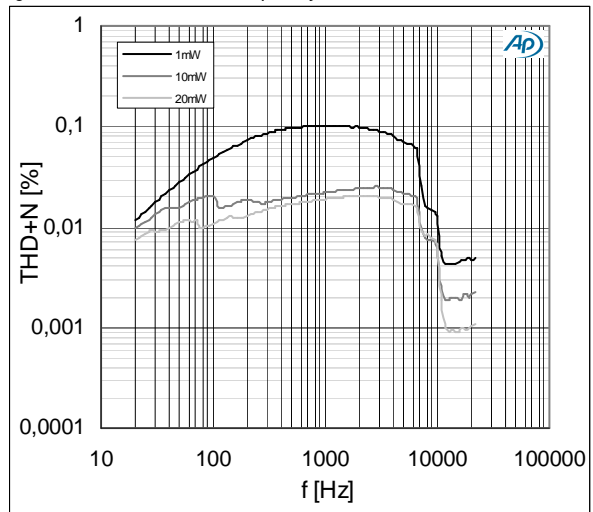


Figure 13. THD+N versus output power for AVDD=5.5V, RL=32 Ω

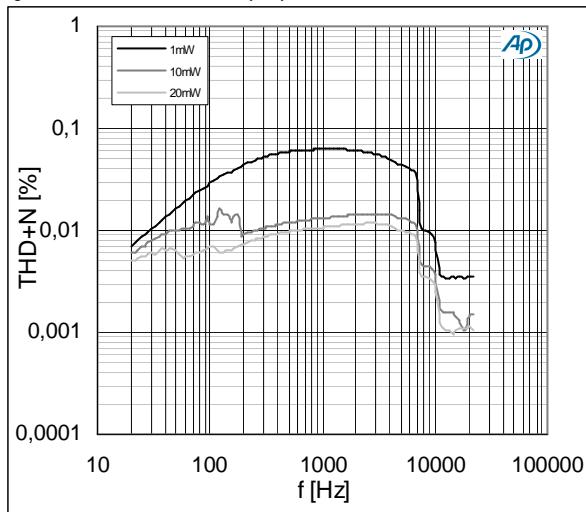


Figure 14. THD+N versus output power for AVDD=5.5V, RL=16 Ω

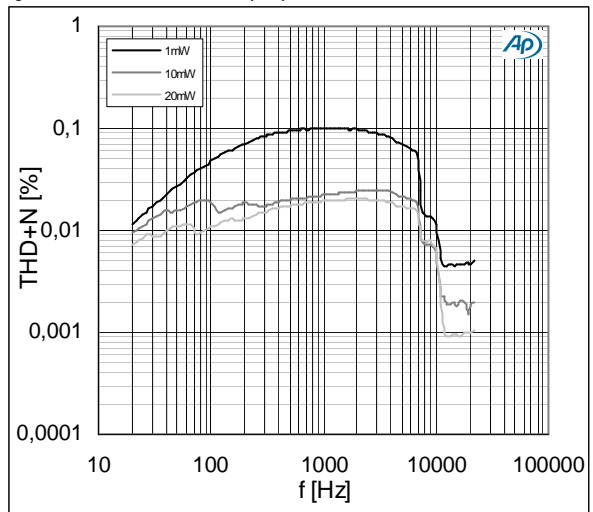




Figure 15. Supply Current versus POUT for AVDD=2.5V (POut is the output power per channel)

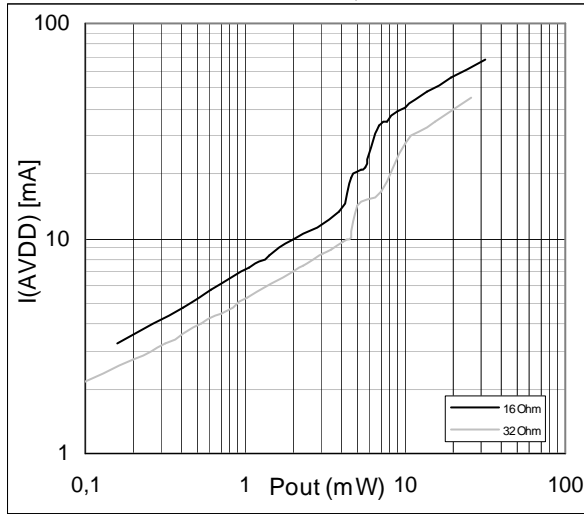


Figure 16. Total Power Consumption vs. POUT for AVDD=2.5V (POut is the output power per channel)

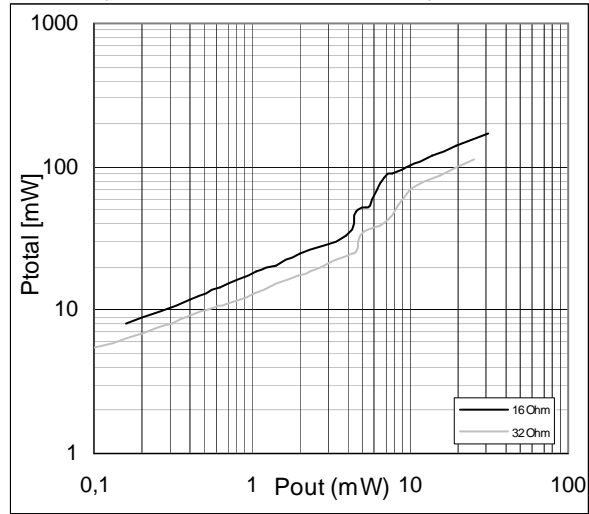


Figure 17. Supply Current versus POUT for AVDD=3.6V (POut is the output power per channel)

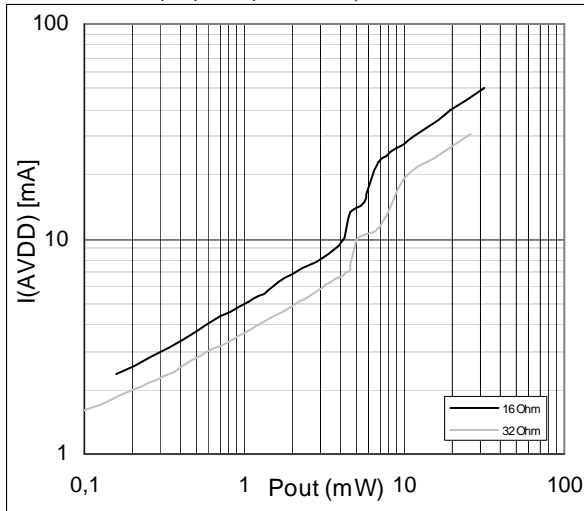


Figure 18. Total Power Consumption vs. POUT for AVDD=3.6V (POut is the output power per channel)

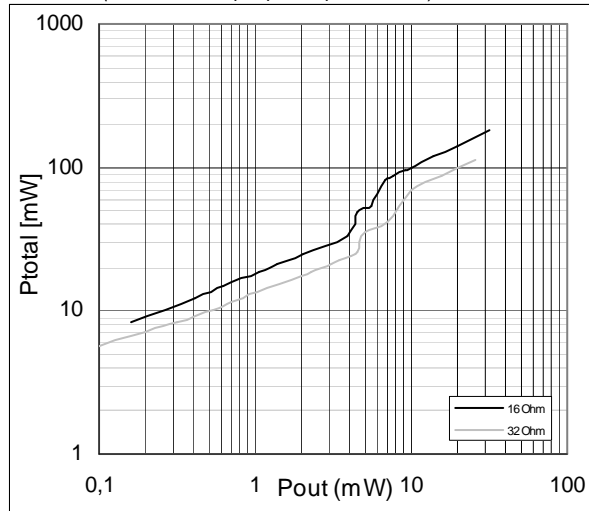


Figure 19. Supply Current versus POUT for AVDD=5.5V (POut is the output power per channel)

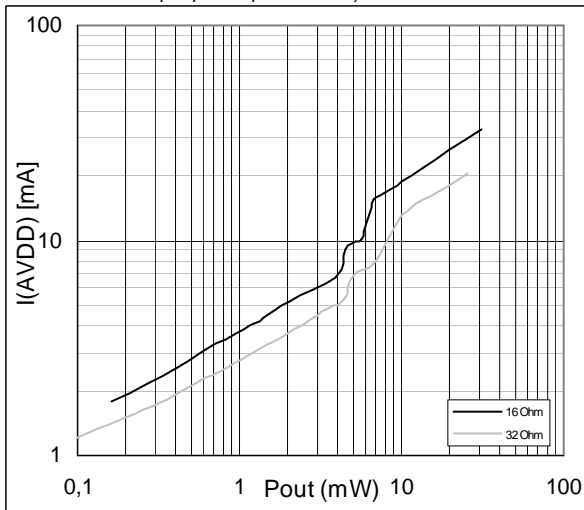


Figure 20. Total Power Consumption vs. POUT for AVDD=5.5V (POut is the output power per channel)

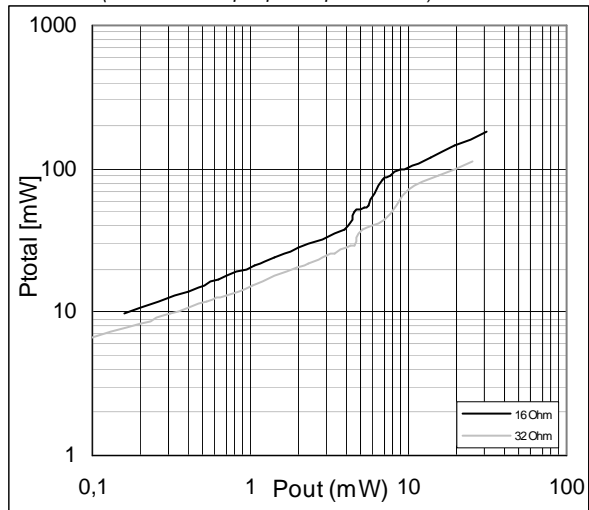


Figure 21. Quiescent Current Consumption versus AVDD

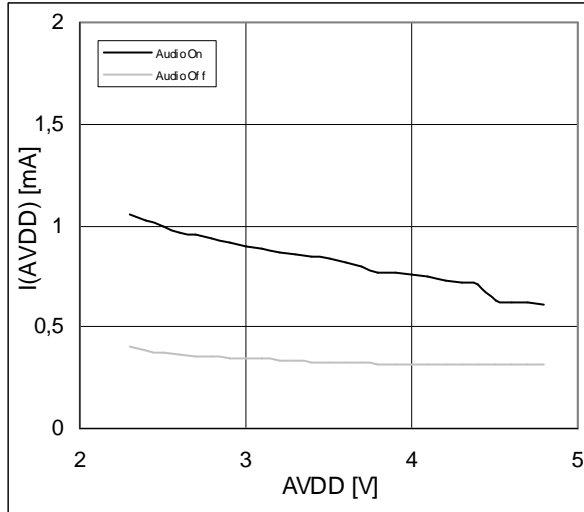


Figure 22. PSRR versus Frequency (200mVpp supply ripple)

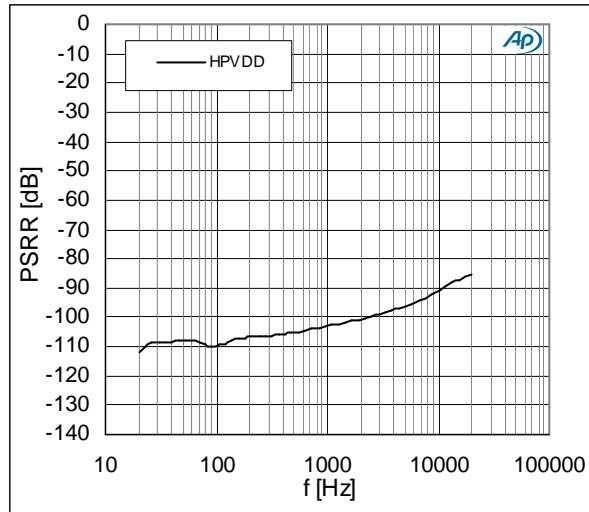


Figure 23. Crosstalk versus Frequency (700mVrms, RL= 32 Ω)

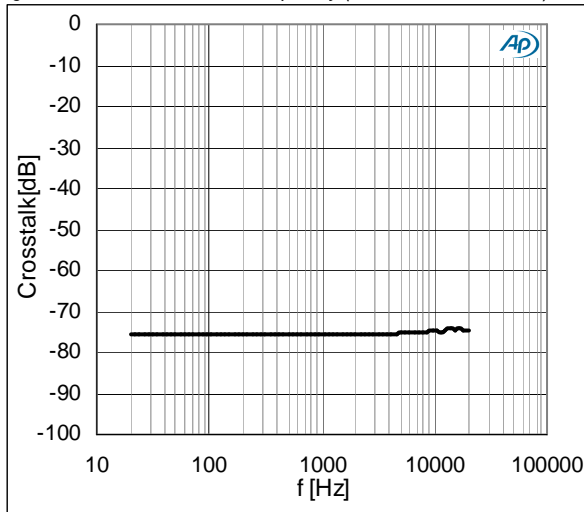


Figure 24. Startup Pop Noise for AVDD=3.6V, RL=16 Ω

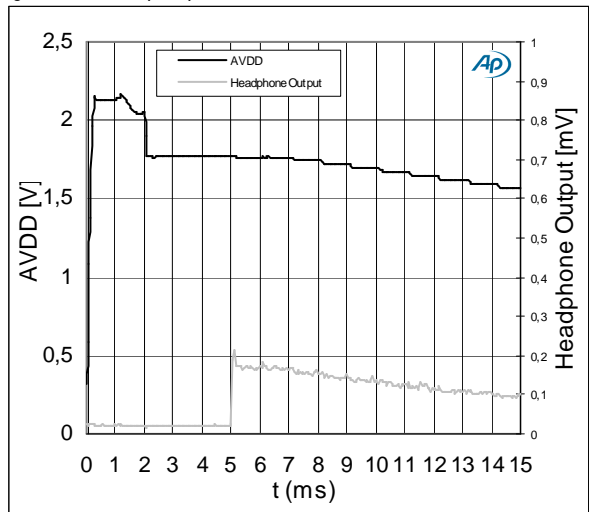
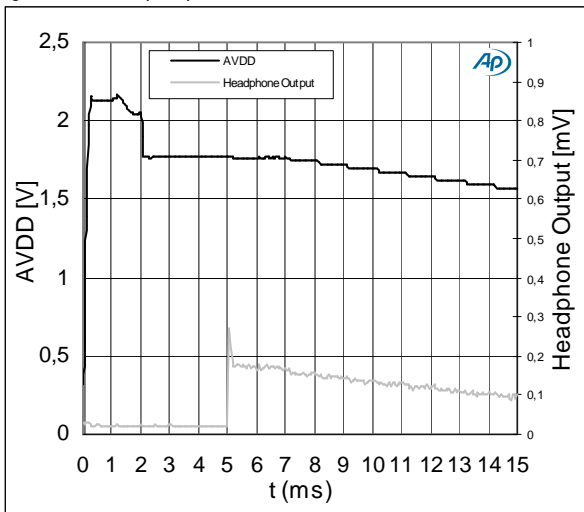


Figure 25. Startup Pop Noise for AVDD=3.6V, RL=32 Ω



## 8 Detailed Description

### 8.1 I2C Control Interface

An I2C slave interface is implemented for read/write access of the internal registers. SCL is the corresponding clock input pin and SDA the data input pin.

Access is done in 7-bit addressing mode, addresses for read and write are defined by

C0h = 11000000b ... write

C1h = 11000001b ... read

Figure 26. I2C block diagram

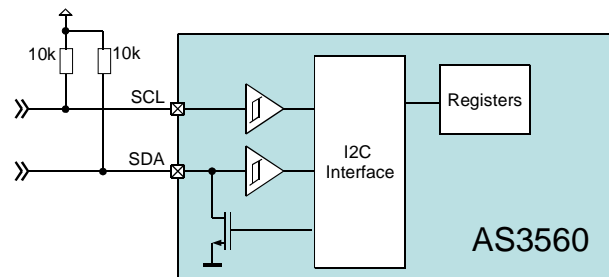


Figure 27. I2C Timing Definition

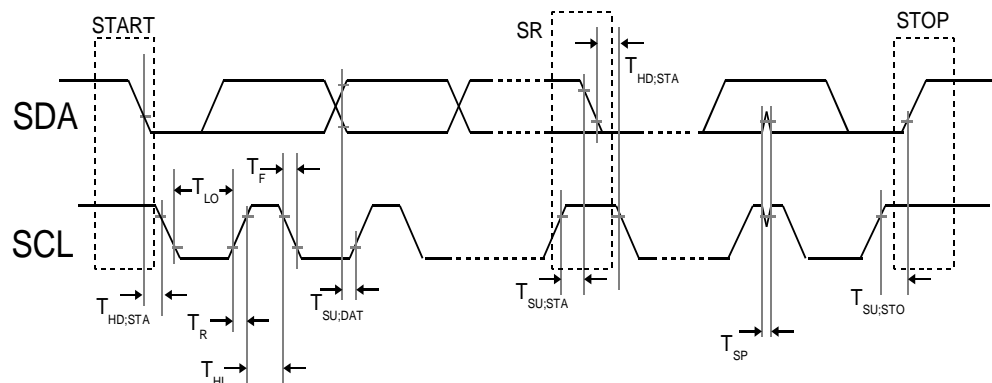


Table 4. I2C Timing Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$T_{SP}$	Spike Insensitivity		50	100		ns
$T_{HI}$	High Clock Time	400 KHz clock speed	330			ns
$T_{LO}$	Low Clock Time		660			ns
$T_{SU}$		SDA has to change Tsetup before rising edge of SCLK	30			ns
$T_{HD}$		no hold time needed for SDA relative to rising edge of CSCL	-40			ns
$T_{HD;STA}$	Within start condition, after low going SDA, SCL has to stay constant for the specified hold time		300			ns
$T_{SU;STO}$	After high going edge of SCL, SDA has to stay constant for the specified setup time before STOP or repeated start condition is applied		100			ns
$T_{SU;STA}$			100			ns

## 9 Register Definition

### 9.1 Register Overview

Register	Description
ENABLE Register (1h)	General control register to switch on/off the device and enable the headphone amplifier stages.
Volume Register (2h)	Allows the use to configure the output volume of the headphone amplifier from -59dB up to +4dB.
HiZ Register (3h)	Configures the headphone amplifier for a high impedance output for power optimization.
Info Register (4h)	This register contains general information like IC version number and supplier information.

### 9.2 Detailed Register Descriptions

Table 5. ENABLE Register (1h)

Bit	Bit Name	Default	Access	Bit Description
Bit 7	HP_EN_L	0	RW	0 ... Disable Headphone Left; 1 ... Enable Headphone Left Channel
Bit 6	HP_EN_R	0	RW	0 ... Disable Headphone Right; 1 ... Enable Headphone Right Channel
Bit 5	-	-	-	-
Bit 4	-	-	-	-
Bit 3	-	-	-	-
Bit 2	-	-	-	-
Bit 1	Thermal	0	S_RC	0 ... Normal Operation; 1 ... Thermal Shutown
Bit 0	SWS	1	RW	0 ... Normal Operation; 1 ... Software ShutDown

Table 6. Volume Register (2h)

Bit	Bit Name	Default	Access	Bit Description
Bit 7	Mute_L	1	RW	0 ... Unmuted Left Channel; 1 ... Mute Left Channel
Bit 6	Mute_R	1	RW	0 ... Unmuted Right Channel; 1 ... Mute Right Channel
Bit[5:1]	Vol[ 4:0]	0	RW	0d ... -59 dB; 1d ... -55 dB; 2d ... -51 dB; 3d ... -47 dB; 4d ... -43 dB; 5d ... -39 dB; 6d ... -35 dB; 7d ... -31 dB; 8d ... -27 dB; 9d ... -25 dB; 10d ... -23 dB; 11d ... -21 dB; 12d ... -19 dB; 13d ... -17 dB; 14d ... -15 dB; 15d ... -13 dB; 16d ... -11 dB; 17d ... -10 dB; 18d ... -9 dB; 19d ... -8 dB; 20d ... -7 dB; 21d ... -6 dB; 22d ... -5 dB; 23d ... -4 dB; 24d ... -3 dB; 25d ... -2 dB; 26d ... -1 dB; 27d ... 0 dB; 28d ... 1 dB; 29d ... 2 dB; 30d ... 3 dB; 31d ... 4 dB
Bit 0	-	-	-	-

Table 7. HiZ Register (3h)

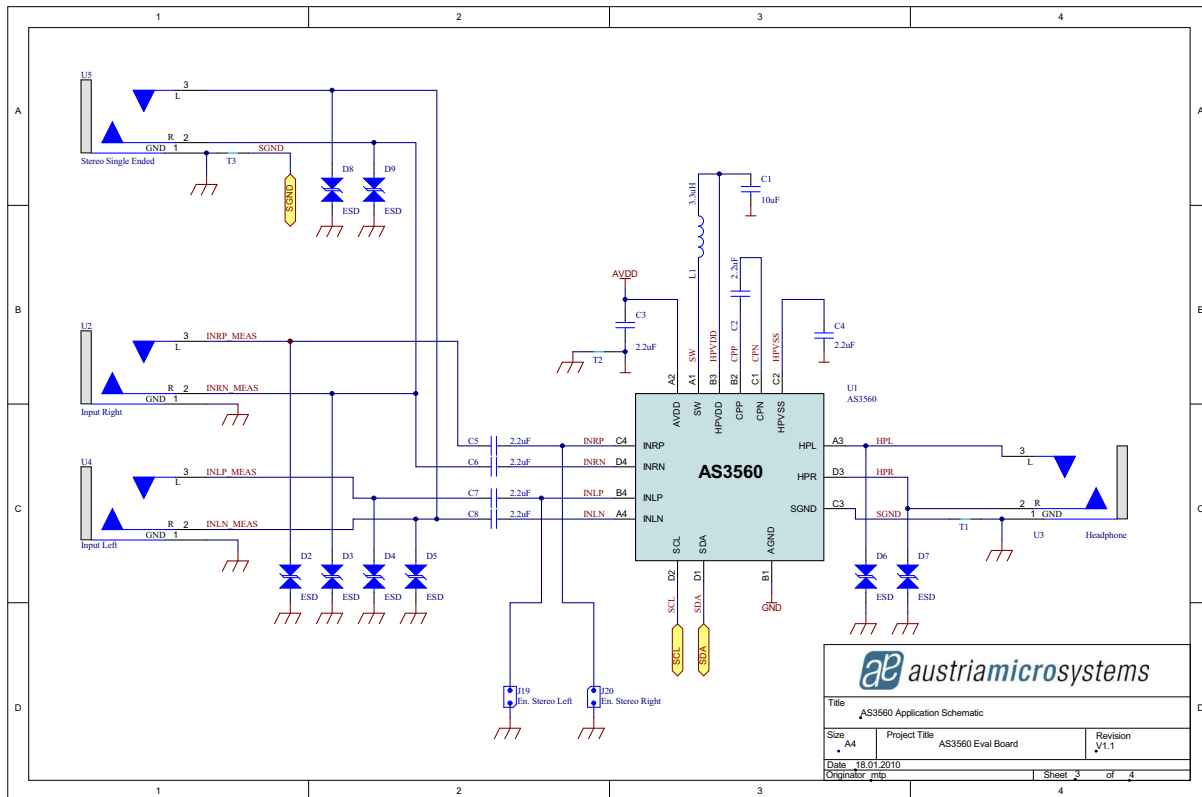
Bit	Bit Name	Default	Access	Bit Description
Bit 7	-	-	-	-
Bit 6	-	-	-	-
Bit 5	-	-	-	-
Bit 4	-	-	-	-
Bit 3	-	-	-	-
Bit 2	-	-	-	-
Bit 1	HiZ_L	0	RW	0 ... Normal Operation; 1 ... High Impedance on HPH_Output Left
Bit 0	HiZ_R	0	RW	0 ... Normal Operation; 1 ... High Impedance on HPH_Output Right

Table 8. Info Register (4h)

Bit	Bit Name	Default	Access	Bit Description
Bit 7	Supplier Bit [1:0]	RO	1	11b ... Default Supplier ID; else ... unused
Bit 6			1	
Bit 5	-	-	-	-
Bit 4	-	-	-	-
Bit 3	Version Bit [3:0]	RO	0	0 ... First Version; else ... unused
Bit 2			0	
Bit 1			0	
Bit 0			0	

# 10 Application Information

Figure 28. AS3560 application board



## 10.1 GND Connections

The SGND pin is an input reference and must be connected to the headphone ground connector pin. This ensures no turn-on pop and minimizes output offset voltage. Do not connect more than  $\pm 0.3V$  to SGND. AGND is a power ground. Connect supply decoupling capacitors for AVDD, HPVDD, and HPVSS to AGND.

## 10.2 External Elements

1 x 3.3 uH Coil (SW-HPVDD)

7 x 2.2 uF  $\pm 10\%$  X5R (AVDD, CPP-CPN, HPVSS, INRP, INRN, INLP, INLN)

1 x 10 uF  $\pm 10\%$  X5R (HPVDD)

## 10.3 Software Shutdown

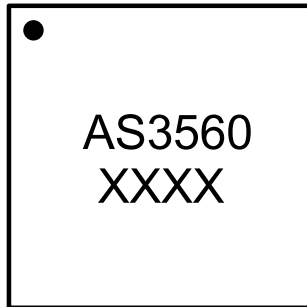
Set software shutdown by writing a logic 1 in [ENABLE Register \(1h\)](#), bit 0 (SWS bit). Software shutdown places the device in the lowest power state. See [Operating Conditions](#) for values. Engaging software shutdown turns off the buck regulator and charge pump and disables the amplifier outputs. Write a logic 0 to the SWS bit to reactivate the device.

**Note:** When the device is in SWS mode all registers will maintain their values. The HP\_EN\_L and HP\_EN\_R bits can be reset because a full word must be used when writing just one bit to the register.

Note that I2C read and write access is still possible in shutdown mode.

## 11 Package Drawings and Markings

Figure 29. WL-CSP (1.615x1.615mm) Marking

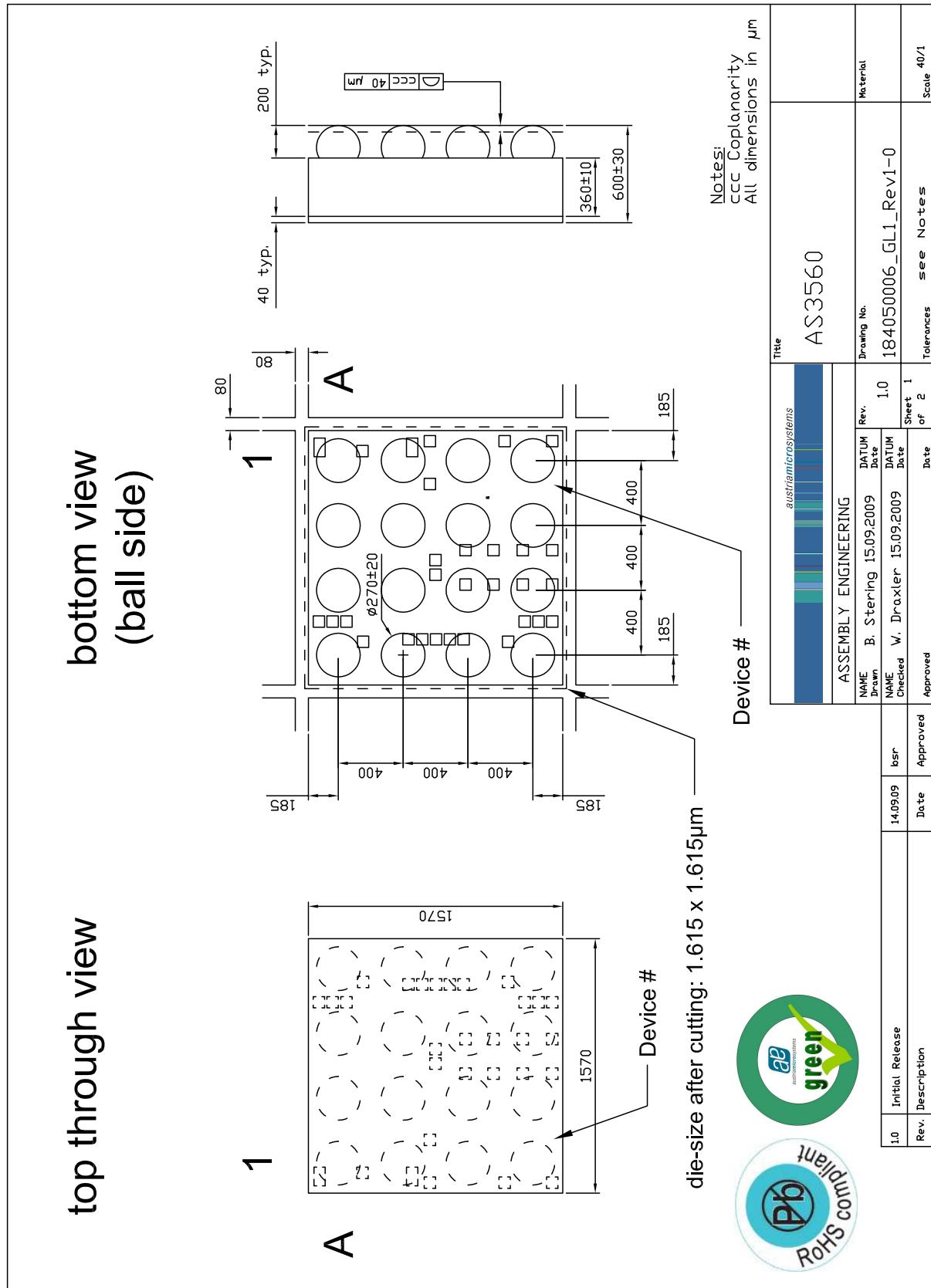


Packaging Code XXXX

XXXX
encoded Datecode

The device is available in a WL-CSP (1.615x1.615mm) package.

Figure 30. WL-CSP (1.615x1.615mm) Package





## Revision History

Revision	Date	Owner	Description
0.01	Sep 10 <sup>th</sup> , 2009	pkm	Initial draft template
0.02	Sep 23 <sup>rd</sup> , 2009	wsg	revised draft
0.04	Sep 29 <sup>th</sup> , 2009	wsg	after first review
0.06	Feb 9 <sup>th</sup> , 2010	wsg	update on detailed operating characteristics
0.07	Sep 17 <sup>th</sup> , 2010	hgt	updated operating characteristics and package drawing
0.99	Nov 23rd, 2010	hgt	layout change of operating characteristic
1.01	Dec 20th, 2010	hgt	first official release
1.02	June 6th, 2011	hgt	changed order information
1.03	June 27th, 2011	hgt	changed order information

**Note:** Typos may not be explicitly mentioned under revision history.

## 12 Ordering Information

The devices are available as the standard products shown in [Table 9](#).

Table 9. Ordering Information

Ordering Code	Description	Delivery Form	Package
AS3560-BWLT	AS3560 Class-G Stereo Headphone Amplifier	Tape&Reel	WL-CSP 16

**Note:** All products are RoHS compliant and austriamicrosystems green.

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## Contact Information

### Headquarters

austriamicrosystems AG  
Tobelbaderstrasse 30  
A-8141 Unterpremstaetten, Austria  
Tel: +43 (0) 3136 500 0  
Fax: +43 (0) 3136 525 01

For Sales Offices, Distributors and Representatives, please visit:

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