AS8421
Voltage Regulator with LIN I/F

Key Features

- INTERNAL VOLTAGE REGULATOR
- VBAT MONITOR WITH FAULT VBAT SIGNAL GENERATION WHEN VBAT OUT OF OPERATIVE RANGE
- VDD MONITOR WITH INTELLIGENT RESET GENERATION BASED ON VDD LEVEL
- COMPLETE INDIPENDENT WATCHDOG WITH AUTOENABLE BY FIRST TRIGGER SIGNAL (TRES)
- PRECISE STANDBY MODE MANAGEMENT TO PREVENT FALSE COMMANDS AND ACHIEVE VERY LOW STANDBY CURRENT CONSUMPTION: ONE SLEEP-STROBE (EXTERNAL) AND TWO WAKE-UP-STROBES (FROM BUS INTERFACE AND EXTERNAL)
- STANDARD LIN BUS INTERFACE
- OVERTEMPERATURE MONITOR WITH FAULT T-SIGNAL GENERATION (T SENSOR ON CHIP)

General Description

Automotive distributed Power Supply Management System with integrated Bus Interface

Applications

Most of Automotive distributed module subsystem architectures with specific regards to:

- Door modules
- Seat modules
- Junction box

Functional Description

The chip integrates the basic group of functions for most of Automotive distributed Module system architectures as: Regulated power supply from battery, Reset, Supply Monitor, Watchdog, Standby management, Bus inerface.

VOLTAGE REGULATOR: This block is designed for battery input to regulated voltage with maximum current allowed by thermal package limitation (worst case 20mA). Higher current can be delivered using an external transistor.

MONITOR: Battery input is monitored and a fault signal FB becomes active when VBAT is out of operative range. VDD is monitored and a VRES (Voltage controlled Reset) is active when VDD is below a defined voltage threshold (an histeresysis is provided).

WATCHDOG: An internal low frequency oscillator is used to run the Watchdog. The first trigger signal starts the Watchdog timer. Time-out signal TRES (Time controlled Reset) is activated in a defined cycle sequence when the Watchdog timer owerflows. Time-out value may be changed by mask option. The divided internal clock is present at an output pad.

STANDBY: The Standby circuit is a simple and strategic block which precisely controls the sleep and wakeup conditions of a microprocessor system. Sleep signal typically comes from the microprocessor. In sleep mode the Reset is activated and the Regulated voltage is cut-off. All other I/O signals are configured for minimum current except

external Wakeup. In fact the wakeup condition can come from an external circuit but also from the Bus interface when H/L or L/H transition are present on the bus.

BUS INTERFACE: It consists of one wire Bus with seprate TX and RX signals. A Thermal sensor is integrated mainly for protection purposes. The FT (Fault Temperature) output signal is present on a pad.

The Bus Interface circuitry fulfils the LIN standard. A TTP/A Interface will be available soon.
To guarantee a high flexibility and cost effective solution the protocol handler intenionally is not integrated on the chip.
To simplify a system solution we also offer a double chip solution – AS8421 plus µC - in one package.

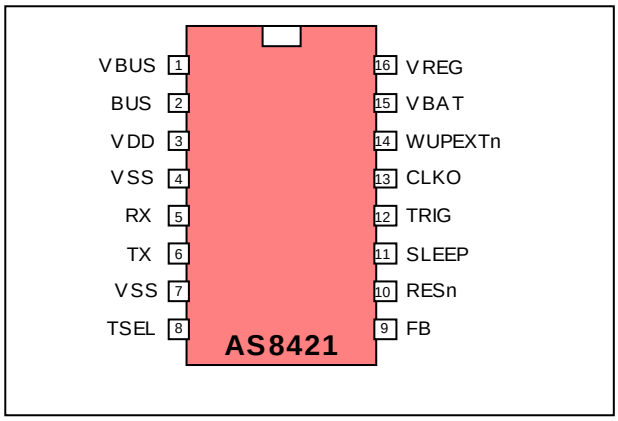

Figure 1 Pinout of AS8421

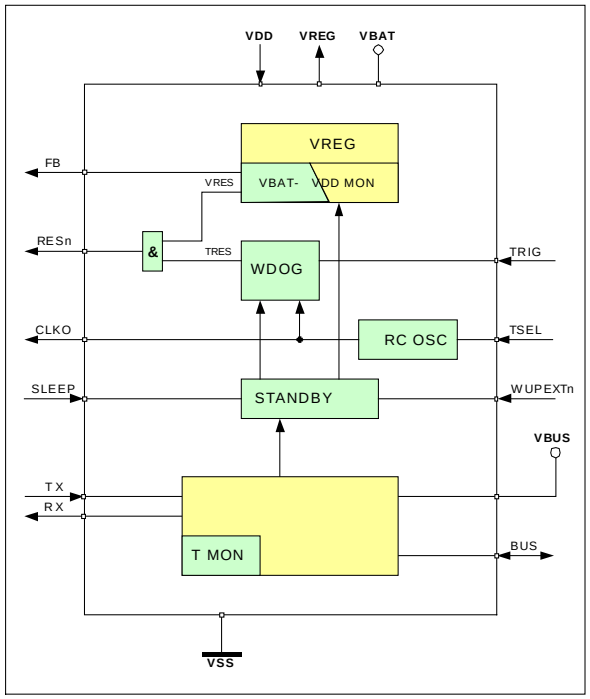

Figure 2 Block Diagram of AS8421

Package Information

SOIC16

Pin Description, Pin Types

S	supply pad
AIO	analog I/O
DI	digital input
DI_PU	digital input with pull-up
DI_PD	digital input with pull-down
DIO	digital I/O
DO	digital ouput
DO_OD	digital output open drain

Pin	Name	Type	Note
1	VBUS	S	Battery Voltage (diode protected)
2	BUS	AIO	Bidirectional ISO K Line bus I/O
3	VDD	S	5 V power supply
4	VSS	S	Power Ground
5	RX	DO	Bus transmission output
6	TX	DI_PU	Bus transmission input
7	VSS	S	Power Ground
8	TSEL	AIO	Timer SELect, watchdog periode select by ext. reference resistor
9	FB	DO	Fault
10	RESn	DO_OD	RESet - open drain
11	SLEEP	DI_PD	Sleep strobe to force sleep mode
12	TRIG	DI	TRIGger input for watchdog
13	CLKO	DIO	Clock Output signal
14	WUPEXTn	DI_PU	Low active External Wakup signal
15	VBAT	S	Battery Voltage (diode protected)
16	VREG	AIO	regulated supply – if ext. transistor is not used, shorted to VDD

Table 1 Pinlist of AS8421

Electrical Parameters

Absolute Maximum Ratings (NON OPERATING)

Stresses beyond those listed under “Absolute Maximum Ratings“ may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Symbol	Min	Max	Unit	Note
Battery Voltage	VBAT	-0.3	20	V	(1) 42 V for 400 ms
Bus Supply Voltage	VBUS	-0.3	20	V	(1) 42 V for 400 ms
Low Power Supply Voltage	VDD	-0.3	7	V	(1)
Input Pin Voltage	V_{in}	-0.3 V	VDD/V + 0.3	V	
Input Current (latchup immunity)	I_{scr}	-100	100	mA	Norm: Jedec 17
ESD		+/-1.0		kV	Norm: MIL 883 E method 3015
Total Power dissipation (all supplies and outputs)	P_t		300	mW	
Storage Temperature	T_{strg}	-55	125	°C	
Soldering conditions	T_{lead}		235	°C	Norm: IEC 61760-1
Humidity non-condensing		5	85	%	

Table 2 Absolute Maximum Ratings

Note 1: Value of these process dependent parameters to be taken from according Process Parameter document, current version

Operating Conditions

Parameter	Symbol	Min	Max	Unit	Note
Battery Supply Voltage	VBAT	7	18	V	(1)
Battery Supply Voltage	VBUS	7	18	V	(1)
5V Low Power Supply Voltage	VDD	4.75	5.25	V	(2)+(3)
Voltage drop on ground potential	VSS-GND	-0.1	0.1	V	
Ambient temperature	Tamb	-45	85	°C	

Table 3 Operating Conditions

Note 1: Load dump 42V

Note 2: Recommended external capacitors ≥ 100nF

Note 3: 40 mA max. load, higher current with external transistor

Characteristics of Analog and Digital Inputs and Outputs

Operational Parameters

Parameter	Symbol	Min	Max	Unit	Note
Under Voltage VBAT	Vfuv	7	7.9	V	(1)
Over Voltage VBAT	Vfov	18.1	20	V	(1)
Under Voltage VDD	Vfuvdd	0.8 * VDD	0.9 * VDD	V	(1)
Over Voltage VDD	Vfovdd	1.1 * VDD	1.2 * VDD	V	(1)
WatchDog signal pulse width	twdres	10	40	µs	(2)+(3) active low
WatchDog time out period	twdtrig	1.0	2.3	s	(4) typ. 1.5sec
Temperature threshold warning	TW			°C	(5) typ. 140°C
Temperature threshold VReg	TOff	160		°C	(5)
Standby Current	IDD		70	µA	(6)
value of external Reference Resistor	Rref			kΩ	±1 % typ. 22kΩ
Frequency of RC oscillator	fRC			kHz	OnChip typ. 100kHz
reset active time after Power On or WakeUp	tRES1	200		ms	(2)
reset active time before Power Off	tRES2	1		ms	(2)
Debounce time WUPEXTn	tdeb1	10	30	ms	(2)
Debounce time SLEEP	tdeb2	1.5	3	ms	(2)

Table 4 analog signal parameters

Note 1: 250 mV Hyteresis
FB becomes active

Note 2: internal time base

Note 3: Active low digital output triggered by Watch Dog overflow.

Note 4: Digital input from µController within a time between 200 and 1000 ms

Note 5: hysteresis > 10 grd

Note 6: internal oscillator NOT running, VBAT = 14 V, 25°C

Analog Output Signals

Parameter	Symbol	Min	Max	Unit	Note
Regulated Output control Voltage	VREG		VDD + 0.7	V	

Table 5 Analog signal parameters

CMOS Input

Parameter	Symbol	Min	Max	Unit	Note
High Level Input Voltage	V_{IH}	0.7 * VDD		V	
Low Level Input Voltage	V_{IL}		0.3 * VDD	V	
Input Leakage Current	I_{LEAK}		1	µA	

Table 6 **CMOS Input parameters**

CMOS output

Parameter	Symbol	Min	Max	Unit	Note
High Level Output Voltage	V_{OH}	VDD/V-0.5		V	
Low Level Output Voltage	V_{OL}		VSS/V+0.4	V	
Capacitive Load	C_L		50	pF	

Table 7 **CMOS output parameters**

LIN I/F

The LIN I/F comply with the LIN standard and is able to wake up the whole circuit out of standby mode if any LIN BUS activity (LOW pegel) can be detected.

Failure Code Generator

Different Failure states are reported by the AS8421 at FB signal. A circulating bitstream allows decoding of these failure states as shown below.

Failure #	description	circulating code
0	normal working	0000 0000 0000 0000
1	Under Voltage VBAT	1111 0100 0000 1010
2	Over Voltage VBAT	1111 0010 0000 1010
3	Under Voltage VDD	1111 0001 0000 1010
4	Over Voltage VDD	1111 0000 1000 1010
5	Temperature warning	1111 0000 0100 1010
6	Over Temperature	1111 0000 0010 1010 hidden, IC switched off

Table 1: Failure codes

In case of more than one active failures failure code signals will be “ORed”.

Application Note

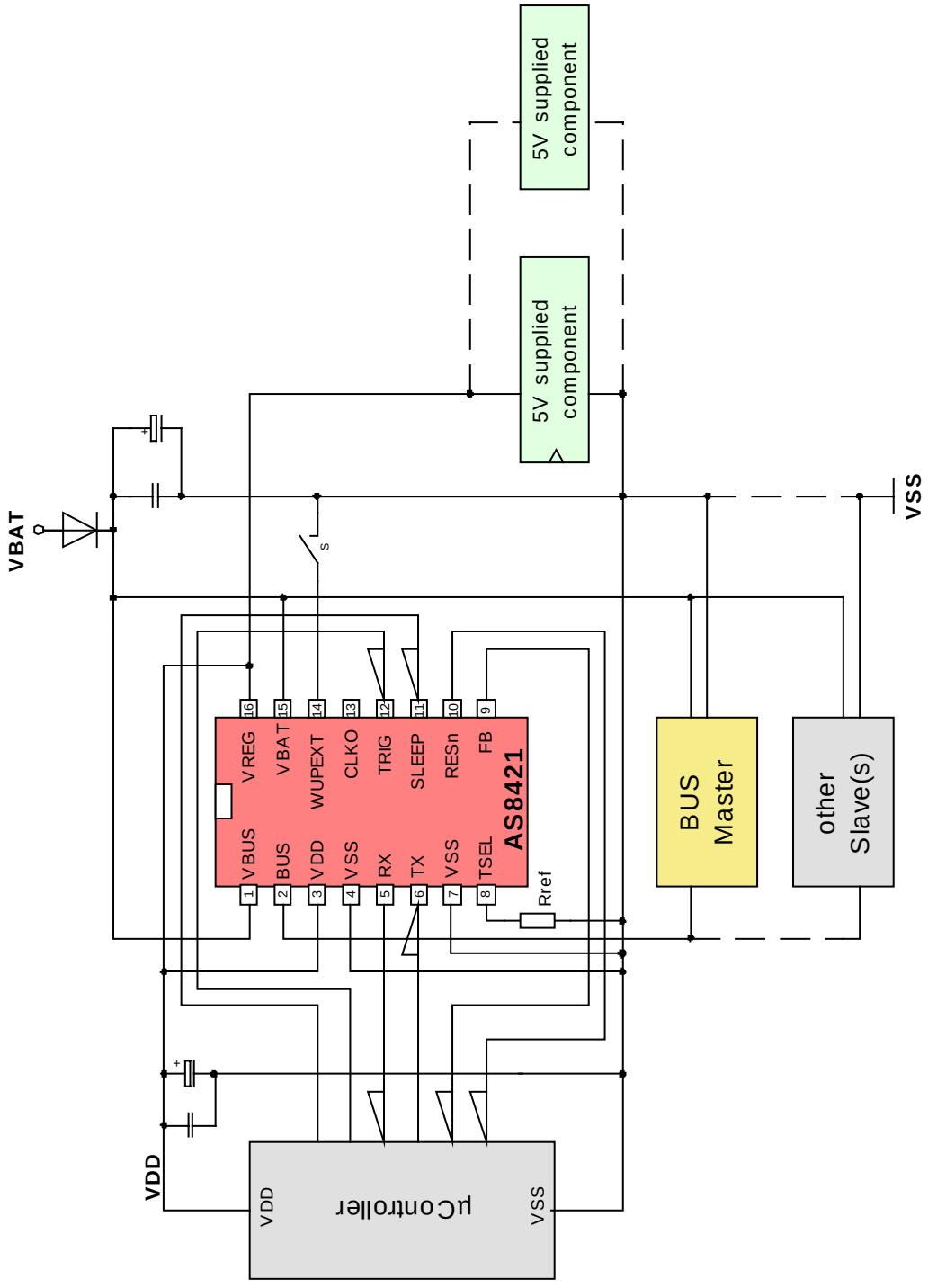

Figure 3 AS8421 in a fully configuered µController driven system

MARKING / PACKAGE - PRODUCTION PARTS

Package type: SOIC16

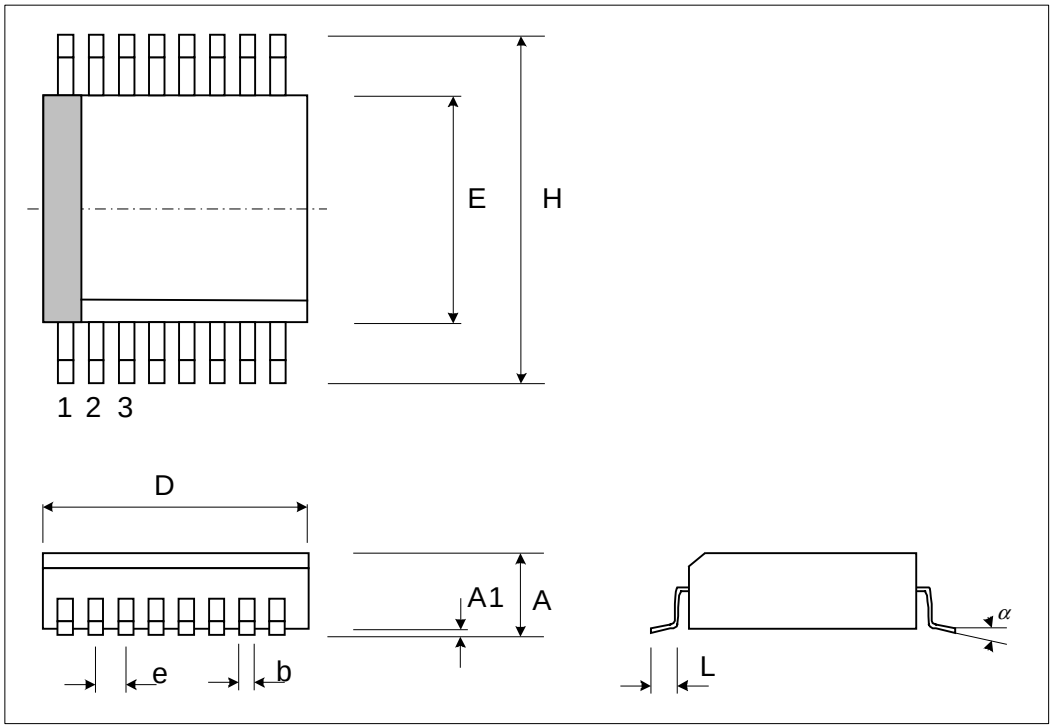

Figure 4 SOIC16 Package

	D	E	H	A	A1	e	b	L	Copl	α
Min	10.10	7.40	10.00	2.35	0.1	1.27	0.33	0.40		0 °
max	10.50	7.60	10.65	2.65	0.30		0.51	1.27	0.10	8 °

Table 1 Package Dimensions

Marking: YYWWIZZ

YY	year
WW	week
I	plant identifier
ZZ	letters of free choice

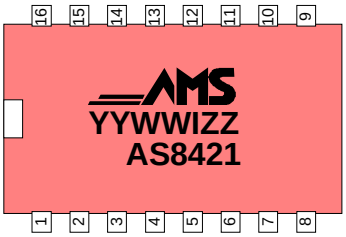

Figure 5 Package Marking

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