CRYSTAL
Semiconductor Corporation

CS6400

Echo-Cancelling Codec

Features

- Applicable in:
  - Digital-Cellular Hands-Free Phones
  - Analog-Cellular Hands-Free Phones
  - Office Speaker Phones
  - Desktop & Video Teleconferencing
  - Network/Base Stations

- Echo Cancellation
  - Up to 60 dB ERLE
  - 512 Tap (64 ms at 8 kHz Fs)
  - Split Mode For Two ECs
  - Cascadable For Longer Response

- Zero-Glue Serial Data/Control Interface

- On-Chip Codec
  - < 1% THD, 8Ω Load On Output
  - > 70 dB S/(N+D) on Input
  - 0-3600 Hz Bandwidth at 8 kHz Fs
  - 0-7200 Hz Bandwidth at 16 kHz Fs

General Description

The CS6400 is an application-specific digital signal processor optimized for acoustic echo and noise cancellation applications. A high-quality codec is integrated with the processor to provide a complete, low-cost echo-cancellation solution.
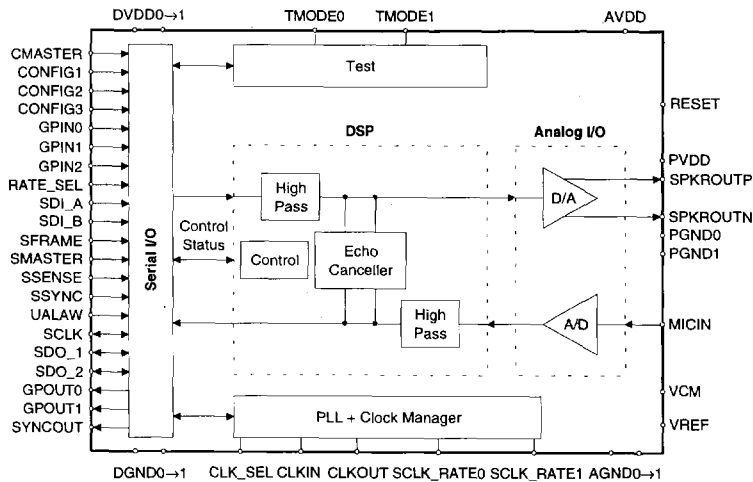
The CS6400 is a fully independent processor that requires no signal processing support to implement its cancellation functions. Volume control, mute, and sleep functions are also provided.

The on-chip A/D and D/A converters employ over-sampling technology, which eliminates the need for complex external anti-aliasing and reconstruction filters, further reducing system cost.

The CS6400 has a zero glue-logic serial interface that is compatible with most DSPs. Clock and sync lines control the transfer of serial data via the separate serial data-in and data-out pins. Both 15-bit audio data and control/status information may be multiplexed on this serial channel using a steering bit.

ORDERING INFORMATION
CS6400-IQ	-40 to +85 °C	44-pin TQFP
CDB6400	Evaluation Board	

6

ADC CHARACTERISTICS

(T_A = 25 °C; All DVDD, AVDD, and PVDD = 5.0V, Digital Input Levels: Logic 0 = 0V, Logic 1 = DVDD; Signal test frequency 1kHz, word rate (Fs) = 8kHz, audio signal measurement bandwidth is 20Hz to 20kHz; Microphone amp gain = 0dB; SPRKOUT outputs connected to 8Ω load; CLKIN frequency = 2.048MHz; unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Units
ADC Resolution With No Missing Codes		12			bits
Instantaneous Dynamic Range	IDR	70	72		dB
Total Harmonic Distortion at -0.5dBFS signal level	THD	0.03			%
Gain Drift			150		ppm/°C
Offset Error			25	50	LSB
Full Scale Input Voltage (Note 1)		0.9	1.0	1.1	V_p
Input Resistance (at MICIN)		25			kΩ
Input Capacitance (at MICIN)			15		pF
Inter-Section Isolation, DAC to ADC			75		dB
Sample Rate	Fs			16	kHz
Microphone Amp Gain (switchable on/off)			+26		dB
Anti-aliasing Rejection			30		dB
Power Supply Rejection (1kHz)	PSR		40		dB
Frequency Response		-0.6		0.6	dB
Transition Band		0.45		0.6	Fs
Stop Band Rejection		70			dB
VREF Reference Voltage Output			2.0		V
VCM Voltage Output constant load only, >100 kΩ			1.0		V
Group Delay (Note 2)			8/Fs		s
Group Delay Variations vs. Frequency (Note 2)			0.0		μs

Notes: 1. This is the peak input voltage (in volts) with the mic amp gain set to 0 dB. Peak-to-peak voltage is 2x peak. Input signals will be properly clipped if the peak signal is greater than full scale, but less than 2x full scale.
2. This group-delay specification is for the ADC only; additional group delay may be introduced by the high-pass filter that is implemented on the CS6400 in software.

DAC CHARACTERISTICS

(T_A = 25 °C; All DVDD, AVDD, and PVDD = 5.0V, Digital Input Levels: Logic 0 = 0V, Logic 1 = DVDD; Signal test frequency 1kHz, word rate (Fs) = 8kHz, audio signal measurement bandwidth is 20Hz to 20kHz; Microphone amp gain = 0dB; SPRKOUT outputs connected to 8Ω load; CLKIN frequency = 2.048MHz; unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Units
DAC Resolution		12			bits
DAC step size error				±0.5	LSB
Instantaneous Dynamic Range	IDR	70	72		dB
Frequency Response		-0.8		+0.6	dB
Programmable Output Level Attenuator Range (Note 3)		-92.2		0	dB
Gain Step Size			2.49		dB
Gain Drift			150		ppm/°C
VREF Reference Output Voltage			2.0		V
VCM Output Voltage constant load only, >100kΩ			1.0		V
Offset Error			25	50	mV
Full Scale Output Voltage (SPKROUT pins) (Note 4)		1.58	1.75	1.93	V_p
Common Mode Output Voltage (SPKROUT pins)			1.35		V
Total Harmonic Distortion at -0.5dBFS level, SPKROUT	THD			0.8	%
Output Impedance SPKROUT pins			0.1		Ω
Load Impedance SPKROUT pins		8			Ω
Short Circuit Current Limit SPKROUT pins (Note 5)				500	mA
Output Capacitance			15		pF
Audible Stop Band Attenuation (<20kHz)		68			dB
Integrated Inaudible Energy (>20kHz) (Note 6)				30	mVrms
Audible Noise with Fs = 8kHz (<20kHz)			-70		dB
Power Supply Rejection (1kHz)	PSR		40		dB
Inter-Section Isolation, ADC to DAC			75		dB
Filter Transition Band		0.45		0.6	Fs
Group Delay (Note 7)			8/Fs		s

Notes: 3. Attenuation settings greater than 92.2 dB will cause a full scale input signal to be completely attenuated to zero signal level.
4. This is the peak differential output voltage. The peak-to-peak signal level on each output pin is equal to the peak differential value.
5. SPKROUTP or SPKROUTN shorted to ground.
6. Assuming an external 43.2 kHz RC output filter.
7. This group-delay specification is for the DAC only; additional group delay may be introduced by the high-pass filter that is implemented on the CS6400 in software.

PHASE-LOCKED LOOP CHARACTERISTICS (T_A = 25°C; AVDD, DVDD, and PVDD = +5V; Input Levels: Logic 0 = 0V, Logic 1 = DVDD)

Parameter	Symbol	Min	Typ	Max	Units
PLL acquisition time				1	ms
PLL frequency range		22.12	24.58	27.03	MHz
PLL jitter			200		ps rms
Input ref frequency		1.84	2.048	2.25	MHz

DIGITAL CHARACTERISTICS (T_A = 25°C; AVDD, DVDD, and PVDD = 5V)

Parameter	Symbol	Min	Typ	Max	Units
High-level Input Voltage	V_{IH}	VD - 1.0			V
Low-level Input Voltage	V_{IL}			1.0	V
High-level Output Voltage at I_0 = -2.0 mA	V_{OH}	VD - 0.3			V
Low-level Output Voltage at I_0 = +2.0 mA	V_{OL}			0.1	V
Input Leakage Current (Digital Inputs)				10	µA
Output Leakage Current (High-Z Digital Outputs)				10	µA
Output Capacitance	C_{OUT}			15	pF
Input Capacitance	C_{IN}			15	pF

ABSOLUTE MAXIMUM RATINGS (All voltages with respect to 0V)

Parameter	Symbol	Min	Typ	Max	Units
Power Supplies		-0.3		6.0	V
Input Current Except Supply Pins & Driver Pins		-		±10.0	mA
Analog Input Voltage		-0.3		VA + 0.3	V
Digital Input Voltage		-0.3		VD + 0.3	V
Ambient Temperature (Power Applied)		-55		125	°C
Storage Temperature		-65		150	°C
ESD using human body model (100pF with series 1.5kΩ)		2000		-	V

Warning: Operation beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.
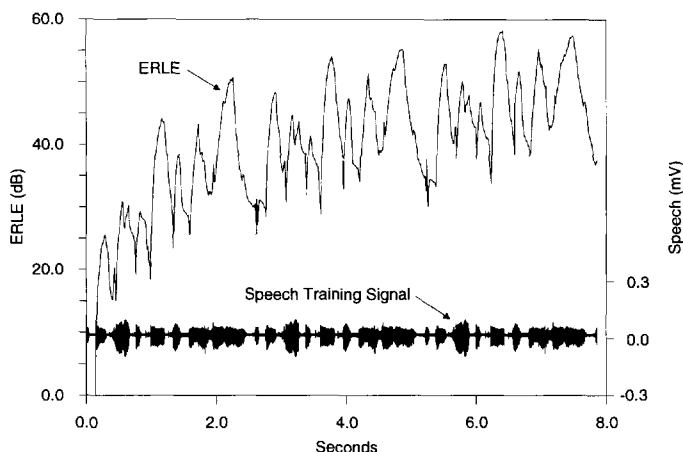
Figure 1. Typical ERLE Convergence Characteristics

Echo Canceller Characteristics

The typical Echo Return-Loss Enhancement (ERLE) convergence characteristics for the CS6400 are illustrated in the above diagram under the following conditions:

- Echo-canceller length: 512 taps

- Echo-canceller initial conditions: zeroed filter taps, updates disabled until t=0.125s

- Sampling rate: 8 kHz

- Echo path (including microphone, speaker, and amplifiers):
  spectrally flat
  linear
  duration < 64 ms
  noise free
  time invariant

- Near-end high-pass filter: enabled

- Pre-emphasis filter: enabled

- Graded-beta profile: 64 echo-canceller filter taps processed per 2x reduction in update gain

- Training signal: speech, full scale

- Unlimited S/(N+D) on linear A/D

Note: Many of these conditions may be significantly different in real applications, resulting in significantly different measured ERLE performance.
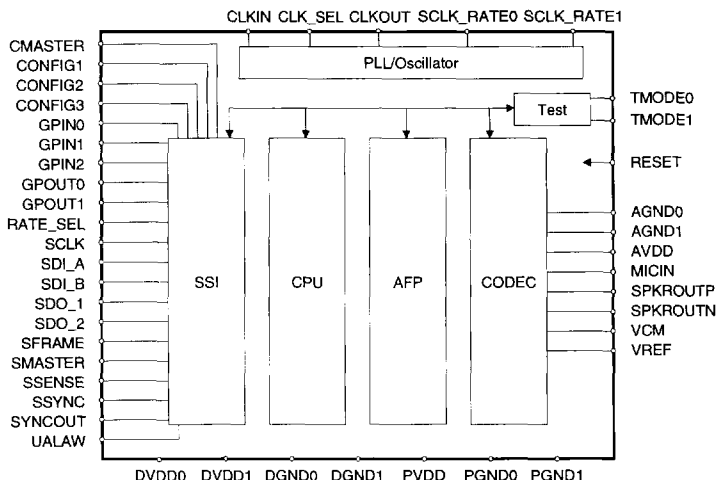
Figure 2. CS6400 Internal Block Diagram

OVERVIEW

In hands-free speakerphones, the signal from the far end may echo about the near-end environment and then be received at the near-end microphone. When heard at the far end, this echo signal can be very annoying, particularly if the signal is delayed by transmission or signal-processing delays.

Voice switching is a particularly simple technique for eliminating this echo, but since it requires half-duplex communication, it seriously compromises conversation quality.

Echo cancellation can provide high-quality, full-duplex communication, but typically must be implemented using expensive digital signal-processing hardware.

Echo Cancellation in the CS6400

The CS6400 provides high-quality echo cancellation at low cost. This breakthrough in cost/performance is made possible on the CS6400 by custom, application-optimized processing blocks, which are integrated on a single die, as shown in Figure 2.

One of these processing blocks is the AFP (Adaptive Filter Processor). This block implements a 512-tap AFIR (Adaptive Finite Impulse-Response) filter which is updated using an enhanced least-mean squared (LMS) algorithm. At a sampling rate of 8 kHz, it can cancel up to 64 ms of echo. In some operating modes, some of the available 64 ms may be allocated to a network canceller (NEC), or the available 64 ms may be split to provide two independent echo-cancellation channels.

Another processing block is the CPU. This block facilitates other processing, like update control. This processing has a critical influence on overall echo-cancellation performance. Double-talk detection is a particularly important part of this processing. Double-talk detection and other algorithms were carefully developed and validated at Crystal under real-world conditions.

To increase the CS6400's echo return-loss enhancement (ERLE), optional echo suppression may be enabled to supplement echo cancellation. To assure the highest-quality conversation, a sophisticated voice-detection algorithm is used to provide graduated, soft-switching echo suppression.
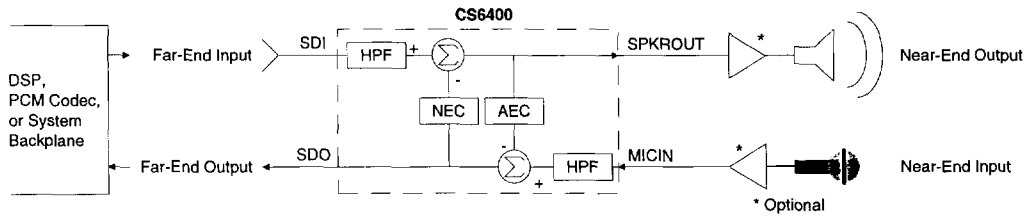
Figure 3. Functional Diagram

As shown in Figure 3, a high-pass filter is provided at the far-end and near-end inputs to remove low-frequency noise that is typically present, for example, in a car environment.

Analog Interface

Another processing block is the codec block. This block provides an A/D and a D/A converter that can be connected directly to a microphone and a speaker, respectively.

The output of the microphone is low-pass filtered, then AC-coupled to the audio input, MICIN. A 26 dB gain stage is included in the CS6400 at the A/D input to amplify the microphone signal. However, this gain stage is bypassed in modes in which a line-level source is connected to the CS6400 instead of a microphone. The CS6400 also includes a speaker driver, which can drive an 8Ω speaker directly, or alternatively, it can drive a high-impedance differential input on an external amplifier.

Both the D/A and A/D paths are bandlimited as a function of sampling rate. At a sampling rate of 8 kHz, the paths are limited to 0-3600 Hz. S/(N+D) is greater than 70 dB for a 20 kHz and 4 kHz bandwidth for the D/A and A/D converter, respectively. For applications that require higher-quality audio, the sampling rate for the codec can be doubled to 16 kHz, increasing the codec bandwidth to 0-7200 Hz. At a 16 kHz sampling rate, however, a CS6400 can compensate for only 32 ms of echo. To extend the echo response back to 64 ms, two CS6400s can be cascaded.

Synchronous Serial Interface

Another processing block is the Synchronous Serial Interface (SSI). This block provides a data and control interface to the CS6400. The SSI can connect to an external codec, DSP, to backplane network, or to another CS6400.

The SSI can be connected to an external network codec (like the MC145503) for applications like speakerphones. The SSI can be connected to a DSP for high-end applications like video teleconferencing. For network applications, the SSI can connect to a network backplane and a TSAC (Time-Slot Assigner Chip).

The CS6400 can operate as either a system-timing master, or as a system-timing slave. When the CS6400 is a system-timing master, timing is generated by a crystal oscillator on the CS6400. When the CS6400 is a system-timing slave (i.e., when the CS6400 is connected to a DSP), timing is generated by an internal PLL (Phase-Locked Loop) on the CS6400, using the SCLK input as a timing reference.

The crystal oscillator will operate only at 2.048 MHz, but the PLL can operate at 256 kHz, 384 kHz, 1.024 MHz, or 2.048 MHz. As a result, when the CS6400 is a timing master, the SCLK will operate only at 2.048 MHz, but can operate at any of the above frequencies when it is a timing slave.

6

|	Configuration		CMASTER	SFRAME	SMASTER	CONFIG3	CONFIG2	CONFIG1
Mode 1:	Interface to CODEC (CODEC⇔CS6400)							
Application:	Low-cost speaker phone							
1.1:	Short-Frame Mode		0	0	1	0	0	1
1.2:	Long-Frame Mode		0	1	1	0	0	1
Mode 2:	Interface to DSP (DSP⇔CS6400)		0	0	0	0	1	1
Application:	Digital cellular							
Mode 3:	Cascade Mode (CS6400(m)⇔CS6400(s))	master:	1	0	1	0	1	0
Application:	Teleconferencing	slave:	1	0	0	0	1	1
Mode 4:	Interface to DSP (DSP⇔CS6400(m)⇔CS6400(s))	slave:	1	0	0	0	1	1
Application:	Teleconferencing							
4.1:	Master's Codec is Bypassed	master:	0	0	0	0	1	0
4.2:	Master's Codec is Used	master:	1	0	0	0	1	0
Mode 5:	Interface to Network: Single Serial Port							
5.1:	1ch data: codec-8bit		0	1	0	0	0	1
5.2:	2ch data: codec-8bit		0	1	0	0	0	0
5.3:	1ch data: dsp-16bit		0	1	0	0	1	1
5.4:	2ch data: dsp-16bit		0	1	0	0	1	0
Mode 6:	Interface to Network: Dual Serial Port							
6.1:	1ch data: codec-8bit		0	1	0	1	0	1
6.2:	2ch data: codec-8bit		0	1	0	1	0	0
6.3:	1ch data: dsp-16bit		0	1	0	1	1	1
6.4:	2ch data: dsp-16bit		0	1	0	1	1	0

Table 1. CS6400 Configurations

The behavior of the CS6400 is controlled by configuration-control input pins. The behavior of the CS6400 for each possible state of these control signals is illustrated in Table 1.

As indicated in Table 1, the CS6400 has six operating modes. These operating modes are illustrated in Figure 4.

The simplest operating mode is Mode 1. This operating mode is useful in applications where the data link to the far end is analog, as in analog cellular hands free, or in analog speaker phones.

Mode 2 is useful in applications where the data link to the far end is digital, as in digital cellular hands free, or in digital (ISDN) speaker phones.
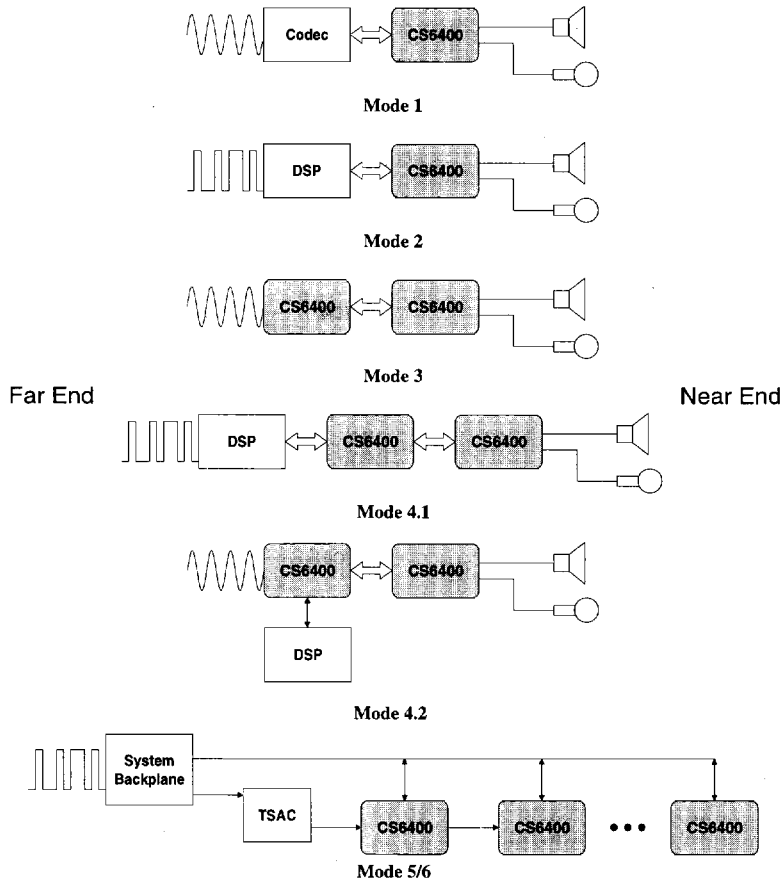
Figure 4. Operating Modes

Mode 3 is similar to Mode 1, except that a second CS6400 is used as the codec. In this configuration, the echo cancellers on the two CS6400s are cascaded, allowing the CS6400 to be used in environments with longer echo response. This mode would be useful in teleconferencing applications.

Mode 4 is similar to Mode 3, except that in Mode 4, the CS6400 is connected to a DSP. Also, in Mode 4, the data link to the far-end may be digital or analog. For example, the codec on the master CS6400 may be used as the far-end interface, and the serial interface to the DSP may be used for control. Alternatively, the master

codec may be bypassed, with the far-end data being passed digitally from the DSP to the master CS6400.

Mode 5 and 6 are for network and base-station applications. In these cases, CS6400s are connected together on a PCM highway; access to the PCM highway is controlled by an external TSAC (Time-Slot Assigner Chip).

In Modes 5 and 6, the taps in the CS6400 may be split to provide two independent 32 ms channels. In Mode 5, these channels are time multiplexed onto a single serial bus. In Mode 6, each channel is assigned to a separate serial bus.
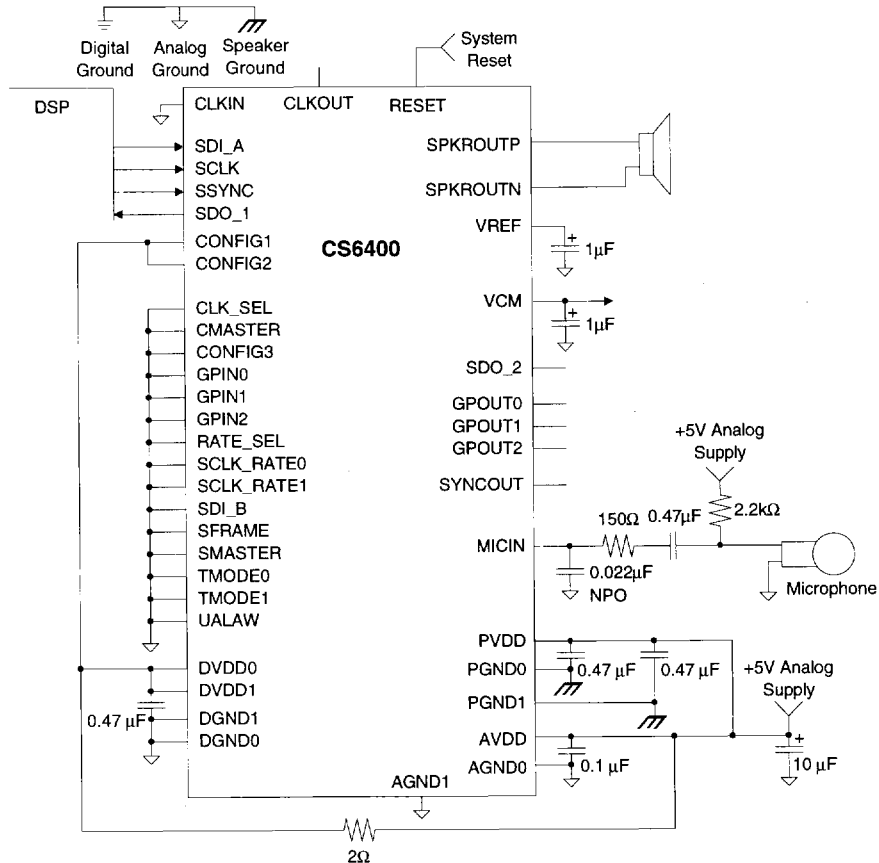
Figure 5. DSP Connection Diagram (Mode 2)

Interfacing to an external DSP

When interfacing to an external DSP (Mode 2), the CS6400 is configured as a serial-bus slave; i.e., SCLK, and SSYNC signals are provided to the CS6400 by the DSP. The recommended interface circuitry for this case is shown in Figure 5.

In this case, the DSP sends a single start-of-frame pulse to the SSYNC input one SCLK period before the start of a data frame. Since there is only one SSYNC input, every data frame includes both a data read from the CS6400 and a data write to the CS6400.

The CS6400's SSI is compatible with industry-standard DSPs. For Motorola, TI, and other popular DSPs, the start-of-frame sync pulse is positive logic. The SSI can be configured to accept a positive start-of-frame pulse by setting SSENSE=0. For AT&T DSPs, the start-of-frame sync pulse is negative logic. In this case, SSENSE=1. The behavior of the serial interface in these cases is illustrated in Figure 6. Note that the sense of SCLK also changes.

When a DSP is connected to a CS6400, the DSP can reconfigure the CS6400 by writing to the CS6400's control registers via the SSI.

To multiplex both data and control on one serial interface, a steering bit is used. The first bit sent (MSB) by the DSP determines whether the data is control or data, as shown in Figure 7.

If the Steering Bit (b15) is zero, then the data transferred on the Serial Interface is audio data. Note that since a transfer consists of 16 bits, this allows 15-bit precision for audio data.

If STR is one, the data transferred on the Serial Interface is control information. If the RNW bit is a zero, the data written by the external DSP is stored by the CS6400 in the indicated destination register, and simultaneously, the state of the destination register before the write is read back into the DSP. If RNW is one, the data written by the external DSP is ignored.
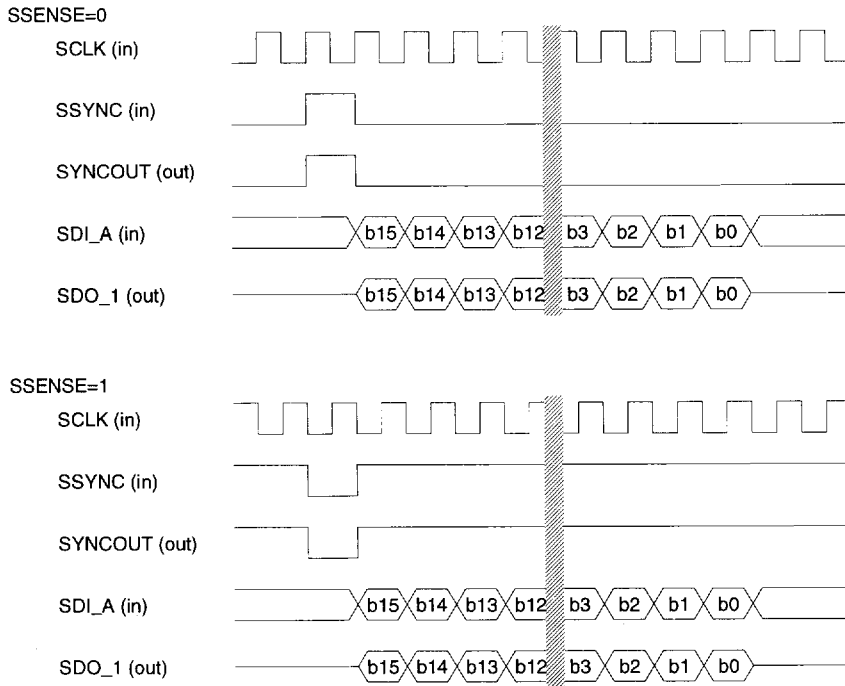
Figure 6. Serial Port Timing for Pulsed Sync Mode (Modes 2 and 4)

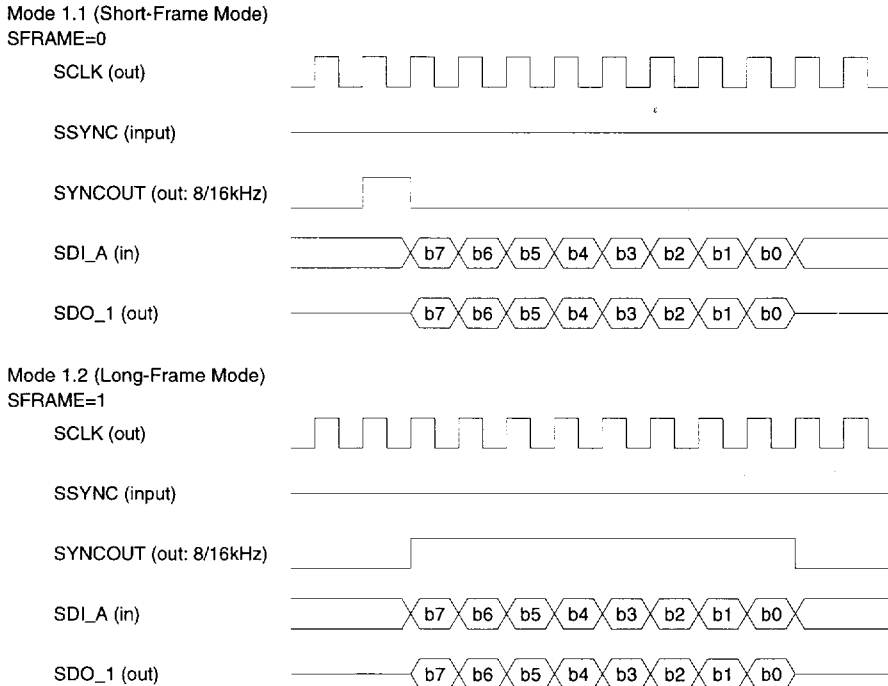Figure 7. Audio and Control Transfer for 16-bit Data Modes
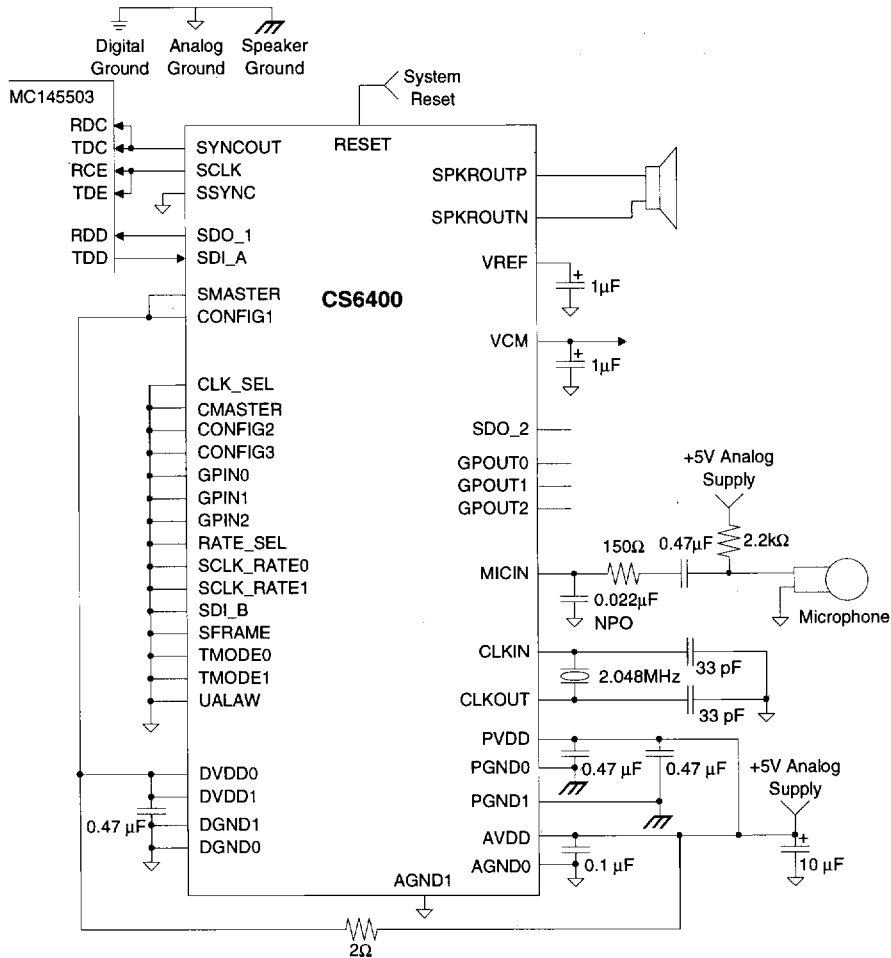
Figure 8. External Codec Connection Diagram

Note that only one control word or one data word may be transferred in a sample time, meaning that no audio data is transferred in sample times where control information is transferred. In such sample times, the CS6400 will reuse (double-sample) the audio data from the previous sample time. As a result, to minimize distortion of the audio signal, control transactions should be made infrequently.

Interfacing to an external codec

In applications like speakerphones, a DSP is normally not present. In such cases, it is possible to connect the CS6400 directly to an external network codec (like the Motorola MC145503). The interface circuit in this case is shown in Figure 8.

Mode 1.1 (Short-Frame Mode)
SFRAME=0

SCLK (out)

SSYNC (input)

SYNCOUT (out: 8/16kHz)

SDI_A (in)   b7 b6 b5 b4 b3 b2 b1 b0

SDO_1 (out)   b7 b6 b5 b4 b3 b2 b1 b0

Mode 1.2 (Long-Frame Mode)
SFRAME=1

SCLK (out)

SSYNC (input)

SYNCOUT (out: 8/16kHz)

SDI_A (in)   b7 b6 b5 b4 b3 b2 b1 b0

SDO_1 (out)   b7 b6 b5 b4 b3 b2 b1 b0

Figure 9. External-Codec Mode Timing (Mode 1)

Interfacing the CS6400 to an external codec (Mode1) is like interfacing to an external DSP (Mode2), except that SSYNC and SCLK are sourced by the CS6400 (i.e., SMASTER=1), and CLKIN is generated locally by connecting a crystal between CLKOUT and CLKIN. The timing for these signals is illustrated in Figure 9.

Unlike audio-data samples in Mode 2, audio-data samples in Mode 1 are 8 bits (μ–law or A-law companded). No control information can be transferred in Mode 1, so there is no control/data steering bit. Also note that since control information cannot be transferred, the default settings of the control registers are used.

Another difference between Mode 1 and Mode 2 is that in Mode 1, 160 echo-canceller taps (out of the available 512) are allocated to network-echo cancellation ("NEC" in Figure 3).

Interfacing to a network backplane

Interfacing the CS6400 to a network backplane is similar to interfacing the CS6400 to DSPs and external codecs. Like an external codec, a network backplane normally does not transfer control data over the SSI to the CS6400; instead, it uses the default control settings. Like an external DSP, the backplane sources SSYNC and SCLK (i.e., SMASTER=0).

In network (TSAC) applications, up to 16 CS6400s may be connected to a single backplane serial interface, providing up to 16 independent 64 ms channels, or 32 independent 32 ms channels.

The hardware connection to the CS6400 depends on the operating mode. For Mode 5 applications (i.e., a single serial port), the hardware connection is as shown in Figure 10. For Mode 6 applications (i.e., a dual serial port), the hardware connection is as shown in Figure 11.

Signal timing for Mode 5 applications is shown in Figures 12-15. As shown in these figures, the transactions for a particular sample time are initiated by a framing pulse from the TSAC. During the framing pulse, the CS6400 connected to the TSAC will make at least two transactions on the serial bus. This CS6400 will then send a similar framing pulse (via SYNCOUT) to the next CS6400 in the chain, which will also make at least two transactions. This CS6400 will send a framing pulse to the next CS6400, and so forth.
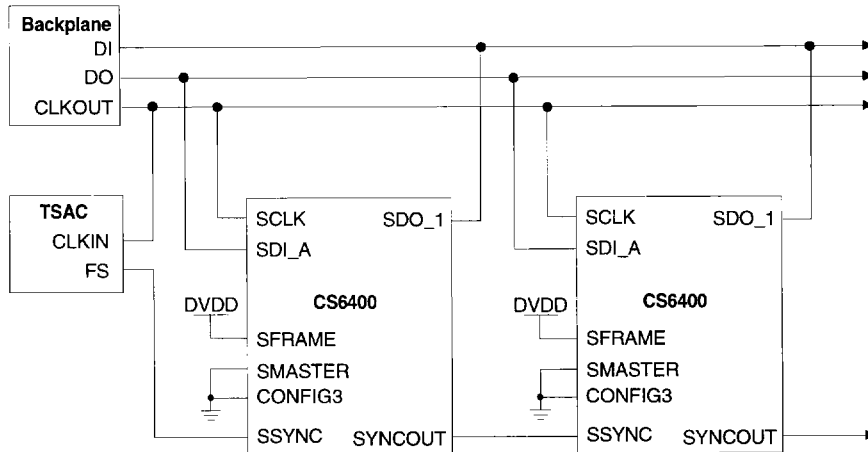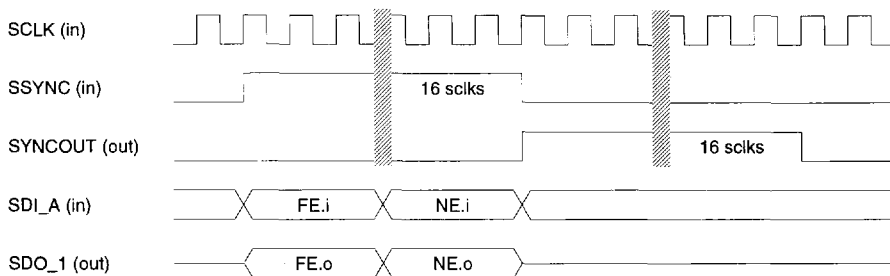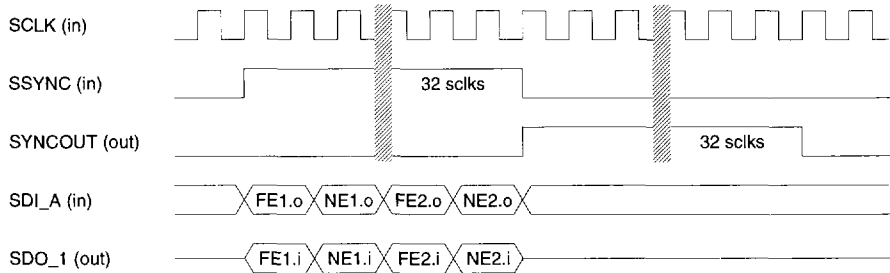
Figure 10. Network Connection Diagram (Mode 5)
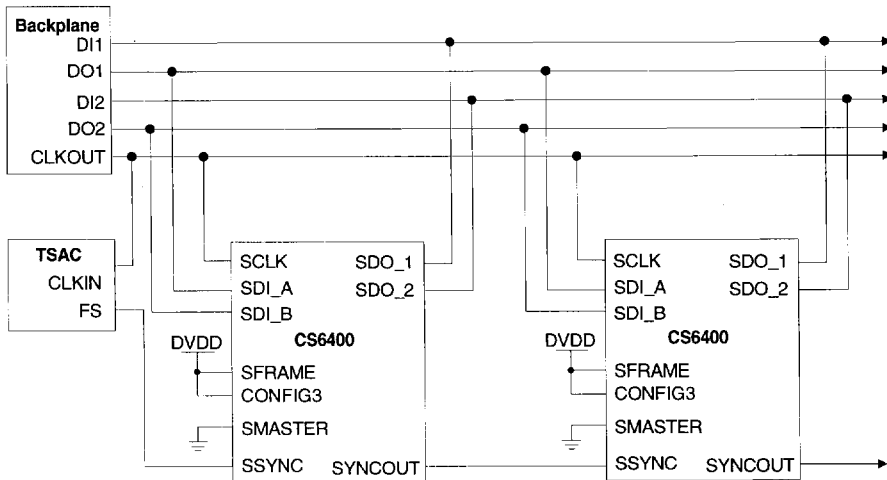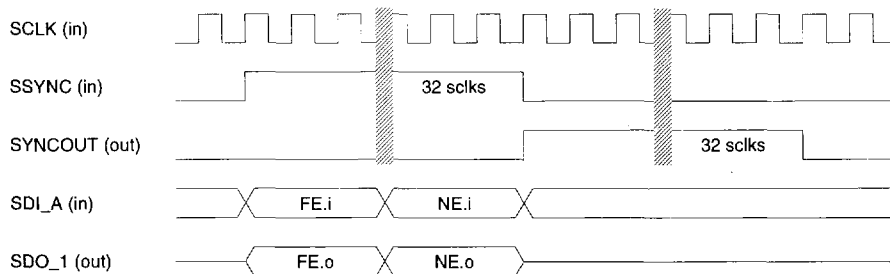
Figure 11. Network Connection Diagram (Mode 6)

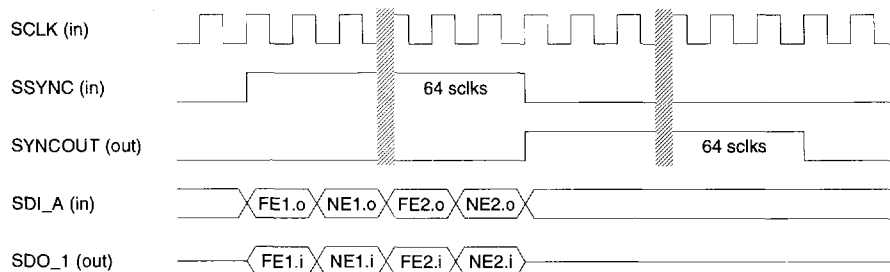**Figure 12. Network mode with 1 channel, 8-bit data (Mode 5.1)**

Figure 13. Network mode with 2 channels, 8-bit data (Mode 5.2)

6

Figure 14. Network mode with 1 channel, 16-bit data (Mode 5.3)

Figure 15. Network mode with 2 channels, 16-bit data (Mode 5.4)

For Mode 6 applications, the hardware connections are shown in Figure 11. In this case, two serial parts are used, doubling the data rate between the backplane and the CS6400. Signal timing for Mode 6 is shown in Figure 16-19.

In Modes 5 and 6, serial-data transactions may be 8 bits or 16 bits. Eight-bit data is always μ-law or A-law companded, and contains no control information.

Operating Modes

### Reset Mode

Reset may be asserted either by setting the RESET pin high, or by setting the RST bit in control register SSI_CR0. The only functional difference between these two operations is that setting the RESET pin clears the RST bit. During Reset, all chip functions are halted except for the Serial Interface, though writes to any control bit except RST are ignored. Power down is not enabled.

Upon exiting Reset, control registers and RAMs are cleared, and then control constants are loaded into Data RAM.
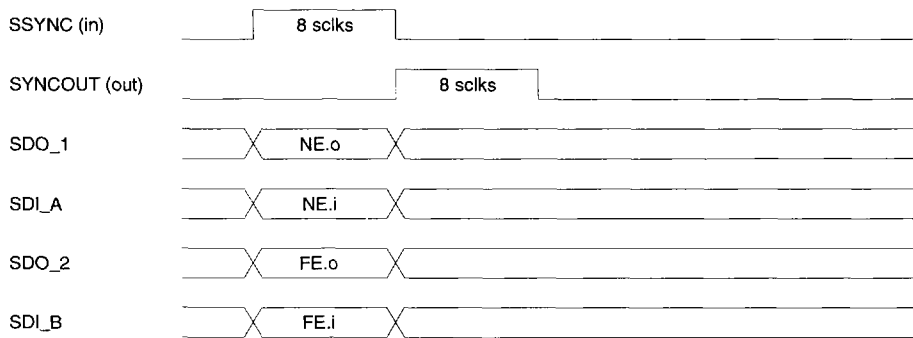
Figure 16. Network mode with 1 channel, 8-bit data (Mode 6.1)
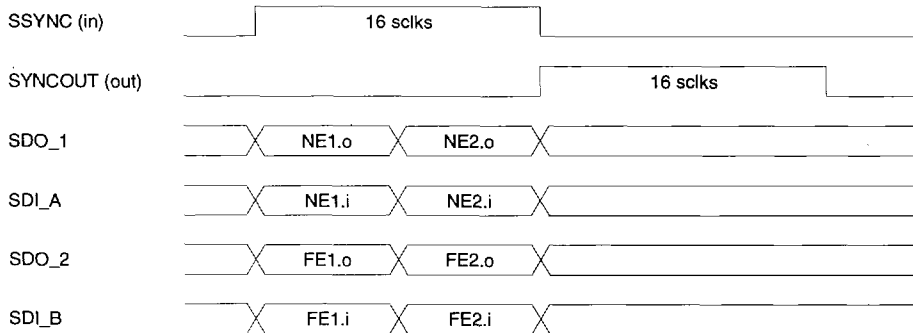
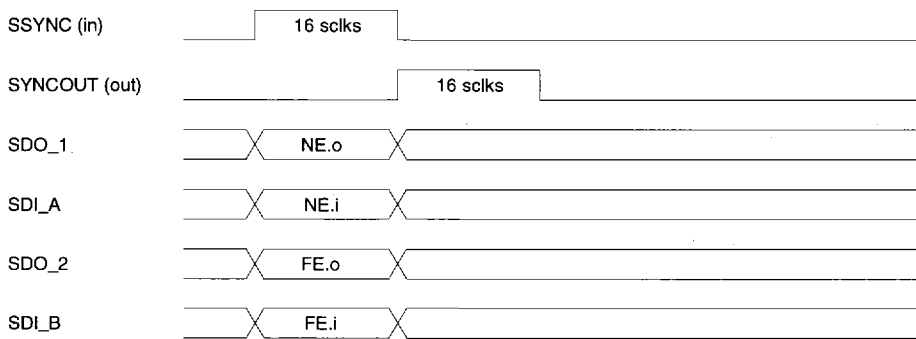Figure 17. Network mode with 2 channels, 8-bit data (Mode 6.2)

Power-Down Mode

Power Down is initiated by setting the "SLP" bit in register SSI_CR0. In Power Down, the CPU and the AFP are powered down, but the SSI and the Codec are still operational.

Since the SSI and the Codec are active during Power Down, it is possible to serially transfer audio and control data while SLP is asserted, bypassing the CPU and AFP. Note, however, that since the CPU is powered down, no scaling is performed on the ADC input, no echo is cancelled, and audio data is not companded. Note also that audio data transfers during power down are possible only in Mode 2.

Isolated Modes

Modes 1 and 2 are the "Isolated" modes for the CS6400. In the Isolated modes, a single CS6400 is connected either to an external codec or to an external DSP. In the Isolated modes, only one data or control transaction may occur in any particular sample time.

Figure 18. Network mode with 1 channel, 16-bit data (Mode 6.3)
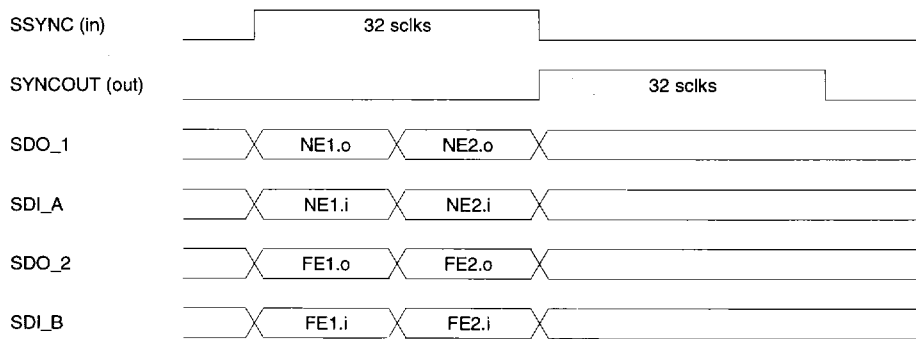
Figure 19. Network mode with 2 channels, 16-bit data (Mode 6.4)

Cascaded Modes

Modes 3 and 4 are the "Cascaded" modes for the CS6400. In the Cascaded modes, two CS6400s are connected together to double the effective adaptive-filter length, and to potentially provide a second codec. With two CS6400's, up to 128 ms of echo can be cancelled at an 8 kHz sample rate, and up to 64 ms can be cancelled at a 16 kHz sample rate.

Mode 3 is used when the interface to the far end is analog. In this case, the codecs in both the master CS6400 and the Slave CS6400 are used: the codec in the Master CS6400 is used for the far-end acoustic interface, and the codec in the slave is used as the near-end interface. The serial-port connections for the Mode 3 are shown in Figure 20. Note that in Mode 3, the 26 dB microphone gain stage in the Master CS6400 is bypassed.

In Mode 3, 20 ms of the available 64 ms are allocated to network echo cancellation when the 8 kHz sampling rate is selected. The network canceller is disabled when the 16 kHz sampling rate is selected.

Mode 4 is used when an external DSP is present. In mode 4, the codec on the Master CS6400 is typically bypassed, meaning that the audio data from the far end is passed to the CS6400 digitally. Alternatively, the codec on the Master CS6400 may be used as the far-end acoustic interface, with control information being provided by the DSP. In this case, acoustic data from the external DSP is ignored. As in Mode 3, the 26 dB microphone gain stage in the Master CS6400 is bypassed. The serial-port connections for the Mode 4 are shown in Figure 21.
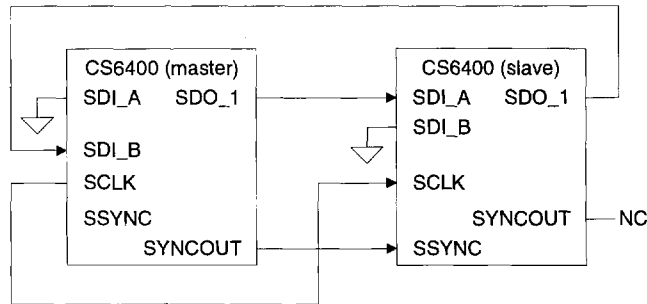
Figure 20. Cascaded Mode (Mode 3)
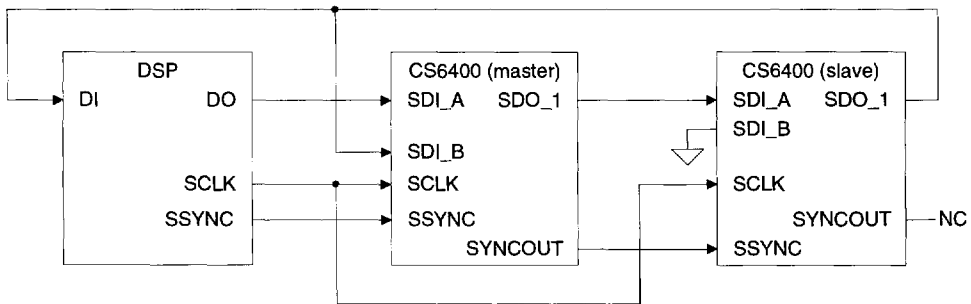
Figure 21. Cascaded Mode (Mode 4)

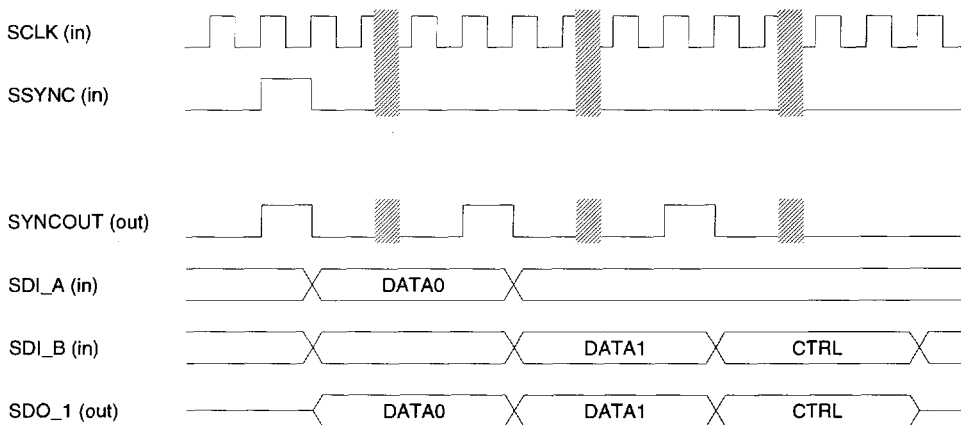| Time | Host DSP | | Master | | Slave | |
Slot	DI	DO	SDI	SDO_1	SDI	SDO_1
1	Conv		Conv	Conv	Conv	Conv
2	NE In		NE In			NE In
3	Ctrl, R1		Ctrl, R1	Ctrl, R1	Ctrl, R1	Ctrl, R1
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
2/6/14						
3/7/15						
4/8/16	FE Out	FE In	FE In	Last M	Last M	FE Out

Table 2. Serial-Interface Transactions in Cascaded Mode (Mode 4)

In Mode 4, 20 ms of the available 64 ms are allocated to network echo cancellation when both the 8 kHz sampling rate is selected and the codec on the Master CS6400 is used. The network canceller is disabled when the 16 kHz sampling rate is selected.

In Mode 3 and Mode 4, a sample time is started when the 16-bit far-end data sample is transferred by the DSP to the Master CS6400. In the ensuing sample time, the two CS6400s exchange convolution results, transparent to the DSP (see Table 2). In the next time slot, the Slave passes the near-end data sample to the Master. To end the transactions for a sample time, the Master sends control information to the Slave, again transparent to the DSP, as illustrated in Figures 22 and 23.

Data must be exchanged quickly between the Master and the Slave to allow time for processing in the CS6400s. In particular, the serial bit rate must be at least 1.024 MHz in Cascaded Mode. Note that the number of time slots present in a sample time is a function of the sampling rate and the serial data rate (see Table 2). For example, with an 8 kHz sampling rate and a 2.048 MHz serial data rate, 16 time slots are present in a sample time. With a 16 kHz sample rate and a 1.024 MHz serial data rate, four time slots are present in a sample time.

Figure 22. Cascaded Master Timing (Mode 3)

SCLK (out)

SSYNC (in)

SYNCOUT (out)

SDI_A (in)   DATA0   DATA1   CTRL

SDO_1 (out)   DATA0   DATA1   CTRL
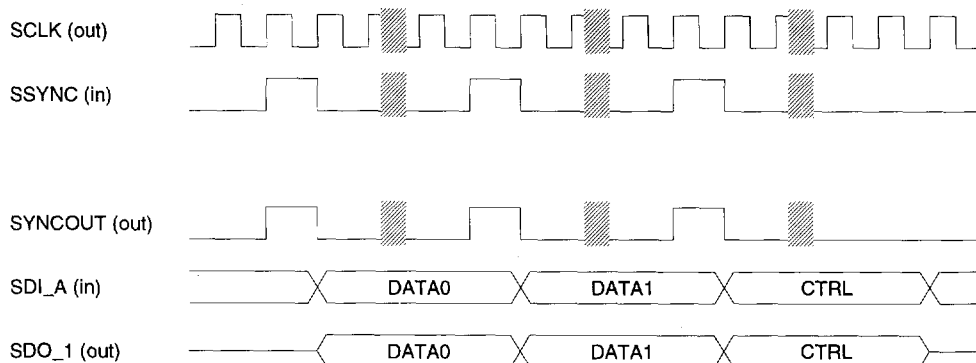
Figure 23. Cascaded Slave Timing (Mode 3)

Control Register Definitions

The CS6400 has four control registers that are accessible via the SSI, which allow a user to monitor and control the behavior of the CS6400. Note that these registers are accessible only when an external DSP is connected to the SSI. Even without a DSP, however, some visibility and control is provided by the GPIN/OUT pins (see PIN DESCRIPTIONS).

The following tables explain the four registers accessible by the serial interface in 16-bit modes. These registers are accessed by setting b15 high. The state of b14 indicates whether the register access operation is a read (high) or a write (low). Bits b13 and b12 together address the register as follows:

In the following tables describing each bit of the control registers, the bit names of each 12-bit register are at the top of the page. The Reset state of these registers is immediately below that. The Reset state is also noted by an "R" beside the appropriate value in the "value" column.

b13 : b12	Register
00	SSI_CR0
01	SSI_CR1
10	SSI_CR2
11	SSI_CR3

Register SSI_CR0

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RST	SLP	SETS	NECD	FHPD	NHPD	CE	NECS	GBC1	GBC0	AECB1	AECB0
0	0	0	0	0	0	0	0	1	0	1	0

This register is read from the SSI by the CPU only upon exit from Reset and Sleep. This register is cleared at reset except for D3-D0 (see below).

BIT	NAME	VALUE		FUNCTION
RST	Reset	0	R	Normal operation.
		1		Control registers and RAMs are cleared, and then control constants are loaded into Data RAM. SSI is still operational, though writes to any control bit except RST are ignored.
SLP	Sleep	0	R	Normal operation.
		1		The CPU and AFP on the CS6400 are powered down. Control registers and RAMs are unaffected. Serial Data transactions that occur during power down are transferred directly between the SSI and the codec, bypassing the CPU. As a result, echo is passed uncancelled.
SETS	Saved-ERL Threshold Select			After reset, the CS6400 will operate in half duplex until the echo canceller(s) have adequately converged. Saved-ERL Threshold Select (SETS) determines the ERLE level required before the CS6400 will transition from half duplex to full
		0	R	duplex.
		1		TBD
				TBD
NECD	NEC Disable	0	R	In Modes 1 & 3, 20 ms of the available 64 ms of EC taps are allocated by default to network echo cancellation.
		1		No taps are allocated to network echo cancellation.
FHPD	FE_IN High-Pass Disable	0	R	A high-pass filter $((1-D)/(1-0.75D))$ is inserted in the far-end input signal path.
		1		This filter is bypassed.
NHPD	NE_IN High-Pass Disable	0	R	A high-pass filter $((1-D)/(1-0.75D))$ is inserted in the near-end input signal path.
		1		This filter is bypassed.
CE	Companding Enable	0	R	Data in 16-bit data modes is linear (i.e., not companded).
		1		b15 is still used as the steering bit, but if b15=0, the next 8 bits are companded.
NECS	NEC-Size Select	0	R	The NEC filter covers 20 ms and the AEC covers 44 ms when the NEC is enabled.
		1		The NEC size is reduced to 10 ms, and the AEC is extended to 54 ms.

6

7

8

9

10

11

12

13

Register SSI_CR0 (cont.)

BIT	NAME	VALUE		FUNCTION
GBC1 GBC0-	Graded-Beta Count			Graded-Beta Count - These bits control the rate at which the update gain decays in the AEC as the adaptive-filter taps are updated in a particular sample time. For each setting below, some number of taps are processed, after which the update gain is divided by two. The possible settings are given below:
				<u>Taps Processed</u> <u>Equivalent path-decay rate</u>
		00		512 0 dB/ms
		01		64 0.75 dB/ms
		10	R	128 0.38 dB/ms
		11		256 0.19 dB/ms
AECB1 AECB0	AEC Beta			These bits scale the adaptive filter update gain that is present at the start of each sample time.
				<u>Update Gain</u>
		00		0.25
		01		0.5
		10	R	1.0
		11		2.0

Recommended settings for D3-D0:

Not Cascaded	Cascaded	
0001	0000	--No graded beta
0111	0111	--"dead" room/car; 0.75 dB/ms path decay
1010	1010	--medium room; (default) 0.28 dB/ms path decay
1100	1100	--large (or "live") room; 0.19 dB/ms decay

Register SSI_CR1

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CSR	CSS	NACD	NDCD	FACD	FDCD	NSD	FSD	NCC	HDD	SD	ACC
0	0	0	0	0	0	0	0	0	0	0	0

This register is read/written by the CPU every sample time. This register is cleared at Reset by the SSI.

BIT	NAME	VALUE		FUNCTION
CSR	Cascade-Slave Reset	0 1	R	Normal operation. Reset the cascade slave in Modes 3 & 4. Note that for control data to propagate from the master CS6400 to the slave, control information must be written twice.
CSS	Cascade-Slave Sleep	0 1	R	Normal operation. This bit will power down the CPU and the AFP in the cascade slave in Modes 3 & 4. Note that for control data to propagate from the master CS6400 to the slave, control information must be written twice.
NACD	NE ADC Clipping Detect	0 1	R	Near-end ADC clipping not detected. Near-end ADC clipping detected. (Modes 1-4 only)
NDCD	NE DAC Clipping Detect	0 1	R	Near-end DAC clipping not detected. Near-end DAC clipping detected. (Modes 1-4 only)
FACD	FE ADC Clipping Detect	0 1	R	Far-end ADC clipping not detected. Far-end ADC clipping detected. (Modes 3 & 4 only)
FDCD	FE DAC Clipping Detect	0 1	R	Far-end DAC clipping not detected. Far-end DAC clipping detected. (Modes 3 & 4 only)
NSD	NE Speech Detect	0 1	R	Near-end speech not detected Near-end speech detected.
FSD	FE Speech Detect	0 1	R	Far-end speech not detected. Far-end speech detected.
NCC	NEC Coefficient Clear	0 1	R	Normal operation. (or if GPIN0 is asserted) The network canceller (or channel 2 in Modes 5/6) coefficients are cleared.
HDD	Half-Duplex Disable	0 1	R	Normal operation. (or if GPIN2 is asserted) Half-duplex mode, which is normally used during convergence, is disabled.
SD	Suppression Disable	0 1	R	Normal operation. (or if GPIN1 is asserted) Supplementary suppression, which normally operates in conjunction with the echo cancellers, is disabled.
ACC	AEC Coefficient Clear	0 1	R	Normal operation. (or if GPIN0 is asserted) The acoustic canceller (or channel 1 in Modes 5/6) coefficients are cleared.

6

Register SSI_CR2

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PDC	PDSD	MGD	DV4	DV3	DV2	DV1	DV0	AV3	AV2	AV1	AV0
0	0	0	0	0	0	0	0	0	0	0	0

This register is cleared at Reset by the SSI. This register is read/written by the CPU every sample time.

BIT	NAME	VALUE		FUNCTION
PDC	Power Down Codec	0	R	Normal operation.
		1		The entire codec is powered down.
PDSD	Power Down Speaker Driver	0	R	Normal operation.
		1		Only the speaker driver in the codec is powered down.
MGD	Microphone 26 dB Gain Disable	0	R	Normal operation.
		1		The 26 dB microphone preamp is bypassed.
DV4-DV0	DAC Volume	00000 . . 11111	R	DAC volume control is implemented in the Codec, with the attenuation being -2.5 dB times the DAC-volume value.
AV3-AV0	ADC Volume	0000 . . 1111	R	ADC volume control is implemented in the CPU, with the attenuation being -3 dB times the ADC-volume value.

Register SSI_CR3 (Test Register)

This register allows real-time access to the CPU data RAM.

To read a particular location, the external DSP will write the address of the desired RAM location into SSI_CR3. The CPU data RAM is only 128 words, so only the seven least-significant bits of the 12-bit word are used for address. The most-significant bit indicates if the access is for the 12 most-significant data bits, or for the 12 least-significant bits. The next most-significant bit indicates write or read.

If the access is a read, the requested CPU-RAM data item is placed in the control register so that it can be read by the external DSP in the next sample time from SSI_CR3.

If the access is a write, the DSP will write the address in one sample time, and then it will write the data that it wishes to write into CPU data RAM in the next sample time. Only 12 bits of the 16-bit data item are affected; the other four bits are unchanged.

If two DCECs are connected in cascade mode, b9 indicates whether a read/write request is for the master or the slave DCEC. In cascade mode, all commands should be sent twice to allow them to propagate to the slave. Read data is read by the DSP two transactions after the second time a command is transmitted.

If bit 8 is set on a read, the revision code is returned instead of RAM data (b11 and b7-0 are ignored). For first silicon, the revision code is "0x101". The first nibble is incremented when an all-layer change is made; the lower byte is incremented on a metal revision.

This register is cleared at reset by the SSI.

	Address written by DSP	Data Written by DSP	Data Read by DSP
D11	top12/!bottom12	data, b15/b11	data, b15/b11
D10	write/!read	data, b14/b10	data, b14/b10
D9	master/!slave	data, b13/b9	data, b13/b9
D8	rev code/!rc	data, b12/b8	data, b12/b8
D7	must be 0	data, b11/b7	data, b11/b7
D6	addr, b6	data, b10/b6	data, b10/b6
D5	addr, b5	data, b9/b5	data, b9/b5
D4	addr, b4	data, b8/b4	data, b8/b4
D3	addr, b3	data, b7/b3	data, b7/b3
D2	addr, b2	data, b6/b2	data, b6/b2
D1	addr, b1	data, b5/b1	data, b5/b1
D0	addr, b0	data, b4/b0	data, b4/b0

Detailed Power Supply Connections

Figure 24 shows the detailed power supply connections. The CS6400 requires a clean analog quality +5V supply. The digital supply for the CS6400 should be derived from the system clean analog supply, and should not be connected directly to the board-level digital 5V supply.

Schematic & Layout Review Service

Confirm Optimum
Schematic & Layout
Before Building Your Board.

For Our Free Review Service
Call Applications Engineering.

C a l l : (5 1 2) 4 4 5 - 7 2 2 2

Grounding and Layout

The CS6400 requires very careful attention to layout, power supplies, and decoupling to achieve rated performance. Extensive use of ground planes and ground-plane fill is recommended. The system circuit board should be partitioned into a digital region and an analog region, each with its own, non-overlapping, ground plane. The CS6400 should be completely over the analog ground plane, close to the digital region. The package should be oriented so that the digital pins face toward the digital region of the board. Figure 25 shows the general guidelines for proper layout.
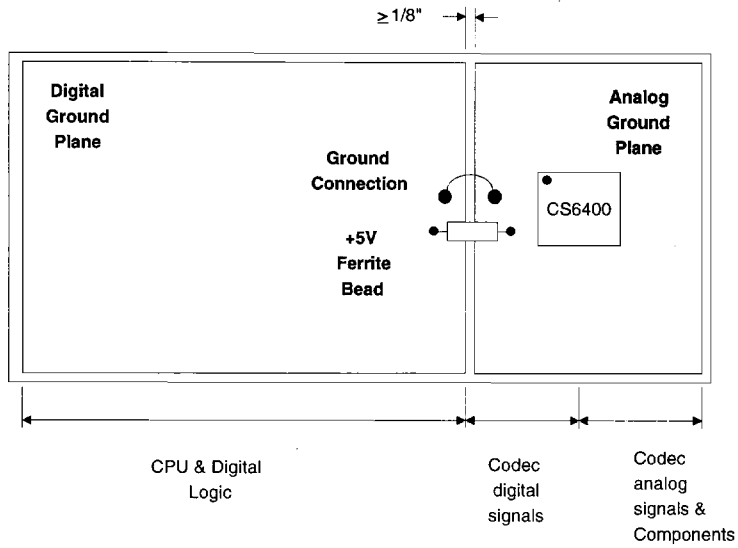
The power and ground connections for the speaker (PVDD and PGND) should be routed separately from the analog power and ground planes to prevent the high speaker currents from flowing in the same ground plane as the microphone signal.

Note: In applications where the codec is not used no separate ground plane is required. The CS6400 may reside on the digital ground plane in this case.
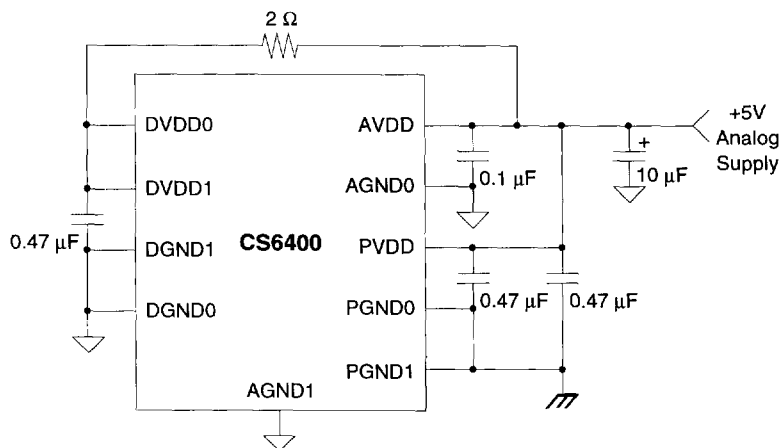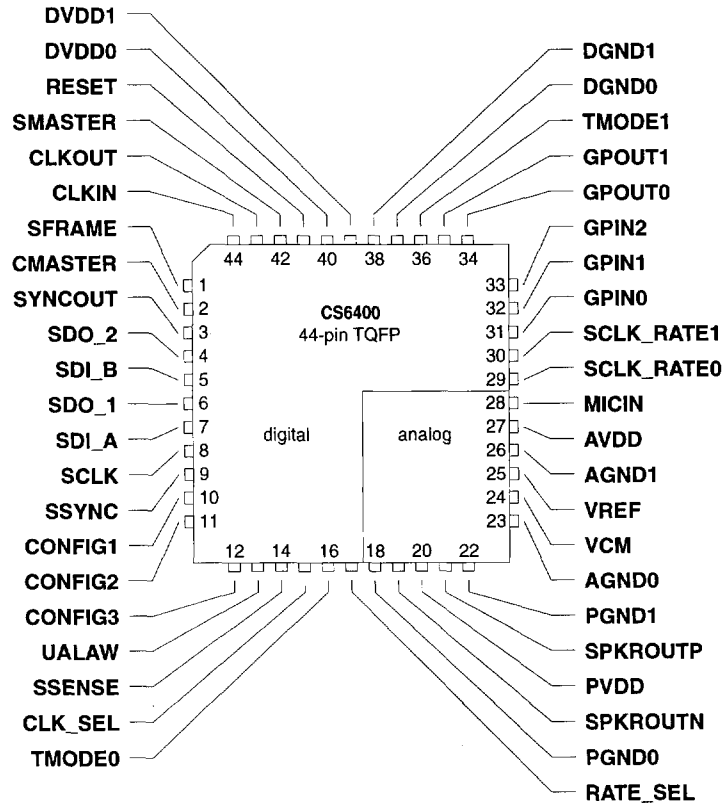
Figure 24. Power Supply Connections

Figure 25. Suggested Layout Guideline

6

PIN DESCRIPTIONS

DVDD1
DVDD0
RESET
SMASTER
CLKOUT
CLKIN
SFRAME
CMASTER
SYNCOUT
SDO_2
SDI_B
SDO_1
SDI_A
SCLK
SSYNC
CONFIG1
CONFIG2
CONFIG3
UALAW
SSENSE
CLK_SEL
TMODE0

CS6400
44-pin TQFP

digital   analog

44 42 40 38 36 34
1
2
3
4
5
6
7
8
9
10
11
12 14 16 18 20 22

33
32
31
30
29
28
27
26
25
24
23

DGND1
DGND0
TMODE1
GPOUT1
GPOUT0
GPIN2
GPIN1
GPIN0
SCLK_RATE1
SCLK_RATE0
MICIN
AVDD
AGND1
VREF
VCM
AGND0
PGND1
SPKROUTP
PVDD
SPKROUTN
PGND0
RATE_SEL

Power Supply

AGND0 - Analog ground, PIN 23
    Analog ground.

AGND1 - Analog ground, PIN 26
    Analog ground.

AVDD - Analog supply, PIN 27
    +5V Analog supply.

DGND0 - Digital ground, PIN 37
    Digital ground.

DGND1 - Digital ground, PIN 38
    Digital ground.

DVDD0 - Digital supply, PIN 40
> Digital +5V supply.

DVDD1 - Digital supply, PIN 39
> Digital +5V supply.

PGND0 - Speaker-driver ground, PIN 18
> Speaker driver ground.

PGND1 - Speaker-driver ground, PIN 22
> Speaker driver ground.

PVDD - Speaker-driver supply, PIN 20
> Speaker-driver +5V supply.

Analog I/O

MICIN - A/D input, PIN 28
> Audio analog input.

SPKROUTN - D/A minus output, PIN 19
> Negative differential speaker-driver output. The voltage on SPKROUTN will decrease if the DAC value is increased.

SPKROUTP - D/A plus output, PIN 21
> Positive differential speaker-driver output. The voltage on SPKROUTP will increase if the DAC value is increased.

VCM - Voltage reference common out, PIN 24
> A stable output voltage for setting the bias level for external analog circuits. No time-varying loads should be attached to VCM. Output voltage is about 1V into a load of not less than $100k\Omega$.

VREF - Voltage reference bypass out, PIN 25
> Voltage reference used internal to the CS6400. Must be connected to AGND0 via a 1 µF capacitor. Connections should be made with short, fat traces.

Test

TMODE0 - Test-mode select pin, PIN 16
> TMODE0 is used in conjunction with TMODE1 to set the test mode. TMODE0 should be grounded in nomal operation.

TMODE1 - Test-mode select pin, PIN 36
> TMODE1 is used in conjunction with TMODE0 to set the test mode. TMODE1 should be grounded in normal operation.

6

Serial Digital I/O

RATE_SEL - Test input, PIN 17
> If RATE_SEL is low, the Codec sampling rate and the SSYNC pulse frequency are 8 kHz; if RATE_SEL is high, they are 16 kHz.

SCLK - Serial clock, PIN 8
> SCLK is the bit clock for the serial interface. It may be an output or an input, depending on the state of SMASTER, and may operate at 256 kHz, 384 kHz, 1.024 MHz, or 2.048 MHz depending on the states of SCLK_RATE0, SCLK_RATE1 and SMASTER.

SCLK_RATE0 - SCLK frequency control, PIN 29
> Used in conjunction with SCLK_RATE1 to set the SCLK frequency when the CS6400 is a timing slave. Possible frequencies are 2.048 MHz, 1.024 MHz, 384 kHz, and 256 kHz, for SCLK_RATE1:SCLK_RATE0 being 11, 10, 01, and 00, respectively. However, if the CS6400 is a timing master (i.e., SMASTER is high), the SCLK frequency may only be 2.048 MHz, so in this case, SCLK_RATE0 must be high.

SCLK_RATE1 - SCLK frequency control, PIN 30
> Used in conjunction with SCLK_RATE0 to set the SCLK frequency when the CS6400 is a timing slave. Possible frequencies are 2.048 MHz, 1.024 MHz, 384 kHz, and 256 kHz, for SCLK_RATE1:SCLK_RATE0 being 11, 10, 01, and 00, respectively. However, if the CS6400 is a timing master (i.e., SMASTER is high), the SCLK frequency may only be 2.048 MHz, so in this case, SCLK_RATE1 must be high.

SDI_A - Serial data in, PIN 7
> SDI_A is the primary serial-data input to the CS6400.

SDI_B - Serial data in, PIN 5
> SDI_B is the secondary serial-data input to the CS6400. This input is used only in cascaded and network modes.

SDO_1 - Serial data out, PIN 6
> Primary serial output.

SDO_2 - Serial data out, PIN 4
> Secondary serial output. Used only in two-channel network modes.

SFRAME - SSYNC frame/pulse control, PIN 1
> If SFRAME is high, SSYNC is high during serial data transactions. If SFRAME is low, SSYNC is pulsed before the start of a serial-data transaction.

SMASTER - SSYNC direction control, PIN 42

SMASTER is used in conjunction with other configuration-control pins to control operating mode (see Table 1). If SMASTER is high, the CS6400 is a timing master, meaning that SCLK is an output, and the SCLK rate is set by the on-board crystal oscillator (nominally 2.048 MHz). If SMASTER is low, the CS6400 is a timing slave, meaning that the SCLK is an input, and the SCLK rate is set by the external DSP, but SCLK_RATE0 and SCLK_RATE1 must be set to reflect the nominal SCLK rate.

SSENSE - SSYNC Sense control, PIN 14

SSENSE controls the sense of SCLK, SSYNC, and SYNCOUT. If SSENSE is high, SSYNC and SYNCOUT are negative logic, and SCLK samples on the rising edge. If SSENSE is low, SSYNC and SYNCOUT are positive logic, and SCLK samples on the falling edge.

SSYNC - Sync signal for serial port, PIN 9

SSYNC is the serial-data sync strobe used when the CS6400 is a system-timing slave.

SYNCOUT - SSYNC cascade out for TSAC applications, PIN 3

SSYNC is the serial-data sync strobe used when the CS6400 is a system-timing master. It is also used when the CS6400 is a system-timing master in network modes and in cascaded modes.

UALAW - PIN 13

When UALAW is high, 8-bit serial data is μ-law; when UALAW is low, 8-bit serial data is A-law.

CONFIG1 - Configuration-control input, PIN 10

CONFIG1 is used in conjunction with other configuration-control pins to control operating mode (see Table 1).

CONFIG2 - Configuration-control input, PIN 11

CONFIG2 is used in conjunction with other configuration-control pins to control operating mode (see Table 1).

CONFIG3 - Configuration-control input, PIN 12

CONFIG3 is used in conjunction with other configuration-control pins to control operating mode (see Table 1).

CMASTER - Cascade Master Configuration Control, PIN 2

CMASTER is used in conjuction with other configuration-control pins to control operating mode (see Table 1).

Miscellaneous

CLK_SEL - PIN 15

If CLK_SEL is high, the CS6400 PLL is bypassed, and the CS6400 24.576 MHz internal system clock is supplied via CLKIN. This mode is intended to facilitate production test.

CLKIN - System input clock from external master, PIN 44

If the CS6400 is a system-timing master, a 2.048 MHz clock-crystal circuit is connected between CLKIN and CLKOUT. If the CS6400 is a system-timing slave, CLKIN must be grounded.

CLKOUT - System output clock, PIN 43

If the CS6400 is a system-timing master, a 2.048 MHz clock-crystal circuit is connected between CLKIN and CLKOUT. Otherwise, CLKOUT is unconnected.

GPIN0 - General-purpose input, PIN 31

When GPIN0 is high, all echo canceller coefficients are cleared.

GPIN1 - General-purpose input, PIN 32

When GPIN1 is high, supplementary suppression is disabled.

GPIN2 - General-purpose input, PIN 33

When GPIN2 is high, half-duplex mode (which is used during convergence) is disabled.

GPOUT0 - General-purpose outputs, PIN 34

GPOUT0 is high while clipping is detected on the ADC input.

GPOUT1 - General-purpose outputs, PIN 35

GPOUT1 is high while the CS6400 is in half-duplex mode during initial convergence.

RESET - System reset, PIN 41

RESET must be asserted high for at least two SCLK periods after powerup to place the CS6400 in a known state.

PARAMETER DEFINITION

Anti-Alias Rejection
 The rejection of input frequencies in the frequency range ±Fs/2 of all multiples of the input sample rate (64 x Fs). This rejection is almost solely dependent on the external input RC.

Audible (<20kHz) Noise
 The DAC audible noise floor. Measured by applying a -60dB, 1kHz sine wave. S/(N+D) is then measured (over a 20Hz to 20kHz bandwidth). Then add 60dB to the answer, to compensate for the -60dB signal level.

Convergence
 The process by which an echo canceller improves its path estimate, thereby improving its echo return-loss enhancement. Convergence is complete once the echo return-loss enhancement reaches its best value for a given environment.

Differential Nonlinearity
 The worst case deviation from the ideal codewidth. Units in LSB.

ERLE
 Echo signal-power reduction (Echo Return-Loss Enhancement) provided by an echo canceller. Maximum ERLE for an echo canceller is dependent on training-signal statistics and echo-path attributes. Units in dB.

6

Frequency Response
 Worst case variation in output signal level versus frequency over the passband (20Hz to 0.45Fs), referenced to the level at 1kHz. Units in dB.

Instantaneous Dynamic Range
 IDR is the ratio of a full-scale rms signal to the rms noise available at any instant in time, without changing the input gain or output attenuation settings. It is measured using S/(N+D) with a 1 kHz, -60 dB input signal, with 60 dB added to compensate for the small input signal. Use of a small input signal reduces the harmonic distortion components to insignificance when compared to the noise. Units in dB.

Integrated Inaudible (>20kHz) Energy
 The integrated signal level on the analog output pin after a 20kHz hi-pass filter. Zero digital input into the DAC. Units in mVrms.

Inter-Section Isolation
 For an ADC, the amount of 1 kHz signal present on the output of the grounded input ADC, with 1 kHz 0 dB signal present on each other ADC/DAC. For a DAC, the amount of 1 kHz signal present on the output of a zero input DAC, with 1kHz 0dB signal present on each other ADC/DAC. Units in dB.

Offset Error

For the ADC, the deviation of the output code from the mid-scale with the selected input at VCM. For the DAC, the deviation of the output from VCM with mid-scale input code. Units in LSB's for the ADC and millivolts for the DAC.

Resolution

The number of bits in the input words to the DAC, and in the output words from the ADC.

Total Dynamic Range

TDR is the ratio of the rms value of a full scale signal to the lowest obtainable noise floor. It is measured by comparing a full scale signal to the lowest noise floor possible in the codec (i.e., attenuation bits for the DAC at full attenuation). Units in dB.

Total Harmonic Distortion

THD is the ratio of the rms amplitude of the test signal to the rms sum of all the harmonic components. 1 kHz is used for testing. Units in dB.