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April 1st, 2010
Renesas Electronics Corporation

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HA16341NT/FP, HA16342NT/FP

Redundant Secondary Switching Power Supply Controller

REJ03F0148-0400
(Previous: ADE-204-035C)
Rev.4.00
Jun 15, 2005

Description

The HA16341NT/FP and the HA16342NT/FP are switching regulator control ICs for the off-line converters of redundant power supplies.

The HA16342NT/FP is reverse current detection less version of the HA16341NT/FP.

The HA16341NT/FP have the functions of current sharing and hot swap control for redundancy. These functions enable high efficiency and high reliability for switching power supplies.

Combination the HA16341 with the HA16141 is suitable for the redundant AC to DC converters.

Features

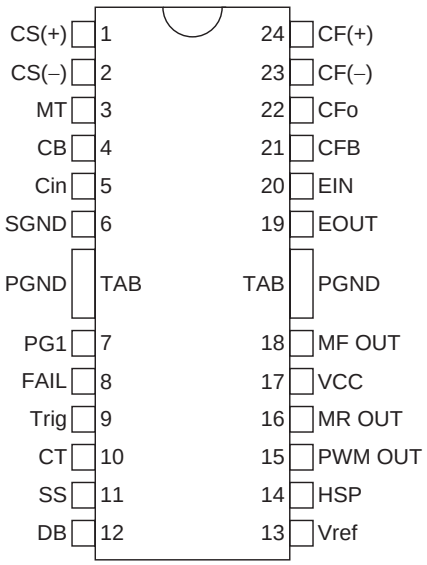
- Secondary-side synchronous rectification control
- Main switching controller
- Dead-time adjustment for synchronous rectification MOS
- Current share function with line resistance compensation
- Hot swap power MOS FET control
- Remote on/off function, FAIL output function
- Synchronized switching with primary side
- Soft start function
- Maximum duty adjustment
- Overcurrent limiting, overcurrent shutdown functions
- Reverse current detection (only the HA16341NT/FP)
- Light load detection
- OVP function
- VCC pin UVL function

Ordering Information

Type No.	Package Code
HA16341NT	DP-24TS
HA16342NT	
HA16341FP	FP-26DT
HA16342FP	

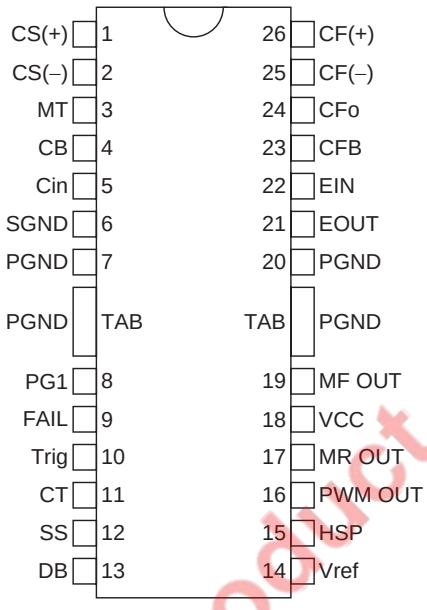
Pin Arrangement

HA16341NT, HA16342NT
(DP-24TS)



(Top view)

HA16341FP, HA16342FP
(FP-26DT)

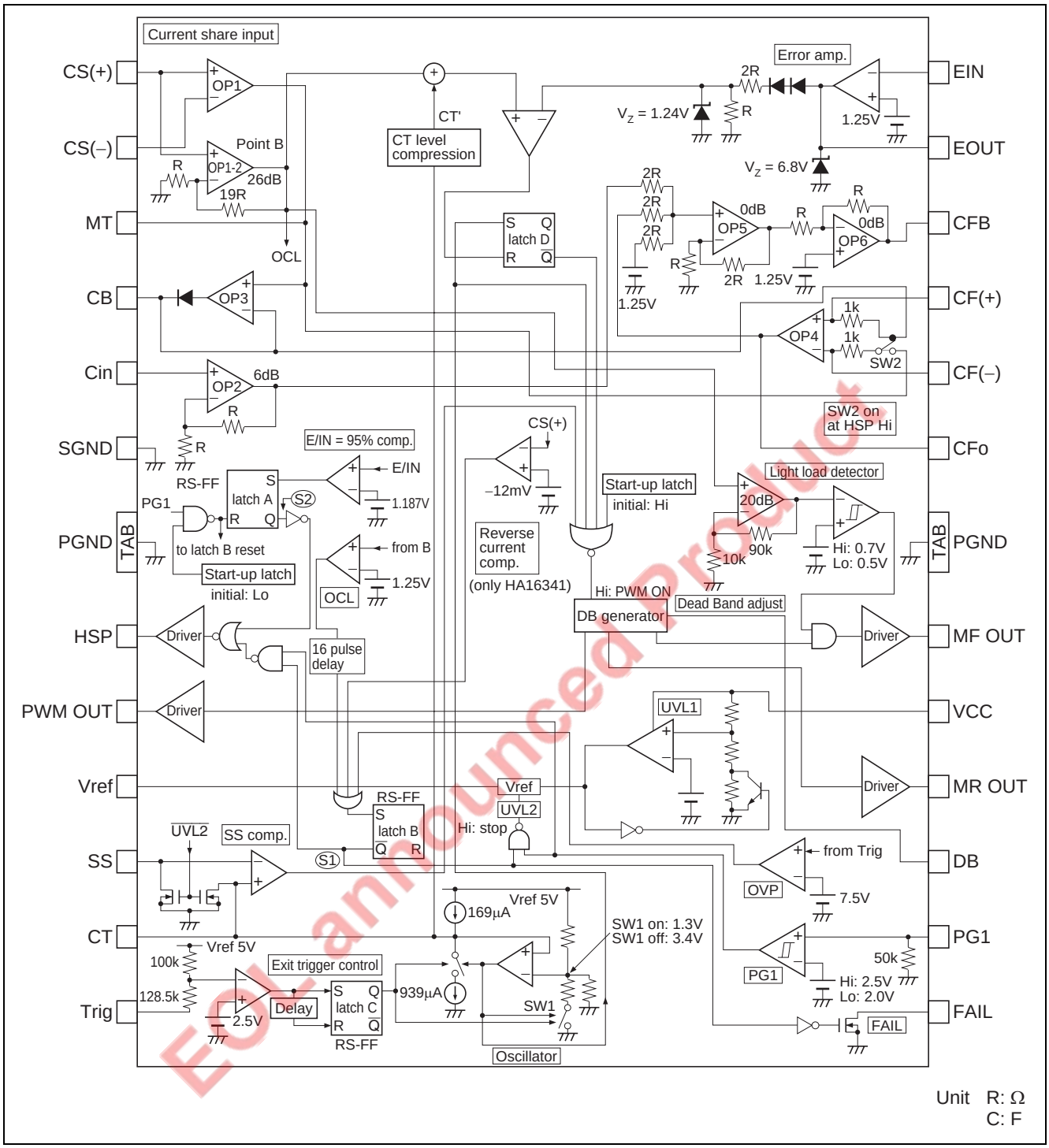


(Top view)

Pin Functions

Pin No.		Symbol	Pin Name
DP-24TS	FP-26DT		
1	1	CS(+)	Current sense amp input (+)
2	2	CS(–)	Current sense amp input (–)
3	3	MT	Current sense amp output
4	4	CB	Current bus output
5	5	Cin	Line resistance compensation input
6	6	SGND	Signal ground
7	8	PG1	Remote on/off
8	9	FAIL	FAIL output (open-drain)
9	10	Trig	External synchronization input
10	11	CT	Timing capacitance
11	12	SS	Soft start
12	13	DB	Dead band
13	14	Vref	Vref (5 V)
14	15	HSP	Hot swap output
15	16	PWM OUT	PWM output
16	17	MR OUT	MR output
17	18	VCC	Power supply voltage
18	19	MF OUT	MF output
19	21	EOUT	Error amp output
20	22	EIN	Error amp input
21	23	CFB	Current share feedback output
22	24	CFo	Current share differential amp output
23	25	CF(–)	Current share differential amp input (–)
24	26	CF(+)	Current share differential amp input (+)
TAB	TAB, 7, 20	PGND	Power ground

Block Diagram



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit	Note
Supply Voltage	VCC	18	V	
DC output current1	Io1	±0.1	A	PWM OUT *1
Peak output current1	Iopeak1	±1.0	A	PWM OUT *2
DC output current2	Io2	±0.2	A	MF OUT *1
Peak output current2	Iopeak2	±2.0	A	MF OUT *2
DC output current3	Io3	±0.1	A	MR OUT *1
Peak output current3	Iopeak3	±1.0	A	MR OUT *2
DC output current4	Io4	–	mA	CB OUT
DC output current5	Io5	±500	µA	CFB OUT
DC output current6	Io6	20	mA	FAIL OUT
DC output current7	Io7	–5.0	mA	Vref OUT
Peak output current4	Iopeak4	0.5	A	HSP sink
DC output current8	Io8	±500	µA	MT OUT
DC output current9	Io9	±500	µA	CFo OUT
DC output current10	Io10	6	mA	EOUT sink
TRIG terminal voltage	Vtrigmax	–1.5 to V_{CC}	V	
CT terminal voltage	VCTmax	–0.3 to Vref	V	
Vref terminal voltage	Vrefmax	–0.3 to Vref	V	
SS terminal voltage	Vssmax	–0.3 to Vref	V	
EIN terminal voltage	VEINmax	–0.3 to Vref	V	
EOUT terminal voltage	VEOUTmax	–0.3 to V_{CC}	V	
PG1 terminal voltage	VPG1max	–0.3 to Vref	V	
FAIL terminal voltage	VFAILmax	–0.3 to V_{CC}	V	
PWM OUT terminal voltage	VoPWMmax	–0.3 to V_{CC}	V	
MR OUT terminal voltage	VoMRmax	–0.3 to V_{CC}	V	
MF OUT terminal voltage	VoMFmax	–0.3 to V_{CC}	V	
HSP terminal voltage	VoHSPmax	–0.3 to V_{CC}	V	
CFB terminal voltage	VCFBmax	–0.3 to Vref	V	
CS(+) terminal voltage	VCS(+)max	–0.3 to Vref	V	
CS(–) terminal voltage	VCS(–)max	–0.3 to Vref	V	
MT terminal voltage	VMTmax	–0.3 to Vref	V	
Cin terminal voltage	VCinmax	–0.3 to Vref	V	

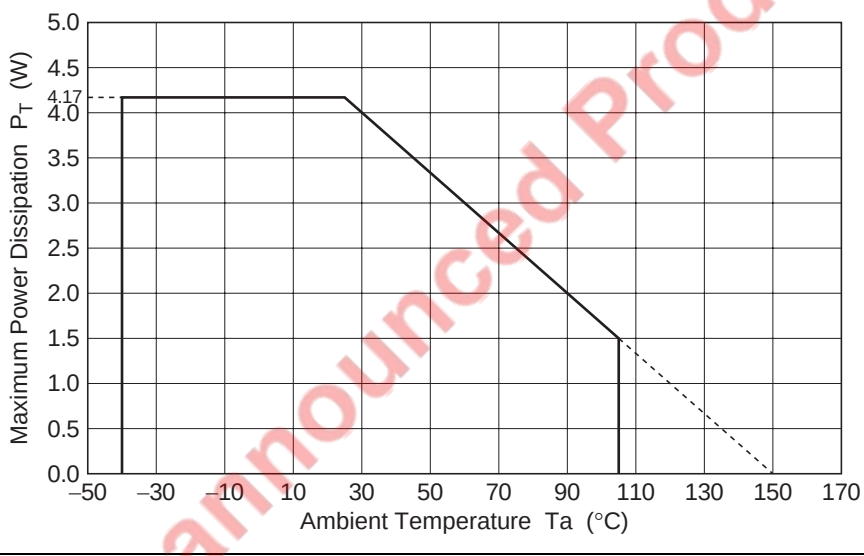
Notes: 1. V_{DS} = 10 V max. Therefore test condition must be $V_{OH} = V_{CC}$ –10 V or over , V_{OL} = 10 V or under.
2. V_{DS} = 10 V max. Pulse duration ≤ 10 ms

Absolute Maximum Ratings (cont.)

(Ta = 25°C)

Item	Symbol	Ratings	Unit	Note
CF(+) terminal voltage	VCF(+)max	–0.3 to Vref	V	
CF(–) terminal voltage	VCF(–)max	–0.3 to Vref	V	
CFo terminal voltage	VCFomax	–0.3 to Vref	V	
CB terminal voltage	VCBmax	–0.3 to Vref	V	
DB terminal voltage	VDBmax	–0.3 to Vref	V	
Maximum power dissipation	P_T	4.17	W	1
Operating temperature	Topr	–40 to +105	°C	
Storage temperature	Tstg	–55 to +150	°C	
Junction temperature	Tj	150	°C	

Note: 1. This is allowable value up to Ta = 25°C.
Derate by θj-a = 30°C/W above that temperature.
θj-a = 30°C/W is the case that HA16341NT is mounted on 30% wiring density glass epoxy board (105 mm × 76.2 mm × 1.6 mmt) and HA16341FP is mounted on a board which thermal resistance is 23°C/W because of θj-pin (SOP) = 7°C/W typ.



Electrical Characteristics

(Ta = 25°C, VCC = 12V, PG1 = 3V, Vtrig = 0V, VCS(+) = 0V, VCin = 0V, CCT = 330pF, GvOP1 = 26dB, GvOP4 = 40dB, RDB = 1.8kΩ)

- Current share

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Note
CB output Hi voltage	VCBH	2.5	–	–	V	Iosource = 300µA VCS(+) = 1V	
CB output Lo voltage	VCBL	–	–	25	mV	VCS(+) = 0V, RCB = 10kΩ	
CFB output Lo voltage	VCFBL	–	–	100	mV	Iosink = 100µA, HSP ON VCS(+) = 0V, VCB = 0.1V	
CFB output typ voltage	VCFBtyp	1.19	1.25	1.31	V	VCS(+) = 0V, VCB = 0V RfOP4 = 1kΩ, HSP ON	
OP1 input offset voltage	VioOP1	–	–	(1)	mV		1
CS(+) input bias current	IibCS(+)	–	–20	–30	µA	VCS(+) = 0V, VCS(–) = 0V	
CS(–) input bias current	IibCS(–)	–	0.2	1.0	µA	VCS(+) = 0V, VCS(–) = 0V	
Cin input bias current	IibCin	–	0.2	1.0	µA	Vcin = 0V	
OP4 input resistance	Rsin	0.75	1.00	1.25	kΩ		1, 2
Open loop gain OP1–OP6	Avo	(70)	80	–	dB		1
Band width OP1–OP6	BWCS	–	700	–	kHz		1
OCL detector threshold voltage	VthOCL	59.5	62.5	65.5	mV	CS(+) terminal voltage sensing	
Light load detector threshold Hi voltage	VthHLL	(2.0)	3.5	(5.0)	mV	CS(+) terminal voltage sensing	1
Light load detector threshold Lo voltage	VthLLL	(1.0)	2.5	(4.0)	mV	CS(+) terminal voltage sensing	1
VthLL hysteresis	dVthLL	(0.5)	1.0	(1.5)	mV		1
Reverse current detector threshold Hi voltage	VthRC	–6	–12	–18	mV	CS(+) terminal voltage sensing	3

Notes: 1. Design spec.
2. Temperature coefficient is 5400ppm/°C.
3. Only HA16341NT/FP.

- Hot swap

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Note
HSP ON threshold voltage	VthHSP	1.14	1.19	1.23	V	95% typ of reference 1.25V	
HSP charge current	IcHSP	–7	–10	–13	µA	VHSP = 5V, VEIN = 2V	
HSP output Lo voltage	VOLHSP	–	0.3	0.6	V	VEIN = 1V, Iosink = 50mA	

Electrical Characteristics (cont.)

(Ta = 25°C, VCC = 12V, PG1 = 3V, Vtrig = 0V, VCS(+) = 0V, VCin = 0V, CCT = 330pF, GvOP1 = 26dB, GvOP4 = 40dB, RDB = 1.8kΩ)

- Oscillator

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Note
Typical oscillating frequency	fosctyp	180	200	220	kHz		±10%
Maximum oscillating frequency	foscmax	400	–	–	kHz		
Typical oscillating temperature stability	dfosc	–	±5	–	%	–20°C < Ta < 85°C	1
CT charge current	Ici	–135	–169	–203	µA		±20%
CT discharge current	Icd	616	770	924	µA		±20%
Upper trip point	VthCTH	–	3.4	–	V		2
Lower trip point	VthCTL	–	1.3	–	V		
Amplitude	dVCT	–	2.1	–	V		
Exit trigger Vth	Vthtrig	–0.3	–0.5	–0.7	V		

Notes: 1. Design spec.
2. In case of external trigger control, CCT should be changed from 330 pF to 430 pF. At this synchronous and 430 pF CCT condition VthCTH becomes about 2.9 V.

- Vref

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Note
Reference voltage	Vref	4.9	5.0	5.1	V	Iosource = 1mA	±2%
Line regulation	Vref-line	–	5	20	mV	Iosource = 1mA 12V < V_{CC} < 18V	
Load regulation	Vref-load	–	5	20	mV	0 < Iosource < 3mA	
Temperature stability	dVref	–	80	–	ppm/°C	–20°C < Ta < 85°C	1

Note: 1. Design spec.

- UVL

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Note
Hi threshold voltage	VH	9.5	10.0	10.5	V		
Lo threshold voltage	VL	8.5	9.0	9.5	V		
Hysteresis	dVUVL	0.6	1.0	1.4	V		

Electrical Characteristics (cont.)

(Ta = 25°C, V_{CC} = 12V, PG1 = 3V, Vtrig = 0V, VCS(+) = 0V, VCin = 0V, CCT = 330pF, GvOP1 = 26dB, GvOP4 = 40dB, RDB = 1.8kΩ)

- PG1

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Note
PG1 threshold Hi voltage	VthHPG1	2.4	2.5	2.6	V		
PG1 threshold Lo voltage	VthLPG1	1.9	2.0	2.1	V		
Input impedance	RinPG1	(37.5)	50.0	(62.5)	kΩ		1

Note: 1. Design spec.

- FAIL

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Note
Leak current	IleakFAIL	–	–	–10	µA	VFAIL = 5V	
Output Lo voltage	VOLFAIL	–	–	0.5	V	Iosink = 10mA	

- Error amp.

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Note
Input threshold voltage	VthEIN	1.23	1.25	1.27	V	VEOUT = 1.25V	±1.6%
Input bias current	IibEIN	–	–0.2	–2.0	µA	VEIN = 2V	
Open loop gain	AvoEA	60	80	–	dB		
Band width	BWEA	(0.7)	1.4	–	MHz		1
EOUT sink current	IosinkEA	0.5	5.0	–	mA	VEIN = 1.5V, EOUT = 1.1V	
EOUT source current	IosourceEA	–100	–250	–	µA	VEIN = 1.0V, EOUT = 5V	
EOUT clamp voltage	VOHEA	5.8	6.8	7.8	V	VEIN = 1.0V	
EOUT Lo voltage	VOLEA	–	–	1.0	V	VEIN = 1.5V, Iosink = 200µA	

Note: 1. Design spec.

- PWM OUT

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Note
Output Lo voltage	VOLPWM	–	0.2	0.4	V	Iosink = 100mA	
Output Hi voltage	VOHPWM	V_{CC}–0.4	V_{CC}–0.2	–	V	Iosource = 100mA	
Rise time	trPWM	20	50	100	ns	CL = 3300pF	
Fall time	tfPWM	20	50	100	ns	CL = 3300pF	
Maximum duty	Dmax	58	65	72	%	VSS = 4V, VEIN = 1.0V	
Minimum duty	Dmin	–	–	0	%	VSS = 4V, VEIN = 1.5V	

Note: 1. Design spec.

Electrical Characteristics (cont.)

(Ta = 25°C, V_{CC} = 12V, PG1 = 3V, Vtrig = 0V, VCS(+) = 0V, VCin = 0V, CCT = 330pF, GvOP1 = 26dB, GvOP4 = 40dB, RDB = 1.8kΩ)

- MR OUT

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Note
Output Lo voltage	VOLMR	–	0.2	0.4	V	Iosink = 100mA	
Output Hi voltage	VOHMR	VCC–0.4	VCC–0.2	–	V	Iosource = 100mA	
Rise time	trMR	20	50	100	ns	CL = 3300pF	
Fall time	tfMR	20	50	100	ns	CL = 3300pF	

- MF OUT

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Note
Output Lo voltage	VOLMF	–	0.2	0.4	V	Iosink = 200mA	
Output Hi voltage	VOHMF	VCC–0.4	VCC–0.2	–	V	Iosource = 200mA	
Rise time	trMF	20	50	100	ns	CL = 6000pF	
Fall time	tfMF	20	50	100	ns	CL = 6000pF	

- Dead band time

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Note
Dead band time1	Td1typ	0	50	100	ns	RDB = 1.8kΩ	
Dead band time2	Td2typ	0	100	200	ns	RDB = 1.8kΩ	
MR to MF delay time	t1	(–20)	–	(50)	ns	t1 = MF off – MR on	1
PWM to MR delay time	t2	(–20)	–	(50)	ns	t2 = MR off – PWM off	1
MR delay time	t3	–	1	–	µs	t3 = CT low trip point – MR on	1
Maximum Dead band adjust time1	Tdadj1	–	Td1typ +300	–	ns	RDB = 47kΩ	1
Maximum Dead band adjust time2	Tdadj2	–	Td2typ +600	–	ns	RDB = 47kΩ	1

Note: 1. Design spec.
Measurement is 50% slice point.

Electrical Characteristics (cont.)

(Ta = 25°C, V_{CC} = 12V, PG1 = 3V, Vtrig = 0V, VCS(+) = 0V, VCin = 0V, CCT = 330pF, GvOP1 = 26dB, GvOP4 = 40dB, RDB = 1.8kΩ)

- SS

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Note
SS sink current	Idss	500	–	–	µA	PG1 = 2V, VSS = 2V	

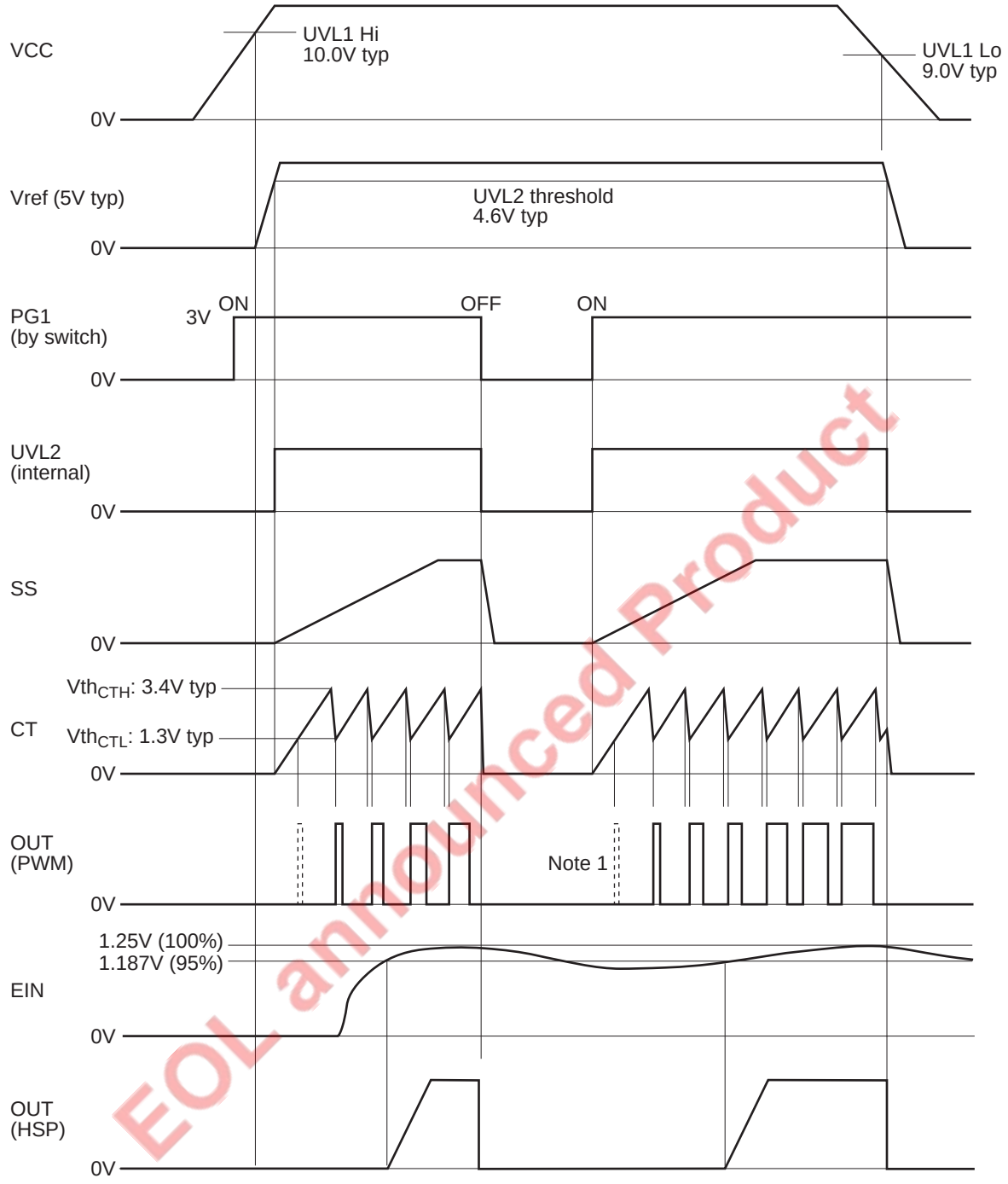
- OVP

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Note
OVP latch voltage	VOVP	6.5	7.5	8.5	V		

- Current consumption

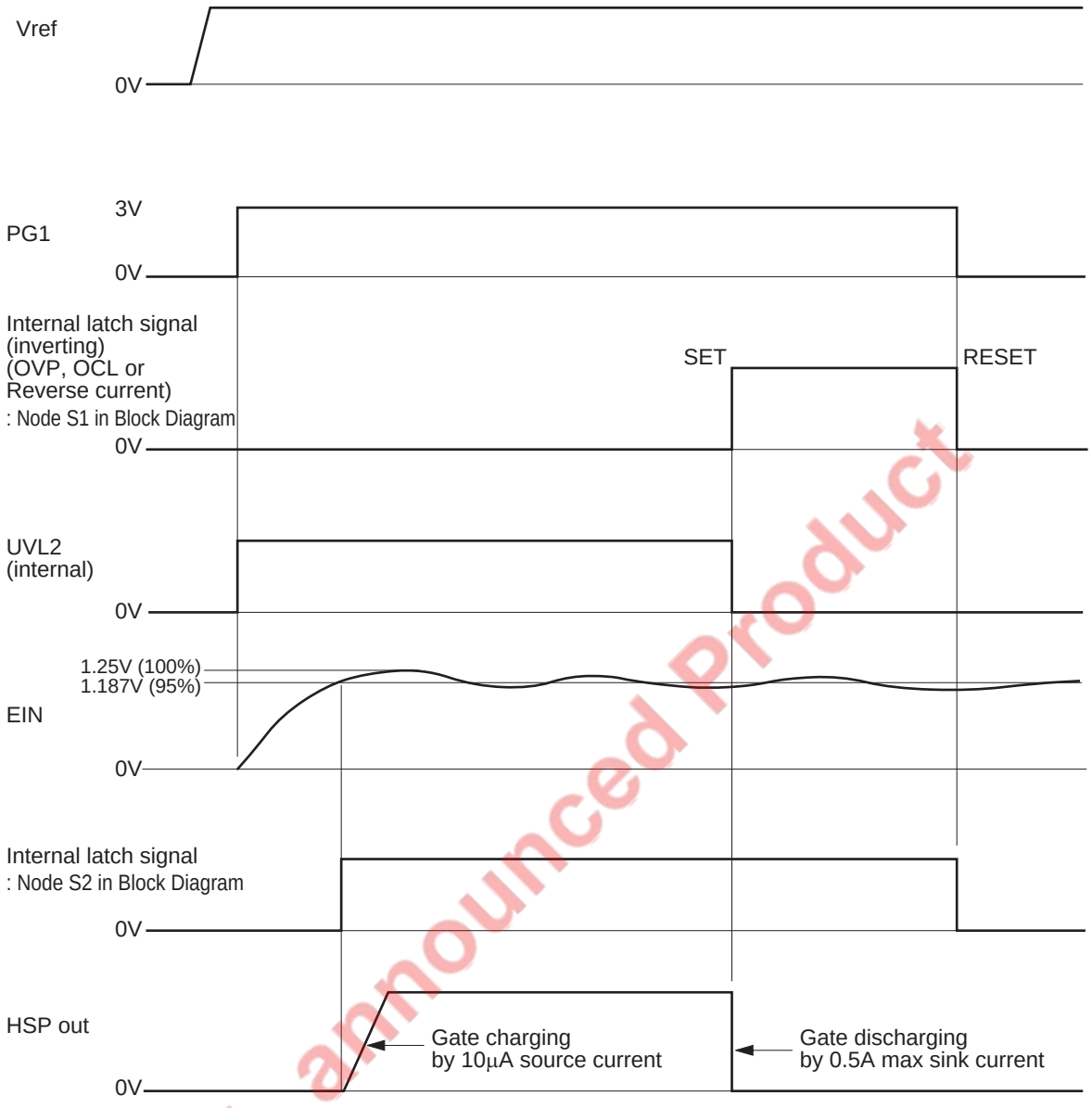
Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Note
Operating current	ICC	5.4	7.4	9.4	mA	VCT = 1V	
Standby current	ISTBY	–	200	600	µA	VCC = 8V, PG1 = 0V	

Timing Chart 1 (Total)



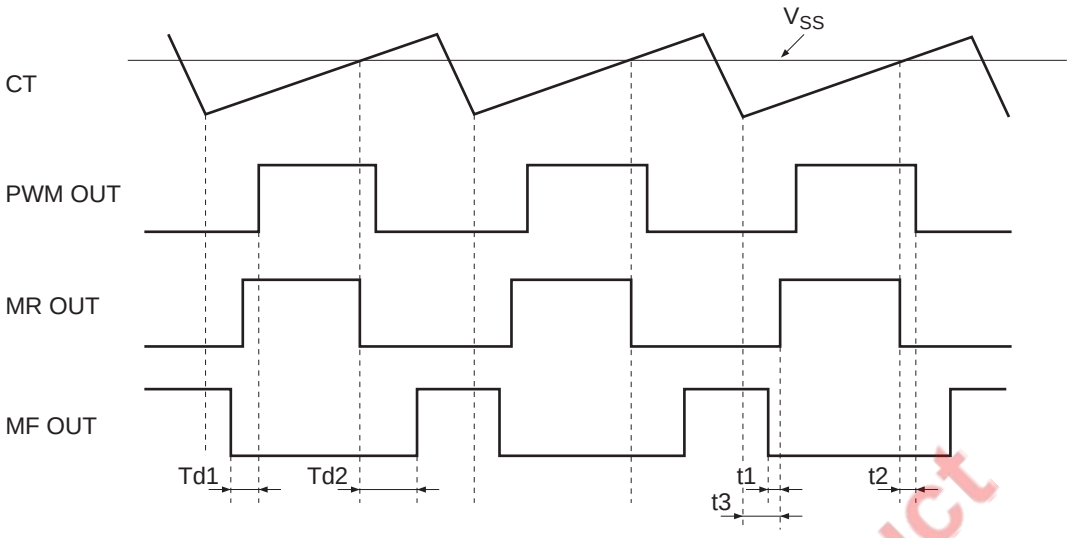
Note: 1. The output of PWM, MR and MF do not appear in the first period of CT cycle due to start-up latch circuit.

Timing Chart 2 (Hot Swap)

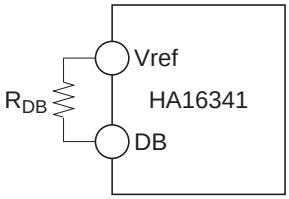


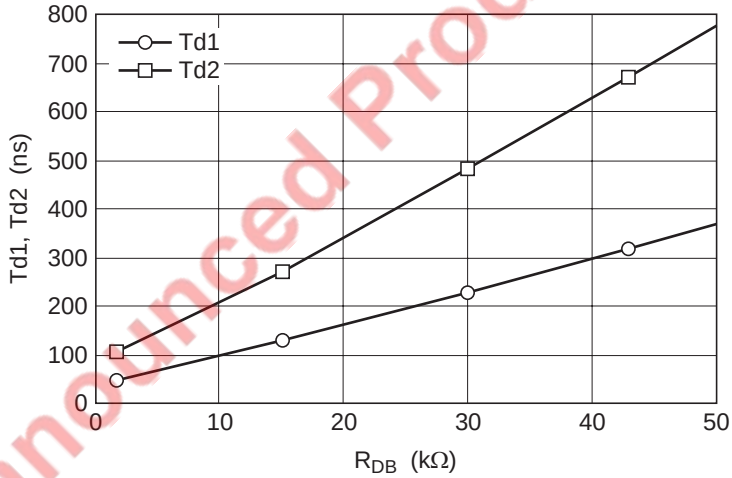
Note: Reverse current is HA16341NT/FP only.

Timing Chart 3 (Dead Band Control)

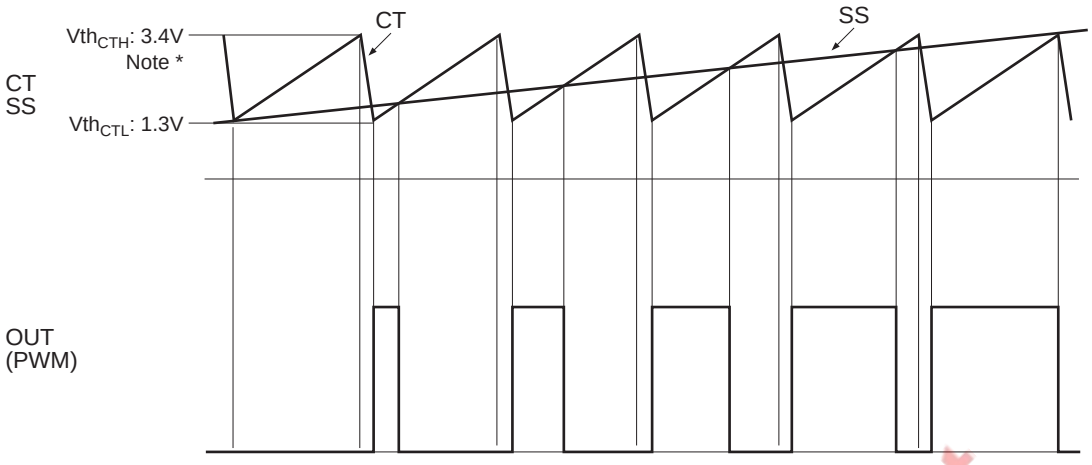


Note: V_{SS} determines maximum duty. This waveform example shows the case of EIN = Lo.
V_{SS}: Voltage of SS pin





Timing Chart 4 (Soft Start)



Note: Self-oscillation: Vth_{CTH} = 3.4V typ
Synchronized operation: Vth_{CTH} = 2.9V typ

Case $V_{HSS} \geq Vth_{CTH}$
Maximum duty would be the value specified in page 9.

Case $V_{HSS} < Vth_{CTH}$
Maximum duty decrease to the corresponding value.

Please refer to formula 1 as design value of maximum duty.

Max duty = (tss – 0.63μs – Td1) × Operating frequency · · · · · Formula 1

$$tss = \frac{C_{CT}}{Ici} (V_{HSS} - Vth_{CTL})$$

Ici : CT charge current
C_{CT} : CT terminal capacitor
Vth_{CTH} : CT upper trip point
Vth_{CTL} : CT lower trip point

Select values R1, R2 and C1 for suitable maximum duty and SS time constant.

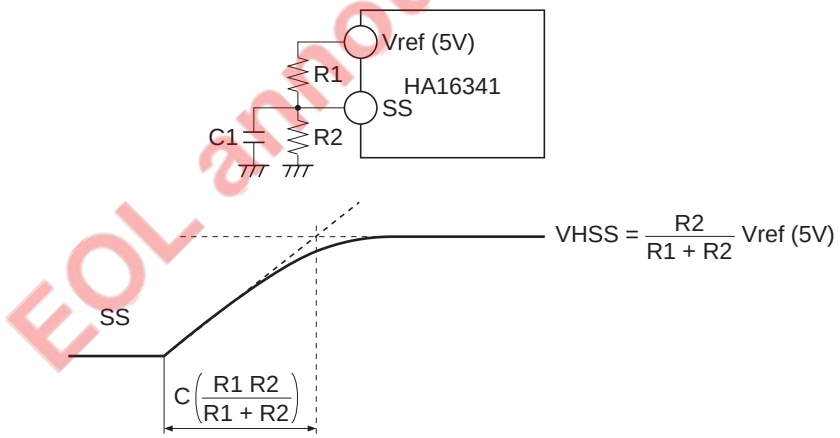
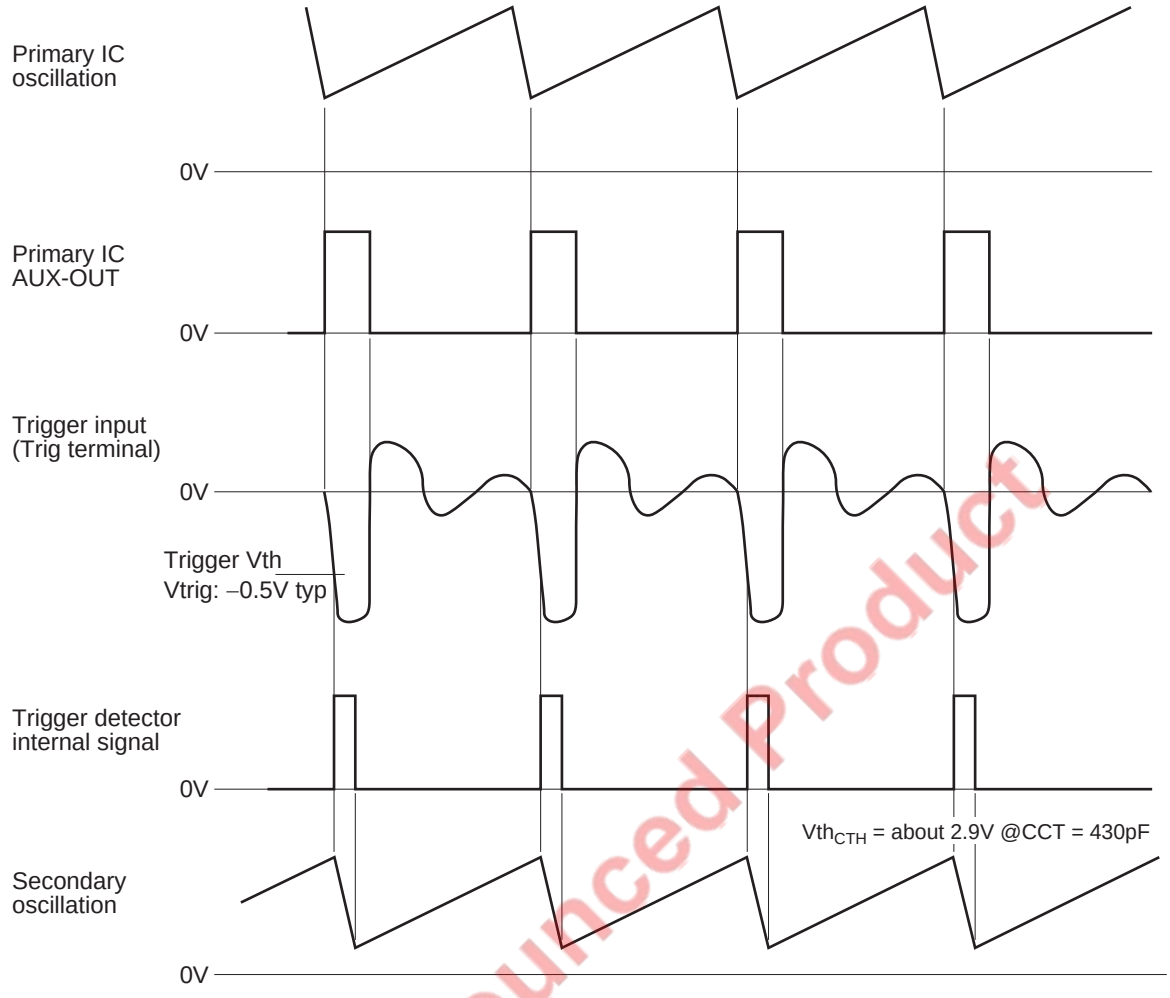


Figure A. SS Terminal Application

Timing Chart 5 (External Trigger Control)



This IC is triggered by negative pulse.
R1 and R2 must be calculated including internal impedance of 230kΩ.

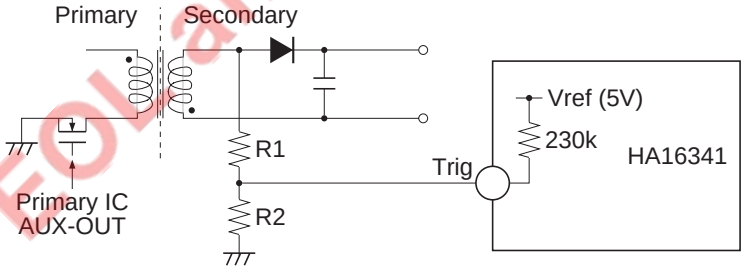
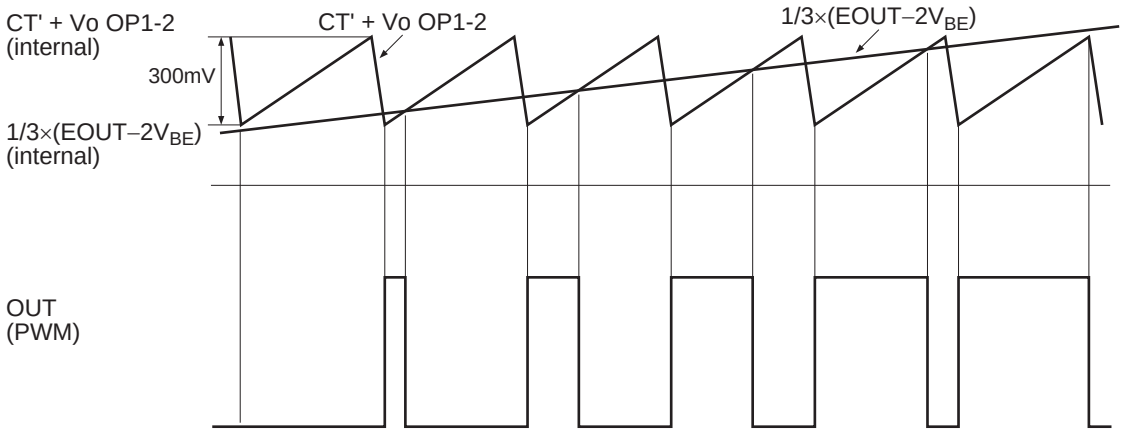


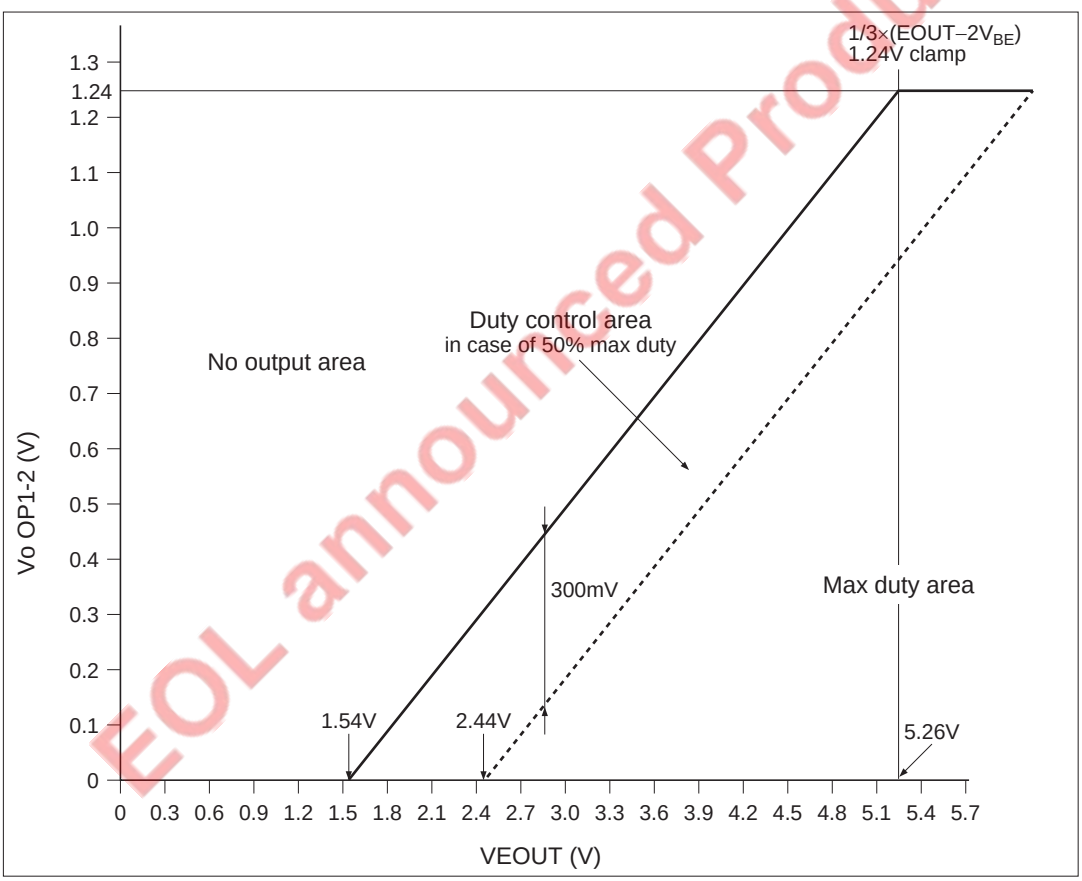
Figure B. External Trigger Application

Timing Chart 6 (Duty Control)

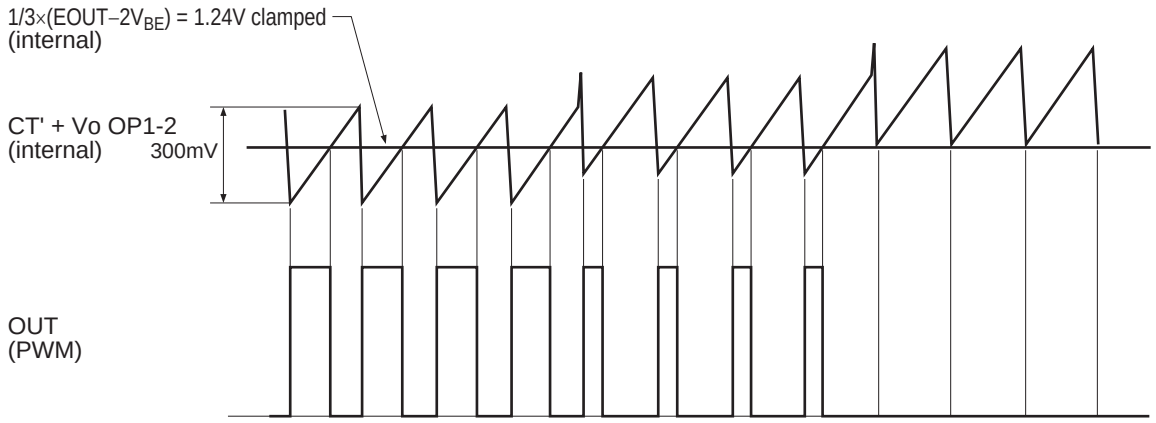


$$CT' = \frac{CT}{5.33}$$

The amplitude of CT' is 300mV typ at synchronous operation with trigger frequency as 200kHz and C_{CT} = 430pF.

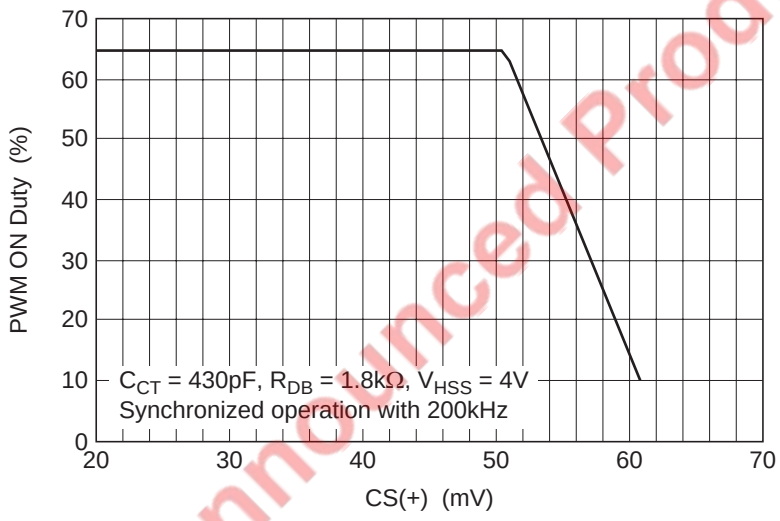


Timing Chart 7 (Current Limitting)

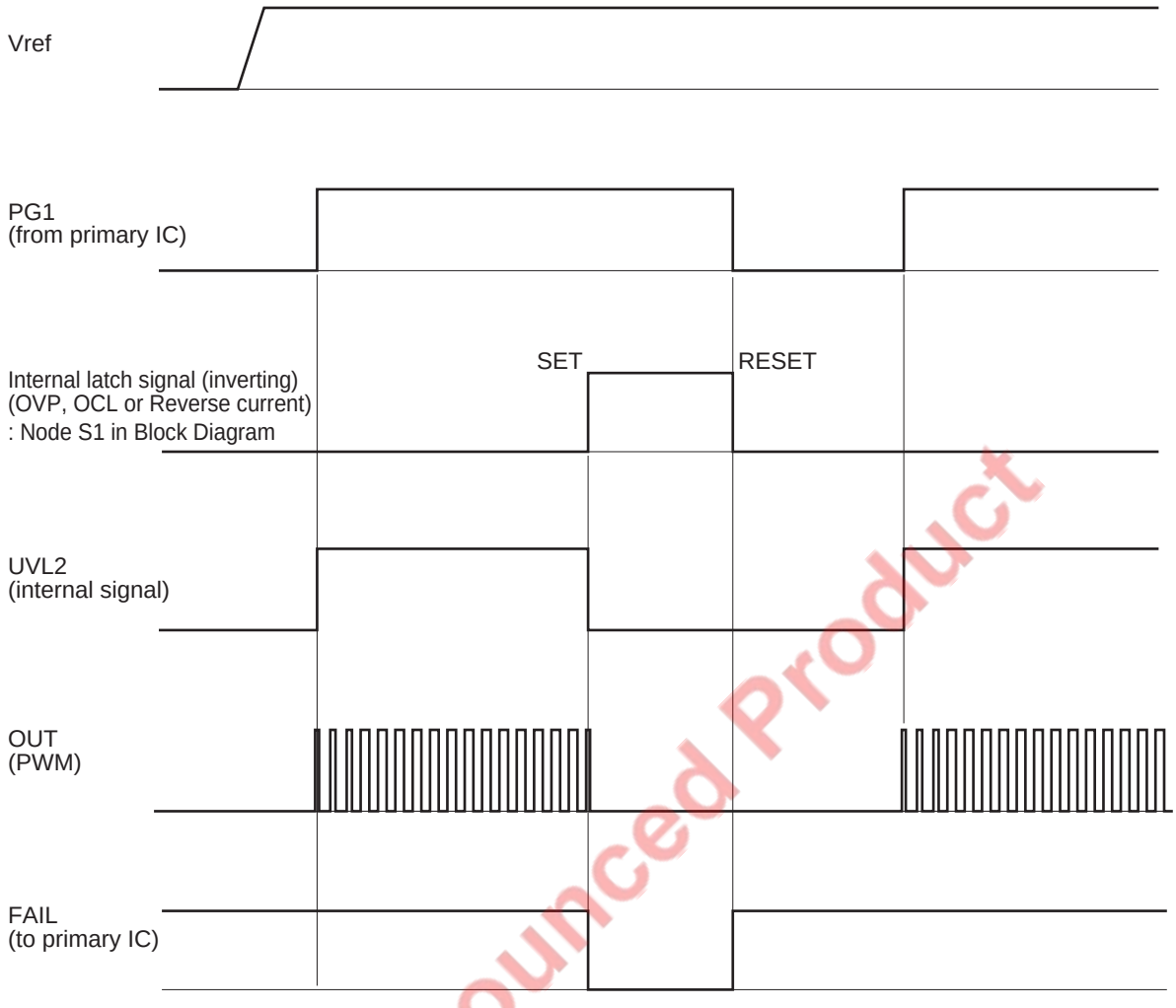


$$CT' = \frac{CT}{5.33}$$

The amplitude of CT' is 300mV typ at synchronous operation with trigger frequency as 200kHz and C_{CT} = 430pF.



Timing Chart 8 (Interface with Primary Control IC)

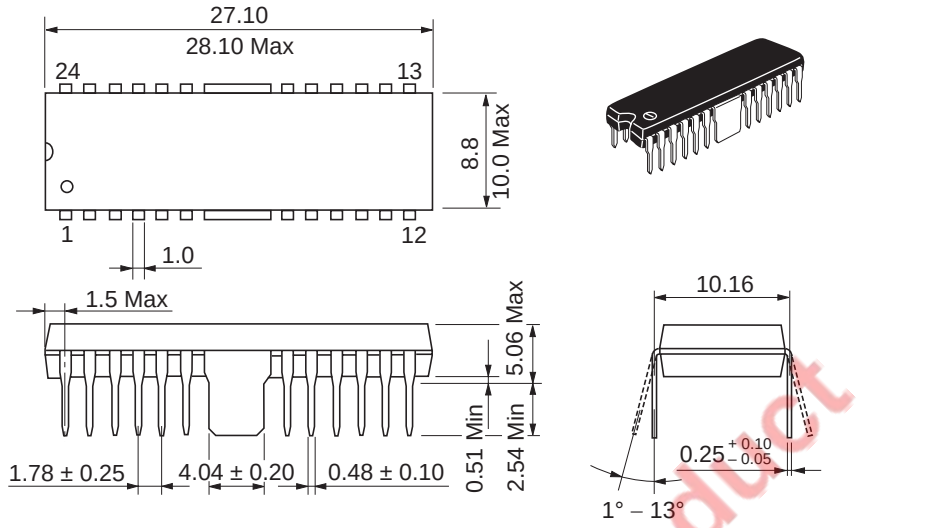


Note: Reverse current is HA16341NT/FP only.

Package Dimensions

As of January, 2003

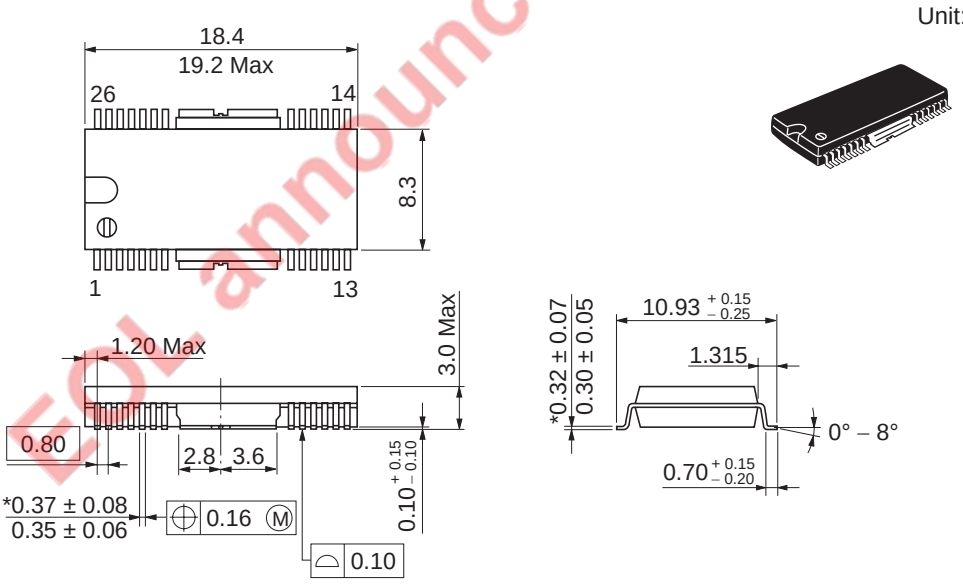
Unit: mm



Package Code	DP-24TS
JEDEC	–
JEITA	–
Mass (reference value)	2.04 g

As of January, 2003

Unit: mm



*Dimension including the plating thickness
Base material dimension

Package Code	FP-26DT
JEDEC	–
JEITA	–
Mass (reference value)	0.98 g

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