QUADRUPLE 2-INPUT NAND GATE

The HEF4011B provides the positive quadruple 2-input NAND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.
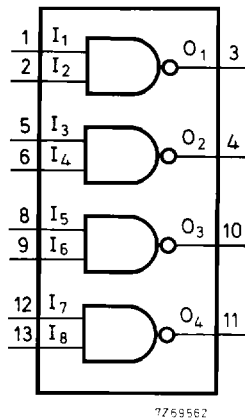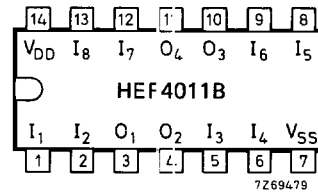

Fig. 1 Functional diagram.

Fig. 2 Pinning diagram.

HEF4011BP(N): 14-lead DIL; plastic
(SOT27-1)
HEF4011BD(F): 14-lead DL; ceramic (cerdip)
(SOT73)
HEF4011BT(D): 14-lead SO; plastic
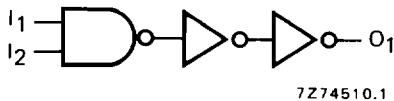(SOT108-1)
( ): Package Designator North America

Fig. 3 Logic diagram (one gate).

FAMILY DATA

I_{DD} **LIMITS category GATES**

see Family Specifications

A.C. CHARACTERISTICS

$V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times $\leqslant 20$ ns

	V_{DD} V	symbol	typ	max		typical extrapolation formula
Propagation delays $I_n \longrightarrow O_n$	5		55	110	ns	28 ns + (0,55 ns/pF) C_L
	10	t_{PHL}; t_{PLH}	25	45	ns	14 ns + (0,23 ns/pF) C_L
	15		20	35	ns	12 ns + (0,16 ns/pF) C_L
Output transition times						
HIGH to LOW	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
LOW to HIGH	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$1300\, f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$6000\, f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$20\,100\, f_i + \Sigma(f_o C_L) \times V_{DD}^2$	