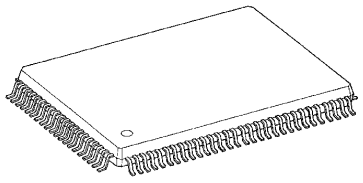
TOSHIBA CMOS DIGITAL LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

TMP04CH00FXXX(JTMP04CH00XXXS)

CMOS 4BIT LL MICROCONTROLLER (LL : LOW POWER CONSUMPTION & VOLTAGE OPERATION MICROCONTROLLER)

◆OUTLINE

The TMP04CH00FXXX is a high-performance microcontroller designed to be in a variety of low-voltage products.
It is a 4bit CMOS LL microcontroller with integrated a 4bit high-performance CPU, memory (static work RAM, data RAM and program ROM). LCD display LL controller driver, and a multi-function timer into a single chip.
The basic features are as follows.



P-QFP100-1420-0.65A

Weight : 1.65g (Typ.)

◆FEATURES

- Number of instructions : 56
- Minimum instruction execution time : 61μs (at 32.768kHz)
  1μs (at 2MHz / 3.0V)
- Oscillating circuit : low speed – crystal oscillator (32.768kHz)
  / internal CR (33kHz at 1.5V)
  high speed – crystal oscillator (2MHz at 3.0V)
  / external CR (200kHz at 1.5V)
- Built-in ROM size : 16K words
  (1 word = 16 bits)
- Built-in RAM size :
  Work RAM : 512×4 bits
  Data RAM : 6K bits
- Input pins : 8 pins (with interrupts)
- I/O pins : 8 pins
- Output pins : 1 pin (Buzzer)
- Interruption : 2 external system (input pins, general purpose I/O pin)
  2 internal system (timer / counter, timings)

980910EBA1

- TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.
- The products described in this document are subject to the foreign exchange and foreign trade laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.

- Timer : 8 bits × 2ch or 16 bits × 1ch (software-selectable)
- LCD display driver controller : 60 seg × 8 com / 58 seg × 10 com 〉 Mask option
- Built-in LCD driver power circuit
- Watchdog timer : Timer / Counter can be used as Watch Dog Timer
- Supply voltage : 1.5 / 3.0V (Typ.) Mask option

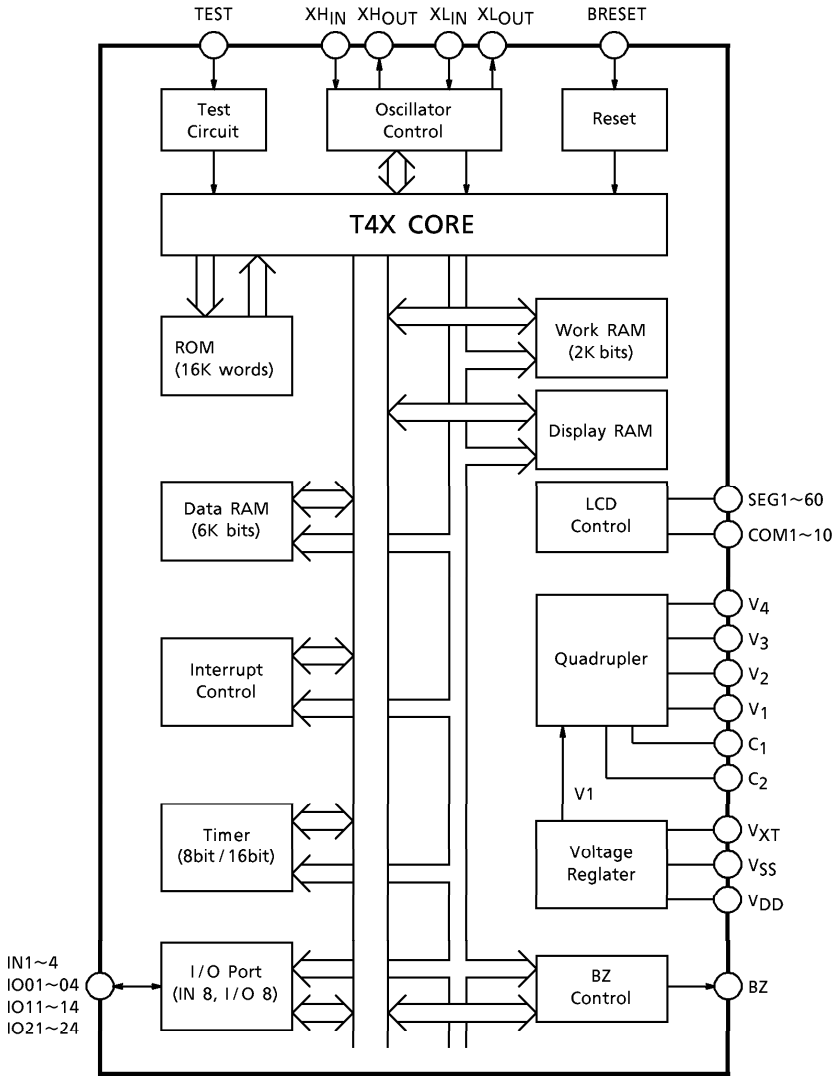
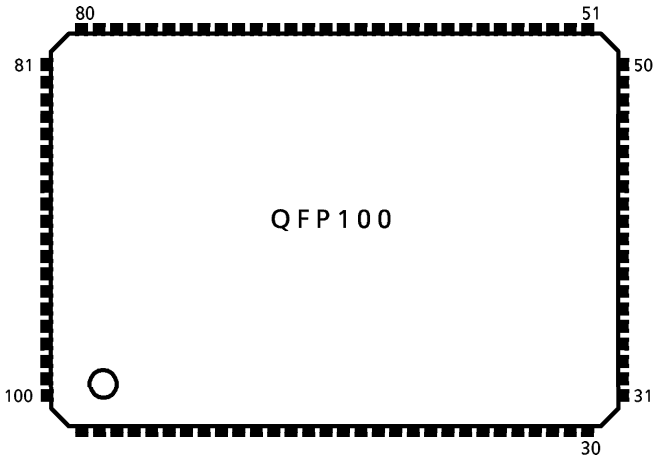


Fig.1 Block diagram

◆PIN CONFIGURATION

1. Pin assignment



PIN No.	PIN NAME
1	V_1
2	C_1
3	C_2
4	V_{SS}
5	VXT
6	BRESET
7	XLIN
8	XLOUT
9	VDD
10	XHIN
11	XHOUT
12	TEST
13	BZ
14	IN1
15	IN2
16	IN3
17	IN4
18	IO01
19	IO02
20	IO03
21	IO04
22	IO11
23	IO12
24	IO13
25	IO14

PIN No.	PIN NAME
26	IO21
27	IO22
28	IO23
29	IO24
30	S_1
31	S_2
32	S_3
33	S_4
34	S_5
35	S_6
36	S_7
37	S_8
38	S_9
39	S_{10}
40	S_{11}
41	S_{12}
42	S_{13}
43	S_{14}
44	S_{15}
45	S_{16}
46	S_{17}
47	S_{18}
48	S_{19}
49	S_{20}
50	S_{21}

PIN No.	PIN NAME
51	S_{22}
52	S_{23}
53	S_{24}
54	S_{25}
55	S_{26}
56	S_{27}
57	S_{28}
58	S_{29}
59	S_{30}
60	S_{31}
61	S_{32}
62	S_{33}
63	S_{34}
64	S_{35}
65	S_{36}
66	S_{37}
67	S_{38}
68	S_{39}
69	S_{40}
70	S_{41}
71	S_{42}
72	S_{43}
73	S_{44}
74	S_{45}
75	S_{46}

PIN No.	PIN NAME
76	S_{47}
77	S_{48}
78	S_{49}
79	S_{50}
80	S_{51}
81	S_{52}
82	S_{53}
83	S_{54}
84	S_{55}
85	S_{56}
86	S_{57}
87	S_{58}
88	S_{59} / COM10
89	S_{60} / COM9
90	COM8
91	COM7
92	COM6
93	COM5
94	COM4
95	COM3
96	COM2
97	COM1
98	V_4
99	V_3
100	V_2

2. Pin description

PIN NAME	FUNCTION
V_{DD}	Power supply (+)
V_{SS}	Power supply (−)
V_{XT}	Voltage regulator1 output (Output for only the mask option 3.0V type)
V1	Voltage regulator2 output
V2~V4	Boosted voltage output
C1, C2	Capacitor pin for LCD booster
XHIN, XHOUT	Crystal / resister connection pin for high-speed oscillator
XLIN, XLOUT	Crystal connection pin for low-speed oscillator
IN1~IN4	Input port (with interruption)
IO01~IO04	Input port (with interruption)
IO11~IO14	I/O port
IO21~IO24	I/O port
SEG1~SEG60	LCD segment output
COM1~COM8	LCD common output
BZ	Buzzer output
BRESET	Reset input (low active)
TEST	Test input

◆MEMORY MAP

1. Program ROM

Program ROM consists of 16 bits 1 word. Op-code and operand are executed in one word units. Program ROM consists of 4K words per page. The internal program ROM area is 4 pages (16K words).

This program ROM area can be used for constant data ROM. In this case, it can be used in byte units (1 byte = 8 bits).

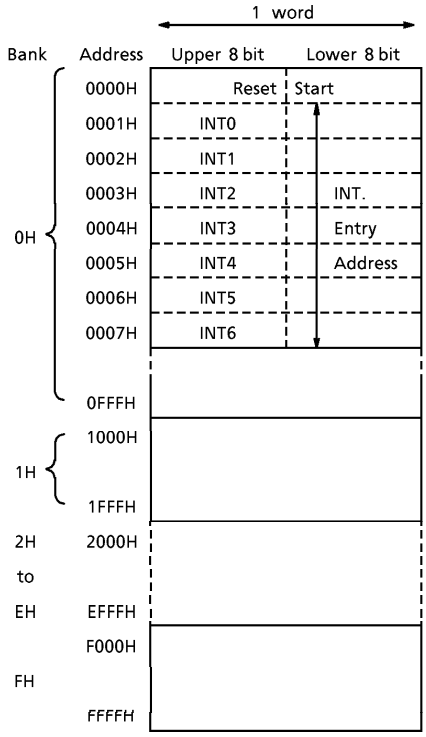


Fig.2 Program memory map

(Note) Use the CALL instruction to write the interrupt entry address. Write NOP for unused interrupts.

```
Example : CALL A ; INT0
          NOP    ; INT1
          CALL B ; INT2
          NOP    ; INT3
          NOP    ; INT4
          NOP    ; INT5
          NOP    ; INT6
```

2. Work RAM

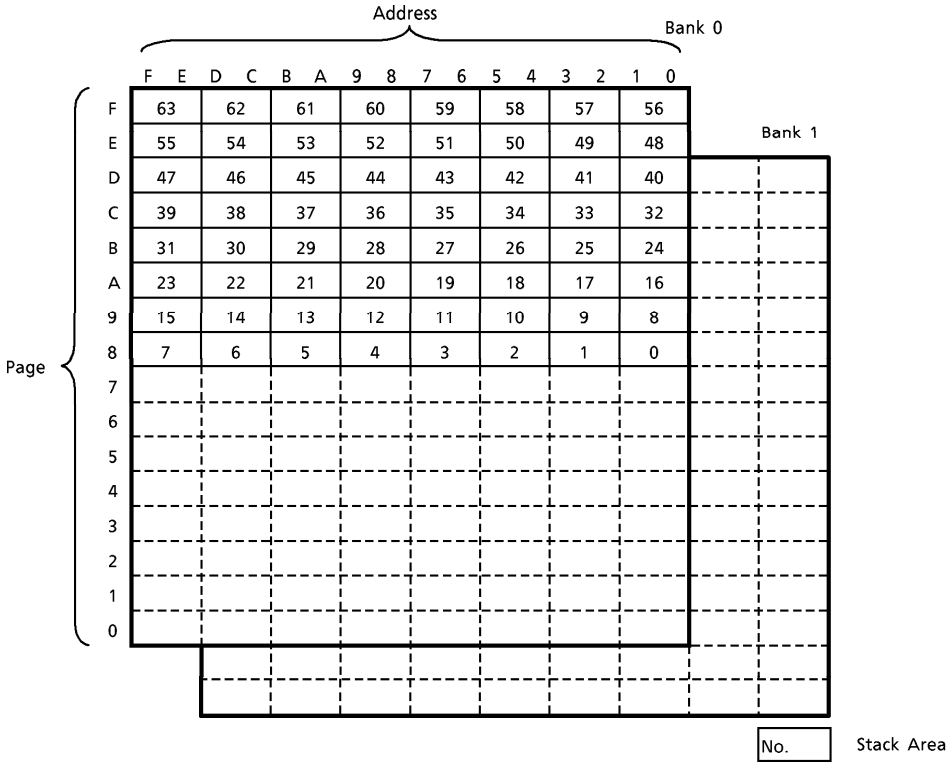


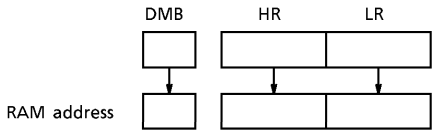
Fig.3 Work RAM

Work RAM consists of 512×4 bits.
R/W is performed at the address specified by bellows.

(1) Indirectly addressing mode (Fig.4 (a))

DMB in F-reg, H, L-reg specify the Work RAM address.
(DMB : bank, H-reg : page, L-reg : address)

LD A, M : A←RAM (HL)

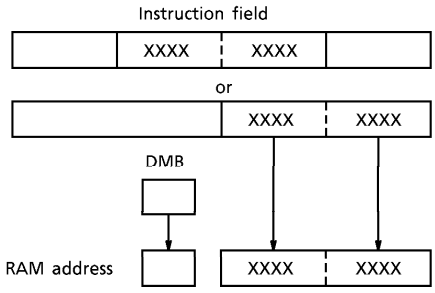


(a) Indirectly addressing

(2) Directly addressing mode (Fig.4 (b))

Immediate data (8 bits) in instruction specify the Work RAM page and address.
Bank is specified by DMB in F-reg.

LDI 2CH, 0AH : RAM (2CH)←AH

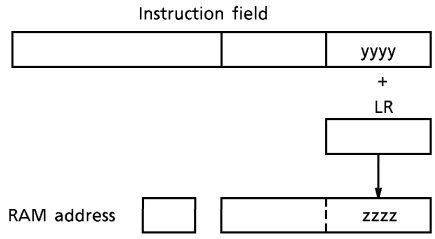


(b) Directly addressing

(3) Index addressing mode (Fig.4 (c))

Address (L-reg) is specified by the immediate data (4 bits) in instruction, and the other immediate data specify Page.

LDRI 4H, 3H : RAM (HL + 4H)
←RAM (3H、L)
L←L + 1, A←A − 1



(c) Index addressing

Fig.4 Addressing mode

BANK 0, PAGE 8~F area can be used as Stack area.
When using the "CALL/CALLS" instruction or start the interruption routine, the data of program counter and Program memory bank are stored in Stack area.
Then, using "RET" instruction, program return according to those data.
And, using "PUSH" instruction, 8 bits data in a pair register can be stored in Stack area.
Then, using "POP" instruction, those data are returned to the register.
Maximum Stack area is 64 (0~63), and each Stack area consist of 8 bits.

3. Data RAM

TMP04CH00FXXX has 6K bits Data RAM (256AD × 3bank × 8bit), and addressing and data read / write is done by Register file, as follows.
When the data is read from Data RAM / written in Data RAM, CE1 (PB0) is needed to set 1.
(PB0 : Register file Page 3, AD0)

	MSB 3	2	1	0 LSB
PB0	—	—	—	CE1

Addressing is decided by RAB1~2 (PB3), RAC1~4 (PB5), RAR1~4 (PB4)

		MSB 3	2	1	0 LSB
BANK	PB3	—	—	RAB2	RAB1
ROW	PB4	RAR4	RAR3	RAR2	RAR1
COLMN	PB5	RAC4	RAC3	RAC2	RAC1

Data is read / written by 8 bits which is set in RAD1~8 (PB6, PB7).
To read from / written into Data RAM, only 8 bits transference instruction can be used.

	MSB 3	2	1	0 LSB
PB7	RAD8	RAD7	RAD6	RAD5
PB6	RAD4	RAD3	RAD2	RAD1

(CAUTION)

When "HALT" instruction is excuted for the next instruction of transference the data to Data RAM, the data of Data RAM is broken. Also, data may be destroyed if the HALT instruction is executed while CE1 is set to 1. Therefore, be sure to set CE1 to 0 before executing the HALT instruction.
RAD1 to 8 (PB6, PB7) are valid for only 8-bit transfer instructions.
4-bit transfer instructions do not have any effect (NOP).

4. Display RAM

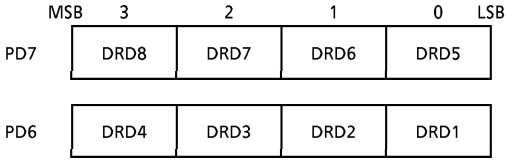
TMP04CH00FXXX has 600 bits Display RAM (60seg × 8com / 58seg × 10com), and addressing and data read / write is decided by Register file, as follows.
When the data is read from / written into Display RAM, DRCE (PC6-bit2) is needed to be 1.

	MSB 3	2	1	0 LSB
PC6		DRCE	DON	DSTA

Addressing is decided by DRR1~4 (PD4), DRC1~3 (PD5) (LSB is DRR1, and MSB is DRC3)

	MSB 3	2	1	0 LSB
PD5		DRC3	DRC2	DRC1
PD4	DRR4	DRR3	DRR2	DRR1

Data is read / written by 8 bits which is set in DRD1~8 (PD6, PD7).
To read from / written into DISPLAY, only 8 bits transference instruction can be used.



When the display duty is selected 1 / 8, S1~S60 are used as segment output and display data is read from / written into Display RAM which address is 00H~3BH.
Also, when using with a 1 / 10 duty cycle, segments are used from S1 up to S58 and the data COM9 and 10 are written to and read from addresses beginning with 40H via DRD1 and DRD2.

(CAUTION)

1. When "HALT" instruction is executed for the next instruction of the transference the data to Display RAM, the data of Display RAM is broken.
2. When "HALT" instruction is executed during DRCE is 1, the data of Display RAM is broken. Therefore, be sure to set DRCE to 0 before executing the HALT instruction.
   DRD1 to 8 (PD6, PD7) are valid for only 8-bit transfer instructions.
   4-bit transfer instructions do not have any effect (NOP).

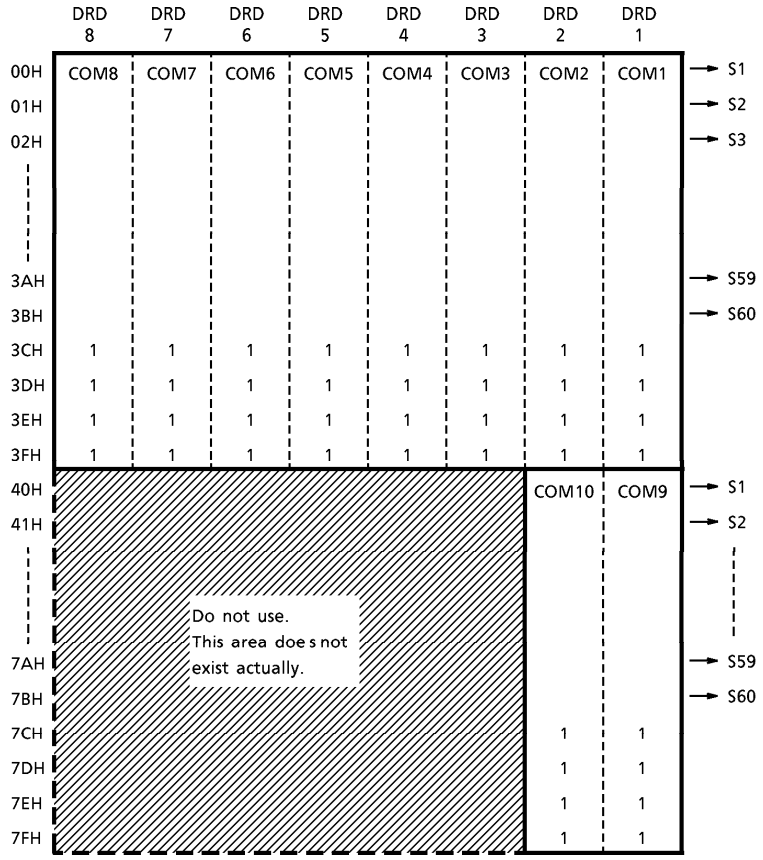


Fig.5 Display RAM

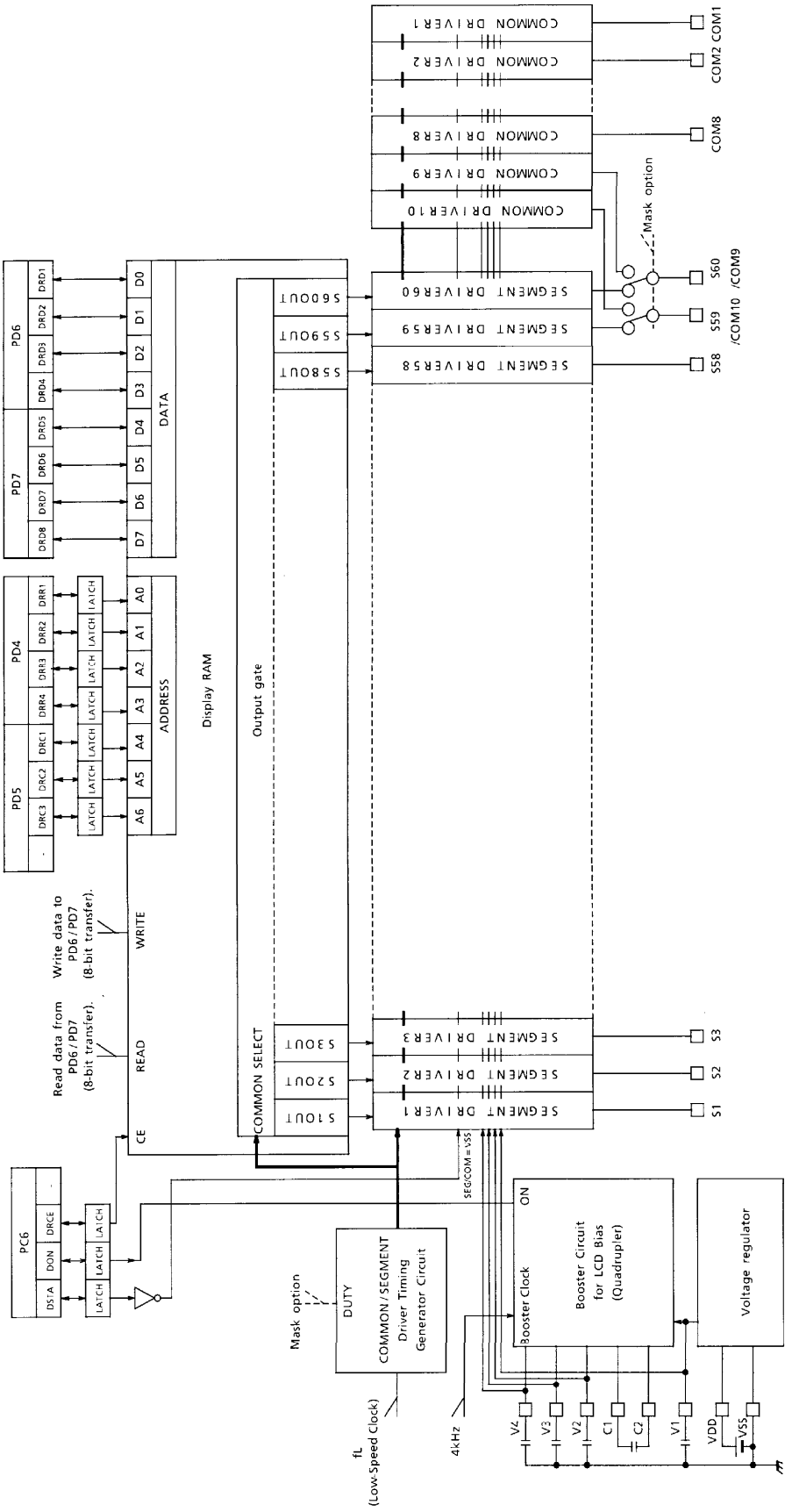


Fig.6 LCD Driver

◆REGISTER FILE

Register files consist of (1) general-purpose registers, (2) system registers, and (3) peripheral I/O registers. Figure 11 shows the overall configuration of register files.

1. General Register

1.1 Flag Register : F-Register (PAGE / AD = 0 / 0)

CF : Carry Flag
ZF : Zero Flag
(0) : Not use
DMB : Work RAM Bank

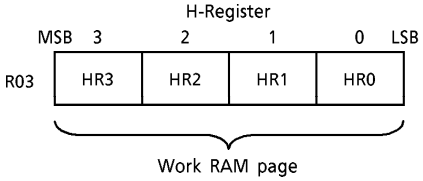
1.2 Accumulater Register : A-Register (PAGE / AD = 0 / 1)

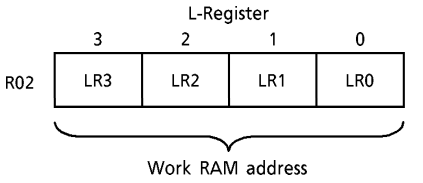
Accumulator for arithmetic operations.

When consecutive instructions are executed, used as a counter register.

1.3 H.L Register (PAGE / AD = 0 / 3~2)

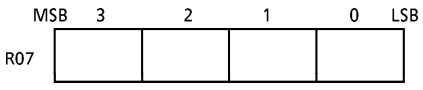
H.L Register are used for Work RAM address setting with DMB.





1.4 Bank Register (PAGE / AD = 0 / 7) : B-Register

B-Register is used for ROM Page.



0000 = Page 0
0001 = Page 1
0010 = Page 2
0011 = Page 3

1.5 D-Register, E-Register, P-Register (B-Register) (PAGE / AD = 0 / 5, 0 / 4, 0 / 6, 0 / 7)

General purpose register.
When using ROM as Data Table Function, B, P, D, E-Register are used for ROM address setting. (Data table function : user can use ROM area for store the constant, and can access those constant by LDBL and LDBH instruction.)

2. System Registers

2.1 Stack pointer (PAGE / AD = 1 / 0, 1 / 1)

The stack pointer shows the location (63 to 0) in the stack area in work RAM.

	MSB 3	2	1	0
R10	SP4	SP2	SP1	—

	MSB 3	2	1	0
R11	—	SP32	SP16	SP8

2.2 Interrupt Enable / Disable Registers (PAGE / AD = 1 / 2, 1 / 3)

Enable / disable interrupts. There are five interrupt vectors (INT0 to INT4). Writing data in the bit corresponding to an interrupt enables / disables the interrupt. The details are described in the section on peripheral circuits.

	MSB 3	2	1	0
R12	INT2	INT1	INT0	(0)

	MSB 3	2	1	0
R13	—	—	INT4	INT3

2.3 Input / Output Registers (PAGE / AD = 1 / 4, 1 / 5)

Used for the input / output pins (IO21 to IO24). Using the bit that corresponds to a pin, output data can be set or input data can be read. The details are described in the section on peripheral circuits.

	MSB 3	2	1	0
R14	IO14	IO13	IO12	IO11

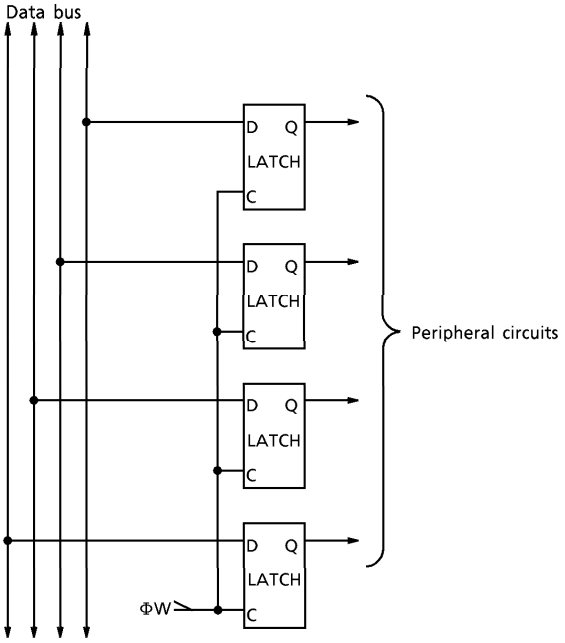
	MSB 3	2	1	0
R15	IO24	IO23	IO22	IO21

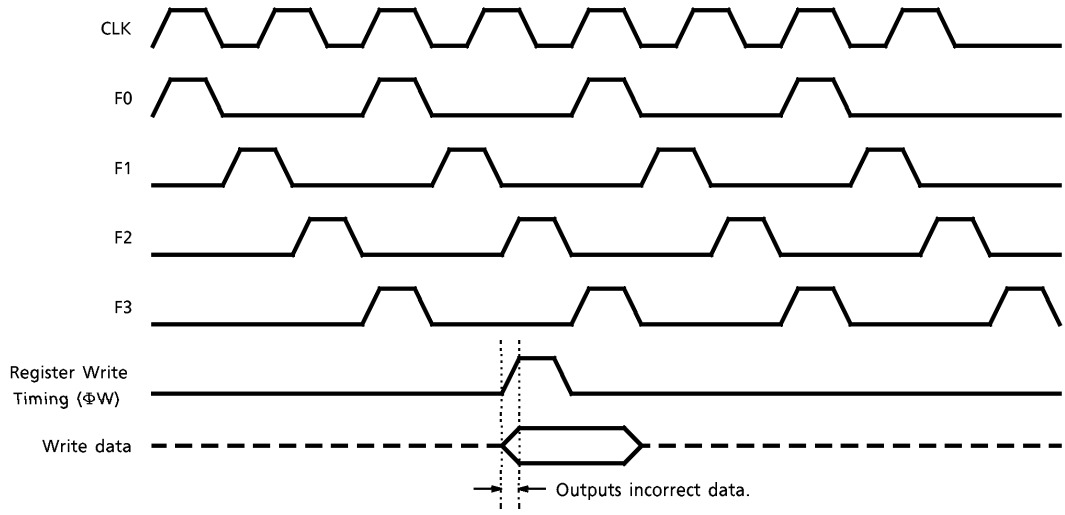
3. Peripheral I / O Registers

Registers used to control peripheral circuits specific to the product are allocated to pages 2 to 7. The details are described in the section on peripheral circuits.

※ A precaution relating to Writes to System Registers / Peripheral I / O Registers.

Writing to System Register and I / O Registers is performed in synchronization with ΦW. Because rising edges of ΦW coincides with the timing at which Write data is output on the data bus, it is possible that incorrect data is output to the peripheral circuits for a very short period of time. Please take this into account when programming.





PAGE (RFB)	ADDRESS	0		1		2		3		4		5		6		7	
	8BIT ADDRESS	0				2				4				6			
		LOWER4BIT		UPPER4BIT		L4BIT		H4BIT		L4BIT		H4BIT		L4BIT		H4BIT	
	R / W	READ	WRITE	READ	WRITE	READ	WRITE	READ	WRITE	READ	WRITE	READ	WRITE	READ	WRITE	READ	WRITE
0	MSB BIT3	F REGISTER		A REGISTER		L REGISTER		H REGISTER		E REGISTER		D REGISTER		P REGISTER		B REGISTER	
	BIT2																
	BIT1																
	LSB BIT0																
1 (R1x)	MSB BIT3	STACK POINTER (SP)		0		INT2				IOD14	IOO14	IOD24	IOO24				
	BIT2					INT1				IOD13	IOO13	IOD23	IOO23				
	BIT1					INT0		INT4		IOD12	IOO12	IOD22	IOO22				
	LSB BIT0	0				0		INT3		IOD11	IOO11	IOD21	IOO21				
2 (PAx)	MSB BIT3	IND4		IOD04													RST4
	BIT2	IND3		IOD03										LOWCP			RST3
	BIT1	IND2		IOD02										CPMODE2			RST2
	LSB BIT0	IND1		IOD01										CPMODE1			RST1
3 (PBx)	MSB BIT3									RAR4		RAC4		RAD4		RAD8	
	BIT2									RAR3		RAC3		RAD3		RAD7	
	BIT1							RAB2		RAR2		RAC2		RAD2		RAD6	
	LSB BIT0	CE1						RAB1		RAR1		RAC1		RAD1		RAD5	
4 (PCx)	MSB BIT3			IIN4		IIE4											
	BIT2	ESELT		IIN3		IIE3									DRCE		
	BIT1	ESELIO		IIN2		IIE2									DON	P2	
	LSB BIT0	ESELI		IIN1		IIE1		IOIE0							DSTA	P1	
5 (PDx)	MSB BIT3	TI4		1 / 2			TIR4	TIE4		DRR4				DRD4		DRD8	
	BIT2	TI3		4 / 8			TIR3	TIE3		DRR3		DRC3		DRD3		DRD7	
	BIT1	TI2		16 / 32			TIR2	TIE2		DRR2		DRC2		DRD2		DRD6	
	LSB BIT0	TI1		128 / 256			TIR1	TIE1		DRR1		DRC1		DRD1		DRD5	
6 (PEx)	MSB BIT3	TCR14	SET14	TCR18	SET18			TC1EN								2 / 4K	
	BIT2	TCR13	SET13	TCR17	SET17	CKS13			TC1R							BZ3	
	BIT1	TCR12	SET12	TCR16	SET16	CKS12		CMPEN1		TCI1E						BZ2	
	LSB BIT0	TCR11	SET11	TCR15	SET15	CKS11		WDT1			TCI1R					BZ1	
7 (PFx)	MSB BIT3	TCR24	SET24	TCR28	SET28	TCPS		TC2EN									
	BIT2	TCR23	SET23	TCR27	SET27	CKS23			TC2R								
	BIT1	TCR22	SET22	TCR26	SET26	CKS22		CMPEN2		TCI2E							
	LSB BIT0	TCR21	SET21	TCR25	SET25	CKS21					TCI2R						

Fig.7 Register file

(Note) Blank columns are indeterminate.

◆**PERIPHERAL CIRCUIT**

Each peripheral circuits can be accessed (Read / Write / Circuit setting) by Register files.

1. Oscillator Block

	MSB 3	2	1	0 LSB
PA6	—	LOWCP	CPMODE2	CPMODE1

The CPU clock is generated by the asynchronous oscillator switching circuit which has low-speed and high-speed clock oscillator circuit.

This block also provides the clock for the timer circuit, LCD driver, Quadrupler.

Oscillation mode is controlled by Register files "CPMODE1" and "CPMODE2" (PAGE / AD = 2 / 6), as follows.

CPMODE 1	CPMODE 2	Low-speed OSC	High-speed OSC	SYSTEM CP	MODE name
0	0	OFF	OFF	OFF	(CPM0)
1	0	ON	OFF	Low speed	(CPM1)
0	1	OFF	ON	High speed	(CPM2)
1	1	ON	ON	High speed	(CPM3)

CPMODE 1, 2 are initially 1 (CPM3).

"LOWCP" is the display clock control bit. When "LOWCP" is set to 1, Low OSC clock is supplied to LCD circuit. "LOWCP" is initially "0". Even if LOWCP is set to 1, clock cannot be occupied to display circuit during Low-speed OSC stopped, and display cannot be shown.

Low-speed OSC circuit can select X'tal or internal CR oscillation by Mask option.

High-speed OSC circuit can select X'tal or external CR oscillation by Mask option.

Setting a register to CPM1 and executing a HALT instruction sets the mode to Halt (system CP off, high-speed oscillator off, low-speed oscillator on). Setting a register to CPM0 and executing a HALT instruction sets the mode to Stop (system CP off, high-speed oscillator and low-speed oscillators off). Even if, mode is changed to MODE 0 from MODE 1 / 2 / 3, there are no changing until use "HALT" instruction.

The High / Low-speed OSC circuit has WARM UP function.

The warm-up function disables the crystal oscillator as the system clock from when the crystal oscillator starts oscillation to when the frequency stabilizes. The warm-up circuit in the high-speed crystal oscillator circuit consists of a 15-stage binary counter. The warm-up time is 16,384 pulses of the high-speed clock. The warm-up circuit in the low-speed crystal oscillator circuit consists of a 9-stage binary counter. The warm-up time is 256 pulses of the high-speed clock.

The low-speed oscillation does not have enough warm-up time, therefore, when the oscillation is started, software need to make warming up time enoughly.

Set the warm-up time by software to approx. 500 ms as standard.

When the System CP is changed between Low and High (CPM1→CPM2 / 3 or CPM2→CPM1), changing System CP waits to finish the warming up time.

Also that until the system CP is changed, instructions are executed with the previous system CP.

If the CR oscillator is selected as the high- or low-speed oscillator circuit, the warm-up function is disabled.

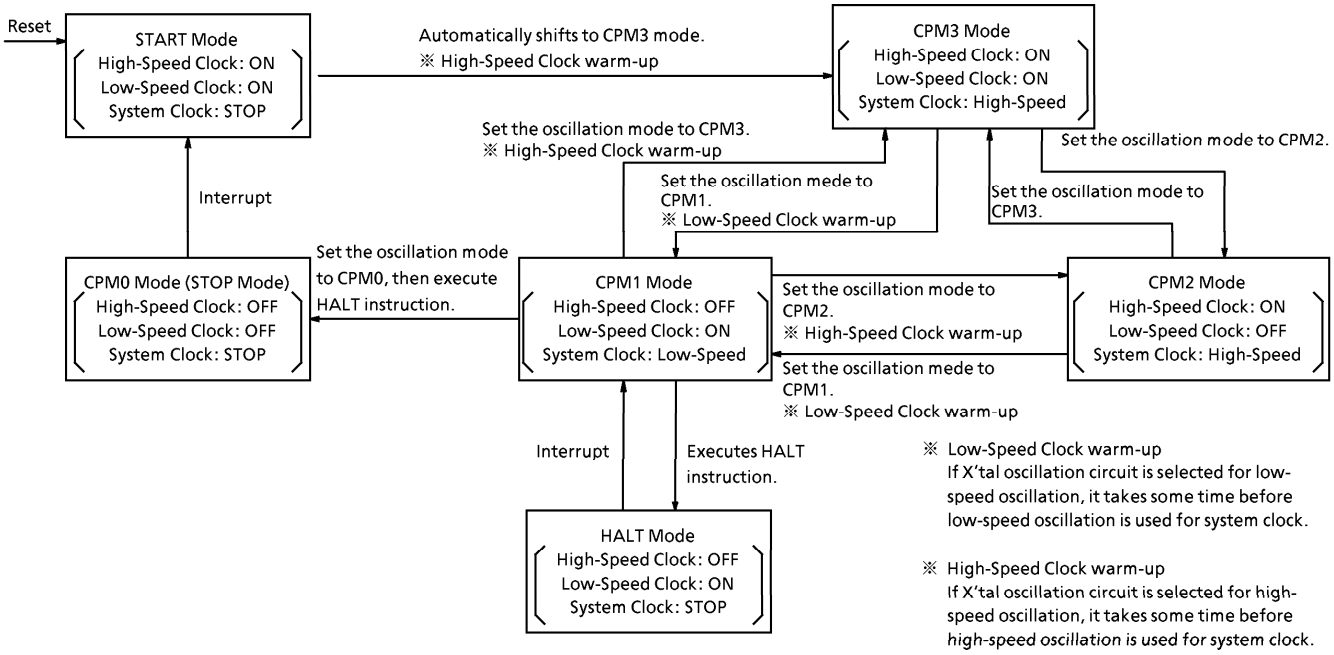


Fig.8 Mode transition

TMP04CH00FXXX has 21 bits Divider.
The divider circuit of bits 1 to 6 generates a clock from 1 MHz to 32 kHz by dividing the high-speed clock (2 MHz). The divider circuit of bits 7 to 21 generates a clock from 16 kHz to 1 Hz by dividing the 32 kHz clock. When the low-speed oscillator circuit is on (CPM1 / CPM3), a low-speed clock (32 MHz) is supplied to the divider circuit of bits 7 to 21. When the low-speed oscillator circuit is off (CPM2), output from bit 6 is supplied.

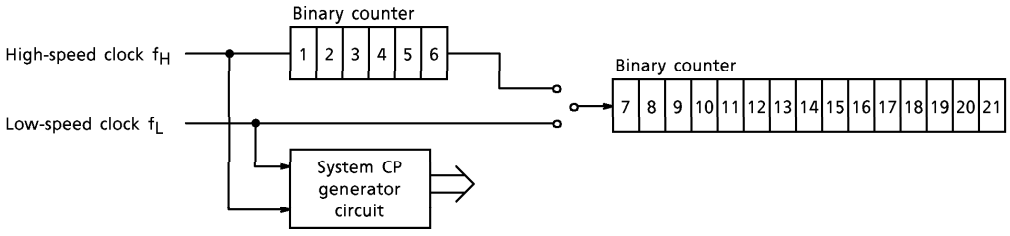
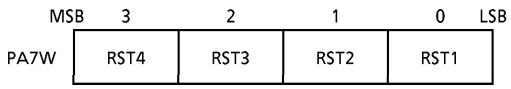


Fig.9 Divider circuit

The reset for this Divider circuit is done by Register file RST1~4 (PA7W).



RST1 : Binary counter 1~6 (2M~32kHz) reset
RST2 : Binary counter 7~12 (16k~512Hz) reset
RST3 : Binary counter 13~17 (256~16Hz) reset
RST4 : Binary counter 18~21 (8~1Hz) reset
(when using 2MHz, 32kHz crystal)

(CAUTION)

1. Do not set System CP to low speed when the Low-speed OSC is not in operation or before stable.
2. Do not set System CP to high speed when the High-speed OSC is not in operation or before stable.
3. And, when Low-speed OSC is on, low-speed frequency is supplied from 7th bit Divider circuit (when use 2MHz crystal for High-speed OSC and 32kHz crystal for Low-speed OSC and the mode is CPM3, 1MHz~32kHz are made by 2MHz crystal, 16kHz~1Hz are made by 32kHz crystal. And when the mode is CPM2, all frequency are made by 2MHz crystal. Therefore if the mode change between CPM1 and CPM2 or CPM2 and CPM3, the frequency which is supplied by Binary counter 7~21 shift the timing).
4. When operated with a 1.5V power supply, the oscillation frequency on the high-speed side is 200kHz (max.), so that the output of binary counter 6 is 3.125kHz (max.). Consequently, if the mode is changed from CPM1 or 3 to CPM2 or from CPM2 to CPM1 or 3, the generated timing changes greatly.
5. When the crystal oscillator circuit is used for low-speed oscillation, a long time is required from oscillation stop to oscillation start. The LCD circuit operates using a low-speed clock. LCD cannot be performed until oscillation starts. After power on, operate the low-speed oscillator circuit at all times and do not change to STOP mode.

Example 1

START mode (After warming up, program start at address 0000.)
↓
CPM3 (High / Low speed ON, SYSCP = High, LOWCP OFF)
↓ LD 26O, 7H
CPM3 (High / Low speed ON, SYSCP = High, LOWCP ON)
↓ LD 26O, 4H
CPM0 (High / Low speed ON, SYSCP = High, LOWCP ON)
↓ HALT
STOP mode (High / Low-speed OSC, STOP, SYSCP OFF, LOWCP OFF)

When an interruption occurs, the mode is changed to START mode and program start at the address which is decided by each interruption (refer to Fig.2).

Example 2

START mode (After warming up, program start at address 0000.)
↓
CPM3 (High / Low speed ON, SYSCP = High, LOWCP OFF)
↓ LD 26O, 5H
CPM1 (Low speed ON, SYSCP = Low, LOWCP ON)
↓ HALT
HALT mode (High-speed OSC OFF, Low-speed OSC ON, SYSCP OFF, LOWCP ON)

When an interruption occurs, the mode is changed to slow mode (CPM1) and program start at the address which is decided by each interruption.

Example 3

START mode (After warming up, program start at address 0000.)

↓

CPM3 (High / Low speed ON, SYSCP = High, LOWCP OFF)

↓ LD 26O, 7H

CPM3 (High / Low speed ON, SYSCP = High, LOWCP ON)

↓ LD 26O, 4H

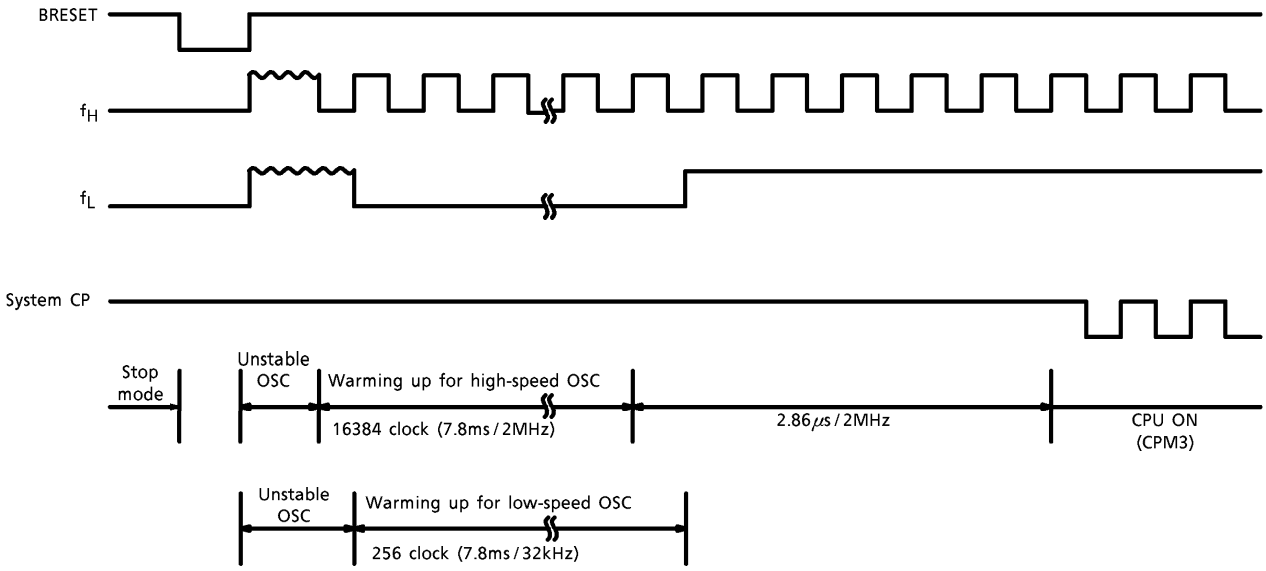
CPM0 (High / Low speed ON, SYSCP = High, LOWCP ON)

(There are no change after shift to CPM0.)

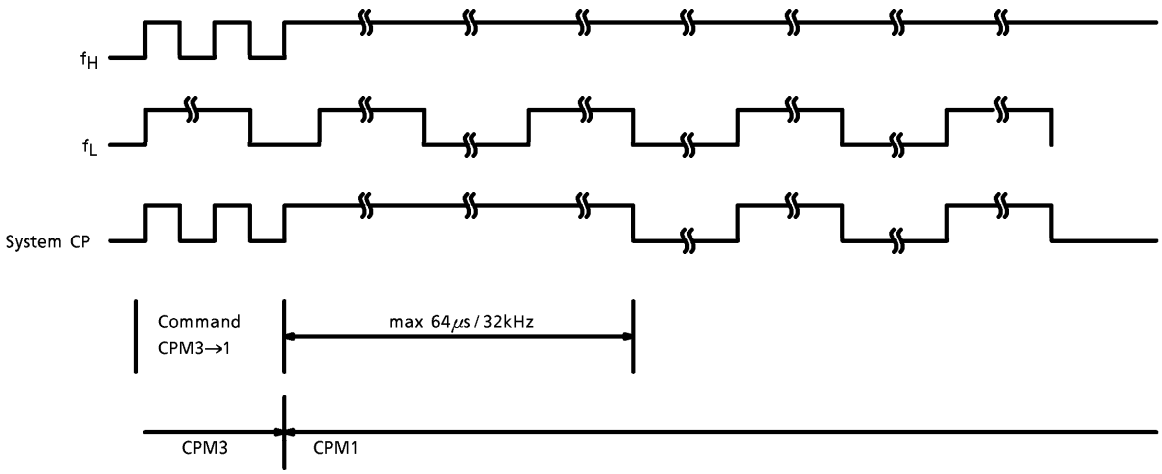
↓ LD 26O, 7H

CPM3 (High / Low speed ON, SYSCP = High, LOWCP ON)

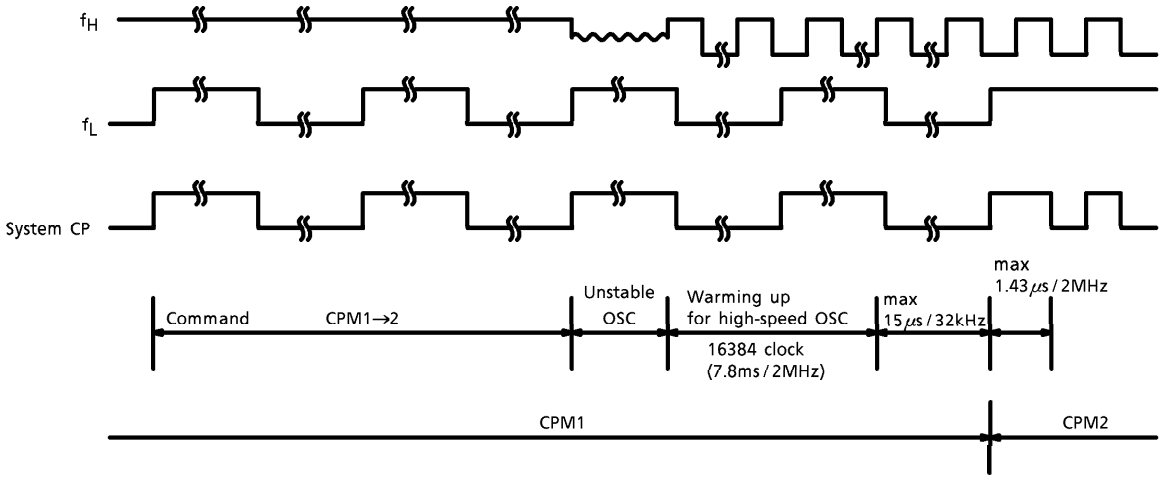
Example 4 (After reset)



Example 5 (CPM3→1)



Example 6 (CPM1→2)



(Note) No warm-up is provided for high-speed and low-speed RC oscillations by mask options.

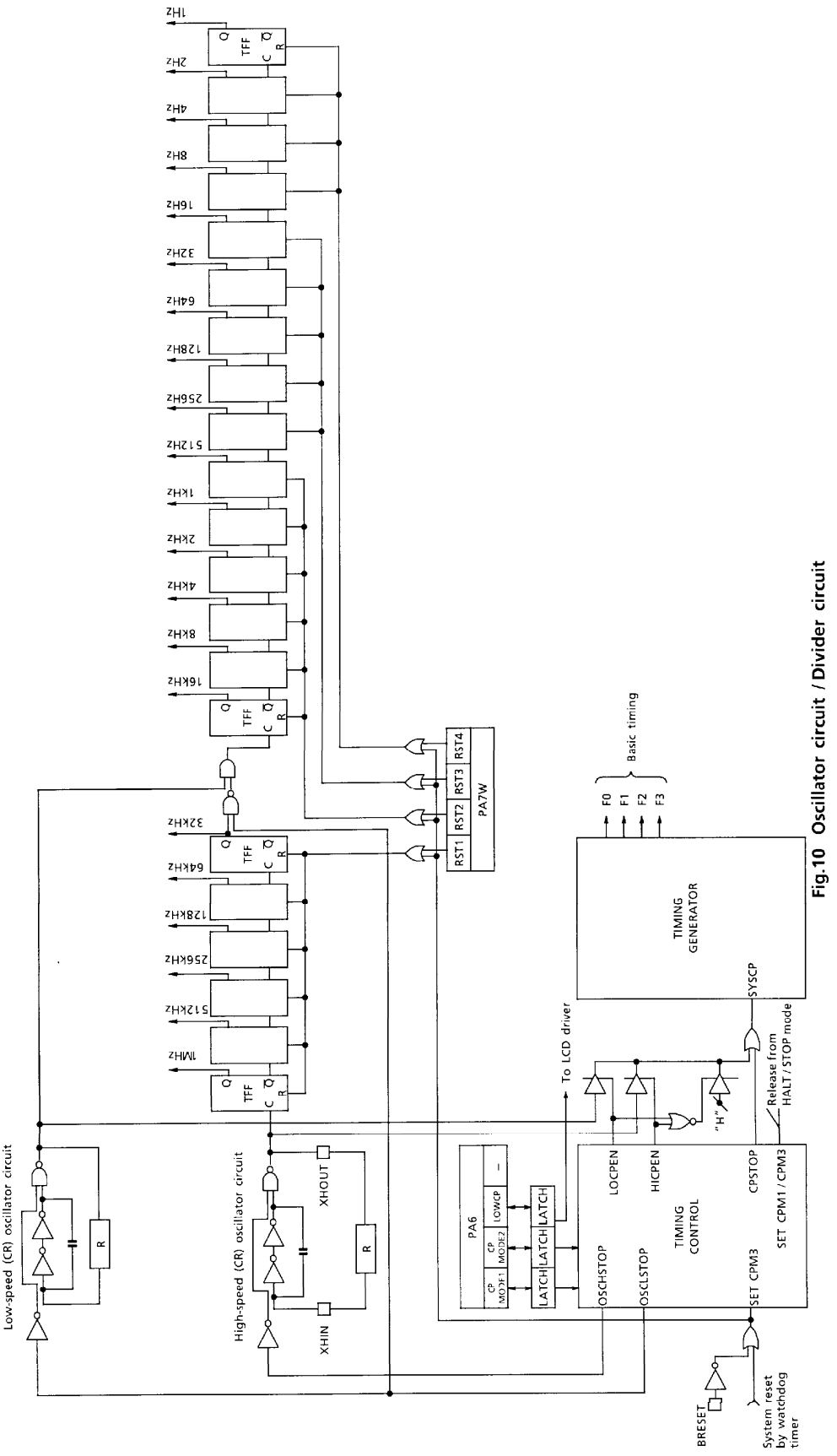


Fig.10 Oscillator circuit / Divider circuit

TMP04CH00FXXX-20

2. Interruption Block

Interruption is supplied by IN1~4, IO01~04, Timer / Counter1~2, Timing.

(Interruption Priority)

Interruption priority can be selected by Register file P1 and P2.

Interrupt priority is valid only when multiple interrupts occur simultaneously.

P1 and P2 are initially 0.

	MSB 3	2	1	0 LSB
PC7	—	—	P2	P1

P1	P2	INT0	INT1	INT2	INT3	INT4
0	0	IIN	IOIN	TIN	TCIN1	TCIN2
1	0	IOIN	IIN	TIN	TCIN1	TCIN2
0	1	TIN	IIN	IOIN	TCIN1	TCIN2
1	1	TCIN1	IIN	IOIN	TIN	TCIN2

(Higher) ← Priority → (Lower)

IIN : IN1~4, IOIN : IO01~04, TIN : Timing, TCIN1 / 2 : Timer / Counter1 / 2

(Interruption enable / disable)

Each interruption (IIN, IOIN, TIN, TCIN1, TCIN2) is decided enable / disable as follows.

IIN : IIE1~4 (R42 BIT 0~3)
IOIN : IOIE0 (R43 BIT 0)
TIN : TIE1~4 (R53 BIT 0~3)
TCIN1 : TCI1E (R64 BIT 1)
TCIN2 : TCI2E (R74 BIT 1)

After deciding priority by P1, P2 each interruption is decided enable / disable by INT0~4.

Disable the unnecessary interrupts in your application by initial settings of IIE1-4, IOIE, TIE1-4, and TCI1E / 2E.

INT0~4 are initially 0 (disable)

	MSB 3	2	1	0 LSB
R12	INT2	INT1	INT0	(0)
R13	—	—	INT4	INT3

INT0~4 = 0 INT0~4 disable
= 1 INT0~4 enable

Interrupt reset

After an interrupt occurs, reset the interrupt following the procedures described below.
First, reset IN1~IN4 interrupt / IO01~IO04 Interrupt / Timing Interrupt / Timer Counter 1 Interrupt / Timer counter 2 Interrupt.
Then reset the signal "Release from HALT / STOP Mode" by executing a transfer instruction to R12 or R13.
How to deactivate respective interrupts will be explained in the sections which describe each of the interrupts.

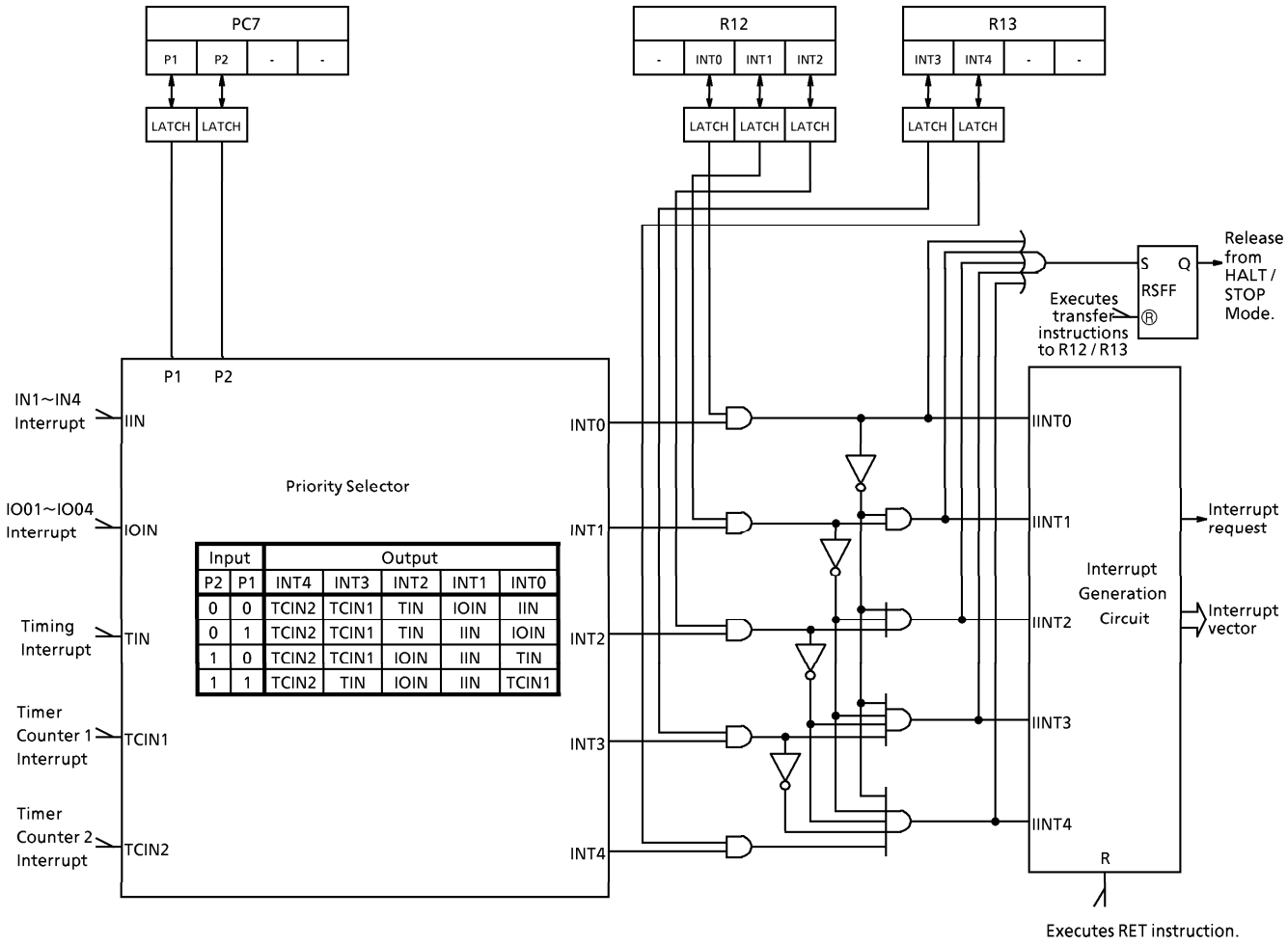


Fig.11 Interruption circuit block

2.1 Input or I / O Interruption

(Interruption enable / disable)

	MSB 3	2	1	0 LSB
PC2	IIE4	IIE3	IIE2	IIE1

IIE1 = 0 : IN1 Interruption disable
= 1 : IN1 Interruption enable
IIE2 = 0 : IN2 Interruption disable
= 1 : IN2 Interruption enable
IIE3 = 0 : IN3 Interruption disable
= 1 : IN3 Interruption enable
IIE4 = 0 : IN4 Interruption disable
= 1 : IN4 Interruption enable

IIE1~4 are initially 0 (IN1~4 Interruption disable).

	MSB 3	2	1	0 LSB
PC3	—	—	—	IOIE0

IOIE0 = 0 : IO01~4 Interruption disable
= 1 : IO01~4 Interruption enable

IOIE0 is initially 0 (disable).
Interruption enable / disable bit can use as interruption reset.
When the interruption occurs and after recognizing the interruption, it can be resetted by setting IIE1~4 or IOIE0.

(Interruption Data Read)

Interruption Data of IN1~4 can be read by Register file IIN1~4.

	MSB 3	2	1	0 LSB
PC1R	IIN4	IIN3	IIN2	IIN1

Example

```
LD 42O, 0FH    (set enable to IN1~4)
      IN1 interruption occurs.
   ↓  program goes to the address which is decided by each interruption.
LD M, 4IO      (read IN1~4 interruption)
      recognize which interruption is occurred.
   ↓  (recognize IN1 interruption is occurred.)
LD 42O, 0EH    (reset IN1 interruption)
   ↓
LD 12O, 0FH    (set enable to INT0~2)
   ↓
LD 13O, 0FH    (set enable to INT3~4)
   ↓
LD 42O, 0FH    (set enable to IN1~4 interruption)
```

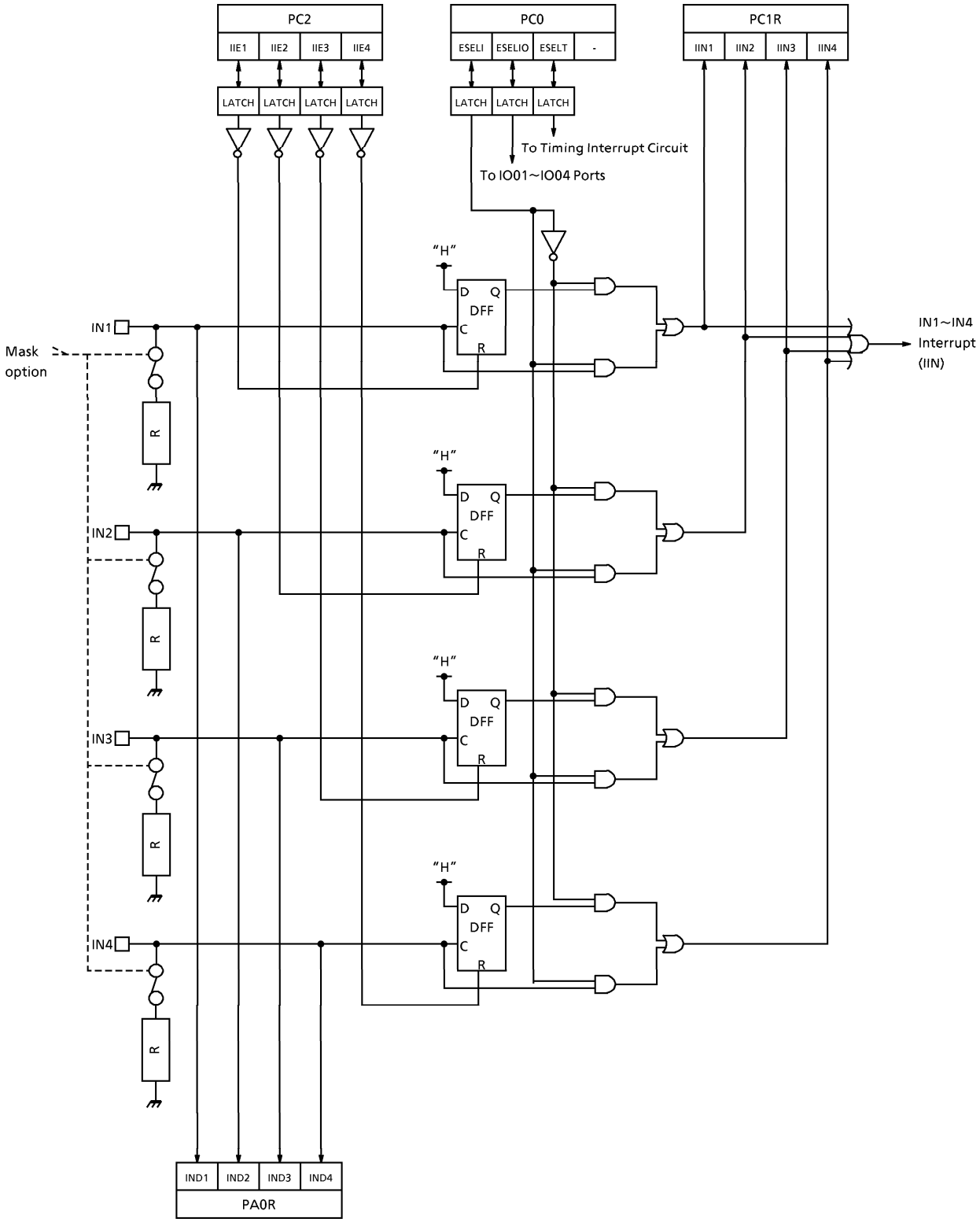


Fig.12 IN1~IN4 Interrupts

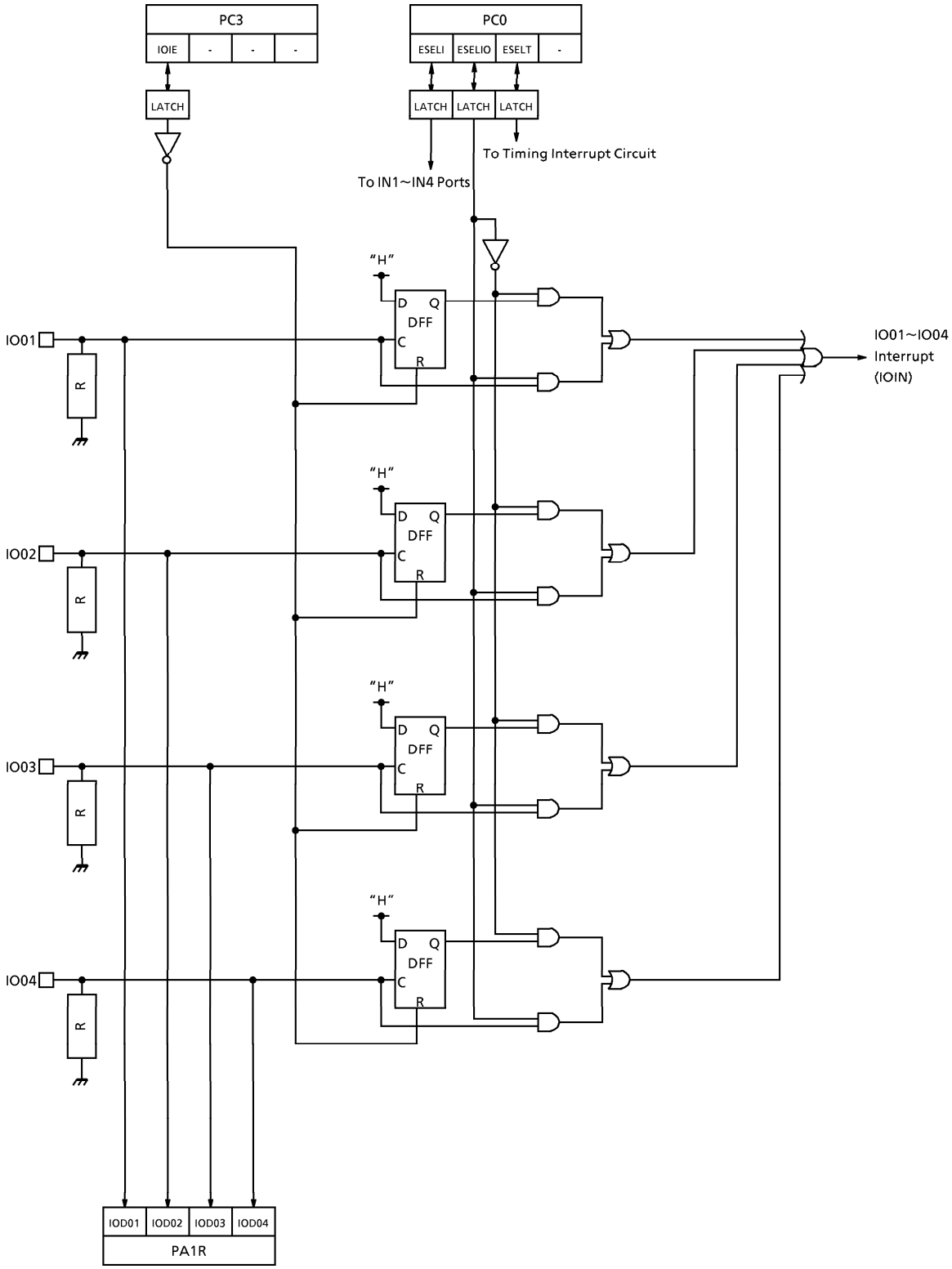


Fig.13 IO01~IO04 Interrupts

(Note) Disabling input or input / output interrupts using PC2 or PC3 is valid only when a rising edge interrupt (see 4, Input / Output ports) is selected. If a level interrupt is selected, disabling interrupts using PC2 or PC3 is invalid.

2.2 Timing Interruption

(Timing Interruption selecting)

Timing Interruptions are selectable by Register file (PD1) 128 / 256, 16 / 32, 4 / 8, 1 / 2.

	MSB 3	2	1	0 LSB
PD1	1 / 2	4 / 8	16 / 32	128 / 256

128 / 256 = 0 : 128Hz INT. select
= 1 : 256Hz INT. select
16 / 32 = 0 : 16Hz INT. select
= 1 : 32Hz INT. select
4 / 8 = 0 : 4Hz INT. select
= 1 : 8Hz INT. select
1 / 2 = 0 : 1Hz INT. select
= 1 : 2Hz INT. select

128 / 256, 16 / 32, 4 / 8 and 1 / 2 are initially 0 (1Hz, 4Hz, 16Hz, 128Hz is selected).

(Timing Interruption enable / disable)

Selected Timing Interruption can be controlled enable / disable by Register file TIE1~4 (PD3).

	MSB 3	2	1	0 LSB
PD3	TIE4	TIE3	TIE2	TIE1

TIE1 = 0 : 1Hz or 2Hz INT. disable
= 1 : 1Hz or 2Hz INT. enable
TIE2 = 0 : 4Hz or 8Hz INT. disable
= 1 : 4Hz or 8Hz INT. enable
TIE3 = 0 : 16Hz or 32Hz INT. disable
= 1 : 16Hz or 32Hz INT. enable
TIE4 = 0 : 128Hz or 256Hz INT. disable
= 1 : 128Hz or 256Hz INT. enable

TIE1~4 are initially 0 (disable).

(Timing Interruption Reset)
The timing interruption for the selected timing interruption is reset by register files TIR1 to 4 (PD2W).

	MSB 3	2	1	0 LSB
PD2W	TIR4	TIR3	TIR2	TIR1

TIR1 = 1 : 1Hz or 2Hz Interruption reset
TIR2 = 1 : 4Hz or 8Hz Interruption reset
TIR3 = 1 : 16Hz or 32Hz Interruption reset
TIR4 = 1 : 128Hz or 256Hz Interruption reset

(Timing Interruption Read)
Selected Timing Interruption can be read by Register file TI1~4 (PD0R).

	MSB 3	2	1	0 LSB
PD0R	TI4	TI3	TI2	TI1

TI1 : Interruption data of 1Hz or 2Hz
TI2 : Interruption data of 4Hz or 8Hz
TI3 : Interruption data of 16Hz or 32Hz
TI4 : Interruption data of 128Hz or 256Hz

(Interruption Edge Selection)
TIN Interruption can be selected the reading point (⌐ or ¬) by Register file ESELT.
ESTLT is initially 0 (rising EDGE).

	MSB 3	2	1	0 LSB
PC0	—	ESELT	(ESLIO)	(ESELI)

ESELT = 0 : Interruption at rising Edge of Timing INT.
= 1 : Interruption at down Edge of Timing INT.

Example

LD 51O, 01H (256Hz, 16Hz, 4Hz, 1Hz, select)

↓

LD 53O, 07H (256Hz disable, 16Hz, 4Hz, 1Hz enable)

↓ When the 1Hz interruption occurs.

LD M, PD0 (read timing interruption)

↓ Recognize 1Hz interruption.

LD 52O, 01H (reset 1Hz interruption)

(Note) Since a mode transition from CPM1 or 3 to CPM2 or from CPM2 to CPM1 or 3 causes the timing of the binary counters 7-21 to change, timing interrupts also have their timings changed.

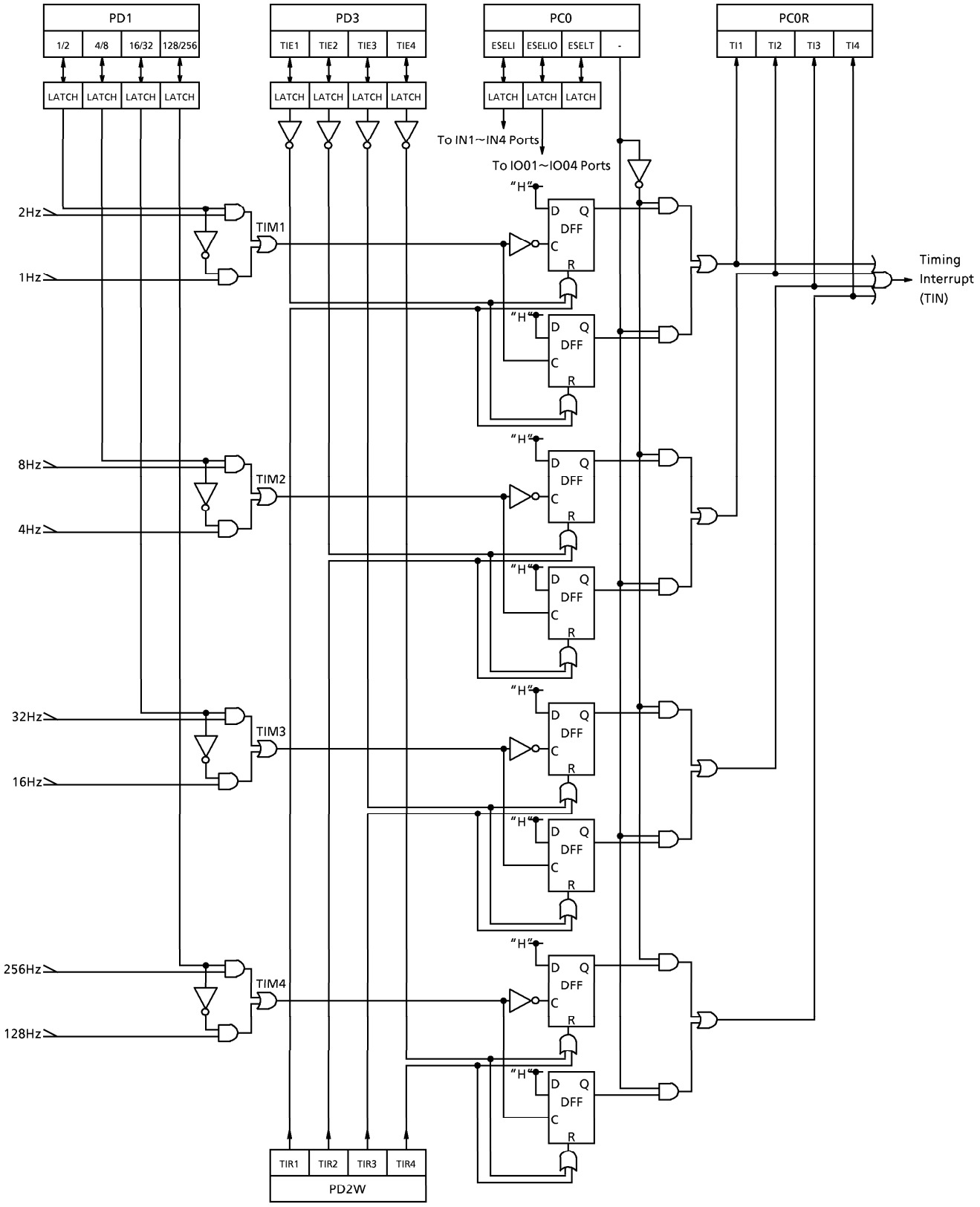
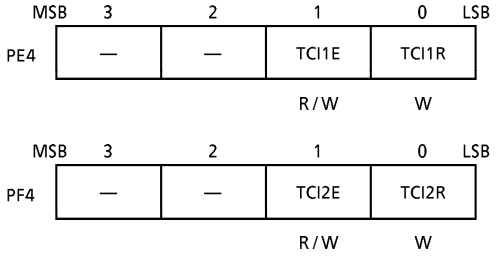


Fig.14 Timing Interrupt Circuit

2.3 8 bits / 16 bits Timer Counter Interruption

When Timer / Counter1, 2 overflow or coincide with setting Time / Count, each Interruption occurs.



TCI1E / TCI2E = 1 : Timer / Counter1, 2 Interruption enable
= 0 : Timer / Counter1, 2 Interruption disable
TCI1R / TCI2R = 1 : Timer / Counter1, 2 Interruption reset

TCI1E, TCI2E and TCI2R are initially 0 (DISABLE).

3. Timer / Counter

The Timer / Counter circuit can use as 8 bit × 2ch or 16 bit × 1ch Timer / Counter.
And there Time / Counter can be use as general Timer / Counter, Watch Dog Timer, or Multi Interruption Timer.

8 bits / 16 bits can be switched by Register file TCPS. And input frequency also can be changed by Register CKS11~13 and CKS21~23, as follows.

	MSB 3	2	1	0 LSB
PE2	—	CKS13	CKS12	CKS11

	MSB 3	2	1	0 LSB
PF2	TCPS	CKS23	CKS22	CKS21

CKS 11	CKS 12	CKS 13	Input Frequency for Timer Counter1 (f_H = 2MHz, f_L = 32kHz)		
0	0	0	$fH / 2^{21}$ ($fL / 2^{15}$)	1Hz	(1.0s)
1	0	0	$fH / 2^{12}$ ($fL / 2^{6}$)	512Hz	(19.5ms)
0	1	0	$fH / 2^{8}$ ($fL / 2^{2}$)	2^{13}kHz	(122μs)
1	1	0	$fH / 2^{3}$	2^{18}kHz	(3.81μs)
—	—	1	OFF		

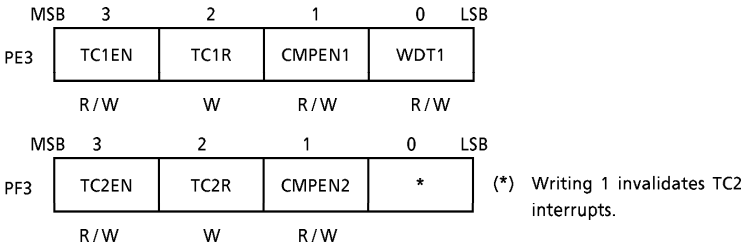
CKS 21	CKS 22	CKS 23	Input Frequency for Timer Counter2 (f_H = 2MHz, f_L = 32kHz)		
0	0	0	$fH / 2^{15}$ ($fL / 2^{9}$)	64Hz	(15.6ms)
1	0	0	$fH / 2^{9}$ ($fL / 2^{3}$)	2^{12}kHz	(244μs)
0	1	0	$fH / 2^{5}$	2^{16}kHz	(15.2μs)
1	1	0	$fH / 2^{2}$	2^{19}kHz	(1.90μs)
—	—	1	OFF		

TCPS = 0 : 8bit × 2ch Timer / Counter
= 1 : 16bit × 1ch Timer / Counter

(When Timer / Counter is used as 16 bits timer, TIMER2 is used as lower bits.
And CKS11~13 are ignored. Input Frequency is decided by CKS21~23.)

CKS11~13, CKS21~23, TCPS are initially 0.
(Timer / Counter1 : 1Hz, Timer / Counter2 : 64Hz, 8bit × 2ch)
(CAUTION)
256kHz of Timer / Counter1, 512kHz, 64kHz of Timer / Counter2 can be used when High-speed OSC is on.

Timer function can be selected by Register file / WDT1 and CMPEN1, 2.
Timer / Counter1 can be used as Watch Dog Timer.
And Input Frequency can be controlled by Register file TC1EN and TC2EN.
Timer / Counter is resetted by Register file TC1R, TC2R.

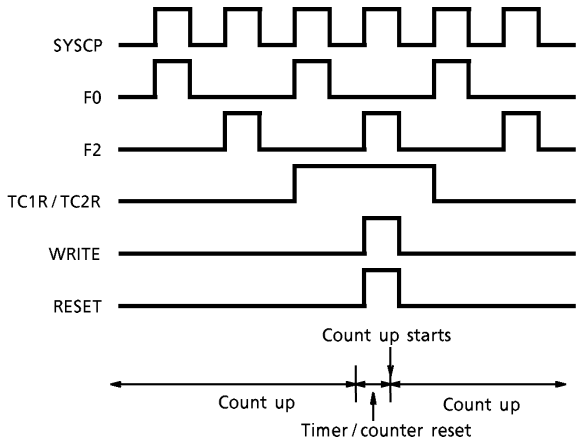


Timer / Counter1 setting is made in PE3.
Timer / Counter2 setting is made in PF3.

All the bits of PE3 and PF3 are initially 0.

PE3	WDT1	= 0	:	Used as 8-Bit Timer / Counter.
		= 1	:	Used as Watchdog Timer.
	CMPEN1	= 0	:	An interrupt is generated if Timer / Counter1 overflows. (The entire system is reset if WDT1 = 1.)
		= 1	:	An interrupt is generated if Timer / Counter1 values match Time / Count set values. (The entire system is reset if WDT1 = 1.)
	TC1R	= 1	:	Timer / Counter1 is reset (cleared). Timer / Counter1 resumes counting up after reset. (Refer to the timing chart below.)
	TC1EN	= 0	:	Reference clock input on Timer / Counter1 is stopped.
		= 1	:	Reference clock input on Timer / Counter1 is started.
PF3	BIT0	= 1	:	Timer / Counter2 cannot be used as 8-Bit Timer / Counter.
		= 0	:	Timer / Counter2 is used as 8-Bit Timer / Counter.
	CMPEN2	= 0	:	An interrupt occurs if Timer / Counter2 overflows.
		= 1	:	An interrupt occurs if Timer / Counter2 values match Time/Count set values.
	TC2R	= 1	:	Timer / Counter2 is reset (cleared). Timer / Counter2 resumes counting up after reset. (Refer to the timing chart below.)
	TC2EN	= 0	:	Reference clock input on Timer / Counter2 is stopped.
		= 1	:	Reference clock input on Timer / Counter2 is started.

Timing chart for timer / counter 1 / 2 reset



Timer / Counter1, 2 data can read from Register file TCR11~18 and TCR21~28.

	MSB 3	2	1	0 LSB
PE0R	TCR14	TCR13	TCR12	TCR11
PE1R	TCR18	TCR17	TCR16	TCR15
PF0R	TCR24	TCR23	TCR22	TCR21
PF1R	TCR28	TCR27	TCR26	TCR25

Timer / Counter1, 2 Comparison data is set by Register file SET11~18 and SET21~28.

	MSB 3	2	1	0 LSB
PE0W	SET14	SET13	SET12	SET11
PE1W	SET18	SET17	SET16	SET15
PF0W	SET24	SET23	SET22	SET21
PF1W	SET28	SET27	SET26	SET25

SET11~18 and SET21~28 are initially 0.

(CAUTION)

1. When generating an interrupt for the timer / counter by comparing it with the setup value (SET11-18, SET21-28) or resetting the system, set the setup values in register files SET11-18 and SET21-28 before enabling CMPEN1 and 2.
2. When generating an interrupt by a 16-bit timer by comparing it with the setup value, enable all of CMPEN1, CMPEN2, TC1EN, and TC2EN using instructions.
3. Since the setup values and timer / counter values both are 0 after initialization, an interrupt is generated or the system is reset immediately when CMPEN1 is enabled.
4. Since a mode transition from CPM1 or 3 to CPM2 or from CPM2 to CPM1 or 3 causes the timing of the binary counters 7-21 to change, the timer / counters also have their timings changed.
5. Do not change the timer / counter from 8bits to 16bits in the middle of operation after the timer / counter has started counting, because such a change could cause the data to be destroyed.

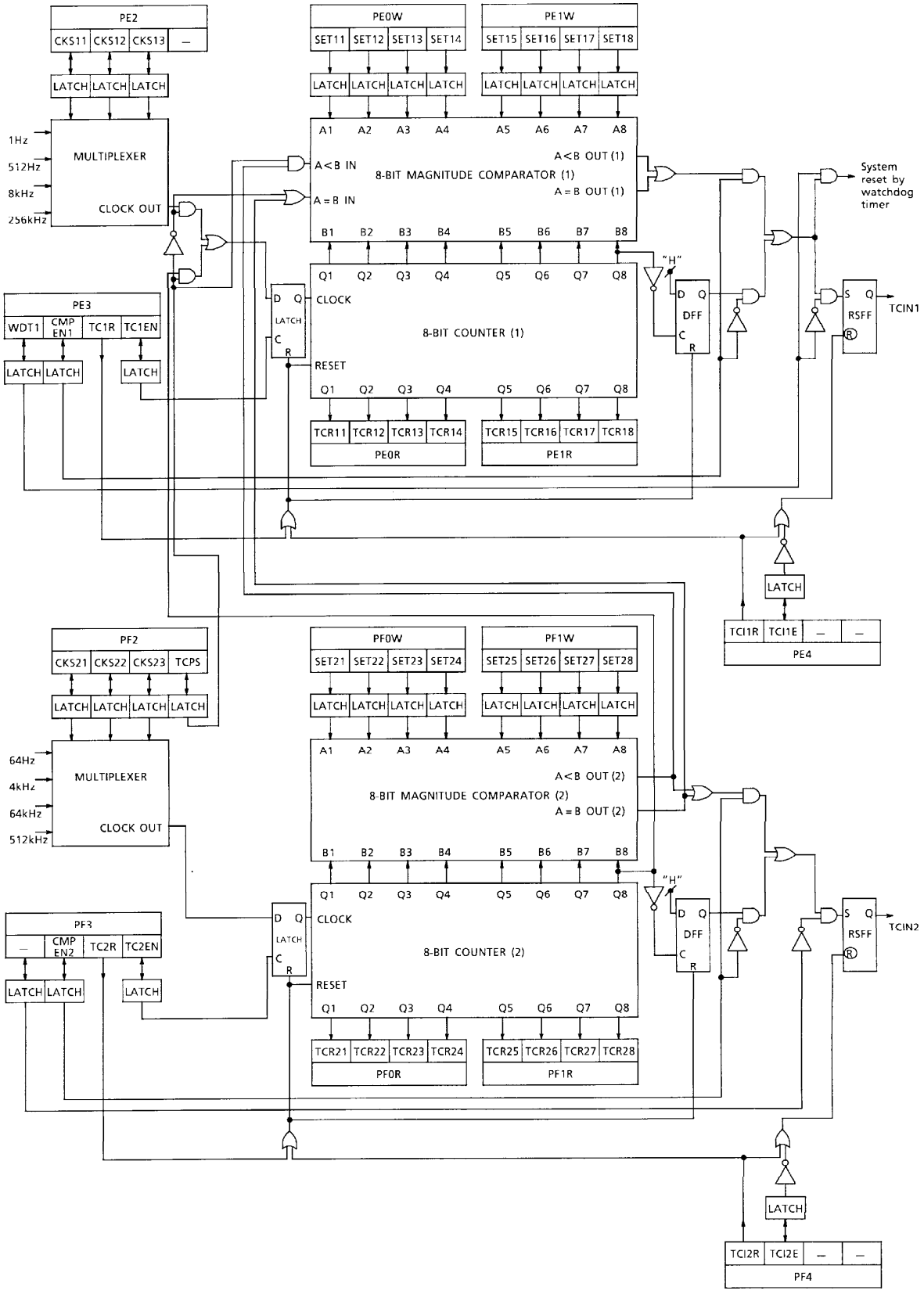


Fig.15 Timer / Counter

4. Input / IO PORTS (Refer to Fig.18)

TMP04CH00FXXX has 8 inputs and 8 I / O ports.
8 input ports have Interruption.

4.1 INPUT (IN1~4)

Each input data can be read by Register file IND1~4.

	MSB 3	2	1	0 LSB
PA0R	IND4	IND3	IND2	IND1

Each input Interruption function can be set enable / disable by Register file IIE1~4.

	MSB 3	2	1	0 LSB
PC2	IIE4	IIE3	IIE2	IIE1

IIE1~4 = 0 : IN1~IN4 each Interruption disable
= 1 : IN1~IN4 each Interruption enable

(Note) IIE1 to IIE4 interrupt disable / enables are register files that are effective when rising-edge interrupts are selected.
When level interrupts are selected, interrupts are disabled / enabled by the data input from ports. In this case, therefore, interrupts cannot be disabled / enabled by the register files.

4 inputs (IN1~4) Interruption data can be read by Register file IIN1~4.

	MSB 3	2	1	0 LSB
PC1R	IIN4	IIN3	IIN2	IIN1

(Note) Interrupt data IO01 to IO04 cannot be read out. Only the data input from ports can be read out. (Refer to Fig.13.)
Interrupt timings (rising edge / level) can be selected using register file ESELI.

Each input Interruption recognized timing (rising edge / High level) can be selected by Register file ESELI (R40 bit1).

	MSB 3	2	1	0 LSB
PC0	—	(ESELT)	(ESELIO)	ESELI

ESELI = 0 IN1~4 : Interruption at rising edge of input INT.
= 1 IN1~4 : High level of input INT .

Input level-triggered interrupts are possible when ESELI = 1. In this case, if interrupts have been enabled by register files INT0-4, the interrupt remain asserted while the input level is high.

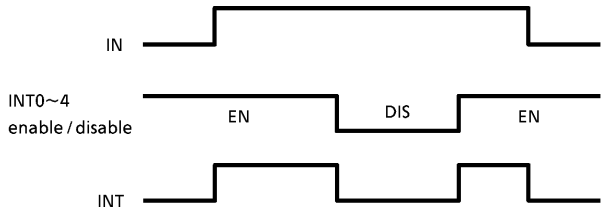


Fig.16 Interruption by high level-read

Input ports (IO01~IO04)

The input data can be read out via register files IOD01~IOD04.

	MSB 3	2	1	0 LSB
PA1R	IOD04	IOD03	IOD02	IOD01

IOD01 to IOD04 have an interrupt facility, so that interrupts can be disabled / enabled by register file IOIE0. (Four interrupt sources are collectively disabled / enabled by IOIE0.)

	MSB 3	2	1	0 LSB
PC3	—	—	—	IOIE0

IOIE0 = 0 : Interrupts IO01~IO04 are disabled.
= 1 : Interrupts IO01~IO04 are enabled.

(Note) The IO01~IO04 interrupt disable / enables are the register files that are effective when rising-edge interrupts are selected.
When level interrupts are selected, interrupts are disabled / enabled by the data input from ports. In this case, therefore, interrupts cannot be disabled / enabled by the register files.
The interrupt data IO01~IO04 cannot be read out. Only the data input from ports can be read out. (Refer to Fig.13.)

Interrupt timings of IO01~IO04 (rising edge / level) can be selected using register file ESELIO.

	MSB 3	2	1	0 LSB
PC0	—	(ESELT)	ESELIO	(ESELI)

ESELIO = 0 : Interrupts IO01~IO04 are rising edge-triggered.
= 1 : Interrupts IO01~IO04 are level-triggered.

Input level-triggered interrupts are possible when ESELIO = 1. In this case, if interrupts have been enabled by register files INT0~4, the interrupt remain asserted while the input level is high.

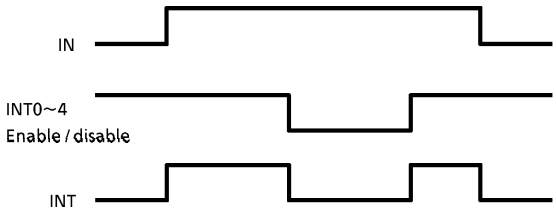


Fig.17 Level-triggered interrupts

4.2 I/O ports (IO11~IO14, IO21~IO24)

Each input data can be read by following Register file, when using input port.

	MSB 3	2	1	0 LSB
R14R	IOD14	IOD13	IOD12	IOD11
R15R	IOD24	IOD23	IOD22	IOD21

When using each input/output port for output, the output data can be set using the register file shown below.

	MSB 3	2	1	0 LSB
R14R	IOD14	IOD13	IOD12	IOD11
R15R	IOD24	IOD23	IOD22	IOD21

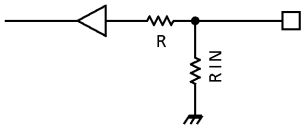
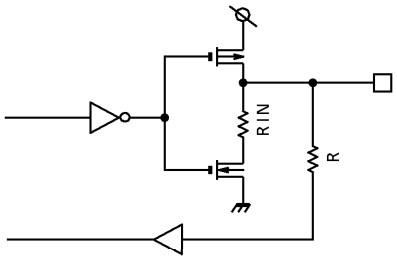
	Input/Output Circuit
IN1~IN4 IO01~IO04	
IO11~IO14 IO21~IO24	

Fig.18 Structure of input/output port

RIN : Internal pull-down resistor, 400kΩ (typ.)
R : Input protective resistor, 100Ω (typ.)

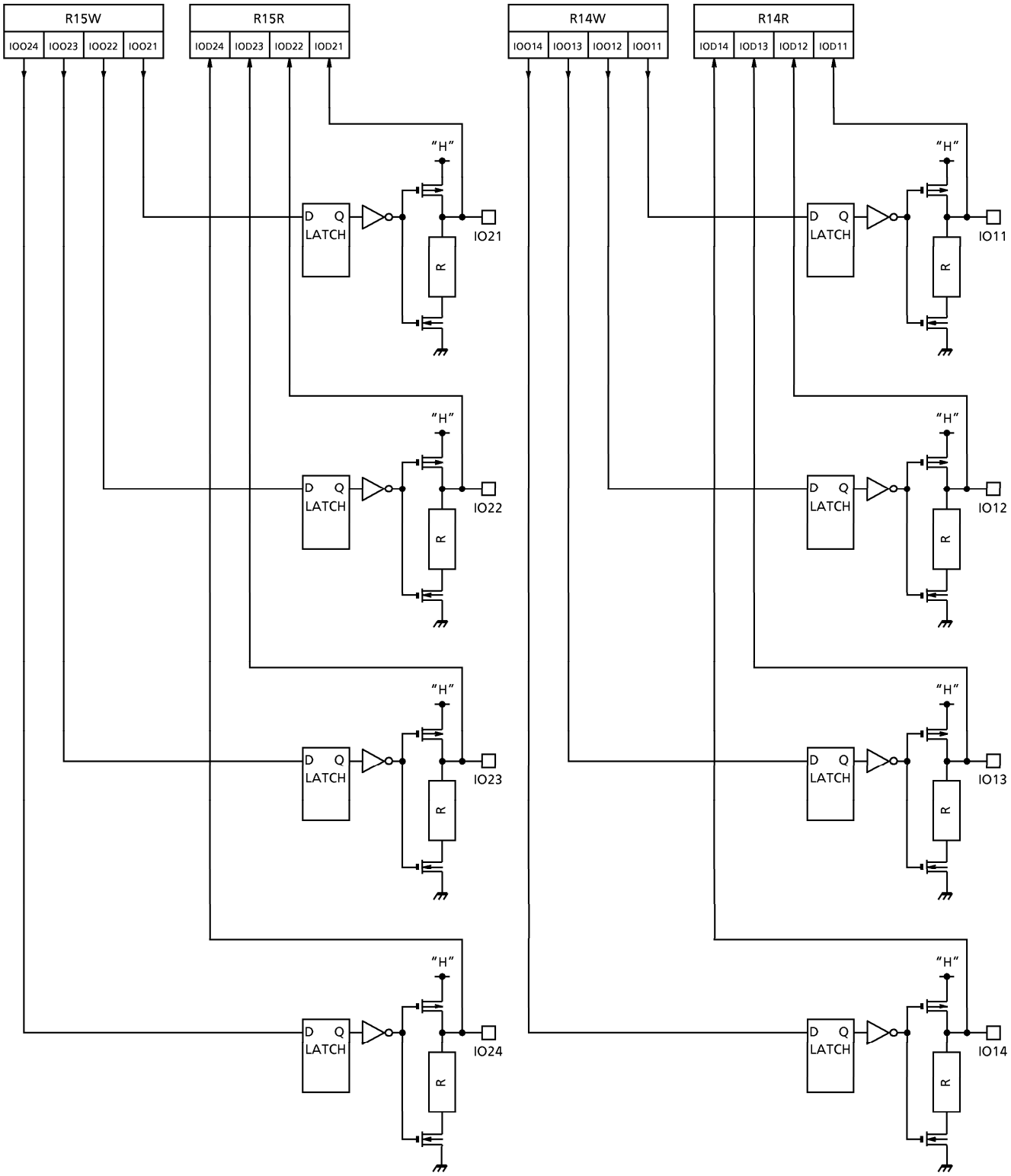


Fig.19 IO11~IO14, IO21~IO24

5. Buzzer Circuit

Buzzer sound can be selected by Register file BZ1, BZ2, BZ3 and 2k / 4k.

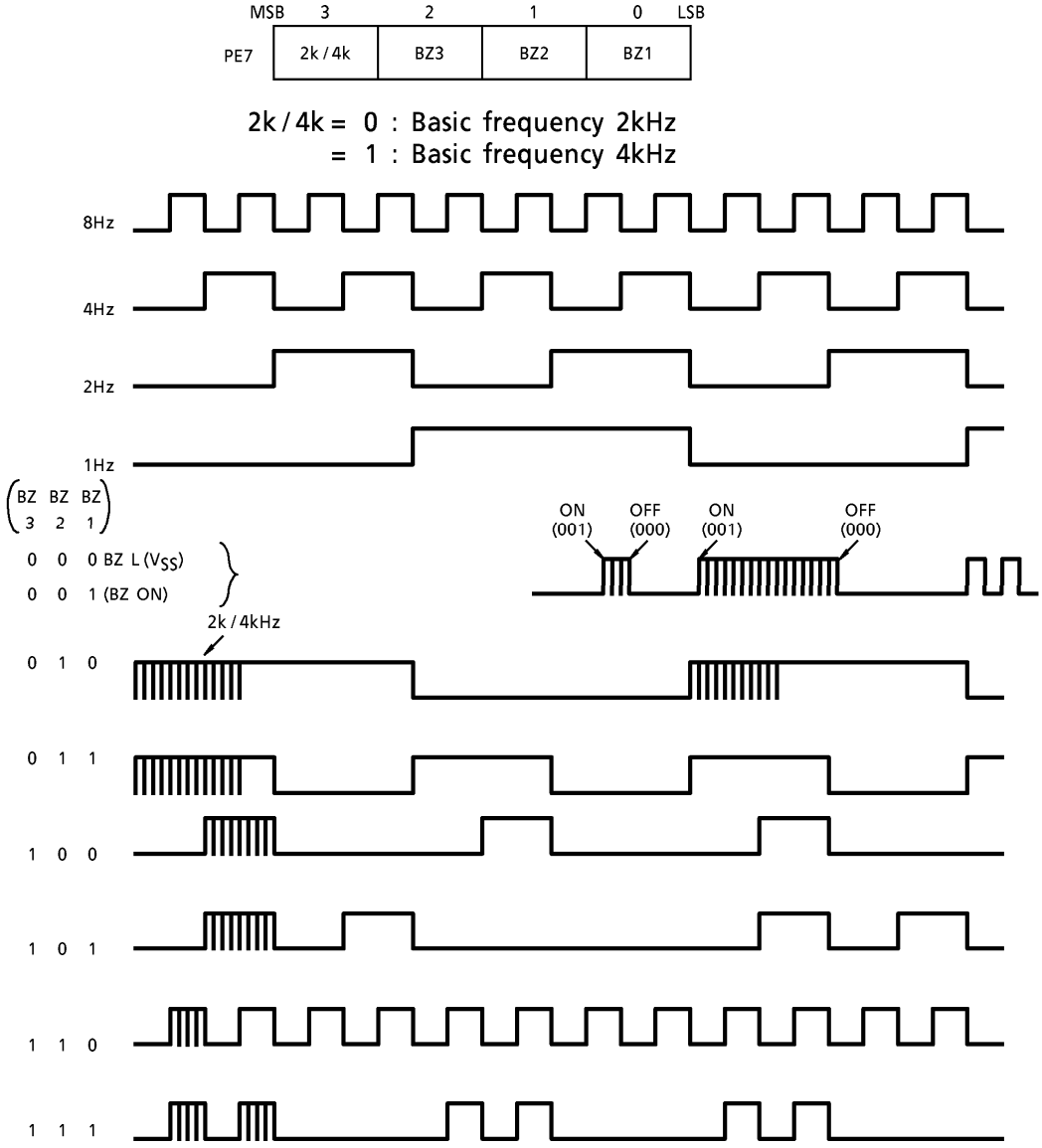
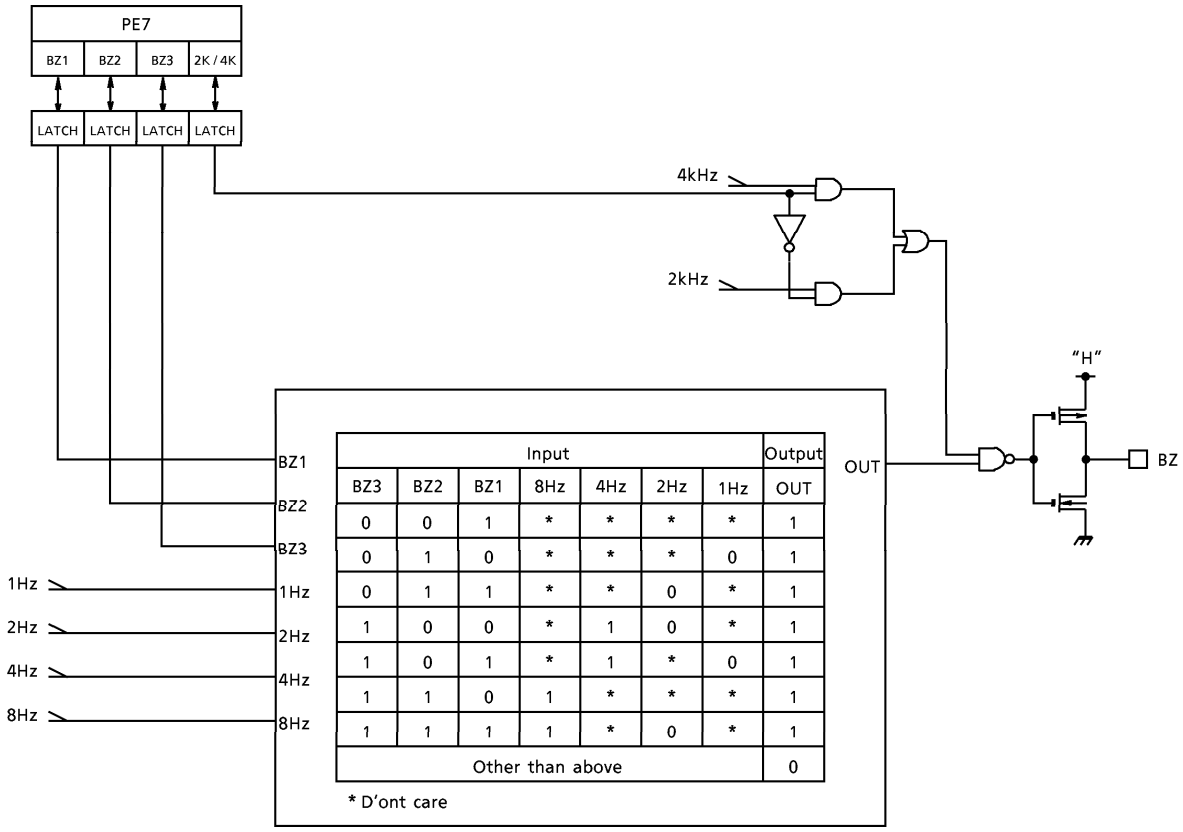


Fig.20 Buzzer sound

BZ sound can be made by software using (000), (001) setting, as above.
When the Register file R67 is set the above ((BZ3, BZ2, BZ1) = (010)~(111)), each BZ sound is continuously released setting (BZ3, BZ2, BZ1) to (000).

(Note) The above buzzer sounds are shown with respect to timings in the CPM2 mode where the high-speed oscillation frequency is 2MHz, the CPM1 / 3 mode where the low-speed oscillation frequency is 32kHz, and in the HALT mode.



Input							Output
BZ3	BZ2	BZ1	8Hz	4Hz	2Hz	1Hz	OUT
0	0	1	*	*	*	*	1
0	1	0	*	*	*	0	1
0	1	1	*	*	0	*	1
1	0	0	*	1	0	*	1
1	0	1	*	1	*	0	1
1	1	0	1	*	*	*	1
1	1	1	1	*	0	*	1
Other than above							0

Fig.21 Buzzer Circuit

6. LCD Circuit

The LCD driver circuit has common signals and segment signals to drive 4.5V, 1/8 or 1/10 duty, 1/4 bias LCD.

Duty can be selected by Mask option either 1/8 or 1/10.

Duty	Frame Frequency	COMMON	SEGMENT
1/8	97.5Hz	COM1~COM8	S1~S60 (S53~S60 = COM9~COM16)
1/10	117.0Hz	COM1~COM10	S1~S58 (S53~S58 = COM11~COM16)

The LCD driver circuit is controlled by Register file both DSTA and DON, and Display RAM is enable on DRCE = 1.

	MSB 3	2	1	0 LSB
PC6W	—	DRCE	DON	DSTA

DSTA = 0 : com / seg = V_{SS}
= 1 : enable normal Display
DON = 0 : Booster circuit (Quadrupler) OFF
= 1 : Booster circuit (Quadrupler) ON
DRCE = 0 : disable Display RAM
1 : enable Display RAM

(CAUTION)

1. Display signals from segment and common are made by the clock which come from low-speed oscillation. Even though the high-speed oscillator may be operating no display is output unless the low-speed oscillator is operating.
2. Register file DON and DSTA are read to Display Driver circuit by the clock which is made by LOWCP.
   When the LOWCP is needed OFF it is needs max. 103ms after changing the data of DON and DSTA.

LCD drive waveform

(1) 1 / 8 duty

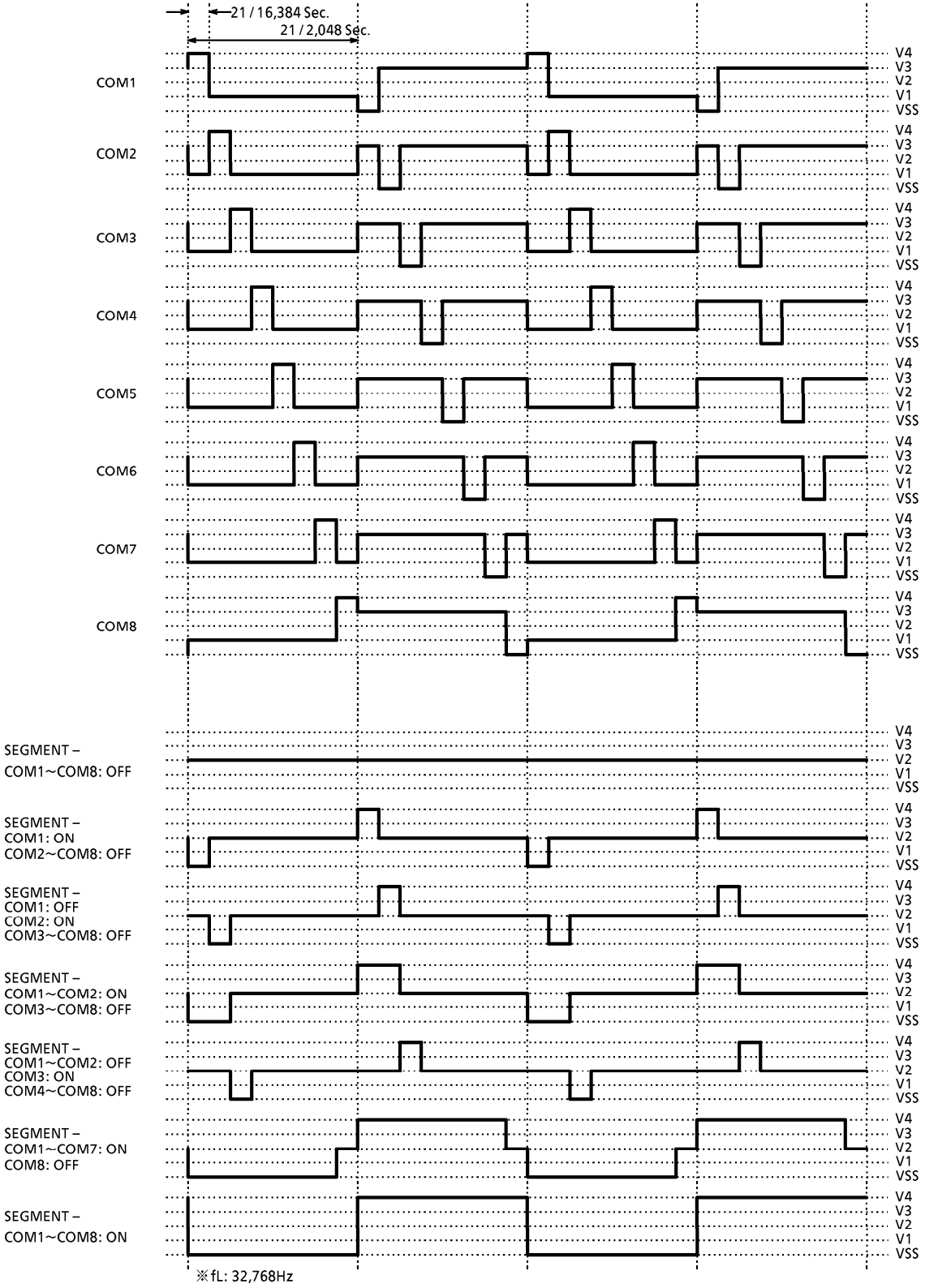


Fig.22 LCD drive waveform (1 / 8 duty)

(2) 1 / 10 duty

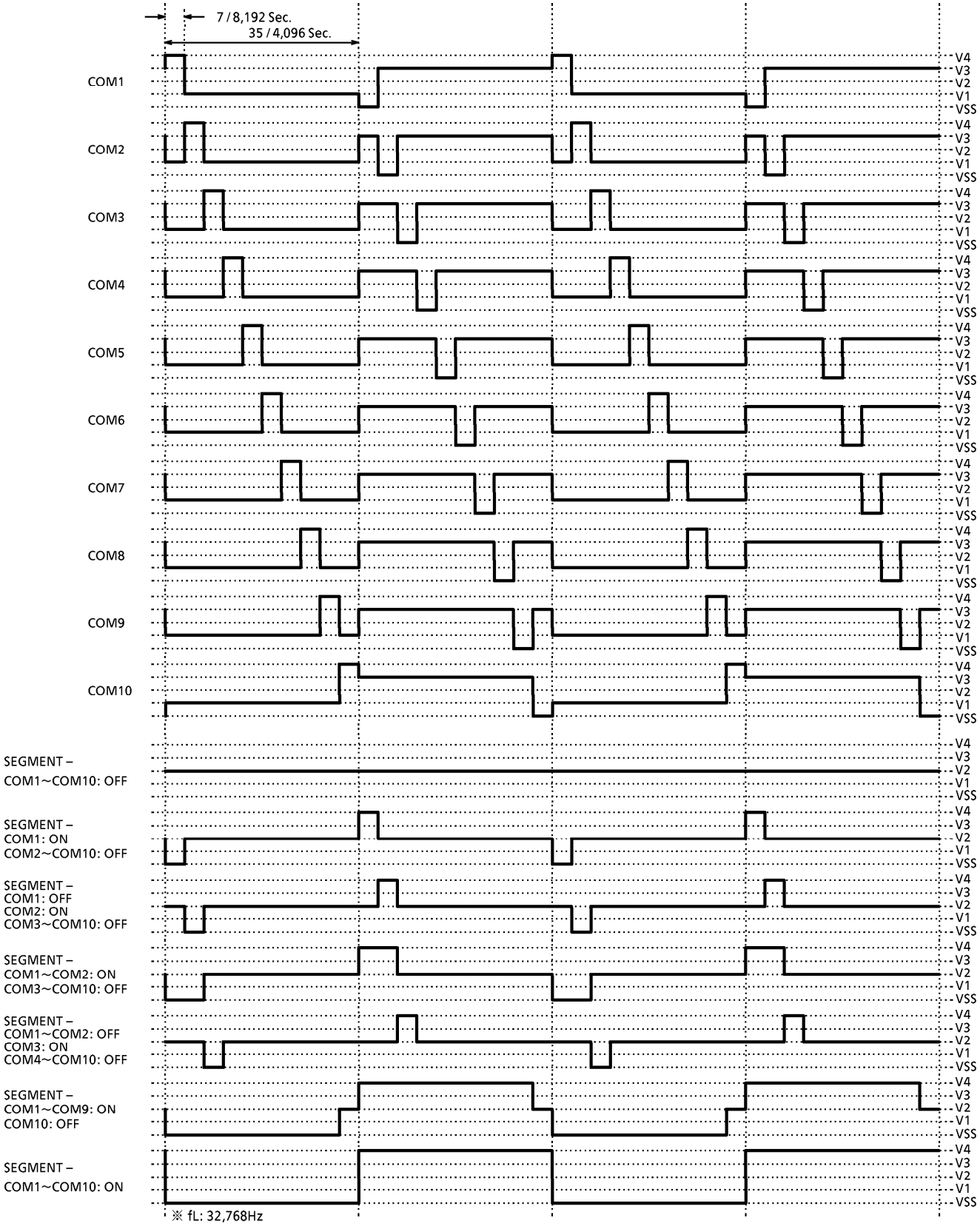


Fig.23 LCD drive waveform (1 / 10 duty)

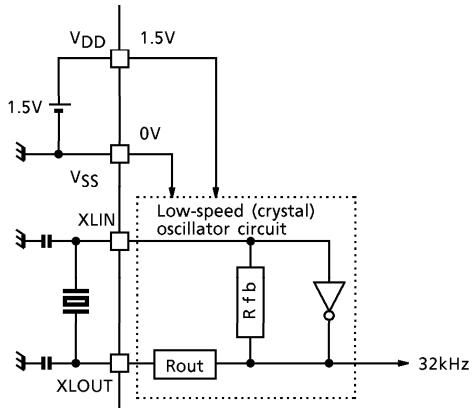
7. Mask option

TMP04CH00FXXX has 10 Mask option.

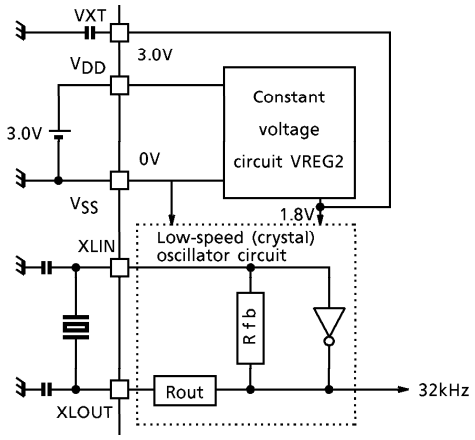
Mask code	Battery	Duty	Segment	High-speed OSC	Low-speed OSC	IN1~IN4 Pull-down Resister
A1081	1.5V	1 / 8	60	CR	X'tal	Incorporated
A1083	1.5V	1 / 8	60	CR	CR	Incorporated
A10A1	1.5V	1 / 10	58	CR	X'tal	Incorporated
A10A3	1.5V	1 / 10	58	CR	CR	Incorporated
A3080	3.0V	1 / 8	60	X'tal	X'tal	Incorporated
A3081	3.0V	1 / 8	60	CR	X'tal	Incorporated
A3083	3.0V	1 / 8	60	CR	CR	Incorporated
A30A0	3.0V	1 / 10	58	X'tal	X'tal	Incorporated
A30A1	3.0V	1 / 10	58	CR	X'tal	Incorporated
A30A3	3.0V	1 / 10	58	CR	CR	Incorporated
A3480	3.0V	1 / 8	60	X'tal	X'tal	Not incorporated
A34A0	3.0V	1 / 10	58	X'tal	X'tal	Not incorporated

(1) Supply voltage

Either 1.5V or 3.0V can be selected as the supply voltage. When 3.0V is used, the low-speed oscillator circuit is driven by output from the internal constant voltage circuit (VREG2) thus reducing current dissipation.



When 1.5V selected



When 3.0V selected

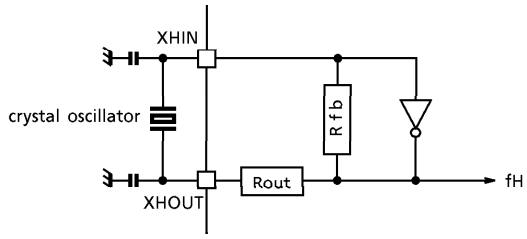
(2) LCD duties / number of segments

Either 1 / 8 or 1 / 10 can be selected as the LCD duty. When 1 / 8 is selected, the number of segment pins is 60. When 1 / 10 is selected, the number of segment pins is 58. Among LCD drive pins, the functions (segment / common) of S59 / COM10 and S60 / COM9 are switched depending on the duty selected.

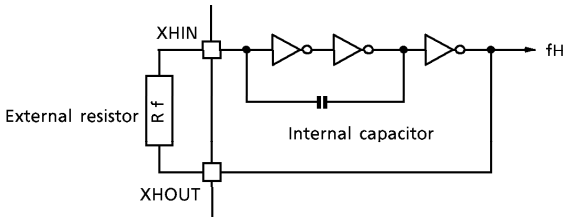
(3) High-speed oscillator circuit

Either the crystal or the CR oscillator circuit can be selected as the high-speed oscillator circuit.

(Note)After a reset, the CPU starts operating using the high-speed clock as the system clock. Therefore, even if only a low-speed clock is used for the following processes, the high-speed oscillator circuit must operate normally at startup. Select either the crystal or the CR oscillator circuit and correctly connect the external component (crystal oscillator or resistor) to the XHIN / XHOUT pin.



When crystal oscillator circuit is selected

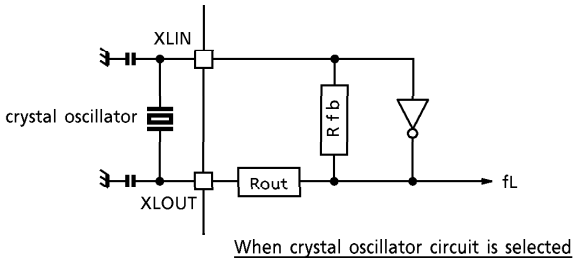


When CR oscillator circuit is selected

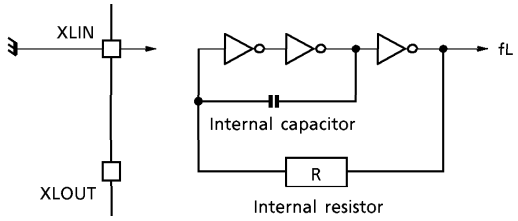
(4) Low-speed oscillator circuit

Either the crystal or the CR oscillator circuit can be selected as the low-speed oscillator circuit.

(Note)A low-speed clock is used in the LCD driver circuit. To display the LCD, the low-speed oscillator circuit must be operated. When the CR oscillator circuit is selected, because both resistor and capacitor are built in, an external component is not required. Connect the XLIN pin to V_{SS}. If the pin is left open, the internal circuit gates become unstable, possibly allowing surge current to flow.



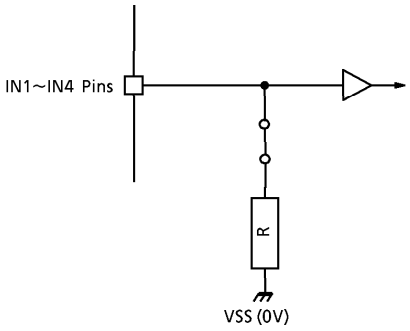
When crystal oscillator circuit is selected



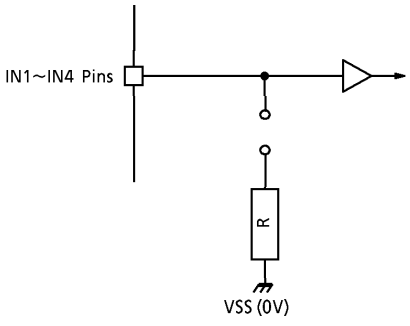
When CR oscillator circuit is selected

(5) IN1~IN4 pull-down resistor

Pull-down resistor for IN1~IN4 Pins can be chosen to be incorporated or not incorporated.



Pull-down resistor incorparated



Pull-down resistor not incorporated

◆ELECTRICAL CHARACTERISTICS

1. Absolute maximam ratings (V_{SS} = 0V)

Characteristic	Symbol	Rating	Unit
Power Supply Voltage	V_{DD}	−0.3~6.0	V
Input Voltage	V_{IN}	−0.3~V_{DD} + 0.3	V
Power Dissipation (T_{ope} = 80°C)	P_D	350	mW
Solder Temperature	TSOLDER	260 (10sec.)	°C
Storage Temperature	T_{stg}	−55~125	°C
Operating Temperature	T_{ope}	0~40	°C

2. 1.5V version (Unless otherwise specified, V_{SS} = 0V, T_{opr} = 0~40°C)

(Recommended operating condition)

Characteristic		SymboL	Test condition	Min	Typ.	Max	Unit
Power Supply Voltage		V_{DD}	f_{XTH} = 200kHz	1.2	1.5	1.8	V
Oscillation Frequency		f_{XTL1}	V_{DD} = 1.2~1.8V (Note 1)	—	32.768	—	kHz
		f_{XTL2}	V_{DD} = 1.5V (Note 2)	20	33	55	
		f_{XTH1}	V_{DD} = 1.5V (Note 3)	—	200	—	
Input Voltage	"H" Level	V_{IH}	V_{DD} = 1.3V	V_{DD} ×0.8	—	V_{DD}	V
			V_{DD} = 1.7V	V_{DD} ×0.7	—	V_{DD}	
	"L" Level	V_{IL}	V_{DD} = 1.3V	0	—	V_{DD} ×0.2	
			V_{DD} = 1.7V	0	—	V_{DD} ×0.3	
Quadrupler Capacitance		C_1, C_2		—	0.1	—	μF
Voltage Capacitance		V_1		—	0.1	—	μF
		V_2		—	0.1	—	
		V_3		—	0.1	—	
		V_4		—	0.1	—	

(Note 1) Crystal oscillation circuit is used for low-speed oscillator.
(Note 2) Internal CR oscillator is used for low-speed oscillator.
(Note 3) An RC oscillating circuit configured with an external R is used for the high-speed oscillator.

Oscillation

Characteristic	Symbol	Test condition	Min	Typ.	Max	Unit
OSC Starting Voltage	V_{STA}	T_{STA} = 10s, T_{opr} = 25°C (Note 1)	1.4	—	—	V
OSC Holding Voltage	V_{HOLD}	(Note 1)	1.2	—	—	V
Frequency of Internal CR OSC	f_{OSC1}	V_{DD} = 1.5V (Note 2)	20	33	55	kHz
Frequency of High-Speed OSC	f_{OSC2}	V_{DD} = 1.5V, R_f = 150kΩ (Note 3)	—	200	—	kHz

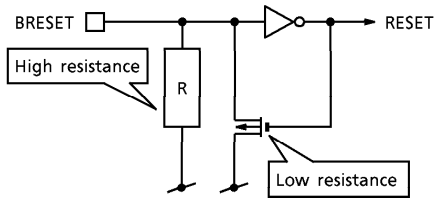
(Note 1) Crystal oscillation circuit for low-speed oscillator.Input 1.4V or more at power-on.
(Note 2) Internal CR oscillator for low-speed oscillator.
(Note 3) An RC oscillating circuit configured with an external R is used for the high-speed oscillator.

DC CHARACTERISTICS

Characteristic	Symbol	Test condition		Min	Typ.	Max	Unit
Input Current (1) (IN1~4, IO01~04, IO11~14, IO21~24)	I_{IH1}	V_{DD} = 1.8V, V_{IN} = 0V		−500	—	500	nA
	I_{IL1}	V_{DD} = 1.8V, V_{IN} = 1.8V		3.21	4.5	7.5	μA
Input Current (2) (BRESET)	I_{IH2L} (Note)	V_{DD} = 1.8V, V_{IN} = 0V Low Resistor side		−60	−36	−25.7	μA
	I_{IH2H}	V_{DD} = 1.8V, V_{IN} = 0V High Resistor side		−6	−3.6	−2.57	
Input Current (3) (TEST)	I_{IL3}	V_{DD} = 1.8V, V_{IN} = 1.8V		6.43	9.0	15.0	μA
Output Current (1) (IO11~14, IO21~24)	I_{OH1}	V_{DD} = 1.2V, V_{OH} = 0.7V		—	—	−150	μA
	I_{OL1}	V_{DD} = 1.2V, V_{OL} = 0.5V		0.89	1.25	2.08	
Output Current (2) (BZ)	I_{OH2}	V_{DD} = 1.2V, V_{OH} = 0.7V		—	—	−500	μA
	I_{OL2}	V_{DD} = 1.2V, V_{OL} = 0.5V		500	—	—	
Output Current (3) (SEGMENT)	I_{OH3}	V_1 = 1.125V, V_2 = 2.25V, V_3 = 3.375V, V_4 = 4.5V	$V_{OH} = V_4 - 0.5V$	—	—	−100	μA
	I_{OL3}		V_{OL} = 0.5V	100	—	—	
	I_{OM3}		$V_{OM} = V_2 - 0.5V$	—	—	−50	
Output Current (4) (COMMON)	I_{OH4}	V_1 = 1.125V, V_2 = 2.25V, V_3 = 3.375V, V_4 = 4.5V	$V_{OH} = V_4 - 0.5V$	—	—	−100	μA
	I_{OL4}		V_{OL} = 0.5V	100	—	—	
	I_{OM4}		$V_{OM} = V_3 - 0.5V$	—	—	−50	
	I_{OM4}		$V_{OM} = V_1 + 0.5V$	50	—	—	
Quadrupler Output Voltage	V_1	V_1 = 1.125V, Ta = 25°C		1.075	1.125	1.175	V
	V_2			2.05	2.25	2.45	
	V_3			3.175	3.375	3.575	
	V_4			4.3	4.5	4.7	

Characteristic	Symbol	Test condition		Min	Typ.	Max	Unit
Power Supply Current (1) (Low-speed Crystel Oscillation Circuit)	I_{DDOP}	V_{DD} = 1.5V, f_H = 200kHz fL = 32kHz At High speed operation	Display ON	—	48	77	μA
			Display OFF	—	—	73	
	I_{DDSLOW}	V_{DD} = 1.5V, f_L = 32kHz At Low speed operation	Display ON	—	9.5	12	
			Display OFF	—	—	11	
	I_{DDHOLD}	V_{DD} = 1.5V, f_L = 32kHz In HOLD mode	Display ON	—	4	7	
			Display OFF	—	—	6	
	I_{DDSTOP}	V_{DD} = 1.5V In STOP mode		—	0.4	1	
Power Supply Current (2) (Low-speed CR Oscillation Circuit)	I_{DDOP}	V_{DD} = 1.5V, f = 200kHz f_L = Internal At High speed operation	Display ON	—	50	77	μA
			Display OFF	—	—	73	
	I_{DDSLOW}	V_{DD} = 1.5V, f_L = Internal At Low speed operation	Display ON	—	12	17	
			Display OFF	—	—	16	
	I_{DDHOLD}	V_{DD} = 1.5V, f_L = Internal In HOLD mode	Display ON	—	5	7.5	
			Display OFF	—	—	6.5	
	I_{DDSTOP}	V_{DD} = 1.5V In STOP mode		—	0.4	1	

(Note)The BRESET pin is connected to V_{DD} (High level) via two resistors as shown below. To minimize the current that flows at reset, the low resistance consists of a P-channel FET. When the input level is V_{SS} (Low level), the FET is off. The resistance is ∞. The specified input current (2), IIH2L, is the current that flows when the low resistance = P-channel FET is on. However, the low-resistance is off when V_{IN} = 0V, so actual measurement is impossible.



V_{DD} = High level

3. 3.0V version (Unless otherwise specified, V_{SS} = 0V, T_{opr} = 0~40°C)
(Recommended operating condition)

Characteristic		Symbol	Test condition	Min	Typ.	Max	Unit
Power Supply Voltage		V_{DD}	f_{XTH} = 2MHz	2.4	3.0	3.6	V
Oscillation Frequency		f_{XTL1}	V_{DD} = 2.4~3.6V (Note 1)	—	32.768	—	kHz
		f_{XTL2}	V_{DD} = 3.0V (Note 2)	20	35	60	
		f_{XTH1}	V_{DD} = 2.4~3.6V (Note 3)	—	2.0	—	MHz
		f_{XTH2}	V_{DD} = 3.0V (Note 4)	—	2.0	—	
Input Voltage	"H" Level	V_{IH}	V_{DD} = 2.4V	V_{DD} ×0.8	—	V_{DD}	V
			V_{DD} = 3.6V	V_{DD} ×0.7	—	V_{DD}	
	"L" Level	V_{IL}	V_{DD} = 2.4V	0	—	V_{DD} ×0.2	
			V_{DD} = 3.6V	0	—	V_{DD} ×0.3	
Quadrupler Capacitance		C_1, C_2		—	0.1	—	μF
Voltage Capacitance		V_2		—	0.1	—	μF
		V_3		—	0.1	—	
		V_4		—	0.1	—	
		V_{XT}		—	0.1	—	

(Note 1) Crystal oscillation circuit is used for low-speed oscillator.
(Note 2) Internal CR oscillator is used for low-speed oscillator.
(Note 3) Crystal oscillation circuit is used for high-Speed oscillator.
(Note 4) An RC oscillating circuit configured with an external R is used for the high-speed oscillator.

Oscillation

Characteristic	Symbol	Test condition	Min	Typ.	Max	Unit
OSC Starting Voltage (Low speed)	V_{STA1}	T_{STA} = 10s, T_{opr} = 25°C	1.85	—	—	V
OSC Starting Voltage (High speed)	V_{STA2}	T_{STA} = 8ms	2.10	—	—	V
OSC Holding Voltage (Low speed)	V_{HOLD1}		1.65	—	—	V
OSC Holding Voltage (High speed)	V_{HOLD2}		1.90	—	—	V
Frequency of Internal CR OSC	f_{OSC1}	V_{DD} = 3.0V (Note 1)	20	35	60	kHz
Frequency of High-Speed OSC	f_{OSC2}	V_{DD} = 3.0V R_f = 13.0kΩ (Note 2)	—	2.0	—	MHz

(Note 1) Internal CR oscillator for low-speed oscillator.
(Note 2) An RC oscillating circuit configured with an external R is used for the high-speed oscillator.

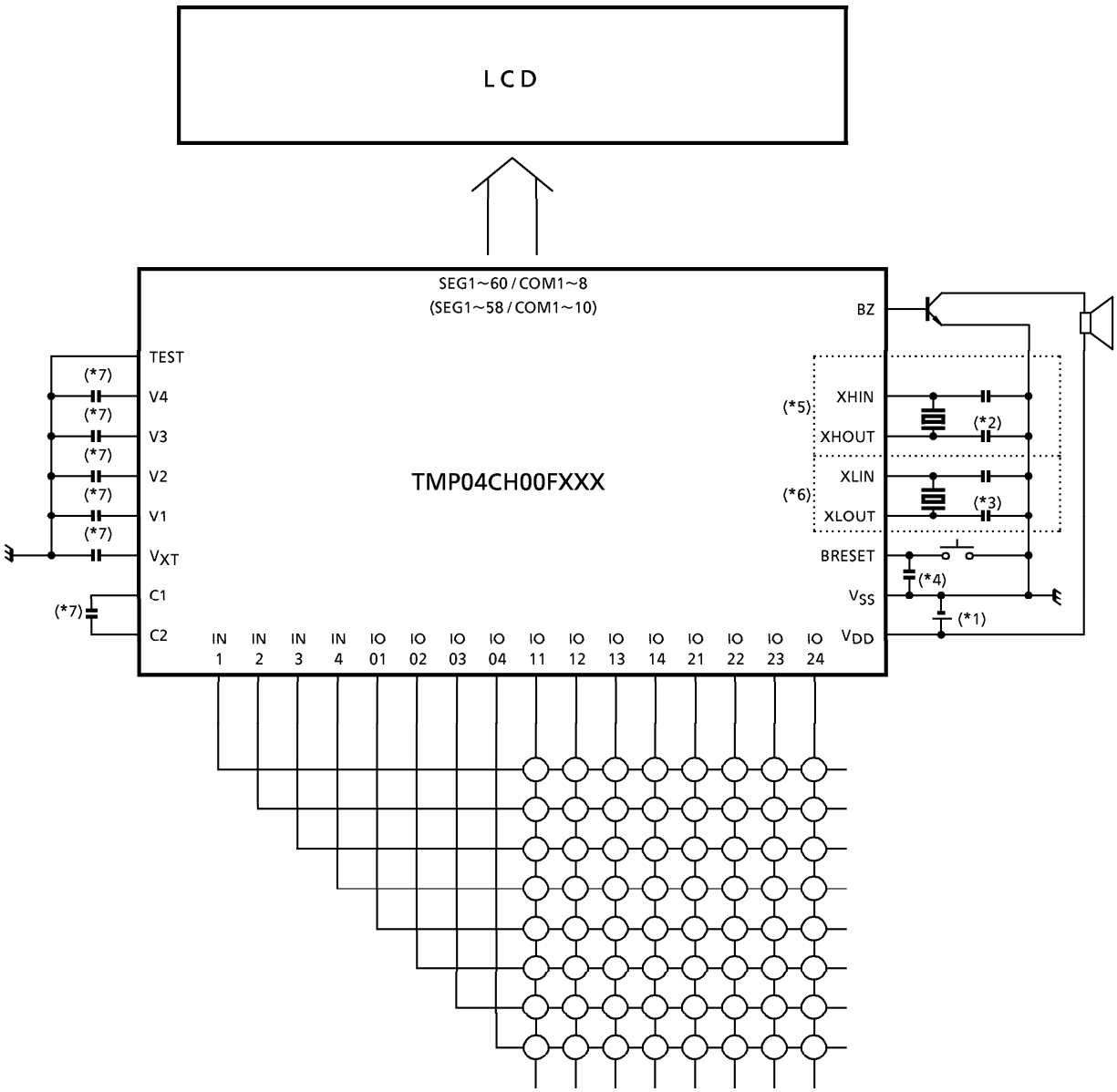
DC CHARACTERISTICS

Characteristic	Symbol	Test condition		Min	Typ.	Max	Unit
Input Current (1) (IN1~4, IO01~04, IO11~14, IO21~24)	I_{IH1}	V_{DD} = 3.6V, V_{IN} = 0V		– 500	—	500	nA
	I_{IL1}	V_{DD} = 3.6V, V_{IN} = 3.6V		6.43	9.0	15.0	μA
Input Current (2) (BRESET)	I_{IH2L}	V_{DD} = 3.6V, V_{IN} = 0V Low Register side		– 120	– 72	– 51.4	μA
	I_{IH2H}	V_{DD} = 3.6V, V_{IN} = 0V High Register side		– 12	– 7.2	– 5.14	
Input Current (3) (TEST)	I_{IL3}	V_{DD} = 3.6V, V_{IN} = 3.6V		12.9	18.0	30.0	μA
Output Current (1) (IO11~14, IO21~24)	I_{OH1}	V_{DD} = 2.4V, V_{OH} = 1.9V		—	—	– 1.5	mA
	I_{OL1}	V_{DD} = 2.4V, V_{OL} = 0.5V		0.89	1.25	2.08	μA
Output Current (2) (BZ)	I_{OH2}	V_{DD} = 2.4V, V_{OH} = 1.9V		—	—	– 2.0	mA
	I_{OL2}	V_{DD} = 2.4V, V_{OL} = 0.5V		2.0	—	—	
Output Current (3) (SEGMENT)	I_{OH3}	V_{DD} = 3.0V, V_{REG} = 1.125V, V_2 = 2.25V, V_3 = 3.375V, V_4 = 4.5V	V_{OH} = V_4 – 0.5V	—	—	– 100	μA
	I_{OL3}		V_{OL} = 0.5V	100	—	—	
	I_{OM3}		V_{OM} = V_2 – 0.5V	—	—	– 50	
Output Current (4) (COMMON)	I_{OH4}	V_{DD} = 3.0V, V_{REG} = 1.125V, V_2 = 2.25V, V_3 = 3.375V, V_4 = 4.5V	V_{OH} = V_4 – 0.5V	—	—	– 100	μA
	I_{OL4}		V_{OL} = 0.5V	100	—	—	
	I_{OM4}		V_{OM} = V_3 – 0.5V	—	—	– 50	
	I_{OM4}		V_{OM} = V_1 + 0.5V	50	—	—	
Voltage Regulater Output	V_{REG1}	V_{DD} = 3.0V	(Note 1)	1.075	1.125	1.175	V
	V_{REG2}		(Note 2)	—	1.8	—	
Quadrupler Output	V_2	V_{DD} = 3.0V, V_{REG} = 1.125V, Ta = 25°C		2.05	2.25	2.45	V
	V_3			3.175	3.375	3.575	
	V_4			4.3	4.5	4.7	

(Note 1) Voltage regulator for quadrupler
(Note 2) Voltage output regulator for low-speed oscillator

Characteristic	Symbol	Test condition		Min	Typ.	Max	Unit
Power Supply Current (1) (High-Speed Crystal Oscillation Circuit) (Low-speed Crystal Oscillation Circuit)	I_{DDOP}	V_{DD} = 3.0V, f_H = 2MHz f_L = 32kHz At High speed operation	Display ON	—	0.85	1.2	mA
			Display OFF	—	—	1.2	
	I_{DDSLOW}	V_{DD} = 3.0V, f_L = 32kHz At Low speed operation	Display ON	—	17.0	24.0	μA
			Display OFF	—	—	23.0	
	I_{DDHOLD}	V_{DD} = 3.0V, f_L = 32kHz In HOLD mode	Display ON	—	5.5	11.0	
			Display OFF	—	—	10.0	
	I_{DDSTOP}	V_{DD} = 3.0V In STOP mode		—	0.8	1.2	
Power Supply Current (2) (High-Speed CR Oscillation Circuit) (Low-Speed Crystal Oscillation Circuit)	I_{DDOP}	V_{DD} = 3.0V, f_H = 2MHz f_L = 32kHz At high-speed operation	Display ON	—	0.85	1.5	mA
			Display OFF	—	—	1.5	
	I_{DDSLOW}	V_{DD} = 3.0V, f_L = 32kHz At low-speed operation	Display ON	—	17.0	24.0	μA
			Display OFF	—	—	23.0	
	I_{DDHOLD}	V_{DD} = 3.0V, f_L = 32kHz In HOLD mode	Display ON	—	5.5	11.0	
			Display OFF	—	—	10.0	
	I_{DDSTOP}	V_{DD} = 3.0V In STOP mode		—	0.8	1.2	
Power Supply Current (3) (High-Speed CR Oscillation Circuit) (Low-Speed CR Oscillation Circuit)	I_{DDOP}	V_{DD} = 3.0V, f_H = 2MHz f_L = Internal At high-speed operation	Display ON	—	0.85	1.5	mA
			Display OFF	—	—	1.5	
	I_{DDSLOW}	V_{DD} = 3.0V, f_L = Internal At low-speed operation	Display ON	—	23.0	40.0	μA
			Display OFF	—	—	39.0	
	I_{DDHOLD}	V_{DD} = 3.0V, f_L = Internal In HOLD mode	Display ON	—	6.5	14.0	
			Display OFF	—	—	12.0	
	I_{DDSTOP}	V_{DD} = 3.0V In STOP mode		—	0.8	1.4	

◆EXAMPLE OF APPLICATION CIRCUIT



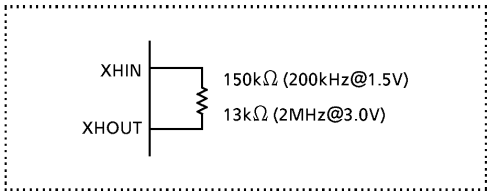
(*1) Either 1.5V or 3V can be selected as the supply voltage.

(*2) Recommended high-speed oscillator circuit capacitor: 22pF

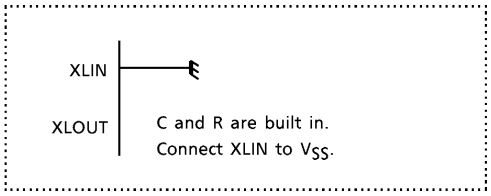
(*3) Recommended low-speed oscillator circuit capacitor : 15pF

(*4) Insert a 0.1μF capacitor between BRESET and V_{SS}.

(*5) High-speed CR oscillator circuit (optional)



(*6) Low-speed CR oscillator circuit (optional)

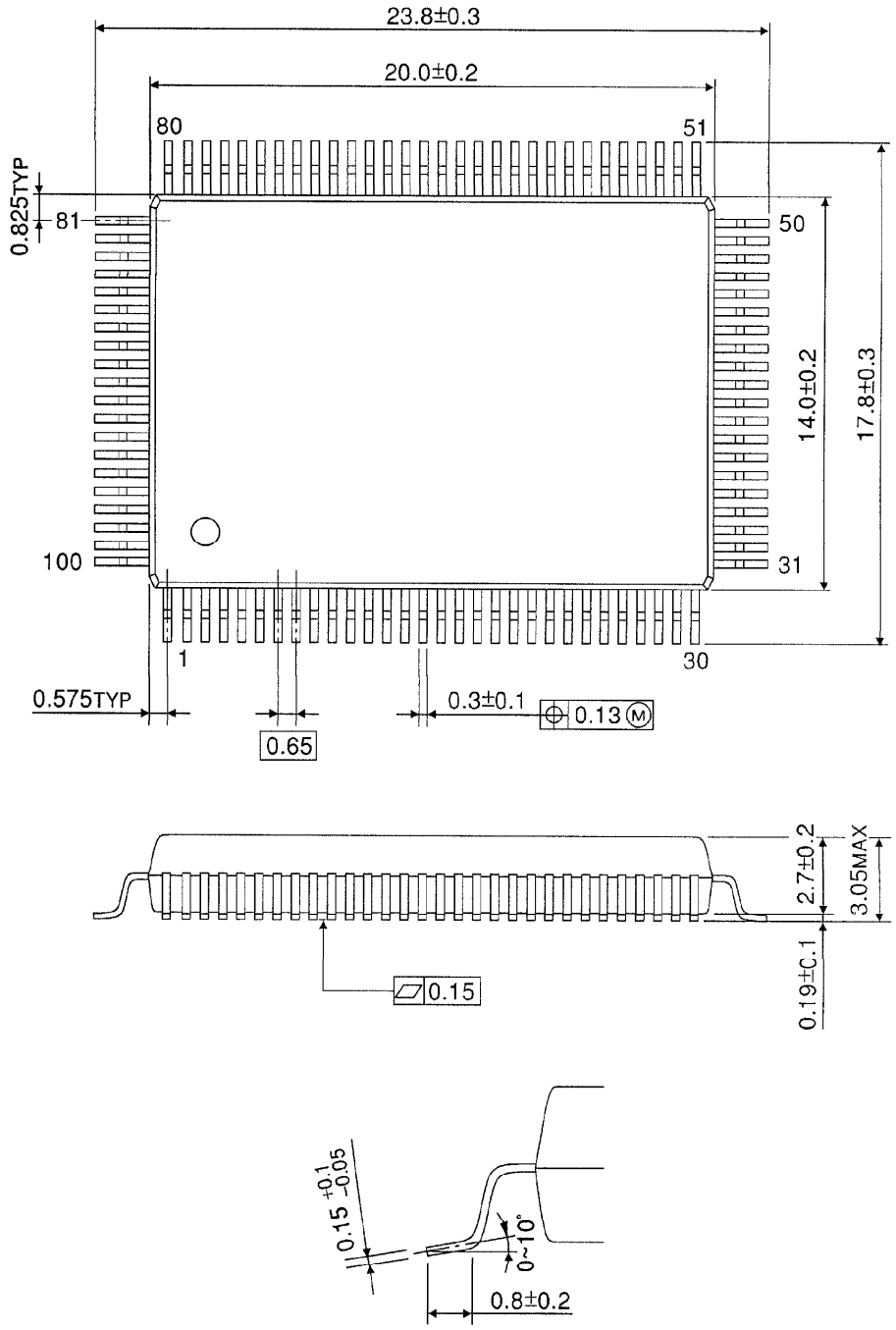


(*7) Adjust between 0.1 to 1.0μF depending on the size of the LCD panel used.

◆PACKAGE DIMENSIONS

(1) P-QFP100-1420-0.65A

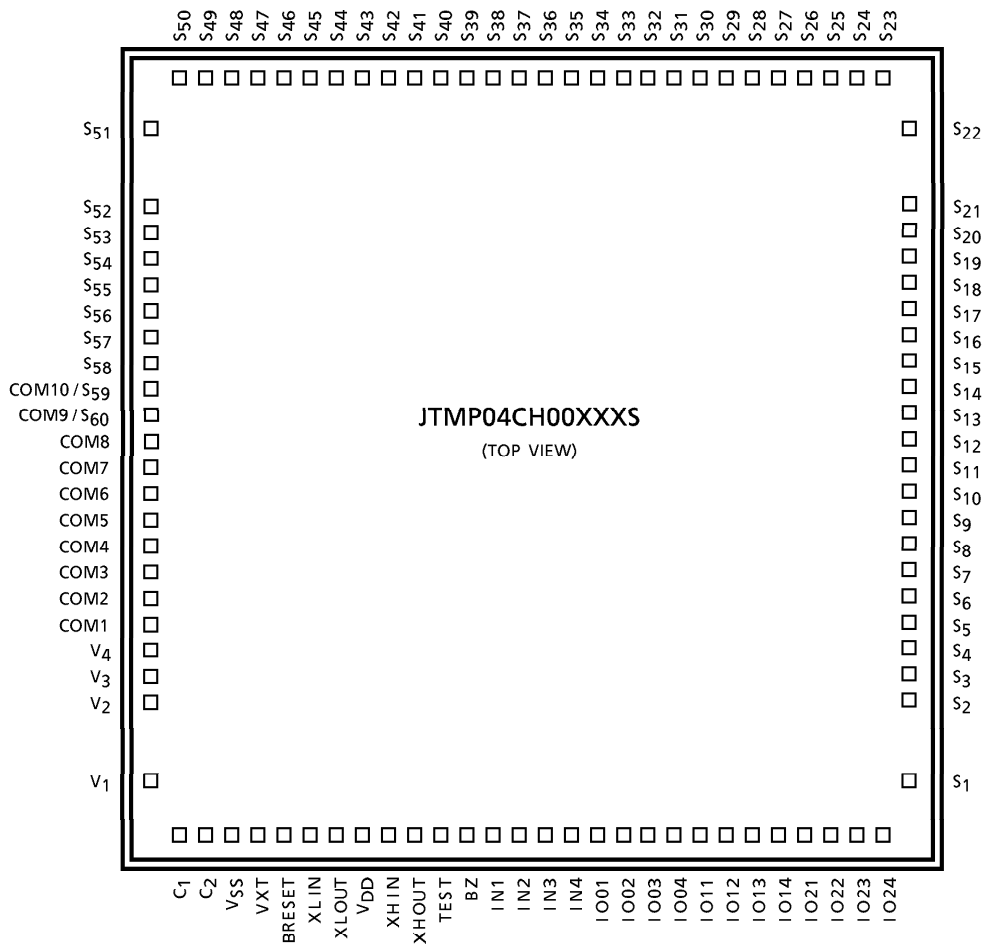
Unit : mm



Weight : 1.65g (Typ.)

(2) Bare chip

1. Pad assignment



Chip size	5.87 × 5.39 (mm)
Chip thickness	450 ± 30 (μm)

Substrate voltage V_{SS}

2. Pad location table

($\times 10^{-3}$mm)

No.	PAD NAME	X POINT	Y POINT
1	V_1	– 2695	– 2031
100	V_2	– 2695	– 1694
99	V_3	– 2695	– 1514
98	V_4	– 2695	– 1330
97	COM1	– 2695	– 1148
96	COM2	– 2695	– 968
95	COM3	– 2695	– 788
94	COM4	– 2695	– 608
93	COM5	– 2695	– 428
92	COM6	– 2695	– 248
91	COM7	– 2695	– 68
90	COM8	– 2695	112
89	S_{60} / COM9	– 2695	292
88	S_{59} / COM10	– 2695	472
87	S_{58}	– 2695	652
86	S_{57}	– 2695	832
85	S_{56}	– 2695	1012
84	S_{55}	– 2695	1192
83	S_{54}	– 2695	1372
82	S_{53}	– 2695	1552
81	S_{52}	– 2695	1732
80	S_{51}	– 2695	2150
79	S_{50}	– 2428	2427
78	S_{49}	– 2248	2427
77	S_{48}	– 2068	2427
76	S_{47}	– 1888	2427
75	S_{46}	– 1708	2427
74	S_{45}	– 1528	2427
73	S_{44}	– 1348	2427
72	S_{43}	– 1168	2427
71	S_{42}	– 988	2427
70	S_{41}	– 808	2427
69	S_{40}	– 628	2427
68	S_{39}	– 448	2427
67	S_{38}	– 268	2427
66	S_{37}	– 88	2427

No.	PAD NAME	X POINT	Y POINT
65	S_{36}	92	2427
64	S_{35}	272	2427
63	S_{34}	452	2427
62	S_{33}	632	2427
61	S_{32}	812	2427
60	S_{31}	992	2427
59	S_{30}	1172	2427
58	S_{30}	1352	2427
57	S_{28}	1532	2427
56	S_{27}	1712	2427
55	S_{26}	1892	2427
54	S_{25}	2072	2427
53	S_{24}	2252	2427
52	S_{23}	2432	2427
51	S_{22}	2695	2150
50	S_{21}	2695	1733
49	S_{20}	2695	1553
48	S_{19}	2695	1373
47	S_{18}	2695	1193
46	S_{17}	2695	1013
45	S_{16}	2695	833
44	S_{15}	2695	653
43	S_{14}	2695	473
42	S_{13}	2695	293
41	S_{12}	2695	113
40	S_{11}	2695	– 67
39	S_{10}	2695	– 252
38	S_9	2695	– 432
37	S_8	2695	– 612
36	S_7	2695	– 792
35	S_6	2695	– 972
34	S_5	2695	– 1152
33	S_4	2695	– 1332
32	S_3	2695	– 1512
31	S_2	2695	– 1692
30	S_1	2695	– 2031

No.	PAD NAME	X POINT	Y POINT
29	IO24	2444	– 2427
28	IO23	2264	– 2427
27	IO22	2084	– 2427
26	IO21	1904	– 2427
25	IO14	1724	– 2427
24	IO13	1544	– 2427
23	IO12	1364	– 2427
22	IO11	1184	– 2427
21	IO04	1004	– 2427
20	IO03	824	– 2427
19	IO02	644	– 2427
18	IO01	464	– 2427
17	IN4	272	– 2427
16	IN3	92	– 2427
15	IN2	– 88	– 2427
14	IN1	– 268	– 2427
13	BZ	– 452	– 2427
12	TEST	– 633	– 2427
11	XHOUT	– 813	– 2427
10	XHIN	– 933	– 2427
9	V_{DD}	– 1202	– 2427
8	XLOUT	– 1408	– 2427
7	XLIN	– 1588	– 2427
6	BRESET	– 1768	– 2427
5	VXT	– 1948	– 2427
4	V_{SS}	– 2116	– 2427
3	C_2	– 2281	– 2427
2	C_1	– 2461	– 2427