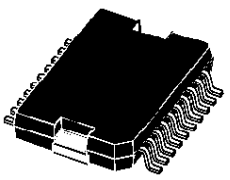
SGS-THOMSON MICROELECTRONICS

L9346

QUAD INTELLIGENT POWER LOW SIDE SWITCH

- QUAD POWER LOW SIDE DRIVER WITH 2 x 5A AND 2 x 3A OUTPUT CURRENT CAPABILITY
- LOW R_{DSON} TYPICALLY 200mΩ AND 300mΩ @ Tj = 25°C
- INTERNAL OUTPUT CLAMPING STRUCTURES WITH V_{FB} = 50V FOR FAST INDUCTIVE LOAD CURRENT RECIRCULATION
- LIMITED OUTPUT VOLTAGE SLEW RATE FOR LOW EMI
- PROTECTED µP COMPATIBLE ENABLE AND INPUT
- WIDE OPERATING SUPPLY VOLTAGE RANGE 4.5V TO 32V
- REAL TIME DIAGNOSTIC FUNCTIONS
  - OUTPUT SHORTED TO GND
  - OUTPUT SHORTED TO VSS
  - OPEN LOAD MEASURED IN ON AND OFF CONDITION
  - LOAD BYPASS DETECTION
  - OVERTEMPERATURE
- DEVICE PROTECTION FUNCTIONS
  - OVERLOAD DISABLE
  - REVERSE SUPPLY VOLTAGE PROTECTED VS UP TO -2V
  - SELECTIVE THERMAL SHUTDOWN



Power SO20

Chip delivery on request

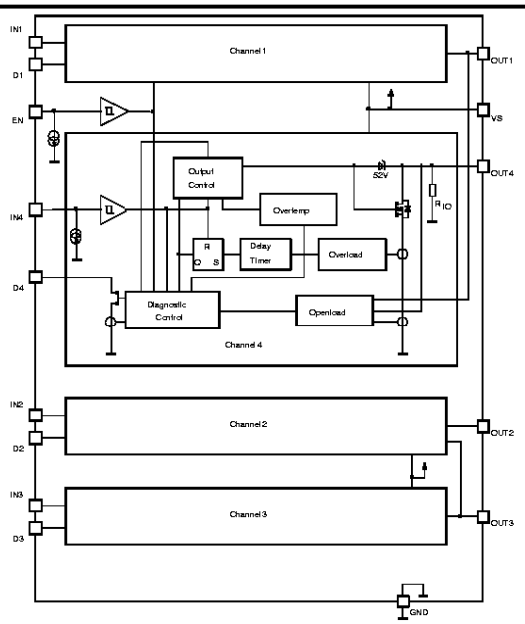
ORDERING NUMBERS: L9346 (power SO20)
L9346DIE (chip)

DESCRIPTION

The L9346 is a monolithic integrated quad low side driver realized in an advanced MultipowerBCD mixed technology. The device is intended to drive valves in automotive environment.

The inputs are µP compatible. Particular care has been taken to protect the device against failutes, to avoid electromagnetic interferences and to offer extensive real time diagnostic.

BLOCK DIAGRAM

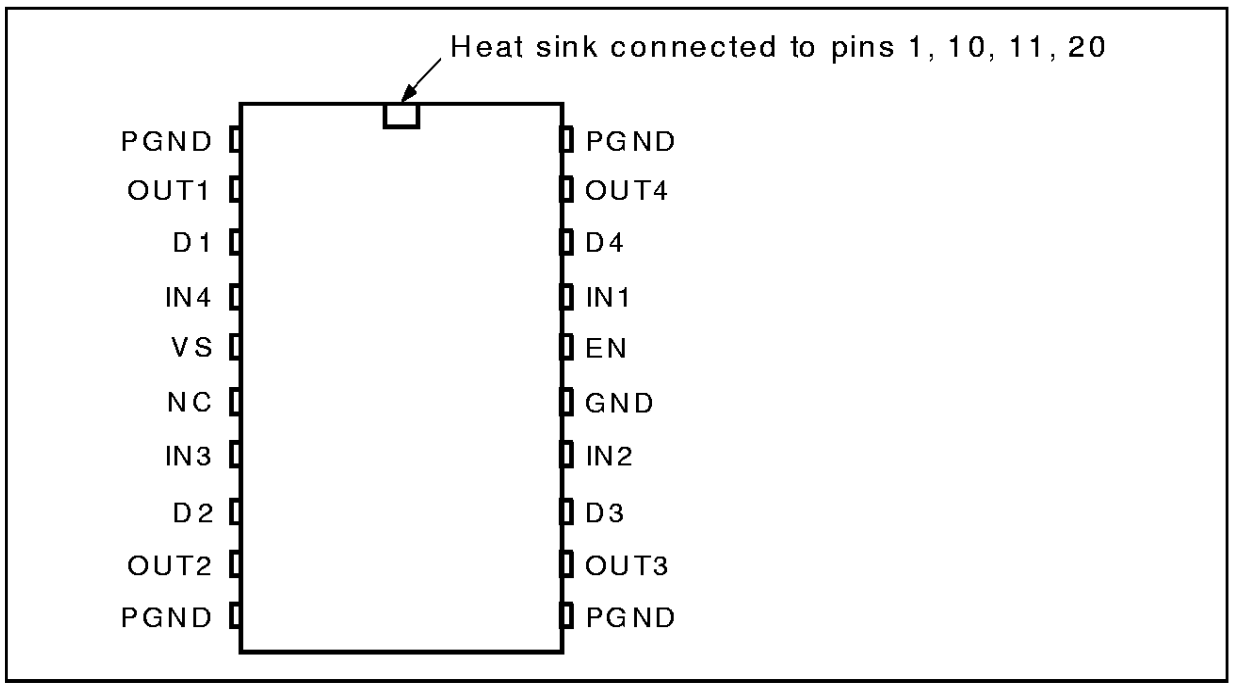


ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Value	Unit
V_S	DC Supply Voltage		-2 to 32	V
V_{SP}	Supply Voltage Pulse (duration <200ms)		-2 to 45	V
$\left\|\frac{dV_S}{dt}\right\|$	Supply Voltage Slope		10	V/µs
$V_{IN, EN}$	Input Voltage	| I | 10mA	-2 to 16	V
V_D	Diagnostic DC Output Voltage	| I | 50mA	-0.3 to 16	V
V_{ODC}	DC Output Voltage		-0.3 to 45	V
$I_{O1, 2}$	DC Output Current Out 1, 2		5	A
$I_{O3, 4}$	DC Output Current Out 3, 4		3	A
$I_{OR1, 2}$	Reverse Output Current		-5	A
$I_{OR3, 4}$	Reverse Output Current		-3	A
$E_{O1, 2}$	Switch-off Energy for Inductive Loads	t_{EO} = 250µs, [1]	50	mJ
$E_{O3, 4}$		T = 5ms	30	mJ
ΔV_{GND}	GND Potential Difference	T_j = -40 to 150°C	±0.3	V
T_{jEO}	Juntion Temperature During Switch-off	$\sum t \leq 30$ min	175	°C
		$\sum t \leq 15$ min	190	°C
T_j	Juntion Temperature		-40 to T_{jDIS}	°C
T_{stg}	Storage Temperature		-55 to 150	°C
T_{jDIS}	Thermal Disable Junction Temp. Threshold		180 to 210	°C

The device is ESD protected, tested according to MIL883C with ±2KV.
Note [1] : t_{EO} is the clamping time (see fig.1)

PIN CONNECTION



THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}c}$	Thermal Resistance junction to case	3	K/W

PIN FUNCTIONS

N.	Name	Function
1	GND	Power Grounded
2	Out 1	Output 1 (5A)
3	D1	Diagnostic 1
4	IN 4	Input 4
5	VS	Supply Voltage
6	NC	Not Connected
7	IN 3	Input 3
8	D2	Diagnostic 2
9	Out 2	Output 2 (5A)
10	GND	Power Ground
11	GND	Power Ground
12	Out 3	Output 3 (3A)
13	D3	Diagnostic 3
14	IN 2	Input 2
15	GND	Signal Ground
16	EN	Common Enable
17	IN 1	Input 1
18	D4	Diagnostic 4
19	Out 4	Output 4 (3A)
20	GND	Power Ground

Figure 1: t_{EO} Clamping Time

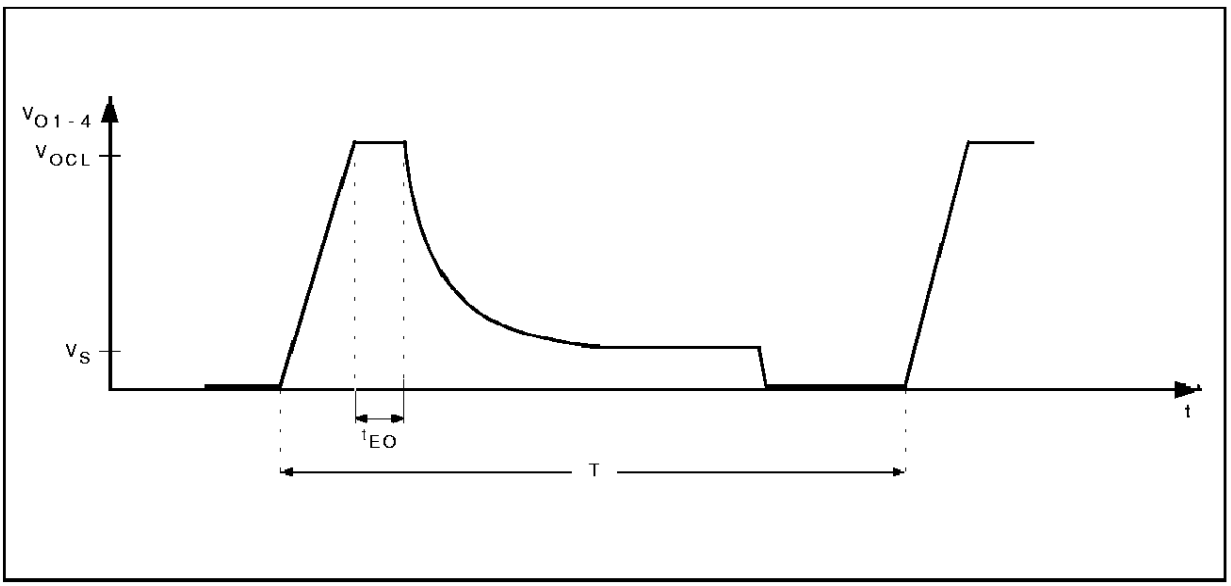
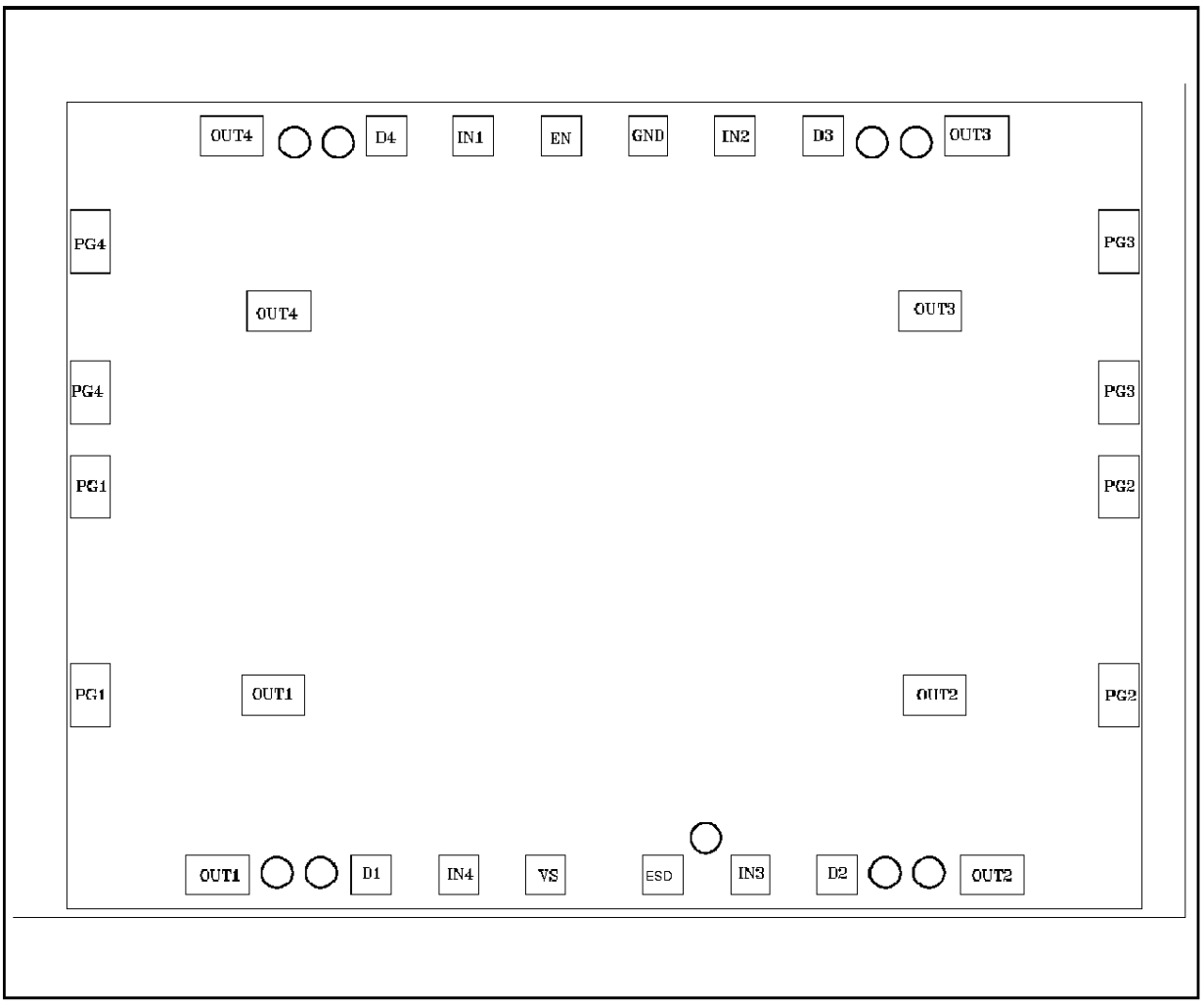


Figure 2: Pat Position (Chipsize 4.95 x 3.88)



Pad Coordinates (Reference point X = 0, Y = 0: Center of die)

Pat opening center position					
Pad Nr.	**Pad Name**	**Size in (µm)**	**Description**	**Coordinates in (µm)**	
				X	**Y**
1	PG3	178 x 280	Power Ground 3	2286.5	1175
2	PG3	178 x 280	Power Ground 3	2286.5	506
3	PG2	178 x 280	Power Ground 2	2286.5	98
4	PG2	178 x 280	Power Ground 2	2286.5	-842
5	OUT2	280 x 178	Output 2 5A	1472.5	-844
6	OUT2	280 x 178	Output 2 5A	1722.5	-1644
7	D2	178 x 178	Diagnostic 2	1036	-1644
8	IN3	178 x 178	Input 3	648	-1644
9	VS	178 x 178	Supply Voltage	-260	-1644
10	IN4	178 x 178	Input 4	-648	-1644
11	D1	178 x 178	Diagnostic 1	-1036	-1644
12	OUT1	280 x 178	Output 1 5A	-1722.5	-1644
13	OUT1	280 x 178	Output 1 5A	-1472.5	-844
14	PG1	178 x 178	Power Ground 1	-2286	-842
15	PG1	178 x 178	Power Ground 1	-2286	98
16	PG4	178 x 178	Power Ground 4	-2286	506
17	PG4	178 x 178	Power Ground 4	-2286	1175
18	OUT4	280 x 178	Output 4 3A	-1448	865
19	OUT4	280 x 178	Output 4 3A	-1656	1644
20	D4	178 x 178	Diagnostic 4	-970	1644
21	IN1	178 x 178	Input 1	-582	1644
22	EN	178 x 178	Common Enable	-194	1644
23	GND	178 x 178	Signal Ground	194	1644
24	IN2	178 x 178	Input 2	582	1644
25	D3	178 x 178	Diagnostic 3	970	1644
26	OUT3	280 x 178	Output 3 3A	1656.5	1644
27	OUT3	280 x 178	Output 3 3A	1448.5	865
	Test pad	**Size**		**X**	**Y**
	Gate 2	d = 102		1447	-1612
	VTERM2	d = 102		1260	-1600
	IOLRED	d = 102		449.5	-1455.5
	ESD	178 x 178		260	-1644
	VTERM1	d = 102		-1260	-1600
	GATE1	d = 102		-1447	-1612
	GATE4	d = 102		-1381	1600
	VTERM4	d = 102		-1194.5	1600
	VTERM3	d = 102		1194.5	1600
	GATE3	d = 102		1381	1600

ELECTRICAL CHARACTERISTICS (Operating Range)

The electrical characteristics are valid within the below defined operating range, unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Board Supply Voltage		4.5	12	32	V
T_{j1}	Junction Temperature		-40		150	°C
T_{j2}	Junction Temperature	$\Sigma t \leq 15min$ [2] over life time	150		T_{jDIS}	°C

NOTE:

2) Parameters guaranteed by correlation

ELECTRICAL CHARACTERISTICS (V_S = 4.5 to 32V; -40°C ≤ T_{j1} ≤ 150°C < T_{j2} ≤ T_{jDIS}, unless otherwise specified.)

Symbol	Parameter	Test Condition	Value T_{j1}			Value T_{j2}		Unit
			Min.	Typ.	Max.	Min.	Max.	
Supply								
$I_{VS\ OFF}$	DC Supply Current Off	EN = 1.0V		5	10			mA
$I_{VS\ ON}$	DC Supply Current On	$V_S \leq 14V$; V_{IN}, V_{EN} = 2V		8				mA
Diagnostic Outputs D 1 - D 4								
V_{DL}	Diagnostic Output Low Voltage	$I_D \leq 3mA$		0.65	1.0		1.5	V
I_{DLE}	Diagnostic Output Leakage Current	V_D = 14V [3]		0.1	2		20	µA
Outputs Out 1 - Out 4								
$V_{OUV\ 1-4}$	Open Load Voltage Threshold	V_{IN} = 1V	0.525 x VS	0.55 x V_S	0.575 x VS	0.5 x Vs	0.65 x VS	V
$V_{OUV\ hys\ 1-4}$	Hysteresis			0.003 x V_S				V
$\Delta V_{OUV\ 1-4,\ 2-3,\ 4-1,\ 3-2}$	Open Load Difference Voltage Threshold	$V_{IN1,4/2,3}$ = 1V; VO_C = 16 to 4.5V VO_C = output voltage of other channel	VO_C - 1.0V	VO_C - 1.25V	VO_C - 1.5V	VO_C - 0.8V	VO_C - 1.7V	V
$V_{OUV\ hys\ 1-4,\ 2-3,\ 4-1,\ 3-2}$	Open Load Hysteresis			40				mV
$I_{OUC\ 1,\ 2,\ 3,\ 4}$	Open Load Current Threshold	V_{EN} = V_{IN} = 2V; V_S = 6.5 to 16V	160	320	480		580	mA
$I_{OOC\ 1,\ 2}$	Over Load Current Threshold	V_S > 6.5V; V_{OUT} = 32V	5	10		4		A
$I_{OOC\ 3,\ 4}$			3	6		2.4		A
V_{OCL}	Output Voltage During Clamping	$I_{OCL} \geq 200mA$	45	52	60			V
$S_{ON,OFF}$	Output (fall, rise) slew rate	[4] $I_{OUC} \leq I_O \leq I_{OOC}$	400	1500	2850	200	3500	V/mA
R_{IO}	Internal Output Pull Down Resistor	V_{EN} = 1V	10	20	40		50	KΩ
$R_{DSON\ 1,\ 2}$	Output On Resistance	T_j = 25°C T_j = 150°C V_S > 9.5V, $I_{O1,2}$ = 2A		200 300	300 500			mΩ
$R_{DSON\ 3,\ 4}$		T_j = 25°C T_j = 150°C; $I_{O3,4}$ = 1.3A		300	450 750			mΩ

NOTE:

[2] Parameters guaranteed by correlation
[3] The diagnostic output is short circuit protected up to V_D = 16V
[4] V_S = 9 to 16V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Value T_{j1}			Value T_{j2}		Unit
			Min.	Typ.	Max.	Min.	Max.	
Inputs IN1-4, EN								
$V_{IN,EN\,L}$	Logic Input/Enable Low Voltage		-0.3		1		0.8	V
$V_{IN,EN\,H}$	Logic Input/Enable High Voltage	IN, EN	2.0		16			V
$V_{EN,IN\,hys}$	Logic Input Hysteresis		0.2	0.4	0.8			V
I_{IN}	Input Sink Current	V_{IN} = 2 to 12V[5]	10	30	60		240	µA
I_{EN}	Enable Sink Current		10	20	40		240	µA
Timing								
$t_{D\,ON}$	Output Delay ON Time	[6] Fig. 7		4	25			µs
$t_{D\,OFF}$	Output Delay OFF Time	[6] Fig. 7	5	15	30			µs
$t_{DH-L,\,Diag}$	Diag. Delay Output OFF Time	[6] Fig. 6	8		65		90	µs
$t_{D\,IOU}$	Diagnostic Open Load Delay Time	V_S = 9 to 16V, Fig 8 $I_O \le I_{OUC}$		8	50			µs
t_{DOL}	Diagnostic Overload Delay Switch-OFF Time	V_S = 9 to 16V, Fig 8 $I_O > I_{OOC}$	50	160	300			µs
$t_{D\,ENON}$	Enable ON Time	[6] Fig. 7		4	25			µs
$t_{D\,ENOFF}$	Enable OFF Time	[6] Fig. 7		4	25			µs

NOTE:

[5] Open pins (EN, IN) are detected as low
[6] V_S = 9 to 16V $\wedge$ $I_{OUC} \le I_O \le I_{OOC}$

DIAGNOSTIC TABLE

CONDITIONS		EN	IN	OUT	DIAG.
Normal Function		L	X	off	L
		H	L	off	L
		H	H	on[7]	H
GND short	$V_{Otyp} < 0.55V_S$	L	X	off	H
Load bypass	$\Delta V_{O1-4/2-3} \ge 1.25V$	H	L	off	H
Open Load	$I_{O1,2,3,4typ} < 320mA$	H	H	on[7]	L
$T_{jtyp} \ge 190°C$ Overtemperature[8]		X	X	off	L
Over Load	$I_{Omin\,1,3} > 5A$ $I_{Omin\,2,4} > 3A$	H	H	off	L
Reset and Overtemperature Latch		X		DC don't care	DC don't care

NOTE:

[7] For V_S = 4.5 to 6.5V, $I_O \le 2A$, the diag. table is valid
[8] If one diag. status shows the overtemperature, recognition, in parallel this output will be switched OFF internally.
The corresponding channel should be switched OFF additionally by its input signal, otherwise the overload latch will be set after t_{DOL} is passed.
This behaviour is related to the overdrop sensing which is used as over load recognition.
The overtemperature is latched (DIAG = L) until the level of the IN signal changes to low.

CIRCUIT DESCRIPTION

The L9346 is a quad low side driver for inductive loads like valves in automotive environment. The internal pull down current sources at the ENABLE and INPUT pins assure in case of open input conditions that the device is switched off. An output voltage slope limitation for du/dt is implemented to reduce the EMI. An integrated active flyback voltage limitation clamps the output voltage during the flyback phase to 50 V.

Each driver is protected against short circuit at V_{OUT} < 32V and thermal overload. In short circuit condition the output will be disabled after a short delay time t_{DOL}. The thermal disable for TJ > 180°C of the output will be reseted if the junction temperature decreases about 20°C below the disable threshold temperature.
The overtemperature information is stored until IN = L.

For the real time error diagnosis the voltage and the current of the outputs are compared with internal fixed values V_{OUV} for OFF and I_{OUC} for ON conditions to recognize open load ($R_L \geq 20$ KΩ, $R_L > 38\Omega$) in OFF and ON conditions.

Also the output voltages V_{O1} - 4 are compared to each other output in OFF condition with a fixed offset of ΔV_{OUV} to recognize load bypasses. To suppress the ΔV_{OUV} diagnoses during the flyback phases of the compared output, the ΔVOUV diagnostic includes a latch function.

Reaching the flyback clamping voltage V_{OCL} the diagnostic signal is reseted by a latch. To activate again this kind of diagnostic a low signal at the correspondent INPUT or the ENABLE pin must be applied (see also Fig.3). The outputs 1 and 4 are compared for ΔV_{OUV} and also outputs 2 and 3 are compared.

The diagnostic output level in connection with different ENABLE and INPUT conditions allows to recognize different fail states, like overtemp, short to V_{SS}, short to GND, bypass to GND and disconnected load (see diagnostic table).

The diagnostic output is protected against short circuit. Exceeding the over load current threshold I_{OOC}, the output current will be limited internally during the diagnostic overload delay switch-off time t_{DOL}.

The device complies the ISO pulses imposed to the supply voltage of the valves without any failures of the functionality.

Figure 3. Diagnostic Overload Delay Time

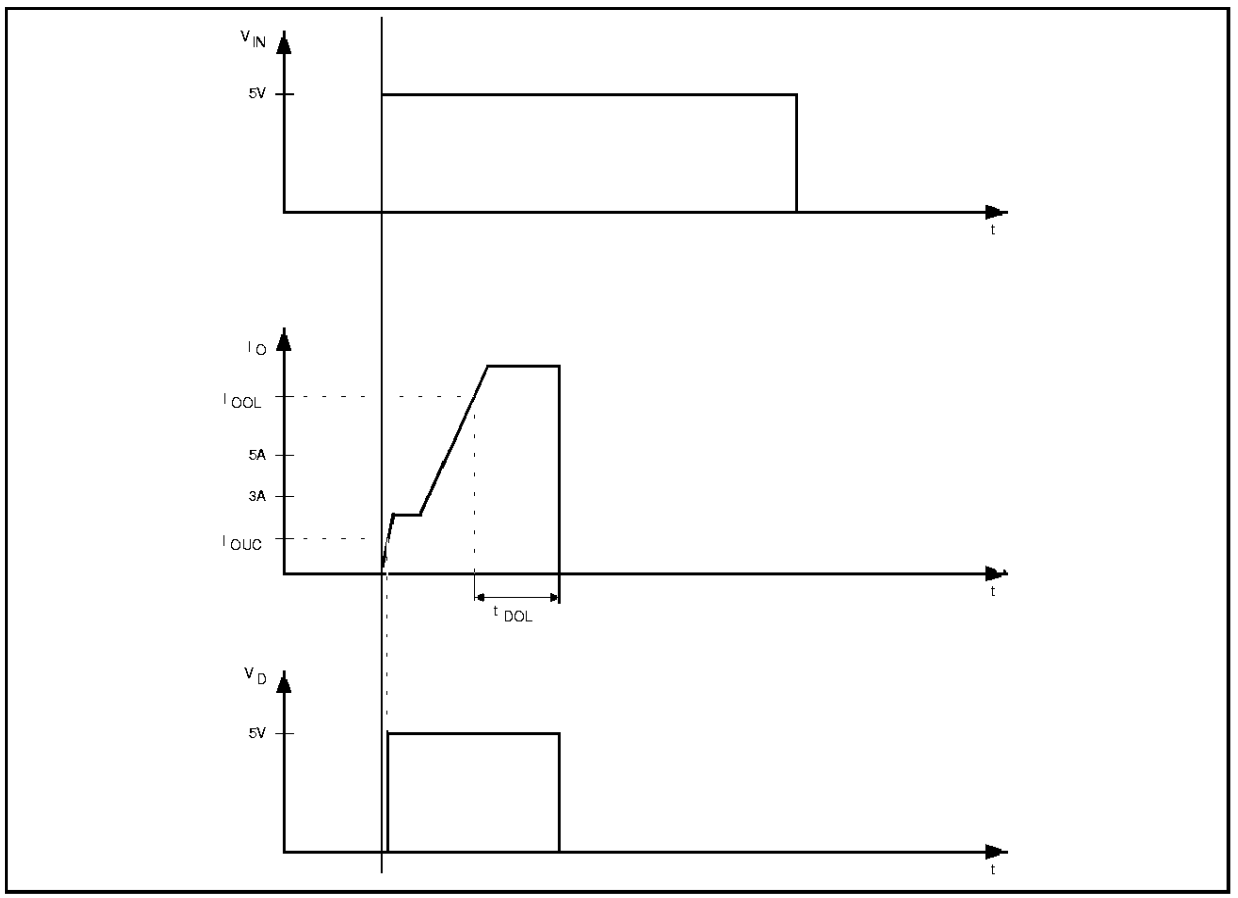


Figure 4. OUTPUT SLOPE (Resistive load for testing)

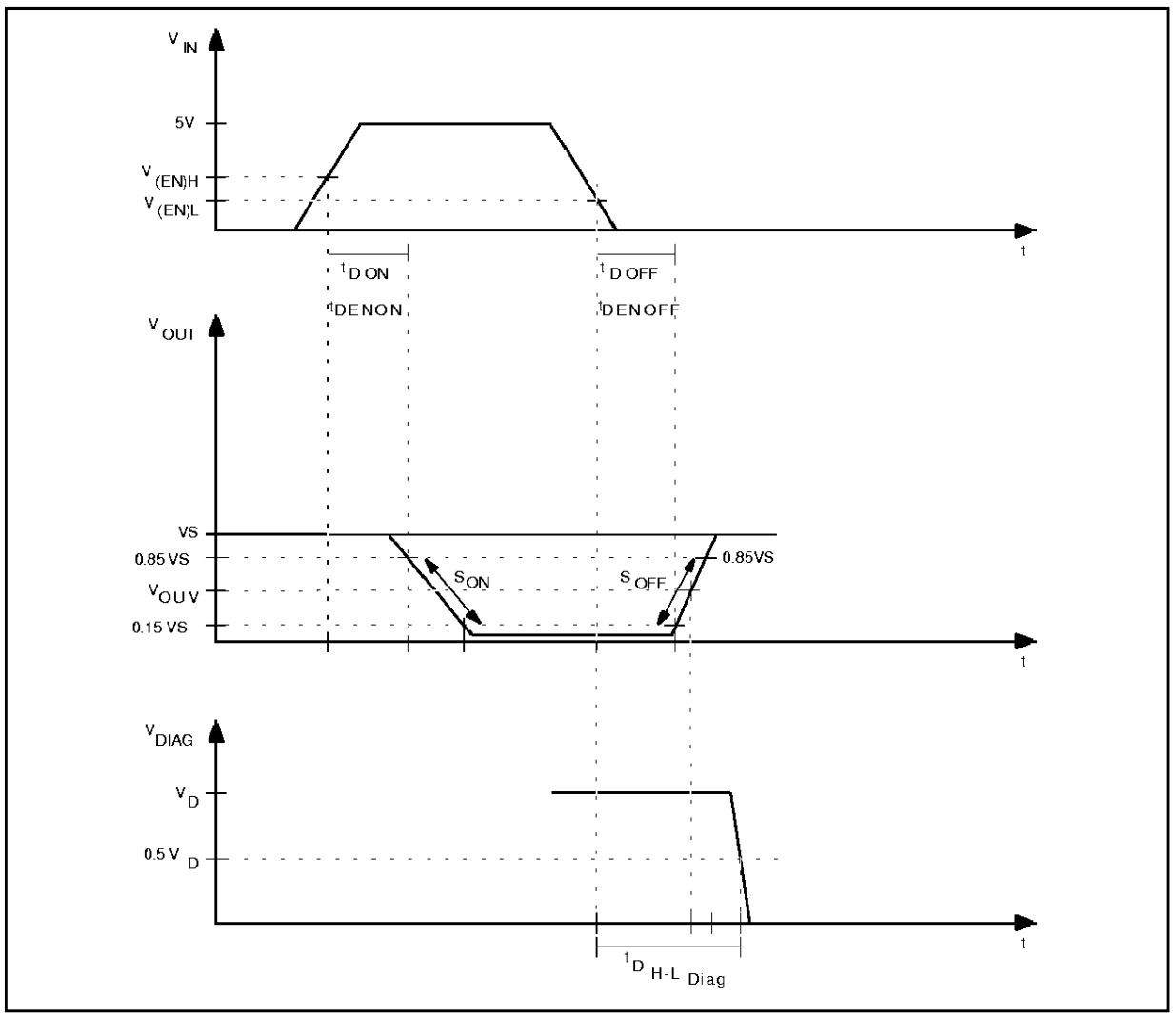


Figure 5. TIMING (t_{DENON}, t_{DON}, t_{DENOFF}, t_{DOFF})

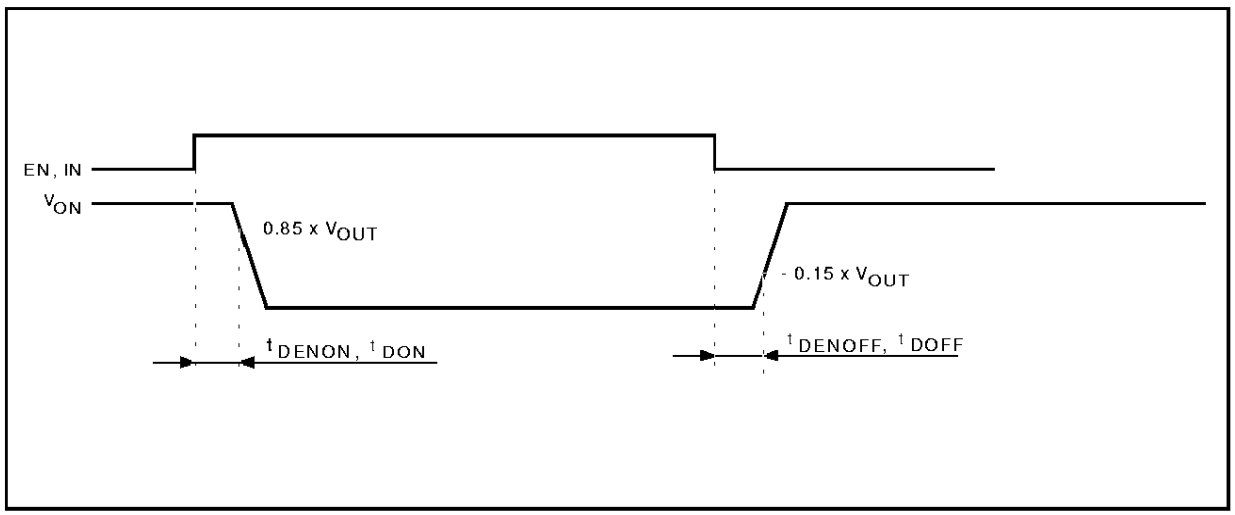


Figure 6. TIMING (t_{DOL}, t_{DIOU})

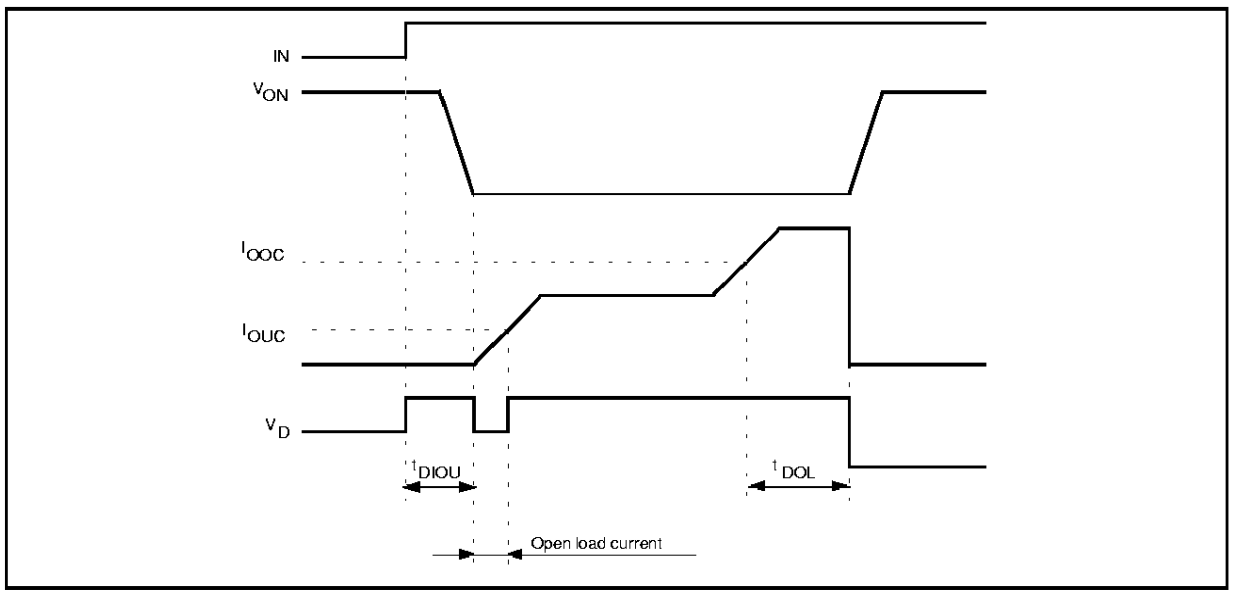


Figure 7. BLOCK DIAGRAM - Open Load Voltage Detection

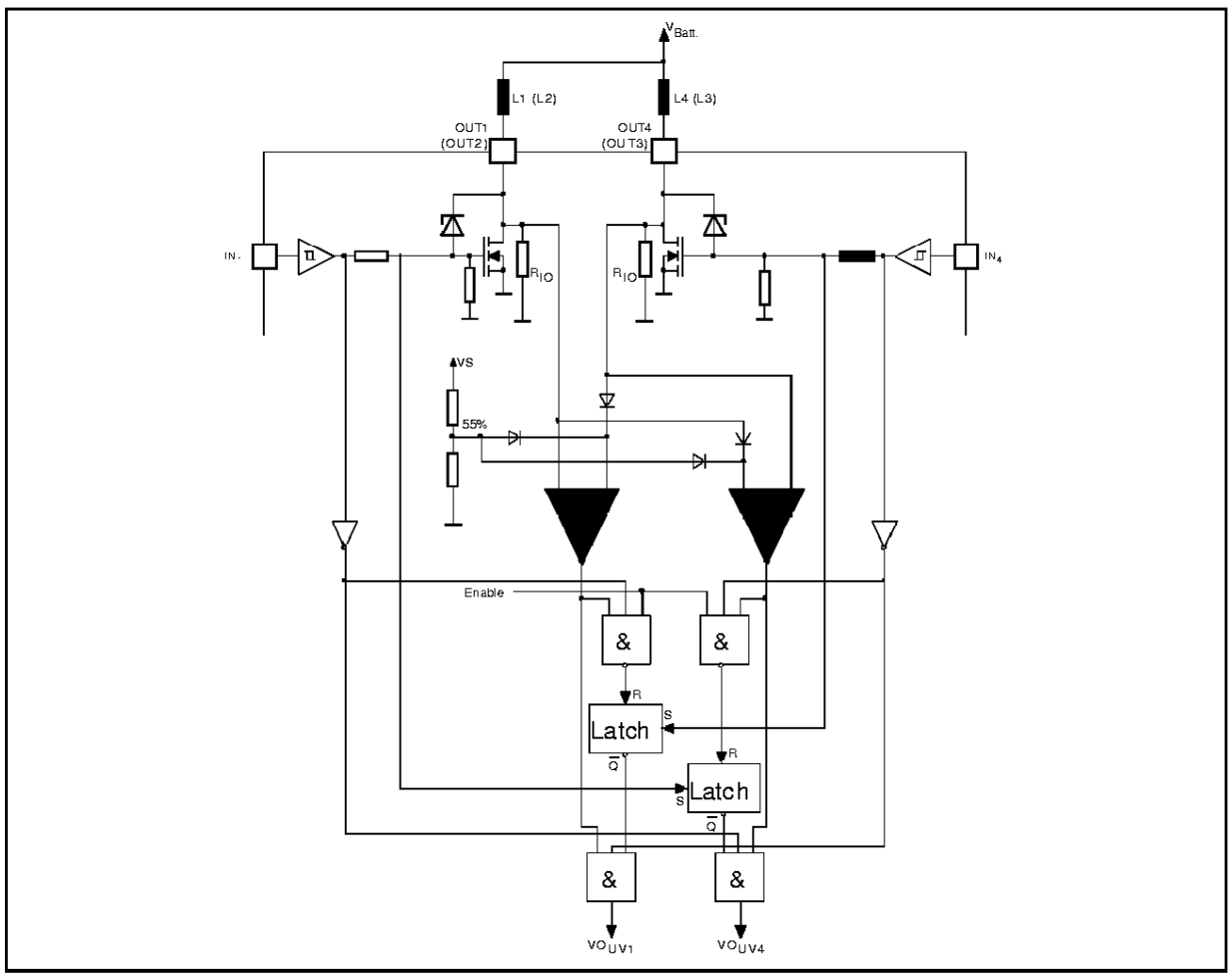


Figure 8. Logic Diagram

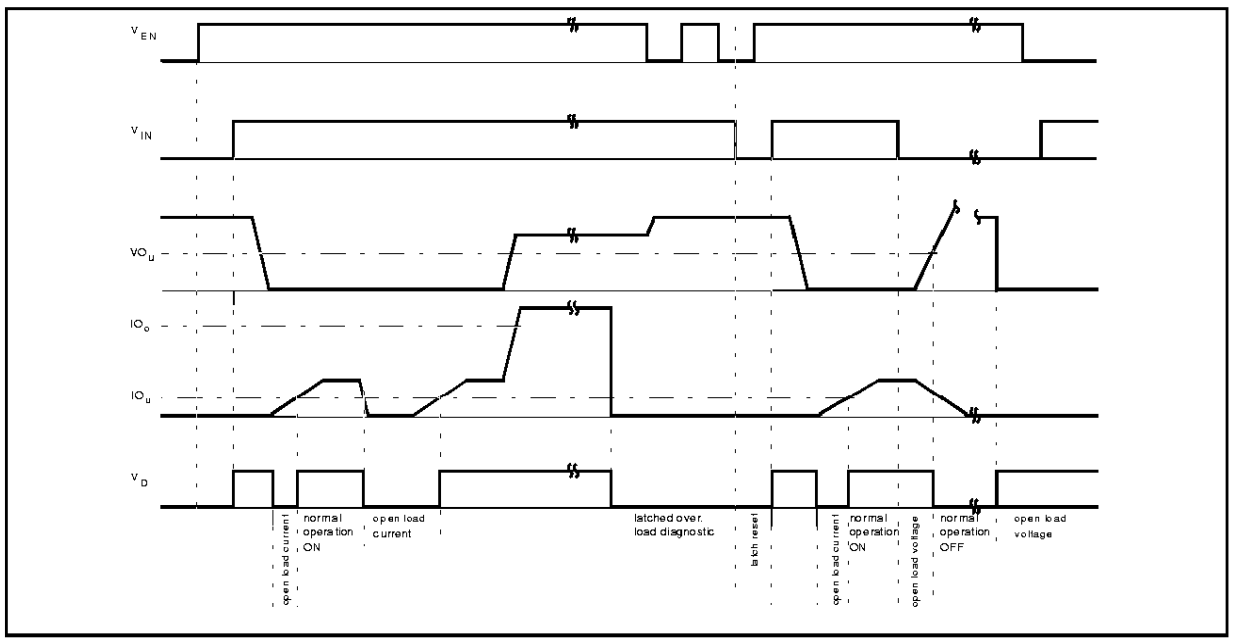
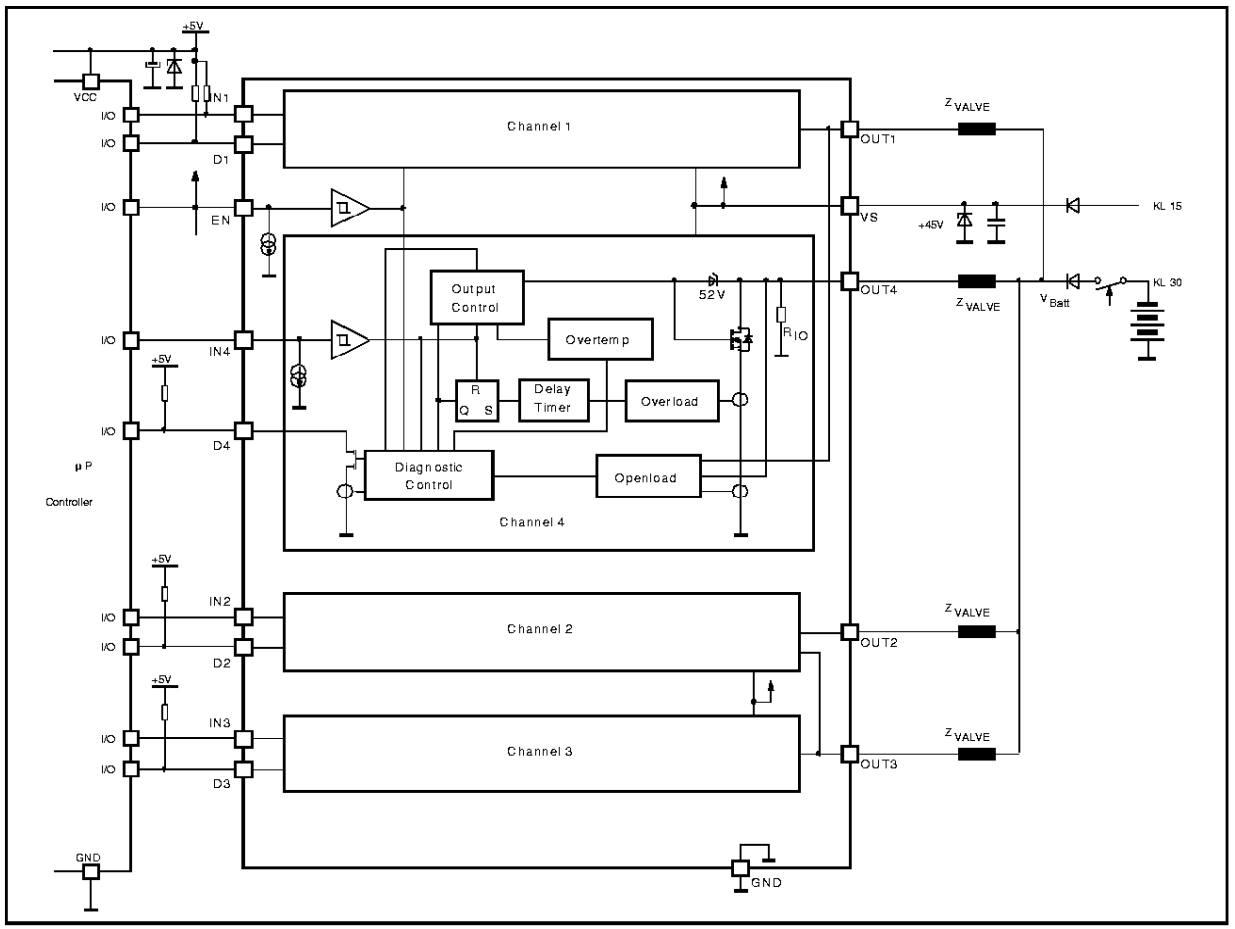


Figure 9. Application Circuit Diagram



POWERSO20 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.60			0.1417
a1	0.10		0.30	0.0039		0.0118
a2			3.30			0.1299
a3	0		0.10	0		0.0039
b	0.40		0.53	0.0157		0.0209
c	0.23		0.32	0.009		0.0126
D (1)	15.80		16.00	0.6220		0.6299
E	13.90		14.50	0.5472		0.570
e		1.27			0.050	
e3		11.43			0.450	
E1 (1)	10.90		11.10	0.4291		0.437
E2			2.90			0.1141
G	0		0.10	0		0.0039
h			1.10			
L	0.80		1.10	0.0314		0.0433
N	10° (max.)					
S	8° (max.)					
T		10.0			0.3937	

(1) "D and E1" do not include mold flash or protrusions
- Mold flash or protrusions shall not exceed 0.15mm (0.006")