Intel StrataFlash® Wireless Memory System (LV18/LV30 SCSP)

768-Mbit LVQ Family with Asynchronous Static RAM

Datasheet

Product Features

- **Device Architecture**
  - —Code and data segment: 128- and 256-Mbit density; PSRAM: 32- and 64-Mbit density; SRAM: 8 Mbit density.
  - —Top or bottom parameter configuration.
  - —Asymmetrical blocking structure.
  - —16-KWord parameter blocks (Top or Bottom); 64-K Word main blocks.
  - —Zero-latency block locking.
  - —Absolute write protection with block lock down using F-WP#.
- **Device Voltage**
  - —Core: V_{CC} = 1.8 V (typ).
  - —I/O: V_{CCQ} = 1.8 V or 3.0 V (typ).
- **Device Concurrent Operations (3 Dies)**
  - —Buffered EFP: 600 KB per second.
  - —Erase Performance: 384 KB per second (main blocks).
- **Device Packaging**
  - —88 balls (8 x 10 active ball matrix).
  - —Area: 8 x 10 mm or 8 x 11 mm.
  - —Height: 1.0 mm to 1.4 mm.
- **Quality and Reliability**
  - —Extended Temp: –25 °C to +85 °C.
  - —Minimum 100 K flash block erase cycle.
- **xRAM Performance**
  - —PSRAM at 1.8 V I/O : 85 ns initial access, 30 ns async page reads; 65 ns initial access, 18 ns async page.
  - —SRAM at 1.8 or 3.0 V I/O: 70 ns initial access.
- **Flash Performance**
  - —Code Segment at 1.8 V I/O: 85 ns initial access; 25 ns async page read; 14 ns sync reads (t_{CHQV}); 54 MHz CLK.
  - —Data Segment at 1.8 V I/O: 170 ns initial access; 55 ns async page read.
- **Flash Architecture**
  - —Hardware Read-While-Write/Erase.
  - —8-Mbit or 16-Mbit Multi-Partition.
  - —2-Kbit One-Time Programmable (OTP) Protection Register.
  - —Software Read-While-Write/Erase.
  - —Single Full-Die Partition size.
- **Flash Software**
  - —Intel® FDI, Intel® PSM, and Intel® VFM.
  - —Common Flash Interface (CFI).
  - —Basic/Extended Command Set.

The Intel StrataFlash® Wireless Memory System (LV18/LV30 SCSP); 768-Mbit LVQ Family with Asynchronous Static RAM device offers a high performance code and large embedded data segment plus RAM combination in a common package with electrical QUAD+ ballout on 0.13 µm ETOX™ VIII flash technology. The code segment flash die features 1.8 V low-power operations with flexible, multi-partition, dual operation Read-While-Write / Read-While-Erase, asynchronous and synchronous burst reads at 54 MHz. The data segment flash die features 1.8 V low-power operations optimized for cost sensitive asynchronous data applications. This device integrates up to three flash dies, two PSRAM dies, and one SRAM die in a low-profile package compatible with other SCSP families using the QUAD+ ballout package.

Notice: This document contains information on new products in production. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

253852-002
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Contents

Revision History

Date	Revision	Description
10/03r	-001	Initial Release
12/03	-002	In the Valid Combinations Table: Added line item mehcanical and ordering information for 256L+256V+64P+64P. Deleted the TBD 5-die stack option. Revised the Matrix table.

1.0 Introduction

This document provides information about the Intel StrataFlash® Wireless Memory System (LV18/LV30 SCSP); 768-Mbit LVQ Family with Asynchronous Static RAM device, including information on the features, characteristics, operations, and specifications for:

- Code and data segment flash dies
- SRAM and PSRAM dies

The intent of this document is to provide information where this 768-Mbit LVQ Family with Asynchronous Static RAM Stacked Chip Scale Package (SCSP) device differs from the Intel StrataFlash® Wireless Memory System (LV18/LV30 SCSP); 1024-Mbit LV Family device. Refer to the latest revision of the *Intel StrataFlash® Wireless Memory System (LV18/LV30 SCSP; 1024-Mbit LV Family Datasheet* (order number 253854) for flash product details not included in this document.

1.1 Nomenclature

0x	Hexadecimal prefix
0b	Binary prefix
Byte	8 bits
CFI	Common Flash Interface
DU	Don't Use
ETOX	EPROM Tunnel Oxide
k (noun)	1 thousand
Kb	1024 bits
KB	1024 bytes
Kword	1024 words
M (noun)	1 million
Mb	1,048,576 bits
MB	1,048,576 bytes
OTP	One-time Programmable
RCR	Read Configuration Register
RFU	Reserved for Future Use
SCSP	Stacked Chip Scale Package
SR	Status Register
SRD	Status Register Data
Word	16 bits

1.8 V Core	range of 1.7 V – 1.95 V
1.8 V I/O	range of 1.7 V – 1.95 V
Asserted	Signal with logical voltage level V_{IL}, or enabled
Deasserted	Signal with logical voltage level V_{IH}, or disabled
High-Z	Tri-stated or High Impedance
Low-Z	Driven

Non-Array Reads	Flash reads which return flash Device Identifier, CFI Query, Protection Register and Status Register information
Program	An operation to Write data to the flash array
Write	Bus cycle operation at the inputs of the flash die, in which a command or data are sent to the flash array
Block	Group of cells, bits, bytes or words within the flash memory array that get erased with one erase instruction
Parameter block	Any 16-Kword flash array block.
Main block	Any 64-Kword flash array block.
Top parameter	Previously referred to as a top-boot device, a device with flash parameter partition located at the highest physical address of its memory map for processor system boot up.
Bottom parameter	Previously referred to as a bottom-boot device, a device with flash parameter partition located at the lowest physical address of its memory map for processor system boot up.
Bottom-Top parameter	Stacked-CSP device configuration of two flash dies in the same segment arranged with the parameter partitions located at the lowest and highest physical address of its memory map.
Partition	A group of flash blocks that shares common status register read state.
Parameter partition	A flash partition containing parameter and main blocks.
Main partition	A flash partition containing only main blocks.
Die	Individual physical flash die used in a stacked-CSP memory subsystem device
Segment	A section of the SCSP memory subsystem divided for different operating characteristics. The SCSP memory subsystem has three segments: a code segment, a data segment, and an xRAM segment.
Code segment	A segment that contains one or two flash memory dies optimized for fast code or data reads. Each die features multi-partition synchronous read-while-write or burst read-while-erase capability.
Data segment	A segment contains one or two flash memory dies optimized for large embedded data. Each die feature single-partition asynchronous read, write, and erase operations.
xRAM segment	A segment contains one or two xRAM memory dies. The xRAM combinations could include SRAM, PSRAM, or LPSDRAM.
Subsystem	A stacked memory integration concept made up of multiple memory dies arranged in Code, Data, and xRAM segments.
Device	An individual flash die or a flash + xRAM SCSP.

1.2 Acronyms

Buffered-EFP	Buffered Enhanced Factory Programming
CUI	Command User Interface
OTP	One-Time Programmable
PLR	Protection Lock Register
PR	Protection Register
RCR	Read Configuration Register
RFU	Reserved for Future Use (all unused active signals in a package ballout)
SR	Status Register
WSM	Write State Machine
APS	Automatic Power Savings
CFI	Common Flash Interface
MLC technology	Multi-Level-Cell technology
RWE	Read-While-Erase
RWW	Read-While-Write

1.3 Conventions

VCC	Signal or voltage connection
V_{CC}	Signal or voltage level
Set	Logical one (1)
Clear	Logical zero (0)
0x	Hexadecimal number prefix
0b	Binary number prefix
SR[4]	Denotes an individual flash status register bit, in this case bit 5 of SR[7:0].
D[15:0]	Denotes a group of similarly named signals, such as data bus.
A5	Denotes one element of a signal group membership, in this case address bit 5.
F[3:1]-CE#, F[2:1]-OE#	This is the method used to refer to more than one chip-enable or output enable at the same time. When each is referred to individually, the reference will be F1-CE# and F1-OE# (for die #1), F2-CE# and F2-OE# (for die #2), and F3-CE# and F3-OE#(for die #3). “F” denotes the flash specific signal and “CE#” is the root signal name of the flash die. Other

	notation includes: “S” to denote SRAM, “P” to denote PSRAM, “D” to denote LPSDRAM, and “R” to denote common RAM type signal names.
ADV#	Denotes a global signal of the device, Address Valid because there is no die specific reference.

2.0 Functional Overview

This section provides an overview of the code and embedded data segment features and capabilities of the 768-Mbit LVQ Family with Asynchronous Static RAM device.

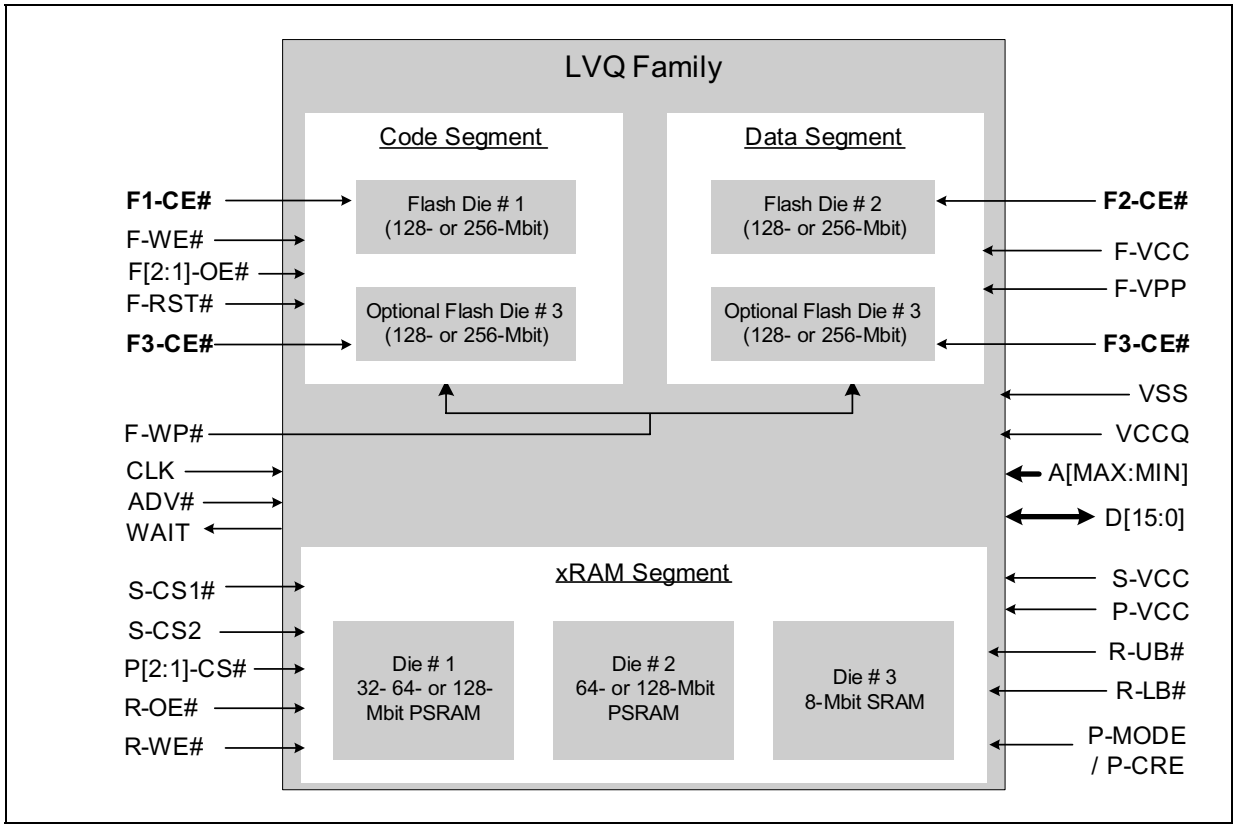
2.1 Device Description

The 768-Mbit LVQ Family with Asynchronous Static RAM device incorporates flash dies used as code segment flash memory and large embedded data segment flash memory, along with xRAM for a high performance, cost-effective high density memory system solution. This stacked device uses the latest Intel StrataFlash® Wireless Memory System on 0.13 µm ETOX™ VIII process technology.

The code segment is a high performance, multi-partition, synchronous burst-mode Read-While-Write (RWW) or Read-While-Erase (RWE) flash memory die, while the large, embedded data segment is a cost efficient, single-partition, asynchronous flash memory die.

The package for this device is available in a QUAD+ ballout, which supports flash only or flash + PSRAM and/or SRAM stacked memory combinations. The SCSP in a QUAD+ ballout with a 0.8 mm ball pitch, 8x10 active ball matrix supports a memory subsystem up to 66 MHz on a x16-bit bus width. See Figure 1, “LV18/LV30 device family block diagram” on page 9 for device block diagram.

Figure 1. LV18/LV30 device family block diagram



The 768-Mbit LVQ Family with Asynchronous Static RAM device consists of a 1.8 V flash memory device with 1.8 V and 3.0 V I/O options. As shown in Figure 1, “LV18/LV30 device family block diagram” on page 9, the device is available with a minimum of one flash die each per code segment and data segment (flash die # 1 and flash die #2). An optional third flash die is available for either the code or data segment. See Table 1, “768 Mbit LVQ Family Matrix” on page 10 for possible combinations.

Designed for low-voltage systems, the LVQ supports read operations with F-V_{CC} at 1.8 V, and erase and program operations with F-Vpp at 1.8 V. Buffered Enhanced Factory Programming (Buffered-EFP) provides the fastest flash array programming performance, with elevated F-V_{PP} at 9.0 V to increase factory throughput. With F-V_{PP} at 1.8 V, F-Vcc and F-Vcc can be tied together for a simple, ultra-low-power design. In addition to voltage flexibility, a dedicated F-V_{PP} connection provides complete data protection when F-Vpp ≤ V_{PPLK}.

The Intel StrataFlash® Wireless Memory System provides data security through its individual zero-latency block lock capability. Each memory block can be unlocked, locked, or locked-down by hardware or software control.

Individualized F-CE# control allows the user to manage which flash die is asserted, furthering the flexibility of power management while controlling data integrity per segment with F-WP#. The F[2:1]-OE# in LVQ products with QUAD+ ballout are common internally

Table 1. 768 Mbit LVQ Family Matrix

Line Item	Flash Components	RAM Components	Package Size	Notes
1.8 V I/O	256L18 + 256L18	None	8x11x1.2	1
	256L18 + 256V18	64PS + 64PS	11x13x1.4	1
3.0 V I/O	256L30 + 256V30	None	8x11x1.2	1

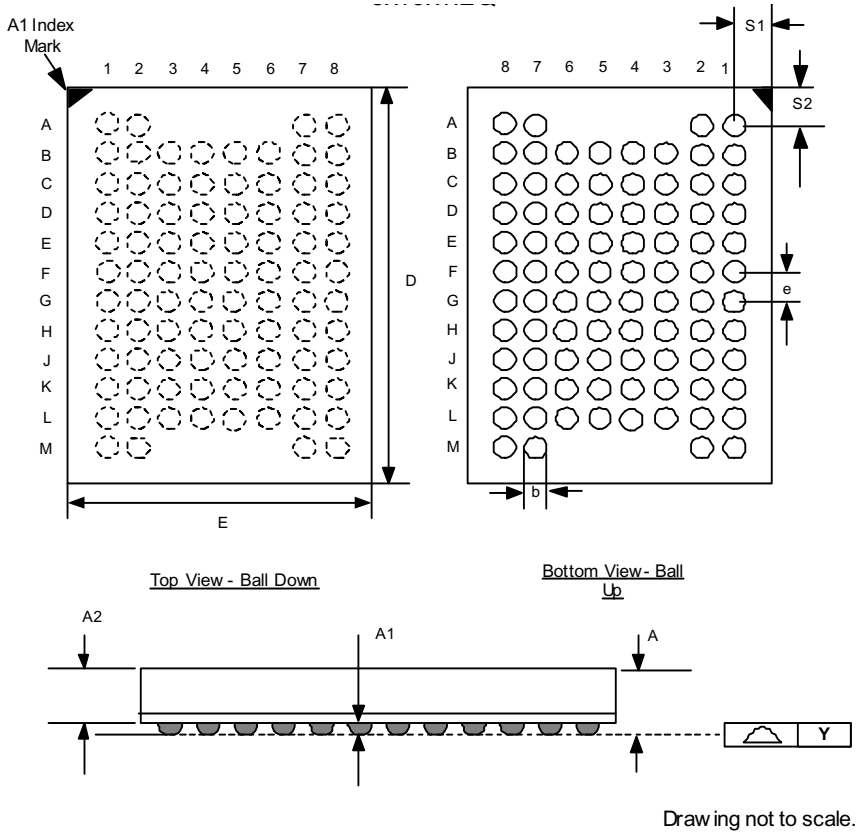
NOTES:
1. Available in Top or Bottom Configurations.

3.0 Package Information

The 768-Mbit LVQ Family with Asynchronous Static RAM device is available with various die combinations in both the standard Stacked Chip Scale Package (SCSP) and the Intel® Ultra-Thin Stacked Chip Scale Package (Intel® UT-SCSP).

3.1 One- and Two-Die SCSP

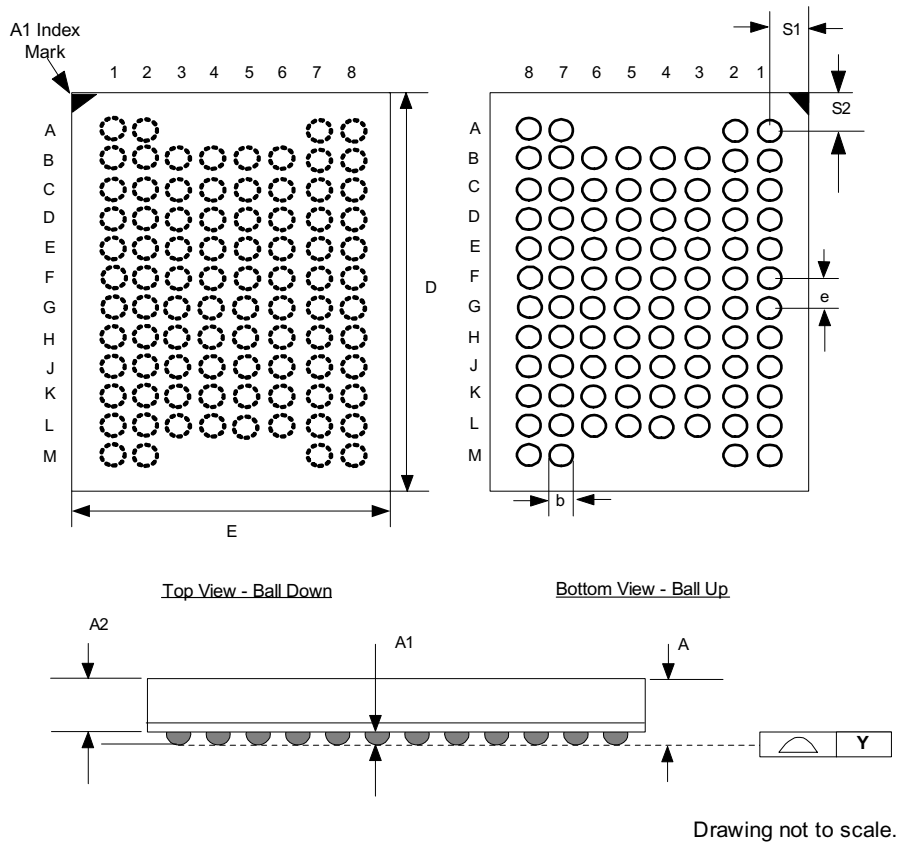
Figure 2. Mechanical Specifications for One/Two-Die SCSP (8x10 mm)



		Millimeters				Inches		
Dimensions	**Symbol**	**Min**	**Nom**	**Max**	**Notes**	**Min**	**Nom**	**Max**
Package Height	A			1.200				0.0472
Ball Height	A1	0.200				0.0079		
Package Body Thickness	A2		0.860				0.0339	
Ball (Lead) Width	b	0.325	0.375	0.425		0.0128	0.0148	0.0167
Package Body Length	D	9.900	10.000	10.100		0.3898	0.3937	0.3976
Package Body Width	E	7.900	8.000	8.100		0.3110	0.3150	0.3189
Pitch	e		0.800				0.0315	
Ball (Lead) Count	N		88				88	
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to Ball A1 Distance Along E	S1	1.100	1.200	1.300		0.0433	0.0472	0.0512
Corner to Ball A1 Distance Along D	S2	0.500	0.600	0.700		0.0197	0.0236	0.0276

3.2 Four-Die SCSP

Figure 3. Mechanical Specifications for Four-Die SCSP (11x13 mm)

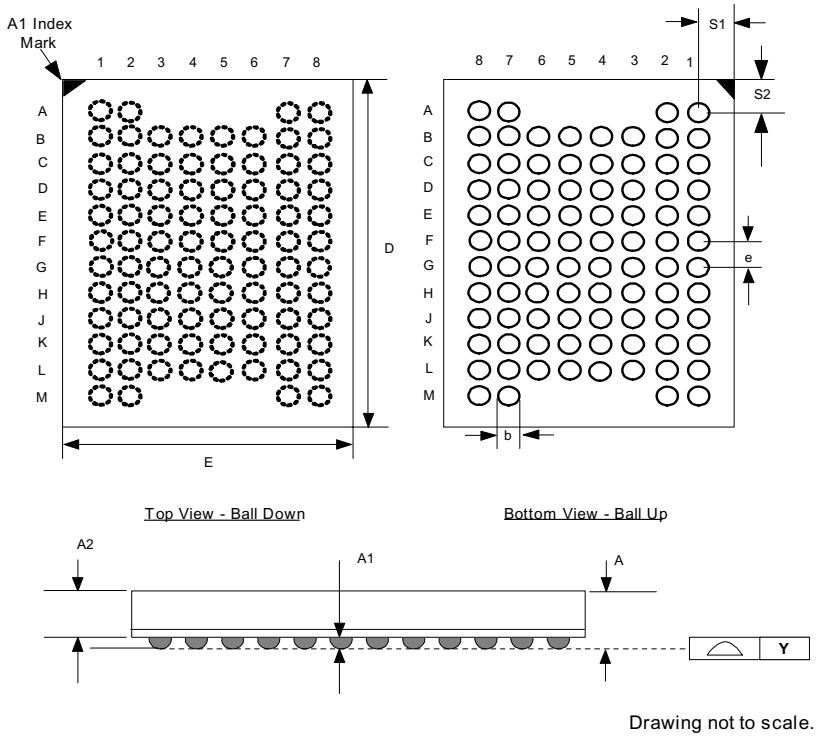


Drawing not to scale.

		Millimeters				Inches		
Dimensions	**Symbol**	**Min**	**Nom**	**Max**	**Notes**	**Min**	**Nom**	**Max**
Package Height	A			1.400				0.0551
Ball Height	A1	0.200				0.0079		
Package Body Thickness	A2		1.070				0.0421	
Ball (Lead) Width	b	0.325	0.375	0.425		0.0128	0.0148	0.0167
Package Body Length	D	12.900	13.000	13.100		0.5079	0.5118	0.5157
Package Body Width	E	10.900	11.000	11.100		0.4291	0.4331	0.4370
Pitch	e		0.800				0.0315	
Ball (Lead) Count	N		88				88	
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to Ball A1 Distance Along E	S1	2.600	2.700	2.800		0.1024	0.1063	0.1102
Corner to Ball A1 Distance Along D	S2	2.000	2.100	2.200		0.0787	0.0827	0.0866

3.3 One-Die Intel® UT-SCSP

Figure 4. Mechanical Specifications for One-Die Intel® UT-SCSP (8x11 mm)



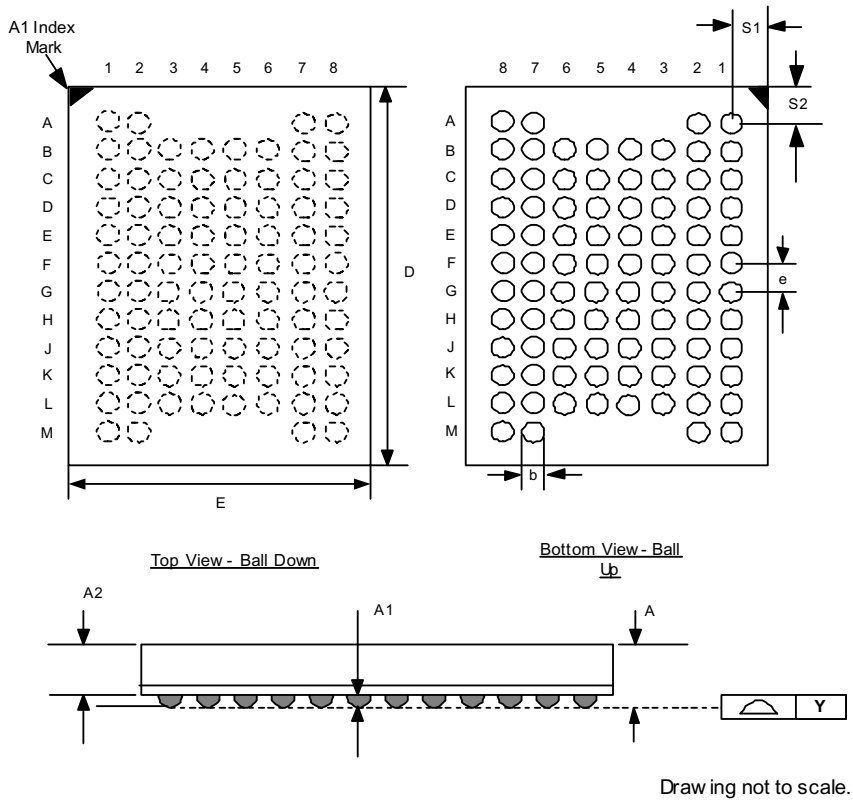
Drawing not to scale.

Note: Dimensions A1, A2, and b are preliminary

		Millimeters				Inches		
Dimensions	**Symbol**	**Min**	**Nom**	**Max**	**Notes**	**Min**	**Nom**	**Max**
Package Height	A			1.00				0.0394
Ball Height	A1	0.117				0.0046		
Package Body Thickness	A2		0.740				0.0291	
Ball (Lead) Width	b	0.300	0.350	0.400		0.0118	0.0138	0.0157
Package Body Length	D	10.900	11.00	11.100		0.4291	0.4331	0.4370
Package Body Width	E	7.900	8.00	8.100		0.3110	0.3150	0.3189
Pitch	e		0.80				0.0315	
Ball (Lead) Count	N		88				88	
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to Ball A1 Distance Along E	S1	1.100	1.200	1.300		0.0433	0.0472	0.0512
Corner to Ball A1 Distance Along D	S2	1.000	1.100	1.200		0.0394	0.0433	0.0472

3.4 Two-Die Intel® UT-SCSP

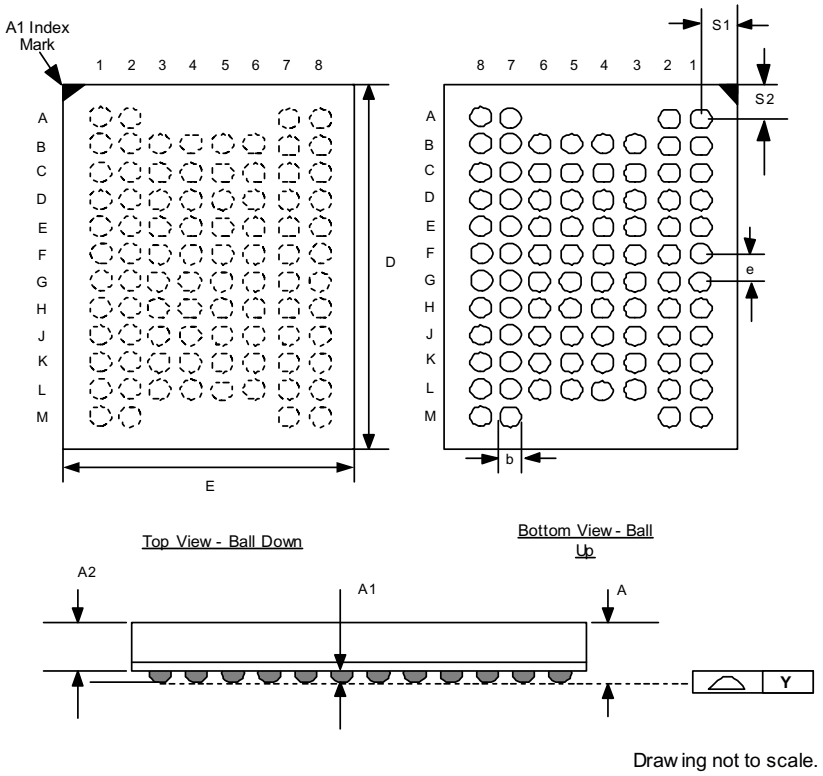
Figure 5. Mechanical Specifications for Two-Die Intel® UT-SCSP (8x11 mm)



		Millimeters				Inches		
Dimensions	**Symbol**	**Min**	**Nom**	**Max**	**Notes**	**Min**	**Nom**	**Max**
Package Height	A			1.200				0.0472
Ball Height	A1	0.200				0.0079		
Package Body Thickness	A2		0.860				0.0339	
Ball (Lead) Width	b	0.325	0.375	0.425		0.0128	0.0148	0.0167
Package Body Length	D	10.900	11.000	11.100		0.4291	0.4331	0.4370
Package Body Width	E	7.900	8.000	8.100		0.3110	0.3150	0.3189
Pitch	e		0.800				0.0315	
Ball (Lead) Count	N		88				88	
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to Ball A1 Distance Along E	S1	1.100	1.200	1.300		0.0433	0.0472	0.0512
Corner to Ball A1 Distance Along D	S2	1.000	1.100	1.200		0.0394	0.0433	0.0472

3.5 Three-Die Intel® UT-SCSP

Figure 6. Mechanical Specifications for Three-Die Intel® UT-SCSP (8x11 mm)



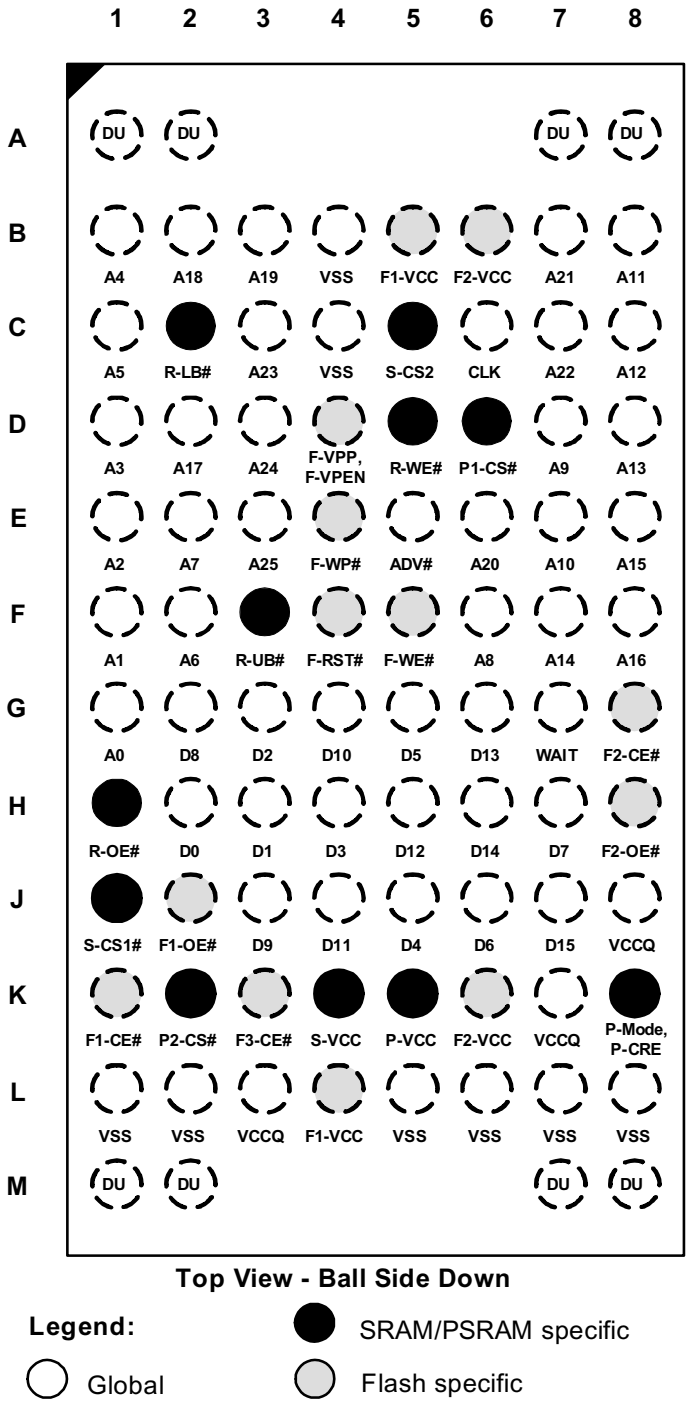
Note: Dimensions A1, A2, and b are preliminary

		Millimeters				Inches		
Dimensions	**Symbol**	**Min**	**Nom**	**Max**	**Notes**	**Min**	**Nom**	**Max**
Package Height	A			1.20				0.0472
Ball Height	A1	0.117				0.0046		
Package Body Thickness	A2		0.910				0.0358	
Ball (Lead) Width	b	0.300	0.350	0.400		0.0118	0.0138	0.0157
Package Body Length	D	10.900	11.00	11.100		0.4291	0.4331	0.4370
Package Body Width	E	7.900	8.00	8.100		0.3110	0.3150	0.3189
Pitch	e		0.80				0.0315	
Ball (Lead) Count	N		88				88	
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to Ball A1 Distance Along E	S1	1.100	1.200	1.300		0.0433	0.0472	0.0512
Corner to Ball A1 Distance Along D	S2	1.000	1.100	1.200		0.0394	0.0433	0.0472

4.0 Ballout and Signal Descriptions

Figure 7, "QUAD+ Signal Ballout for LVQ Device Family" shows the signal ballout for the 768-Mbit LVQ Family with Asynchronous Static RAM device, ideal for space-constrained board applications and allowing density upgrades without PCB redesign. The user is responsible to adapt for density upgrade flexibility in the PCB design.

Figure 7. QUAD+ Signal Ballout for LVQ Device Family



4.1 Signal Descriptions

Table 2 describes the active signals used on the 768-Mbit LVQ Family with Asynchronous Static RAM device.

Table 2. Signal Descriptions (Sheet 1 of 3)

Symbol	Type	Description
A[MAX:MIN]	Input	**ADDRESS INPUTS:** Inputs for all die addresses during read and write operations. • 256-Mbit Die : AMAX= A23 • 128-Mbit Die : AMAX = A22 • 64-Mbit Die : AMAX = A21 • 32-Mbit Die : AMAX = A20 • 8-Mbit Die : AMAX = A18 A0 is the lowest-order 16-bit wide address. A[25:24] denote high-order addresses reserved for future device densities.
D[15:0]	Input/ Output	**DATA INPUTS/OUTPUTS:** Inputs data and commands during write cycles, outputs data during read cycles. Data signals float when the device or its outputs are deselected. Data are internally latched during writes on the flash device.
F[3:1]-CE#	Input	**FLASH CHIP ENABLE:** Low-true input. F[3:1]-CE# low selects the associated flash memory die. When asserted, flash internal control logic, input buffers, decoders, and sense amplifiers are active. When deasserted, the associated flash die is deselected, power is reduced to standby levels, data and WAIT outputs are placed in high-Z state. F1-CE# selects or deselects flash die #1; F2-CE# selects or deselects flash die #2 and is RFU on combinations with only one flash die. F3-CE# selects or deselects flash die #3 and is RFU on stacked combinations with only one or two flash dies.
S-CS1# S-CS2	Input	**SRAM CHIP SELECT:** Low-true / high-true input (S-CS1# / S-CS2 respectively). When either/both SRAM Chip Select signals are asserted, SRAM internal control logic, input buffers, decoders, and sense amplifiers are active. When either/both SRAM Chip Select signals are deasserted, the SRAM is deselected and its power is reduced to standby levels. S-CS1# and S-CS2 are available on stacked combinations with SRAM die and are RFU on stacked combinations without SRAM die.
P[2:1]-CS#	Input	**PSRAM CHIP SELECT:** Low-true input. When asserted, PSRAM internal control logic, input buffers, decoders, and sense amplifiers are active. When deasserted, the PSRAM is deselected and its power is reduced to standby levels. P1-CS# selects PSRAM die #1 and is available only on stacked combinations with PSRAM die. This ball is an RFU on stacked combinations without PSRAM. P2-CS# selects PSRAM die #2 and is available only on stacked combinations with two PSRAM dies. This ball is an RFU on stacked combinations without PSRAM or with a single PSRAM.
F[2:1]-OE#	Input	**FLASH OUTPUT ENABLE:** Low-true input. F[2:1]-OE# low enables the flash output buffers. F[2:1]-OE# high disables the flash output buffers, and places the selected flash outputs in High-Z. F1-OE# controls the outputs of flash die #1; F2-OE# controls the outputs of flash die #2 and flash die #3. F2-OE# is available on stacked combinations with two or three flash die and is RFU on stacked combinations with only one flash die.

Table 2. Signal Descriptions (Sheet 2 of 3)

R-OE#	Input	**RAM OUTPUT ENABLE:** Low-true input. R-OE# low enables the selected RAM output buffers. R-OE# high disables the RAM output buffers, and places the selected RAM outputs in High-Z. R-OE# is available on stacked combinations with PSRAM or SRAM die, and is an RFU on flash-only stacked combinations.
F-WE#	Input	**FLASH WRITE ENABLE:** Low-true input. F-WE# controls writes to the selected flash die. Address and data are latched on the rising edge of F-WE#.
R-WE#	Input	**RAM WRITE ENABLE:** Low-true input. R-WE# controls writes to the selected RAM die. R-WE# is available on stacked combinations with PSRAM or SRAM die and is an RFU on flash-only stacked combinations.
CLK	Input	**CLOCK:** Synchronizes the flash die with the system bus clock in synchronous read mode and increments the internal address generator. During synchronous read operations, addresses are latched on the rising edge of ADV#, or on the next valid CLK edge with ADV# low, whichever occurs first. In asynchronous mode, addresses are latched on the rising edge ADV#, or are continuously flow-through when ADV# is kept asserted.
WAIT	Output	**WAIT:** Output signal. Indicates data is valid in synchronous array or non-array sync flash reads. Configuration Register bit 10 (CR.10, WT) determines its polarity when asserted. With F-CE# and F-OE# at V_{IL}, WAIT's active output is V_{OL} or V_{OH}. WAIT is high-Z if F-CE# or F-OE# is V_{IH}. • In synchronous array or non-array flash read modes, WAIT indicates invalid data when asserted and valid data when deasserted. • In asynchronous flash page read, and all flash write modes, WAIT is deasserted.
F-WP#	Input	**FLASH WRITE PROTECT:** Low-true input. F-WP# enables/disables the lock-down protection mechanism of the selected flash die. • F-WP# low enables the lock-down mechanism where locked down blocks cannot be unlocked with software commands. • F-WP# high disables the lock-down mechanism, allowing locked down blocks to be unlocked with software commands.
ADV#	Input	**ADDRESS VALID:** Low-true input. During synchronous flash read operations, addresses are latched on the rising edge of ADV#, or on the next valid CLK edge with ADV# low, whichever occurs first. In asynchronous flash read operations, addresses are latched on the rising edge of ADV#, or are continuously flow-through when ADV# is kept asserted.
R-UB# R-LB#	Input	**RAM UPPER / LOWER BYTE ENABLES:** Low-true input. During RAM read and write cycles, R-UB# low enables the RAM high order bytes on D[15:8], and R-LB# low enables the RAM low-order bytes on D[7:0]. R-UB# and R-LB# are available on stacked combinations with PSRAM or SRAM die and are RFU on flash-only stacked combinations.
F-RST#	Input	**FLASH RESET:** Low-true input. F-RST# low initializes flash internal circuitry and disables flash operations. F-RST# high enables flash operation. Exit from reset places the flash in asynchronous read array mode.

Table 2. Signal Descriptions (Sheet 3 of 3)

P-Mode, P-CRE	Input	**P-Mode (PSRAM Mode):** Low-true input. P-MODE is used to program the configuration register, and enter/exit Low-Power Mode of PSRAM die. P-Mode is available on stacked combinations with asynchronous-only PSRAM die. **P-CRE (PSRAM configuration register enable):** High-true input. P-CRE is high, write operations load the refresh control register or bus control register. P-CRE is applicable only on combinations with synchronous PSRAM die. P-Mode, P-CRE s RFU on stacked combinations without PSRAM die.
F-VPP, F-VPEN	Power	**FLASH PROGRAM AND ERASE POWER:** Valid F-V_{PP} voltage on this ball enables flash program/erase operations. Flash memory array contents cannot be altered when F-V_{PP}(F-V_{PEN}) < V_{PPLK} (V_{PENLK}). Erase / program operations at invalid F-V_{PP} (F-V_{PEN}) voltages should not be attempted. Refer to flash discrete product datasheet for additional details. F-VPEN (Erase/Program/Block Lock Enables) is not available for L18/L30 SCSP products.
F[2:1]-VCC	Power	**FLASH LOGIC POWER:** F1-VCC supplies power to the core logic of flash die #1; F2-VCC supplies power to the core logic of flash die #2 and flash die #3. Write operations are inhibited when F-V_{CC} < V_{LKO}. Device operations at invalid F-V_{CC} voltages should not be attempted. F2-VCC is available on stacked combinations with two or three flash dies, and is an RFU on stacked combinations with only one flash die.
S-VCC	Power	**SRAM POWER SUPPLY:** Supplies power for SRAM operations. S-VCC is available on stacked combinations with SRAM die, and is RFU on stacked combinations without SRAM die.
P-VCC	Power	**PSRAM POWER SUPPLY:** Supplies power for PSRAM operations. P-VCC is available on stacked combinations with PSRAM die, and is RFU on stacked combinations without PSRAM die.
VCCQ	Power	**DEVICE I/O POWER:** Supply power for the device input and output buffers.
VSS	Power	**DEVICE GROUND:** Connect to system ground. Do not float any VSS connection.
RFU		**RESERVED for FUTURE USE:** Reserved for future device functionality/ enhancements. Contact Intel regarding the use of balls designated RFU.
DU		**Don't Use:** Do not connect to any other signal, or power supply; must be left floating.

5.0 Maximum Ratings and Operating Conditions

5.1 Absolute Maximum Ratings

Warning: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

NOTICE: This document contains information available at the time of its release. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

Table 3. Absolute Maximum Ratings

Parameter		MIN	MAX	Unit	Notes
Temperature under Bias Expanded		–25	+85	°C	5
Storage Temperature		–55	+125	°C	5
Voltage On Any Signal (except F-V_{CC}, V_{CCQ}, F-V_{PP}, S-V_{CC}, and P-V_{CC})		–0.5	+3.6	V	1,5
F-V_{CC} Voltage		–0.2	+2.50	V	1,5
V_{CCQ}, P-V_{CC} and S-V_{CC} Voltage	1.8V I/O	–0.2	+2.50	V	1,5
	3.0 V I/O	–0.2	+3.60	V	1,5
F-V_{PP} Voltage		–0.2	+10.0	V	1,2,3,5
I_{SH} Output Short Circuit Current		–	100	mA	4,5

NOTES:
1. All specified voltages are relative to V_{SS}. Minimum DC voltage is –0.5 V on input/output signals, –0.2 V on V_{CCQ} and F-V_{PP} signals. During transitions, this level may overshoot to –2.0 V for periods < 20 ns. Maximum DC voltage on F-V_{CC} is V_{CC} + 0.5 V, which during transitions may overshoot to F-Vcc +2.0 V for periods <20 ns. Maximum DC voltage on input/output signals and VCCQ is V_{CCQ} +0.5 V, which during transitions may overshoot to V_{CCQ} + 2.0V for periods < 20ns.
2. Maximum DC voltage on F-V_{PP} may overshoot to +10.0 V for periods < 20 ns.
3. Flash program/erase voltage (F-V_{PP}) is typically 1.7 V-2.0 V. F-Vpp can be connected to 8.50 V - 9.50 V for 1000 cycles on main blocks and 2500 cycles on parameter blocks, or for 80 hours maximum total. Operation with 9.0 V program/erase voltage may reduce flash block cycling capability.
4. Output shorted for no more than one second. No more than one output shorted at a time.
5. Absolute DC specifications applies to each flash and RAM die in the SCSP device.

5.2 Operating Conditions

Table 4. Extended Temperature Operation

Symbol	Parameter		Flash + Flash		Flash + PSRAM		Flash + PSRAM + SRAM[2]		Unit
			MIN	MAX	MIN	MAX	MIN	MAX	
T_C	Operating Temperature		–25	+85	–25	+85	–25	+85	°C
F-V_{CC}	Flash Supply Voltage		1.7	2.0	1.7	2.0	1.7	2.0	V
V_{CCQ} P-V_{CC} S-V_{CC}	Flash I/O Voltage	3.0 V I/O	2.2	3.3	2.7	3.1	2.7	3.1	V
	PSRAM and SRAM Supply Voltage	1.8 V I/O	1.7	2.0	1.8	1.95	–	–	V
V_{PPL}[1]	F-V_{PP} Voltage Supply (Logic Level)		0.9	2	0.9	2	0.9	2	V
V_{PPH}[1]	Factory word programming F-V_{PP}		8.5	9.5	8.5	9.5	8.5	9.5	V

NOTES:
1. Flash program/erase voltage (F-V_{PP}) is typically 1.7 V-2.0 V. F-Vpp can be connected to 8.50 V - 9.50 V for 1000 cycles on main blocks and 2500 cycles on parameter blocks, or for 80 hours maximum total. Operation with 9.0 V program/erase voltage may reduce flash block cycling capability.
2. SRAM is available only in 3.0 V I/O option.

6.0 Electrical Specifications

6.1 DC Current Characteristics

The DC current characteristics referenced in this document are for individual flash and RAM die in the SCSP device. The total device current is determined by sum of the active and inactive currents of each flash and RAM die in the SCSP device.

Note: Refer to the latest revision of the *Intel StrataFlash® Wireless Memory System (LV18/LV30 SCSP; 1024-Mbit LV Family Datasheet* (order number 253854) for flash DC characteristics not included in this document.

SRAM DC characteristics are shown in Table 5. PSRAM DC characteristics are shown in Table 6 on page 24.

NOTICE: Individual DC Characteristics of all dies in a SCSP device need to be considered accordingly, depending on the SCSP device stacked combinations and operations.

Table 5. SRAM DC Characteristics

Parameter	Description	Test Conditions	3.0 V SRAM		Unit
			MIN	MAX	
$S\text{-}V_{CC}$	Voltage Range	–	2.7	3.3	V
V_{DR}	$S\text{-}V_{CC}$ for Data Retention	–	1.5	–	V
I_{CC}	Operating Current at minimum cycle time	I_{IO} = 0 mA	–	50	mA
I_{CC2}	Operating Current at maximum cycle time (1 µs)	I_{IO} = 0 mA	–	10	mA
I_{SB}	Standby Current	S-CS1# ≥ $S\text{-}V_{CC}$-0.2V or S-CS2 ≤ V_{SS}+0.2V Address/Data toggling at minimum cycle time	–	25	µA
I_{DR}	Current in Data Retention mode	$S\text{-}V_{CC}$ = 1.5 V	–	12	µA
V_{OH}	Output High Voltage	I_{OH} = -100 µA	$S\text{-}V_{CC}$ - 0.1	–	V
V_{OL}	Output Low Voltage	I_{OL} = 100 µA, V_{CCMIN}	-0.1	0.1	V
V_{IH}	Input High Voltage	–	$S\text{-}V_{CC}$ - 0.4	$S\text{-}V_{CC}$+ 0.2	V
V_{IL}	Input Low Voltage	–	-0.2	0.6	V
$*I_{IL}$	Input Leakage Current	-0.2 < V_{IN} < $S\text{-}V_{CC}$+0.2 V	-1	+1	µA
$*I_{LDR}$	Input Leakage Current in Data Retention Mode	-0.2 < V_{IN} < $S\text{-}V_{CC}$+0.2 V $S\text{-}V_{CC}$ = V_{DR}	-1	+1	µA

NOTE: * Input leakage currents include Hi-Z output leakage for bi-directional buffers with tri-state outputs.

Table 6. PSRAM DC Characteristics

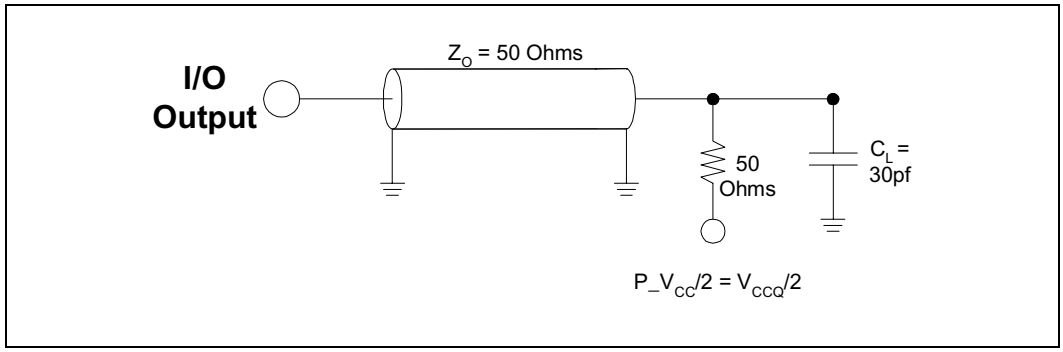
Parameter	Description	Test Conditions			P-V_{CC} = 1.8 V to 1.95 V			P-V_{CC} = 2.7 V to 3.1 V			Unit
					MIN	Typ	MAX	MIN	Typ	MAX	
I_{CC}	Operating Current at minimum cycle time	I_{OUT}=0mA			–	–	35	–	–	45	mA
I_{SB1}	Standby Current	P-CS# ≥ P-V_{CC}-0.2V,P-Mode ≥ P-V_{CC}-0.2V	32-Mbit		–	90	100	–	90	100	µA
			64-Mbit		N/A			–	110	150	µA
I_{SB2}	Partial Array Refresh Current (Standby Mode 2)	P-CS# ≥ P-V_{CC}-0.2V, P-Mode ≤ 0.2V	32-Mbit	16-Mbit	–	60	70	–	60	70	µA
				8-Mbit	–	50	60	–	50	60	µA
				4-Mbit	–	40	50	–	40	50	µA
				0-Mbit	–	20	30	–	20	30	µA
			64-Mbit	16-Mbit	N/A			–	90	110	µA
				8-Mbit				–	80	100	µA
				4-Mbit				–	70	90	µA
				0-Mbit				–	60	80	µA
I_{SBD}	Deep Power Down	P-CS# ≥ P-V_{CC}-0.2V, P-Mode ≤ 0.2V	32-Mbit		–	20	30	–	20	30	µA
			64-Mbit		N/A			–	60	80	µA
V_{OH}	Output High Voltage	I_{OH} = -0.5 mA			0.8V_{CCQ}	–	–	0.8V_{CCQ}	–	–	V
V_{OL}	Output Low Voltage	I_{OL} = 1 mA			–	–	0.2V_{CCQ}	–	–	0.2V_{CCQ}	V
V_{IH}	Input High Voltage	–			0.8V_{CCQ}	–	V_{CCQ} + 0.3	0.8V_{CCQ}	–	V_{CCQ}+ 0.3	V
V_{IL}	Input Low Voltage	–			-0.3	–	0.2V_{CCQ}	-0.3	–	0.2V_{CCQ}	V
*I_{IL}	Input Leakage Current	V_{IN} = 0V to V_{CCQ}			–1.0	–	+1.0	–1.0	–	+1.0	µA
*I_{OL}	Input/Output Leakage Current	$V_{I/O}$ = 0V to V_{CCQ}, P-CS# = V_{IH} or R-WE# = V_{IH} or R-OE# = V_{IH}			–1.0	–	+1.0	–1.0	–	+1.0	µA

NOTE: * V_{IN}: Input voltage, $V_{I/O}$: Input/Output voltage.

7.0 AC Characteristics

7.1 SCSP Device AC Test Conditions

Figure 8. Transient Equivalent Testing Load Circuit[1,2]



NOTES:
1. Test configuration component value for worst case speed conditions.
2. C_L includes jig capacitance.

7.2 SRAM and PSRAM Capacitance

SRAM and PSRAM capacitance is shown in Table 7, "SRAM and PSRAM Capacitance" on page 25.

Note: Refer to the latest revision of the *Intel StrataFlash® Wireless Memory System (LV18/LV30 SCSP; 1024-Mbit LV Family Datasheet* (order number 253854) for flash capacitance details not included in this document.

Table 7. SRAM and PSRAM Capacitance

Symbol	Parameter	MAX (SRAM)	MAX (PSRAM)	Unit	Condition
C_{IN}	Input Capacitance	6	8	pF	V_{IN} = 0 V
C_{OUT}	Output Capacitance	7	10	pF	V_{OUT} = 0 V

NOTE: Sampled, not 100% tested. T_C = +25 °C, f = 1 MHz.

7.3 SRAM AC Read Specifications

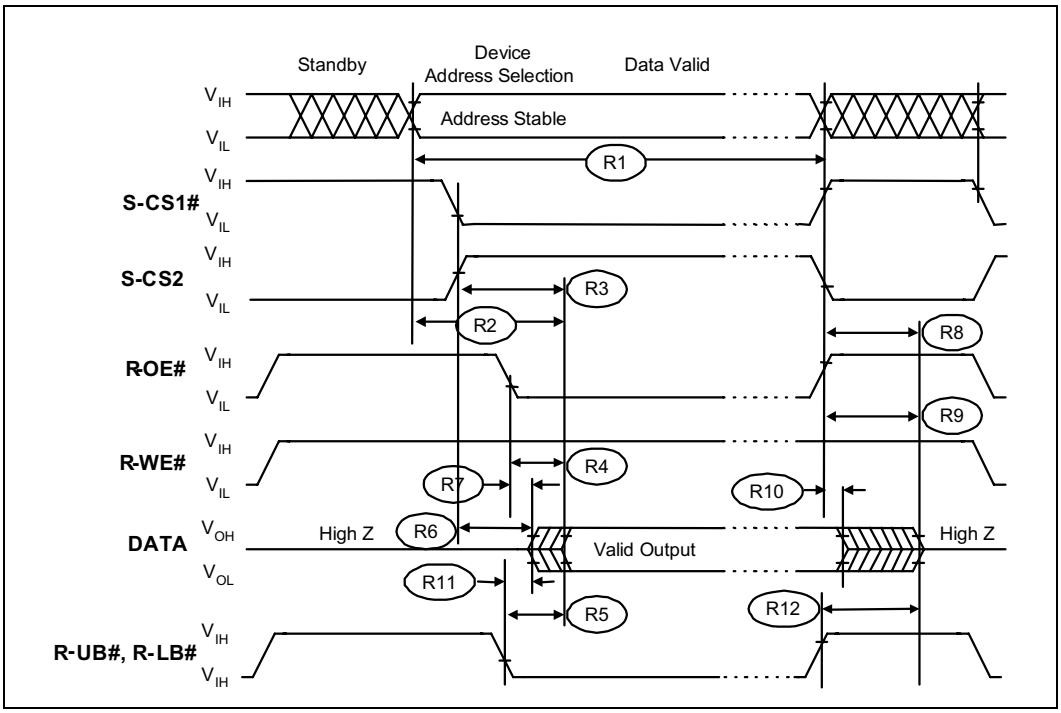
Note: Refer to the latest revision of the *Intel StrataFlash® Wireless Memory System (LV18/LV30 SCSP; 1024-Mbit LV Family Datasheet* (order number 253854) for flash details not included in this document.

Table 8. SRAM AC Read Specifications

#	Symbol	Parameter	MIN	MAX	Unit	Notes
R1	t_{RC}	Read Cycle Time	70	–	ns	
R2	t_{AA}	Address to Output Delay	–	70	ns	
R3	t_{CO1}	S-CS1# to Output Delay	–	70	ns	
R3	t_{CO2}	S-CS2 to Output Delay	–	70	ns	
R4	t_{OE}	R-OE# to Output Delay	–	35	ns	
R5	t_{BA}	R-UB#, R-LB# to Output Delay	–	70	ns	
R6	t_{LZ}	S-CS1# or S-CS2 to Output in Low-Z	5	–	ns	1,2
R7	t_{OLZ}	R-OE# to Output in Low-Z	0	–	ns	1
R8	t_{HZ}	S-CS1# or S-CS2 to Output in High-Z	0	25	ns	1,2,3
R9	t_{OHZ}	R-OE# to Output in High-Z	0	25	ns	1,3
R10	t_{OH}	Output Hold (from Address, S-CS1#, S-CS2, or R-OE# Change, whichever Occurs First)	0	–	ns	
R11	t_{BLZ}	R-UB#, R-LB# to Output in Low-Z	0	–	ns	1
R12	t_{BHZ}	R-UB#, R-LB# to Output in High-Z	0	25	ns	1

NOTES:
1. Sampled, not 100% tested.
2. At any given temperature and voltage condition, t_{HZ} (MAX) is less than t_{LZ} (MAX) for a given device and from device-to-device interconnection.
3. Timings of t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.

Figure 9. SRAM Read Waveform



7.4 SRAM AC Write Specifications

Table 9. SRAM AC Write Specifications (Sheet 1 of 2)

#	Symbol	Parameter	MIN	MAX	Unit	Notes
W1	t_{WC}	Write Cycle Time	70	–	ns	1
W2	t_{AS}	Address Setup to R-WE# (S-CS1#) and R-UB#,R-LB# Going Low	0	–	ns	3
W3	t_{WP}	R-WE# (S-CS1#) Pulse Width	55	–	ns	1
W4	t_{DW}	Data to Write Time Overlap	30	–	ns	
W5	t_{AW}	Address Setup to R-WE# (S-CS1#) Going High	60	–	ns	
W6	t_{CW}	S-CS1# (R-WE#) Setup to R-WE# (S-CS1#) Going High	60	–	ns	2
W7	t_{DH}	Data Hold from R-WE# (S-CS1#) High	0	–	ns	

Table 9. SRAM AC Write Specifications (Sheet 2 of 2)

W8	t_{WR}	Write Recovery	0	–	ns	4
W9	t_{BW}	R-UB#, R-LB# Setup to R-WE# (S-CS1#) Going High	60	–	ns	

NOTES:
1. A write occurs during the S-CS1# and R-WE# asserted overlap (t_{WP}). The write begins with the latest transition of S-CS1# and R-WE# going low (R-UB# and/or R-LB# already asserted). The write ends at the earliest transition of S-CS1# or R-WE# going high.
2. t_{CW} is measured from S-CS1# going low to the end of a write.
3. t_{AS} is measured from address valid to the beginning of a write.
4. t_{WR} is measured from the end of a write to the address change; t_{WR} applied in case a write ends as S-CS1# or R-WE# going high.

Figure 10. SRAM Write Waveform

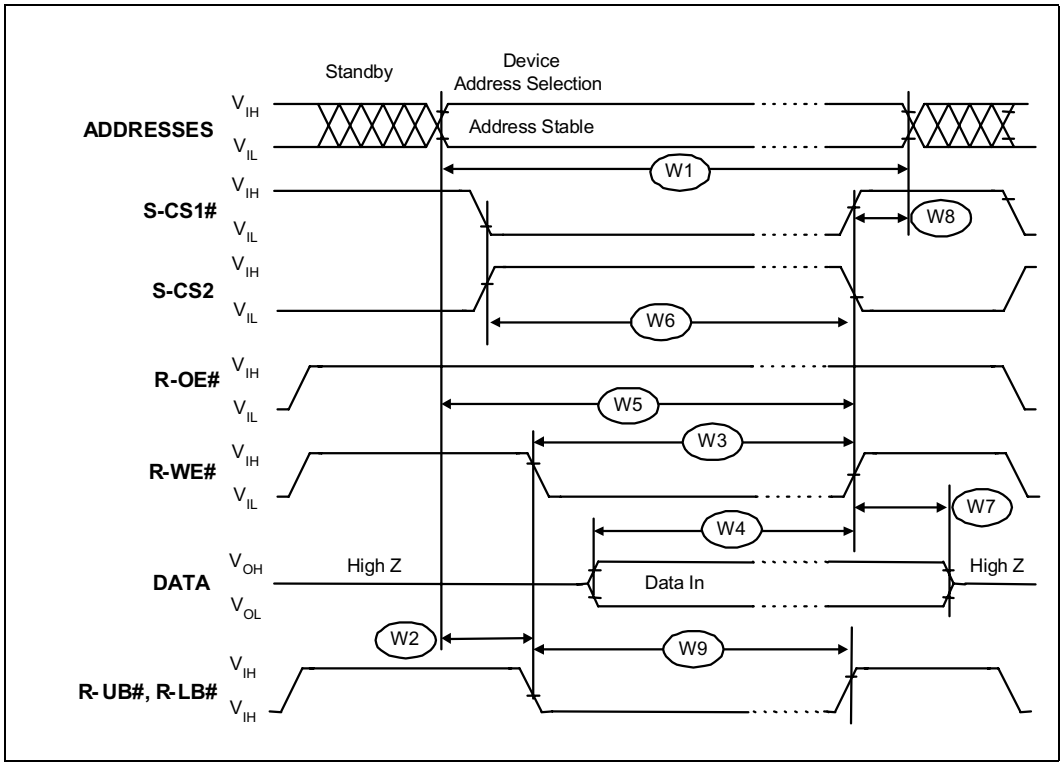


Table 10. SRAM Data Retention Timing

Parameter	Description	MIN	MAX	Unit
t_{SDR}	Data Retention Set-up Time	0	–	ns
t_{RDR}	Data Retention Recovery Time	70	–	ns

Figure 11. SRAM Data Retention Waveform (S-CS1# Controlled)

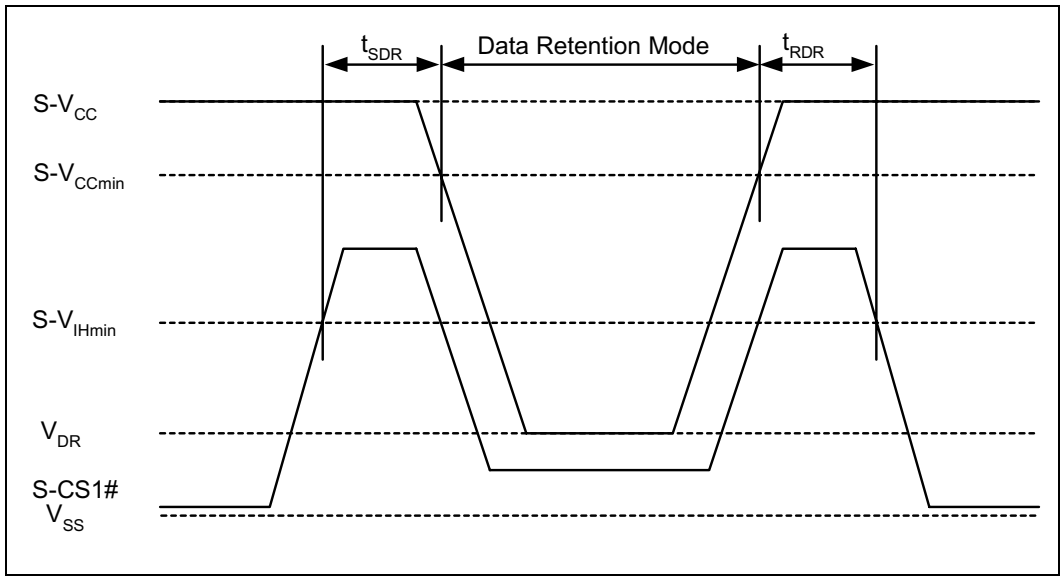
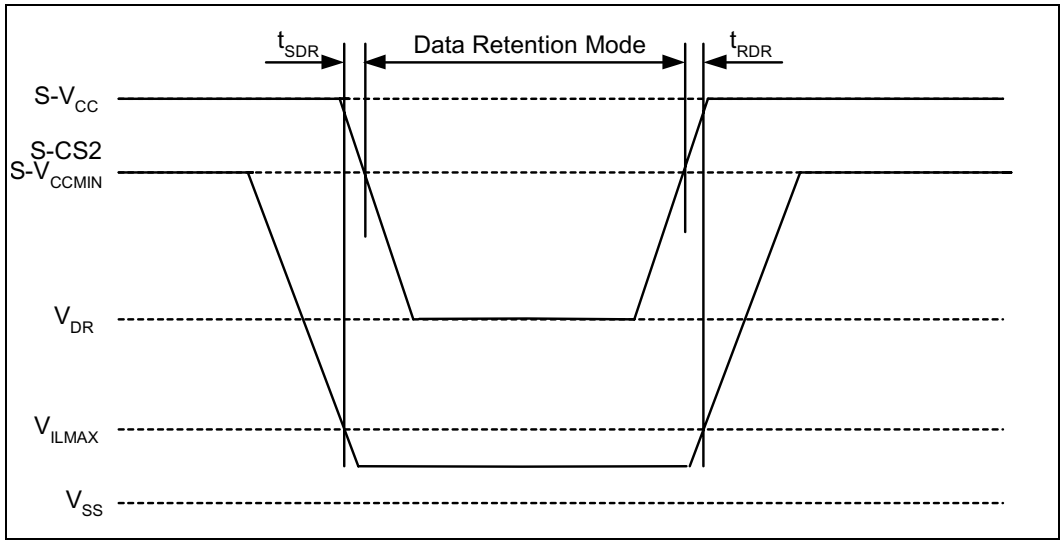


Figure 12. SRAM Data Retention Waveform (S-CS2 Controlled)



7.5 PSRAM AC Read Specifications

Table 11. PSRAM AC Read Specifications

#	Symbol	Parameter	P-V_{CC} = 1.80 V to 1.95 V		P-V_{CC} = 2.7 V to 3.1 V		Unit	Note
			MIN	MAX	MIN	MAX		
Read Cycle								
R1	t_{RC}	Read Cycle Time	85*	–	65	–	ns	5
R2	t_{AA}	Address access time	–	85*	–	65	ns	5
R3	t_{CO}	P-CS# Low to Output Valid	–	85*	–	65	ns	5
R4	t_{OE}	R-OE# Low to Output Valid	–	65	–	45	ns	
R5	t_{BA}	R-UB#, R-LB# Low to Output Valid	–	85*	–	65	ns	5
R6	t_{LZ}	P-CS# Low to Output in Low-Z	10	–	10	–	ns	
R7	t_{OLZ}	R-OE# Low to Output in Low-Z	5	–	5	–	ns	
R8	t_{HZ}	P-CS# High to Output in High-Z	–	25	–	25	ns	
R9	t_{OHZ}	R-OE# High to Output in High-Z	–	25	–	25	ns	
R10	t_{OH}	Output Hold from Address change	5	–	5	–	ns	
R11	t_{BLZ}	R-UB#, R-LB# Low to Output in Low-Z	5	–	5	–	ns	
R12	t_{BHZ}	R-UB#, R-LB# High to Output in High-Z	–	25	–	25	ns	
R13	t_{ASO}	Address set to R-OE# low-level	0	–	0	–	ns	1
R14	t_{OHAH}	R-OE# high-level to address hold	-5	–	-5	–	ns	
R15	t_{CHAH}	P-CS# high-level to address hold	0	–	0	–	ns	1
R16	t_{BHAH}	R-LB#, R-UB# high-level to address hold	0	–	0	–	ns	1,2
R17	t_{CLOL}	P-CS# low-level to R-OE# low-level	0	10,000	0	10,000	ns	3
R18	t_{OLCH}	R-OE# low-level to P-CS# high-level	60	–	45	–	ns	
R19	t_{CP}	P-CS# high-level pulse width	10	–	10	–	ns	
R20	t_{BP}	R-UB#, R-LB# high-level pulse width	10	–	10	–	ns	
R21	t_{OP}	R-OE# high-level pulse width	–	10,000	–	10,000	ns	3
Page Mode								
PR1	t_{PC}	Page Cycle Time	30	–	18	–	ns	4
PR2	t_{PA}	Page Mode Address Access Time	–	30	–	18	ns	

NOTES:
1. When R13 ≥ |R15|, |R16| and R19 ≥ 18 ns, the minimum value for R15 and R16 are -15 ns. (See also Figure 13, "Conditions for Calculating the Minimum Value for R15 and R16" on page 31.)
2. R16 is specified from when both R-LB# and R-UB# become high-level.
3. R17and R21 (MAX) are applied while P-CS# is being hold at low-level.
4. See Figure 14, "AC Waveform for PSRAM Read Operations" on page 31.
5. * 32-Mbit 1.8V PSRAM initial read access timing specifications changed from 85 ns to 88 ns.

Figure 13. Conditions for Calculating the Minimum Value for R15 and R16

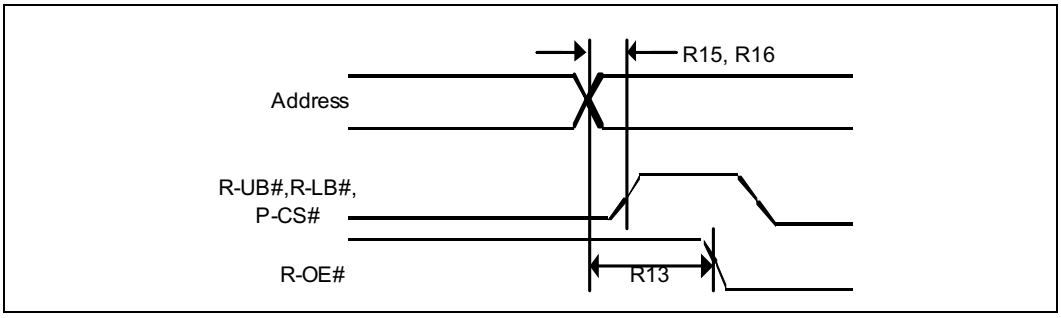
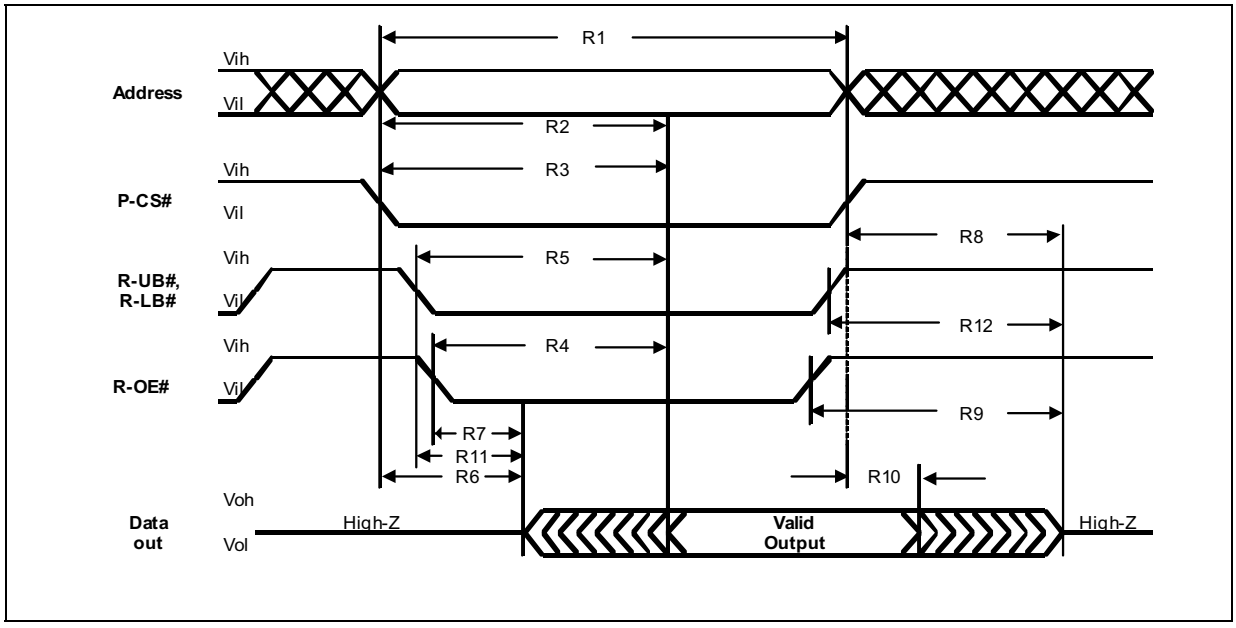
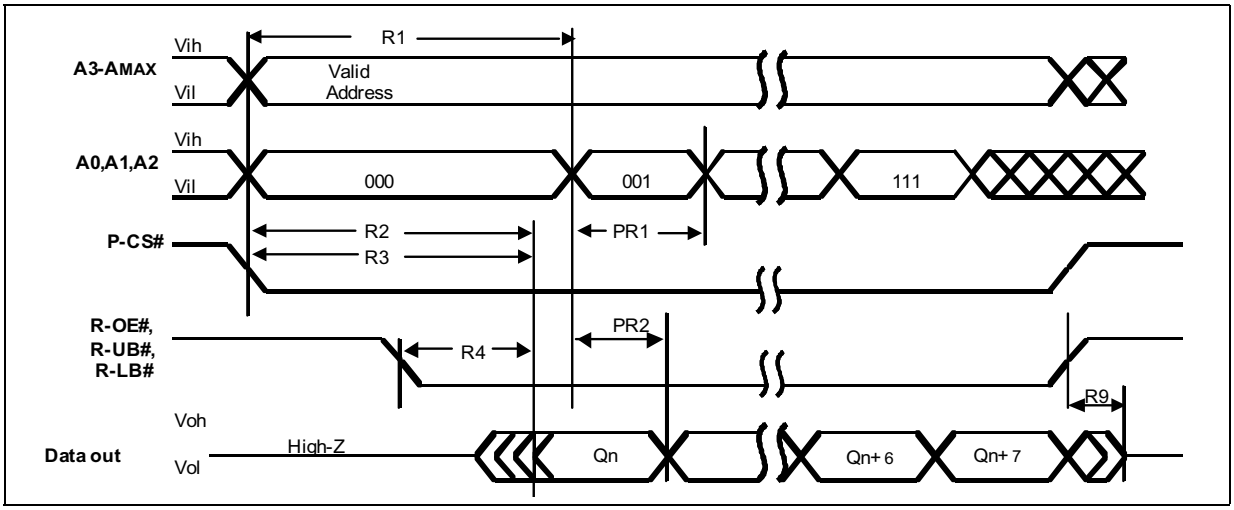


Figure 14. AC Waveform for PSRAM Read Operations



NOTE: In a read cycle, P-Mode and R-WE# should be fixed to high-level.

Figure 15. AC Waveform for PSRAM 8-Word Page Read Operation



NOTE: In a page read cycle, P-Mode and R-WE# should be fixed to high-level, and R-UB#, R-LB# are low-level.

7.6 PSRAM AC Write Specifications

Table 12. PSRAM AC Write Specifications

#	Symbol	Parameter	P-V_{CC} = 1.80 V to 1.95 V		P-V_{CC} = 2.7 V to 3.1 V		Unit	Note
			MIN	MAX	MIN	MAX		
W1	t_{WC}	Write Cycle Time	85	–	65	–	ns	4
W2	t_{AS}	Address Setup Time	0	–	0	–	ns	1,4
W3	t_{WP}	Write Pulse Width	60	–	50	–	ns	4
W4	t_{DW}	Data valid to Write End	30	–	35	–	ns	4
W5	t_{AW}	Address valid to end of write	70	–	55	–	ns	4
W6	t_{CW}	P-CS# to end of write	70	–	55	–	ns	4
W7	t_{DH}	Data Hold time	0	–	0	–	ns	4
W8	t_{WR}	Write Recovery	0	–	0	–	ns	4
W9	t_{BW}	R-UB#, R-LB# Setup to end of Write	70	–	55	–	ns	4
W10	t_{CP}	P-CS# high-level pulse width	10	–	10	–	ns	1
W11	t_{BP}	R-UB#, R-LB# high-level pulse width	10	–	10	–	ns	
W12	t_{WHP}	R-WE# high-level pulse width	10	–	10	–	ns	
W13	t_{OHAH}	R-OE# high-level to address hold	-5	–	-5	–	ns	
W14	t_{CHAH}	P-CS# high-level to address hold	0	–	0	–	ns	1
W15	t_{BHAH}	R-UB#, R-LB# high-level to address hold	0	–	0	–	ns	1,2
W16	t_{OES}	R-OE# high-level to R-WE# set	0	10,000	0	10,000	ns	3
W17	t_{OEH}	R-WE# high-level to R-OE# set	10	10,000	10	10,000	ns	

NOTES:
1. When W2 ≥ |W14|, |W15| and W10 ≥ 18 ns, W14 and W15 (MIN) are -15 ns. (See also Figure 16, “Conditions for Calculating the Minimum Value for W14 and W15” on page 33.)
2. W15 is specified from when both R-LB# and R-UB# become high-level.
3. W16 and W17 (MAX) are applied while P-CS# is being hold at low-level.
4. See Figure 17, “AC Waveform for PSRAM Write Operation” on page 33.

Figure 16. Conditions for Calculating the Minimum Value for W14 and W15

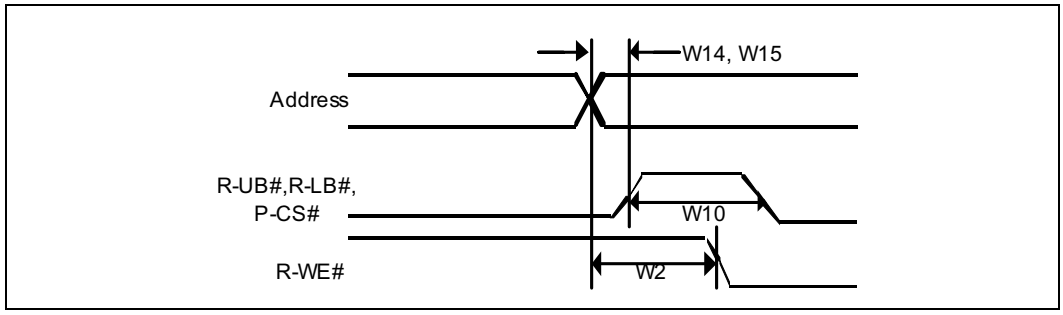
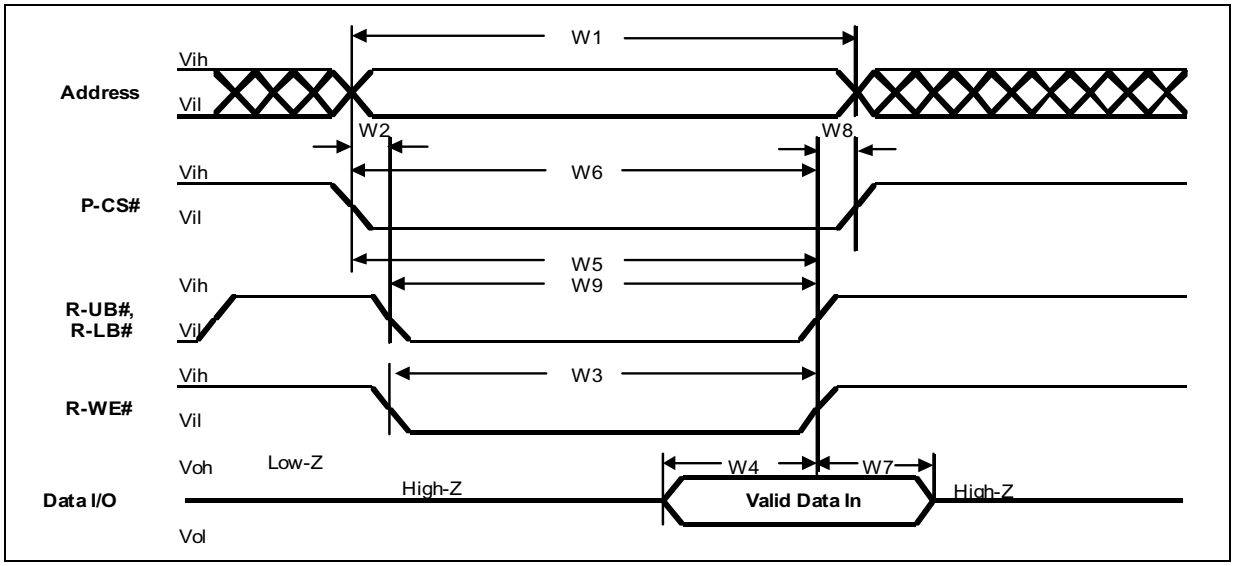


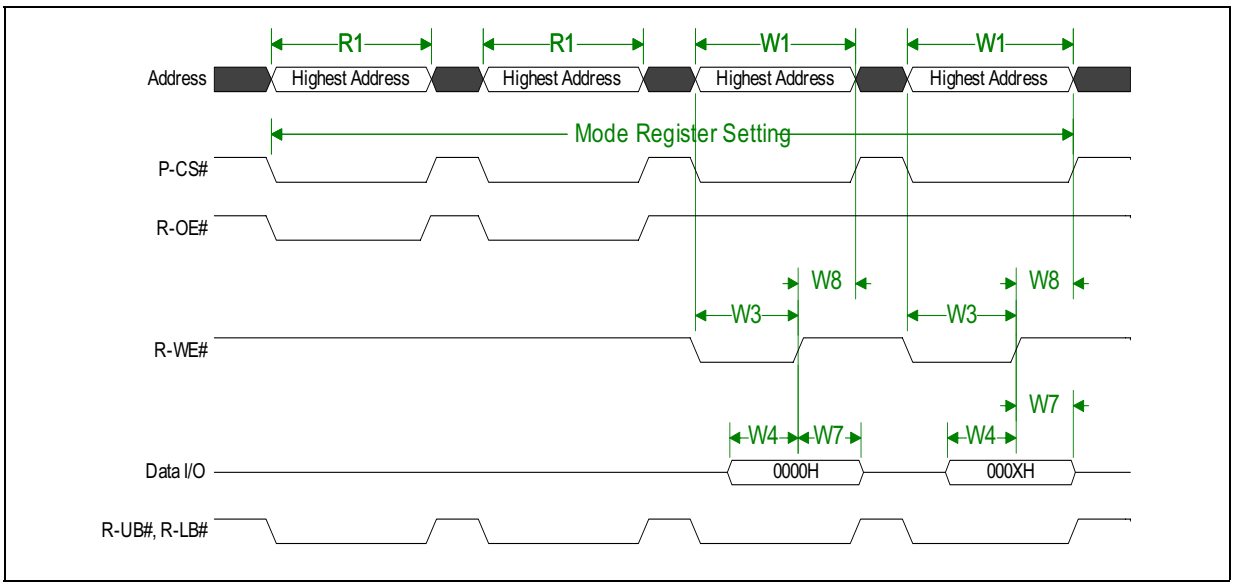
Figure 17. AC Waveform for PSRAM Write Operation



NOTES:

1. During address transition, at least one of the pins P-CS#, R-WE#, or both of R-UB# and R-LB# pins should be deasserted.
2. Do not input data to the I/O pins while they are in an output state.
3. In a write cycle, P-Mode and R-OE# should be fixed to high-level.
4. Write operation is done during the overlap time of a low-level P-CS#, R-WE#, R-LB# and/or R-UB#.

Figure 18. PSRAM Mode Register Update—Timing Waveform



8.0 Power and Reset Specifications

Refer to the latest revision of the *Intel StrataFlash® Wireless Memory System (LV18/LV30 SCSP; 1024-Mbit LV Family Datasheet* (order number 253854) for details not included in this document.

9.0 Design Guide: Operation Overview

9.1 Bus Operations

With F-CE# low and F-RST# high, the flash dies are enabled for normal operations. The flash device internally decodes upper address inputs to determine the accessed partition or block.

In an asynchronous read operation, addresses are latched when ADV# transition from V_{IL} to V_{IH}, or continuously flows through if ADV# is held low. In synchronous-burst mode, addresses are latched by the rising edge of ADV# or the next valid CLK edge when ADV# is low.

Table 13, "Flash + PSRAM + SRAM Bus Operations" summarizes the bus operations and voltage levels that must be applied to individual flash die in each mode

Note: Each flash die within the 768-Mbit LVQ Family with Asynchronous Static RAM device shares basic asynchronous read and write operations unless otherwise specified.

Table 13. Flash + PSRAM + SRAM Bus Operations (Sheet 1 of 2)

Device	Mode	F-RST#	F1-CE#	F2-CE#	F-OE#	F-WE#	WAIT	ADV#	F-VPP	S-CS1#	S-CS2	P-Mode	P-CS#	R-OE#	R-WE#	R-UB#, R-LB#	D[15:0]	Notes
FlashDie #1 (code)	Synchronous Array and Non-Array Read	H	L	H	L	H	Active	L	X	H	X	X	H	X	X	X	Flash D_{OUT}	1,2,3,4,5,6,9
	Asynchronous Read	H	L	H	L	H	Deasserted	L	X	H	X	X	H	X	X	X	Flash D_{OUT}	1,2,3,4,5,6,9
	Write	H	L	H	H	L	Deasserted	L	V_{PP1} or V_{PP2}	H	X	X	H	X	X	X	Flash D_{IN}	3,4,6
	Output Disable	H	L	H	H	H	High-Z	X	High-Z	Any xSRAM mode allowed							Flash High-Z	4
	Standby	H	H	H	X	X	High-Z	X	High-Z								Flash High-Z	4
	Reset	L	X	X	X	X	High-Z	X	High-Z								Flash High-Z	4
Flash Die #2 (data)	Synchronous Array and Non-Array Read	H	H	L	L	H	Deasserted	L	X	H	X	X	H	X	X	X	Flash Die #2 DOUT	1,2,3,4,5,6,9
	Async Read	H	H	L	L	H	Deasserted	L	X	H	X	X	H	X	X	X	Flash Die #2 DOUT	1,2,3,4,5,6,9
	Write	H	H	L	H	L	Deasserted	L	Vpp1 or Vpp2	H	X	X	H	X	X	X	Flash Die #2 DOUT	3,4,6
	Output Disable	H	H	L	H	H	High-Z	X	High-Z	Any xSRAM mode allowed							Flash# 2 High-Z	4
	Standby	H	H	H	X	X	High-Z	X	High-Z								Flash #2 High-Z	4
	Reset	L	X	X	X	X	High-Z	X	High-Z								Flash #2 High-Z	4

Table 13. Flash + PSRAM + SRAM Bus Operations (Sheet 2 of 2)

Device	Mode	F-RST#	F1-CE#	F2-CE#	F-OE#	F-WE#	WAIT	ADV#	F-VPP	S-CS1#	S-CS2	P-Mode	P-CS#	R-OE#	R-WE#	R-UB#, R-LB#	D[15:0]	Notes
PSRAM (#1 or #2)	Read	X	H	L	X	X	High-Z	X	X	H	H	H	L	L	H	L	PSRAM D_{OUT}	1,3
	Write	X	H	L	X	X	High-Z	X	X	H	H	H	L	H	L	L	PSRAM D_{IN}	3
	Output Disable	Any Flash or SRAM mode allowed								H	H	H	L	H	H	X	PSRAM High-Z	4
	Standby									H	H	H	H	X	X	X	PSRAM High-Z	4
	Low-Power Mode									H	H	L	X	X	X	X	PSRAM High-Z	4
SRAM Enabled	Read	X			X	X	High-Z	X	X	L	H	X	H	L	H	L	SRAM D_{OUT}	1,3,8
	Write	X			X	X	High-Z	X	X	L	H	X	H	H	L	L	SRAM D_{IN}	3,8
	Output Disable	Any Flash or PSRAM mode allowed								L	H	X	H	H	H	X	SRAM High-Z	3,8
	Standby									H	H	X	H	X	X	X	SRAM High-Z	4,8
	Data Retention									Same as SRAM Standby							SRAM High-Z	7,8

NOTES:
1. WAIT is active during sync burst read when F-CE# and OE# are asserted. WAIT is High-Z if F-CE# or OE# is deasserted.
2. FX-CE# is F1-CE# for Flash #1, F2-CE# for Flash #2, and F3-CE# for Flash #3. FX-OE# is F1-OE# for Flash #1, and F2-OE# for Flash #2.
3. For Flash, FX-OE# and F-WE# should never be asserted simultaneously. For PSRAM or SRAM, R-OE# and R-WE# should never be asserted simultaneously.
4. X can be V_{IL} or V_{IH} for inputs and V_{PP1}, V_{PP2}, V_{PPLK} or V_{PPH} for F-Vpp.
5. Flash CFI query and status register accesses use D[7:0] only, all other reads use D[15:0].
6. Refer to Intel Strataflash® Wireless Memory System Datasheet for valid D_{IN} during flash writes.
7. The SRAM can be placed into data retention mode by lowering S-VCC to the V_{DR} limit when in standby mode.
8. P-Mode is high if PSRAM is in Standby. P-Mode is low if PSRAM is in Low-Power Mode. Please see Section 18.0, "PSRAM Operations" on page 45 for more details on Standby and Low-Power Mode.
9. Data segment flash only operates in asynchronous mode, CLK is ignored and WAIT is deasserted.

9.2 Flash Device Commands and Command Definitions

Refer to the *Intel StrataFlash® Wireless Memory System (LV18/LV30 SCSP), 1024-Mbit LV Family Datasheet* (order number 253854) for complete descriptions of flash modes and commands, for command bus-cycle definitions, and for flowcharts that illustrate operational routines.

Note: Each flash die within the 768-Mbit LVQ Family with Asynchronous Static RAM device shares basic asynchronous read and write operations unless otherwise specified.

10.0 Flash Read Operation

Refer to the latest revision of the *Intel StrataFlash® Wireless Memory System (LV18/LV30 SCSP; 1024-Mbit LV Family Datasheet* (order number 253854) for details not included in this document.

11.0 Flash Program Operation

Refer to the latest revision of the *Intel StrataFlash® Wireless Memory System (LV18/LV30 SCSP; 1024-Mbit LV Family Datasheet* (order number 253854) for details not included in this document.

12.0 Flash Erase Operation

Refer to the latest revision of the *Intel StrataFlash® Wireless Memory System (LV18/LV30 SCSP; 1024-Mbit LV Family Datasheet* (order number 253854) for details not included in this document.

13.0 Flash Suspend and Resume Operations

Refer to the latest revision of the *Intel StrataFlash® Wireless Memory System (LV18/LV30 SCSP; 1024-Mbit LV Family Datasheet* (order number 253854) for details not included in this document.

14.0 Flash Block Locking and Unlocking Operations

Refer to the latest revision of the *Intel StrataFlash® Wireless Memory System (LV18/LV30 SCSP; 1024-Mbit LV Family Datasheet* (order number 253854) for details not included in this document.

15.0 Flash Protection Register Operation

Refer to the latest revision of the *Intel StrataFlash® Wireless Memory System (LV18/LV30 SCSP; 1024-Mbit LV Family Datasheet* (order number 253854) for details not included in this document.

16.0 Flash Configuration Operation

Refer to the latest revision of the *Intel StrataFlash® Wireless Memory System (LV18/LV30 SCSP; 1024-Mbit LV Family Datasheet* (order number 253854) for details not included in this document.

17.0 Dual Operation Considerations

17.1 Product Configurations and Memory Partitioning

By default, the first flash die is the first code segment flash die, a fast, eXecute-In-Place (XIP) solution ideal for an instruction fetch application. This portion is the user-selected parameter configuration option, made up of either a 128-Mbit flash die or a 256-Mbit flash die, each containing one parameter partition and several main partitions. The parameter partition contains four 16-KWord parameter blocks and seven 64-KWord main blocks; all main partitions consist of eight 64-KWord main blocks.

The large, embedded data segment is a single partition asynchronous page-mode read device that can be made up of multiple dies with densities of 128-Mbit or 256-Mbit. The single partition is made up of four 16-Kword parameter blocks and 64-Kword main blocks. The data segment flash die parameter configuration will always be the opposite of the code segment flash die parameter configuration. See Table 14 on page 39 for examples of configuration options.

The code and embedded data portions of the LVQ device are both asymmetrical in blocking. Each memory block features zero-latency block locking. Data integrity is protected even further with the optional use of F-VPP and F-WP# to implement block lock down.

The user has the choice of selecting either a top or a bottom parameter partition configuration for the code segment flash die. Depending on the choice of configuration, the data segment flash die in the LVQ device will be parametrically opposed. For instance, if the user selects top parameter configuration for the code segment flash die, the data segment flash die in the package will be configured as bottom parameter configuration, and vice-versa. This ensures the largest number of contiguous main block addresses for software efficiency.

The xRAM segment can consist of up to two Pseudo-SRAM (PSRAM) dies and one SRAM die with the following possible densities:

- The first PSRAM die can have a density of 64-Mbit or 128-Mbit.
- The second PSRAM die can have a density of 64-Mbit or 32-Mbit.
- The SRAM die has a density of 8-Mbit.

For the code segment, the 128-Mbit flash die has an 8-Mbit partition block and the 256-Mbit flash die has a 16-Mbit partition block. The minimum code + data density combination for the LV18/ LV30 family is 384 Mbit.

Figure 19. Top and Bottom Parameter Configurations

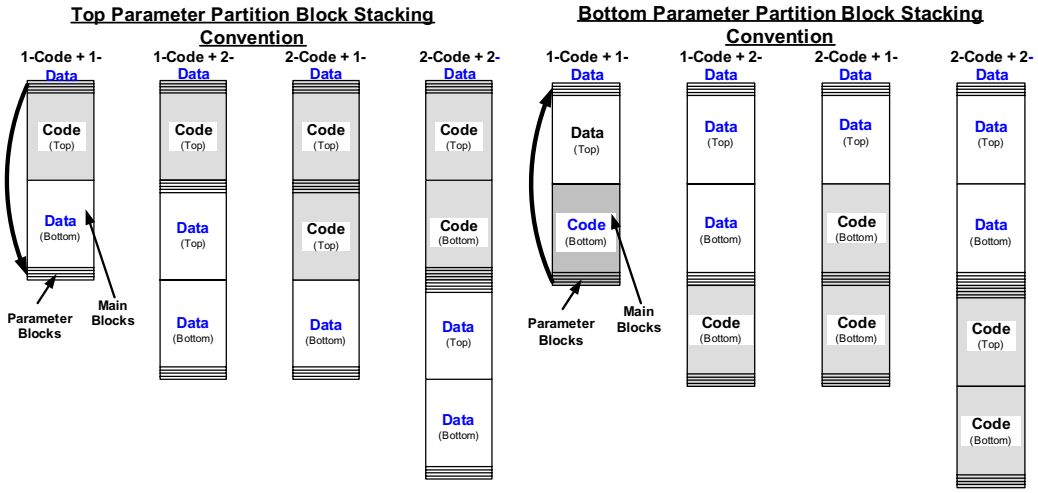


Table 14. LVQ die stacked configuration example (Top / Bottom Parameter)

Stacked Configuration Example (Top Parameter)			
Die Stack Configuration	**Flash die#1 (user selected)**	**Flash die #2**	**Flash die #3**
Code only	Top	NA	NA
Code+Data	Top	Bottom	NA
Code+Data+Data	Top	Top	Bottom
Code+Code+Data	Top	Top	Bottom
Stacked Configuration Example (Bottom Parameter)			
Die Stack Configuration	**Flash die#1 (user selected)**	**Flash die #2**	**Flash die #3**
Code	Bottom	NA	NA
Code+Data	Bottom	Top	NA
Code+Data+Data	Bottom	Bottom	Top
Code+Code+Data	Bottom	Bottom	Top

17.2 Product Segment Unique Features

The code segment of the 768-Mbit LVQ Family with Asynchronous Static RAM device includes the following enhanced features unless specifically noted otherwise:

- 64 unique (Intel pre-programmed) identifier bits and 2,112 user-programmable OTP bits for each code segment flash die.

- Traditional write, erase, and burst-mode read capabilities of Intel® Wireless flash memory.
- Simultaneous RWW/RWE operations, enabling a burst read operation in one partition while simultaneous with program or erase operations in other partitions.
- Burst-read across partition boundaries, but not across segment dies within the subsystem.

Note: User application code is responsible for ensuring that burst-mode reads do not cross into a partition that is in program or erase mode.

The embedded data segment includes the following features unless specifically noted otherwise:

- High Density offerings of up to 512 Mb designated specifically for large embedded data.
- Single partition asynchronous page-mode read operation, allowing for a cost-effective ideal storage format.
- Read-while-program or read-while-erase operations can be accomplished with software through program suspend and erase suspend operations.

17.3 Flash Die Memory Map

The 768-Mbit LVQ Family with Asynchronous Static RAM device is available in several density and parameter configurations. The memory map is based on the stacking of individual flash die density options of 128 Mbit or 256 Mbit. The memory map shows individual flash die configurations and block/partition allocations.

The code segment flash die is made up of 128-Mbit dies or 256-Mbit dies, each containing one parameter partition and several main partitions.

The 128-Mbit memory array is divided into sixteen 8-Mbit partitions. Each die density contains one parameter partition and fifteen main partitions. The 8-Mbit top or bottom parameter partition contains four 16-Kword blocks and seven 64-Kword blocks. Each of the remaining fifteen 8-Mbit main partitions contains eight 64-Kword blocks.

The 256-Mbit memory array is divided into sixteen 16-Mbit partitions. Each device contains one parameter partition and fifteen main partitions. The 16-Mbit top or bottom parameter partition contains four 16-Kword blocks and fifteen 64-Kword blocks. Each of the remaining fifteen 16-Mbit main partitions contains sixteen 64-Kword blocks.

The data segment flash die density is made up of 128-Mbit dies or 256-Mbit dies, each containing a single partition architecture made up of four 16-Kword parameter blocks and 64-Kword main blocks. The memory map and partitioning for various flash die combinations, top and bottom parameters and are shown in the following tables:

Note: Only 128-Mbit and 256-Mbit flash die densities are used in three flash die SCSP combinations.

- Table 17, “Three Flash Dies (Top Parameter) SCSP Memory Map” on page 43
- Table 15, “Two Flash Dies (Top Parameter) SCSP Memory Map” on page 41
- Table 16, “Two Flash Dies (Bottom Parameter) SCSP Memory Map” on page 42
- Table 18, “Three Flash Dies (Bottom Parameter) SCSP Memory Map” on page 44

Table 15. Two Flash Dies (Top Parameter) SCSP Memory Map

Flash Die#	Die Stack Configuration	Partitioning	Block Size (KW)	Partition Size (Mbit)	128-Mbit Flash		Partition Size (Mbit)	256-Mbit Flash	
					Blk#	Address Range		Blk#	Address Range
1	**Code (Top Parameter)**	Parameter Partition (Partition 0)	16	8	130	7FC000-7FFFFF	16	258	FFC000-FFFFFF
			⋮		⋮	⋮		⋮	⋮
			16		127	7F0000-7F3FFF		255	FF0000-FF3FFF
			64		126	7E0000-7EFFFF		254	FE0000-FEFFFF
			⋮		⋮	⋮		⋮	⋮
			64		120	780000-78FFFF		240	F00000-FFFFFF
		Main Partitions (Partition 1 to 7)	64		119	770000-77FFFF		239	EF0000-EFFFFF
			⋮		⋮	⋮			⋮
			64		64	400000-4FFFFF		128	800000-80FFFF
		Main Partitions (Partition 8 to 15)	64		63	3F0000-3FFFFF		127	F70000-F7FFFF
			⋮		⋮	⋮		⋮	⋮
			64		0	000000-00FFFF		0	000000-00FFFF
2	**Data (Bottom Parameter)**	Single Partition 4 x 16-Kword Parameter Blocks 127 x 64-Kword Main Blocks (128-Mb) 255 x 64-Kword Main Blocks (256-Mb	64		130	7F0000-7FFFFF		258	FF0000-FFFFFF
			...		⋮	⋮		⋮	⋮
			64		67	400000-40FFFF		131	100000-10FFFF
			64		66	3F0000-3FFFFF		130	7F0000-7FFFFF
			⋮		⋮	⋮		⋮	⋮
			64		11	080000-08FFFF		11	080000-08FFFF
			64		10	070000-07FFFF		10	070000-07FFFF
			⋮		⋮	⋮		⋮	⋮
			64		4	010000-01FFFF		4	010000-01FFFF
			16		3	00C000-00FFFF		3	00C000-00FFFF
			⋮		⋮	⋮		⋮	⋮
			16		0	000000-003FFF		0	000000-003FFF

Table 16. Two Flash Dies (Bottom Parameter) SCSP Memory Map

Flash Die#	Die Stack Configuration	Partitioning	Block Size (KW)	Partition Size (Mbit)	128-Mbit Flash		Partition Size (Mbit)	256-Mbit Flash	
					Blk#	Address Range		Blk#	Address Range
1	Data (Top Parameter)	Single Partition 4 x 16-Kword Parameter Blocks 127 x 64-Kword Main Blocks (128-Mb) 255 x 64-Kword Main Blocks (256-Mb	16		130	7F0000-7FFFFF		258	FF0000-FFFFFF
			...		⋮	⋮		⋮	⋮
			16		67	400000-40FFFF		131	100000-10FFFF
			64		66	3F0000-3FFFFF		130	7F0000-7FFFFF
			⋮		⋮	⋮		⋮	⋮
			64		11	080000-08FFFF		11	080000-08FFFF
			64		10	070000-07FFFF		10	070000-07FFFF
			⋮		⋮	⋮		⋮	⋮
			64		4	010000-01FFFF		4	010000-01FFFF
			64		3	00C000-00FFFF		3	00C000-00FFFF
			⋮		⋮	⋮		⋮	⋮
2	Code (Bottom Parameter)	Parameter Partition (Partition 0)	64	8	130	7FC000-7FFFFF	16	258	FFC000-FFFFFF
			...		⋮	⋮		⋮	⋮
			64		127	7F0000-7F3FFF		255	FF0000-FF3FFF
			64		126	7E0000-7EFFFF		254	FE0000-FEFFFF
			⋮		⋮	⋮		⋮	⋮
			64		120	780000-78FFFF		240	F00000-FFFFFF
		Main Partitions (Partition 1 to 7)	64		119	770000-77FFFF		239	EF0000-EFFFFF
			⋮		⋮	⋮			⋮
			64		64	400000-4FFFFF		128	800000-80FFFF
		Main Partitions (Partition 8 to 15)	16		63	3F0000-3FFFFF		127	F70000-F7FFFF
			⋮		⋮	⋮		⋮	⋮
			16		0	000000-00FFFF		0	000000-00FFFF

Table 17. Three Flash Dies (Top Parameter) SCSP Memory Map

Flash Die#	Die Stack Configuration	Partitioning	Block Size (KW)	Partition Size (Mbit)	128-Mbit Flash		Partition Size (Mbit)	256-Mbit Flash	
					Blk#	Address Range		Blk#	Address Range
1	Code (Top Parameter)	Parameter Partition (Partition 0)	16	8	130	7FC000-7FFFFF	16	258	FFC000-FFFFFF
			⋮		⋮	⋮		⋮	⋮
			16		127	7F0000-7F3FFF		255	FF0000-FF3FFF
			64		126	7E0000-7EFFFF		254	FE0000-FEFFFF
			⋮		⋮	⋮		⋮	⋮
			64		120	780000-78FFFF		240	F00000-FFFFFF
		Main Partitions (Partition 1 to 7)	64		119	770000-77FFFF		239	EF0000-EFFFFF
			⋮		⋮	⋮			⋮
			64		64	400000-4FFFFF		128	800000-80FFFF
		Main Partitions (Partition 8 to 15)	64		63	3F0000-3FFFFF		127	F70000-F7FFFF
			⋮		⋮	⋮		⋮	⋮
			64		0	000000-00FFFF		0	000000-00FFFF
2	Code (Top Parameter)	Parameter Partition (Partition 0)	16	8	130	7FC000-7FFFFF	16	258	FFC000-FFFFFF
			⋮		⋮	⋮		⋮	⋮
			16		127	7F0000-7F3FFF		255	FF0000-FF3FFF
			64		126	7E0000-7EFFFF		254	FE0000-FEFFFF
			⋮		⋮	⋮		⋮	⋮
			64		120	780000-78FFFF		240	F00000-FFFFFF
		Main Partitions (Partition 1 to 7)	64		119	770000-77FFFF		239	EF0000-EFFFFF
			⋮		⋮	⋮			⋮
			64		64	400000-4FFFFF		128	800000-80FFFF
		Main Partitions (Partition 8 to 15)	64		63	3F0000-3FFFFF		127	F70000-F7FFFF
			⋮		⋮	⋮		⋮	⋮
			64		0	000000-00FFFF		0	000000-00FFFF
3	Data (Bottom Parameter)	Single Partition 4 x 16-Kword Parameter Blocks 127 x 64-Kword Main Blocks (128-Mb) 255 x 64-Kword Main Blocks (256-Mb)	64		130	7F0000-7FFFFF		258	FF0000-FFFFFF
			...		⋮	⋮		⋮	⋮
			64		67	400000-40FFFF		131	100000-10FFFF
			64		66	3F0000-3FFFFF		130	7F0000-7FFFFF
			⋮		⋮	⋮		⋮	⋮
			64		11	080000-08FFFF		11	080000-08FFFF
			64		10	070000-07FFFF		10	070000-07FFFF
			⋮		⋮	⋮		⋮	⋮
			64		4	010000-01FFFF		4	010000-01FFFF
			16		3	00C000-00FFFF		3	00C000-00FFFF
			⋮		⋮	⋮		⋮	⋮
			16		0	000000-003FFF		0	000000-003FFF

Table 18. Three Flash Dies (Bottom Parameter) SCSP Memory Map

Flash Die#	Die Stack Configuration	Partitioning	Block Size (KW)	Partition Size (Mbit)	128-Mbit Flash		Partition Size (Mbit)	256-Mbit Flash	
					Blk#	Address Range		Blk#	Address Range
1	Data (Top Parameter)	Single Partition 4 x 16-Kword Parameter Blocks 127 x 64-Kword Main Blocks (128-Mb) 255 x 64-Kword Main Blocks (256-Mb)	16		130	7F0000-7FFFFF		258	FF0000-FFFFFF
			⋮		⋮	⋮		⋮	⋮
			16		67	400000-40FFFF		131	100000-10FFFF
			64		66	3F0000-3FFFFF		130	7F0000-7FFFFF
			⋮		⋮	⋮		⋮	⋮
			64		11	080000-08FFFF		11	080000-08FFFF
			64		10	070000-07FFFF		10	070000-07FFFF
			⋮		⋮	⋮		⋮	⋮
			64		4	010000-01FFFF		4	010000-01FFFF
			64		3	00C000-00FFFF		3	00C000-00FFFF
			⋮		⋮	⋮		⋮	⋮
			64		0	000000-003FFF		0	000000-003FFF
2	Code (Bottom Parameter)	Parameter Partition (Partition 0)	64	8	130	7FC000-7FFFFF	16	258	FFC000-FFFFFF
			⋮		⋮	⋮		⋮	⋮
			64		127	7F0000-7F3FFF		255	FF0000-FF3FFF
			64		126	7E0000-7EFFFF		254	FE0000-FEFFFF
			⋮		⋮	⋮		⋮	⋮
			64		120	780000-78FFFF		240	F00000-FFFFFF
		Main Partitions (Partition 1 to 7)	64		119	770000-77FFFF		239	EF0000-EFFFFF
			⋮		⋮	⋮			⋮
			64		64	400000-4FFFFF		128	800000-80FFFF
		Main Partitions (Partition 8 to 15)	16		63	3F0000-3FFFFF		127	F70000-F7FFFF
			⋮		⋮	⋮		⋮	⋮
			16		0	000000-00FFFF		0	000000-00FFFF
3	Code (Bottom Parameter)	Parameter Partition (Partition 0)	64	8	130	7FC000-7FFFFF	16	258	FFC000-FFFFFF
			⋮		⋮	⋮		⋮	⋮
			64		127	7F0000-7F3FFF		255	FF0000-FF3FFF
			64		126	7E0000-7EFFFF		254	FE0000-FEFFFF
			⋮		⋮	⋮		⋮	⋮
			64		120	780000-78FFFF		240	F00000-FFFFFF
		Main Partitions (Partition 1 to 7)	64		119	770000-77FFFF		239	EF0000-EFFFFF
			⋮		⋮	⋮			⋮
			64		64	400000-4FFFFF		128	800000-80FFFF
		Main Partitions (Partition 8 to 15)	16		63	3F0000-3FFFFF		127	F70000-F7FFFF
			⋮		⋮	⋮		⋮	⋮
			16		0	000000-00FFFF		0	000000-00FFFF

18.0 PSRAM Operations

18.1 PSRAM Power-up Sequence and Initialization

The PSRAM functionality and reliability are independent of the power-up slew rate of the core P-V_{CC}. Any power-up slew rate is possible under use conditions.

The following power-up sequence and operation should be used before starting normal operation. The PSRAM power-up sequence is represented in Figure 20. At power-up, hold P-Mode low for the period of t_{VHMH} and transition P-CS# from low to high before transitioning P-Mode to a logical high. P-CS# and P-Mode must be held high for the period of t_{MHCL} before normal PSRAM operation is possible once the power up sequence is complete.

Figure 20. Timing Waveform for PSRAM Power-Up Sequence

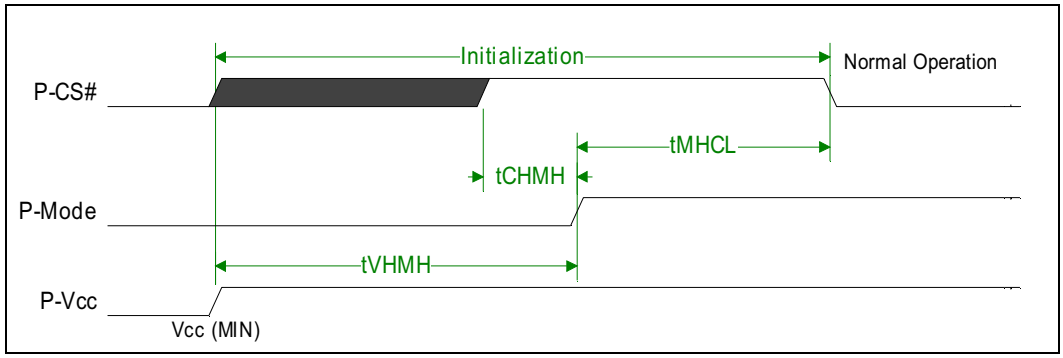


Table 19. PSRAM Initialization Timing

Parameter	Symbol	MIN	MAX	Unit
Power application to P-Mode low-level hold	t_{VHMH}	50	–	µs
P-CS# high-level to P-Mode high-level	t_{CHMH}	0	–	ns
Following power application, P-Mode high-level hold to P-CS# low-level	t_{MHCL}	200	–	µs

18.2 PSRAM Mode Register

The PSRAM die has an internal register that helps control the Low-Power Mode of the PSRAM. This register is called the Mode Register. A fraction of the PSRAM array can be enabled for refresh by setting the Mode Register. Available fixed, partial-refresh fraction densities are 16 Mbit, 8 Mbit, 4 Mbit and 0 Mbit for all density options. Once the refresh density has been set in the Mode Register, these settings are retained until they are set again while applying the power supply. However, the Mode Register setting will become undefined if the power is turned off; therefore, it is important that the Mode Register is set again after power application.

18.2.1 PSRAM Mode Register Setting

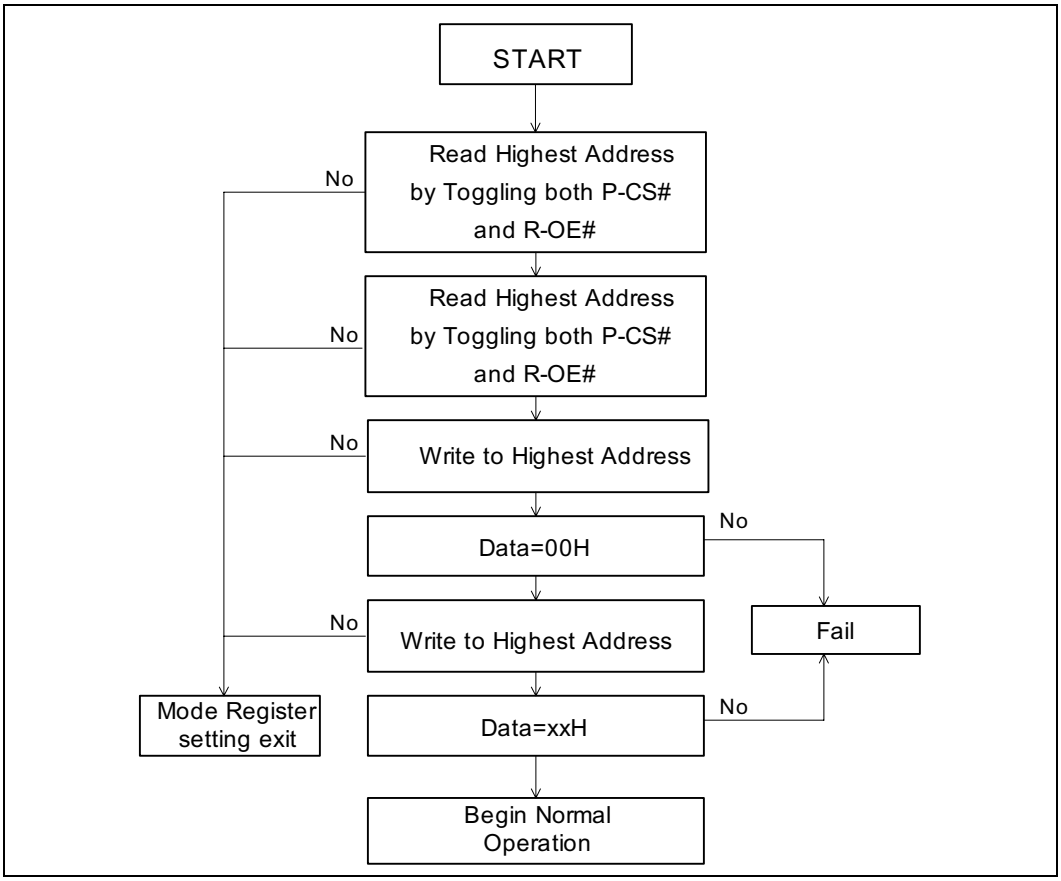
Since the initial value of the PSRAM Mode Register at power application is undefined, the Mode Register must be set after initialization at power application. When setting the density of partial refresh, data is not guaranteed before entering the Low-Power Mode. (This is the same for reset.) However, since Low-Power Mode is not entered unless P-Mode is a logical low, when partial refresh is not used, it is not necessary to set the Mode Register. Also, when using page read without using partial refresh, it is not necessary to set the Mode Register.

The PSRAM Mode Register setting can be entered by successively writing two specific data after two continuous reads of the highest address. The Mode Register setting is a continuous four-cycle operation: two read cycles and two writes cycles. See Table 20 for setting PSRAM Mode Register command sequence. Figure 21, "PSRAM Mode Register Setting Flowchart" on page 47 shows the steps in setting the Mode Register. Figure 18 on page 34 illustrates the timing waveform.

Table 20. Setting PSRAM Mode Register Command Sequence

Command Sequence	1st Bus Cycle (Read Cycle)		2nd Bus Cycle (Read Cycle)		3rd Bus Cycle (Write Cycle)		4th Bus Cycle (Write Cycle)	
Partial refresh density	Address	Data	Address	Data	Address	Data	Address	Data
16-Mbit	Highest Address	–	Highest Address	–	Highest Address	0x00	Highest Address	0x04
8-Mbit	Highest Address	–	Highest Address	–	Highest Address	0x00	Highest Address	0x05
4-Mbit	Highest Address	–	Highest Address	–	Highest Address	0x00	Highest Address	0x06
0-Mbit	Highest Address	–	Highest Address	–	Highest Address	0x00	Highest Address	0x07

Figure 21. PSRAM Mode Register Setting Flowchart



NOTE: xxH=0x04, 0x05, 0x06 or 0x07

18.2.2 Cautions for Setting PSRAM Mode Register

For the PSRAM Mode Register setting, the internal counter status is judged by toggling P-CS# and R-OE#. Therefore, toggle P-CS# at every cycle during entry (read cycle twice, write cycle twice), and toggle R-OE# like P-CS# at the first and second read cycles. If incorrect addresses or data are written, or are written in an incorrect order, the setting of the PSRAM Mode Register will be set incorrectly.

When the highest address is read consecutively three or more times, the Mode Register setting entries are not performed correctly.

Note: Immediately after the highest address is read, the setting of the Mode Register is not performed correctly.

Perform the setting of the Mode Register after power application or after accessing other than the highest address.

Once the refresh density has been set in the Mode Register, the setting is retained until it is reset again while power is continuously applied. However, the Mode Register setting becomes undefined if the power is turned off. The Mode Register must be reset after after any power cycle.

18.3 PSRAM Low-Power Mode

In addition to the regular Standby mode with a full density data hold, Low-Power Mode performs partial density data refresh or zero density data refresh.

The Low-Power Mode allows the user to turn off sections of the PSRAM die to save refresh current. The PSRAM die is divided into four sections allowing certain sections to be refreshed with P-Mode at a logical-low.

In regular Standby mode, both P-CS# and P-Mode are logical-high. But in Low-Power Mode, P-Mode is a logical-low. In Low-Power Mode, if 0-Mbit setting is set as the density, it is necessary to perform initialization the same way as after applying power in order to return to normal operation from Low-Power Mode. Refer to Figure 20, "Timing Waveform for PSRAM Power-Up Sequence" on page 45 for timing charts. When the density has been to set to 16 Mbit, 8 Mbit, or 4 Mbit in Low-Power Mode, it is not necessary to perform initialization to return to normal operation from Low-Power Mode. Refer to Figure 22, "PSRAM Low-Power Mode Entry/Exit (16-, 8-, 4-, 0-Mbit) Waveform" for timing charts.

Figure 22. PSRAM Low-Power Mode Entry/Exit (16-, 8-, 4-, 0-Mbit) Waveform

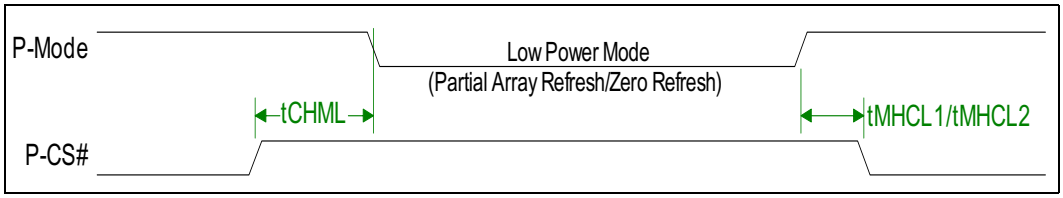


Table 21. PSRAM Low-Power Mode Entry/Exit Timing

Parameter	Description	MIN	MAX	Unit
t_{CHML}	Low-Power Mode entry, P-CS# high-level to P-Mode# low-level	0	–	ns
t_{MHCL1}[1]	Low-Power Mode (16-, 8-, 4-Mbit hold) exit to normal operation, P-Mode high-level to P-CS# low-level	30	–	ns
t_{MHCL2}[2]	Low-Power Mode (0-Mbit data hold) exit to normal operation, P-Mode high-level to P-CS# low-level	200	–	µs

NOTES:
1. t_{MHCL1} is the time it takes to return to normal operation from Low-Power Mode (data hold: 16-, 8-, 4-Mbit).
2. t_{MHCL2} is the time it takes to return to normal operation from Low-Power Mode (0-Mbit data hold).

Appendix A Write State Machine

Refer to the latest revision of the *Intel StrataFlash® Wireless Memory System (LV18/LV30 SCSP; 1024-Mbit LV Family Datasheet* (order number 253854) for details not included in this document.

Appendix B Common Flash Interface

Refer to the latest revision of the *Intel StrataFlash® Wireless Memory System (LV18/LV30 SCSP; 1024-Mbit LV Family Datasheet* (order number 253854) for details not included in this document.

Appendix C Flash Flowcharts

Refer to the latest revision of the *Intel StrataFlash® Wireless Memory System (LV18/LV30 SCSP; 1024-Mbit LV Family Datasheet* (order number 253854) for details not included in this document.

Appendix D Additional Information

Order Number	Document
253853	*Intel StrataFlash® Wireless Memory System (LV 18/30 SCSP); 1024-Mbit LVX Family Datasheet*
253854	*Intel StrataFlash® Wireless Memory System (LV 18/30 SCSP); 1024-Mbit LV Family Datasheet*

NOTES:
1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. For the most current information on Intel® Flash memory products, software and tools, visit our website at http://developer.intel.com/design/flash.

Appendix E Ordering Information

Figure 23 shows the decoder for the flash-only combinations in the 768-Mbit LVQ Family with Asynchronous Static RAM device. Figure 24 shows the decoder for the flash + RAM combinations in the 768-Mbit LVQ Family with Asynchronous Static RAM device.

Figure 23. Decoder for Flash-only Combinations

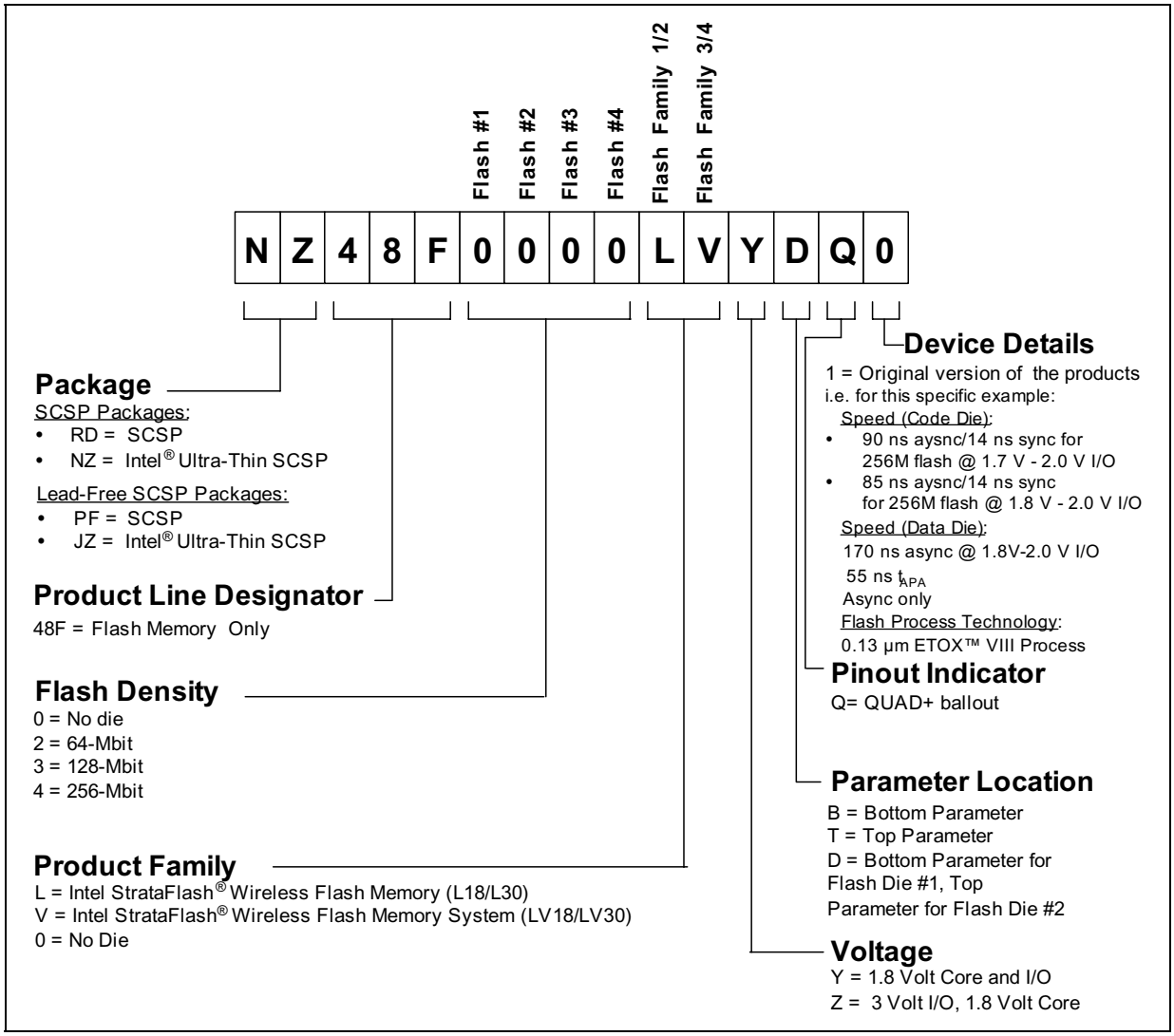


Figure 24. Decoder for Flash + PSRAM Combinations

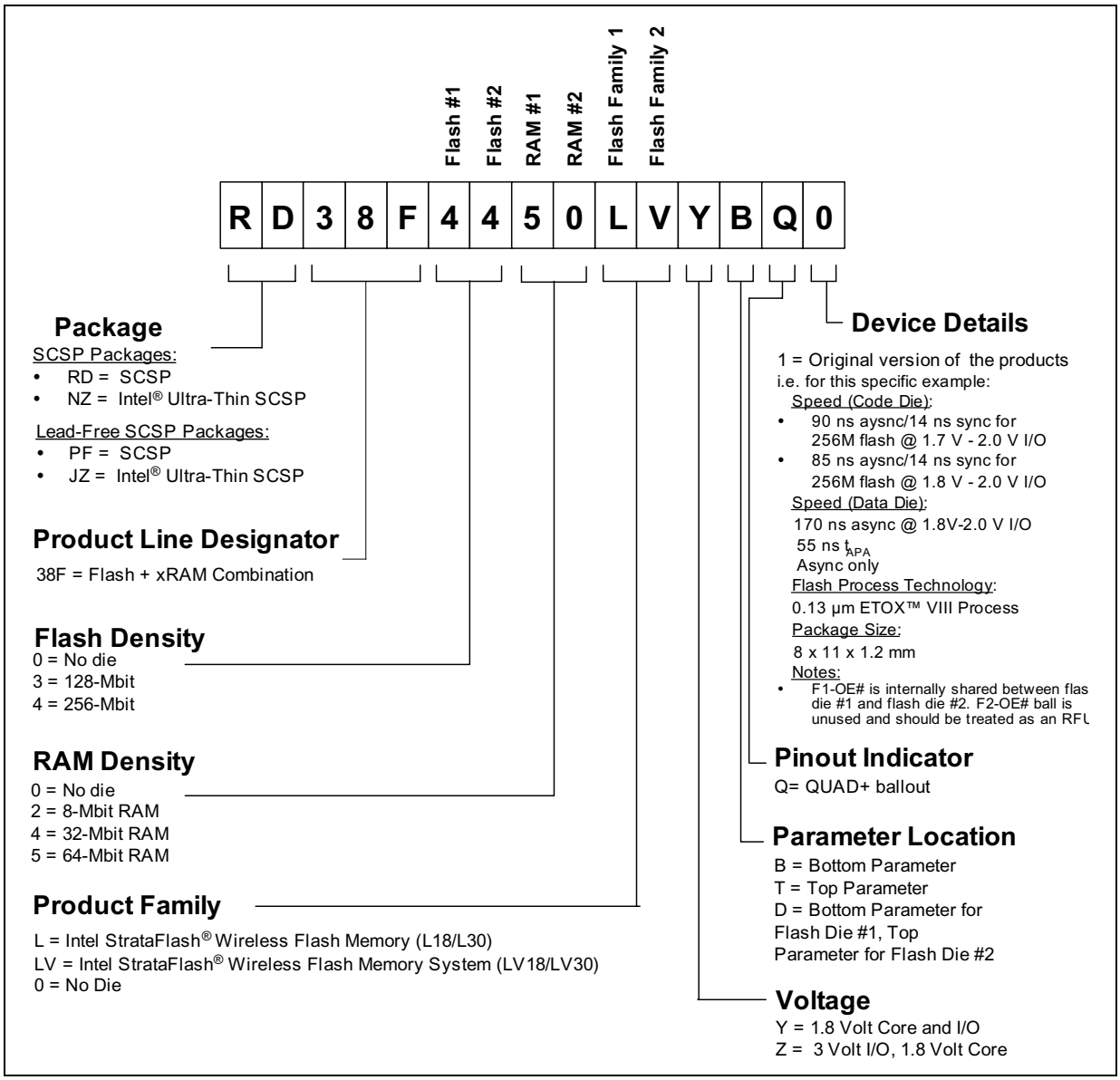


Table 22. Valid Combinations

I/O Voltage	Combinations with 128-Mbit Flash	Combinations with 256-Mbit Flash
1.8 V I/O	RD48F3000L0YTQ0	NZ48F4000L0YTQ0
	RD48F3000L0YBQ0	NZ48F4000L0YBQ0
	RD38F3040L0YTQ0	PF48F4000L0YTQ0*
	RD38F3040L0YBQ0	PF48F4000L0YBQ0*
		RD48F4400L0YDQ0
		PF48F4400L0YDQ0*
		RD38F4455LVYTQ0
		RD38F4455LVYBQ0
3.0 V I/O	RD48F3000L0ZTQ0	NZ48F4000L0ZTQ0
	RD48F3000L0ZBQ0	NZ48F4000L0ZBQ0
	RD38F3040L0ZTQ0	RD48F4400L0ZDQ0
	RD38F3040L0ZBQ0	RD38F4050L0ZBQ0
	RD38F3352LLZDQ0*	RD38F4050L0ZTQ0
	PF38F3352LLZDQ0*	

NOTE: * These are non-standard product line items and may not be productized.