S71NS128JA0/S71NS064JA0

Stacked Multi-Chip Product (MCP)
128 Megabit (8 M x 16-Bit) and 64 Megabit (4 M x 16-Bit), 110 nm CMOS 1.8 Volt-only Simultaneous Read/Write, Burst Mode Flash Memories with 16 Megabit (1M x 16-Bit) pSRAM

Data Sheet

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Publication Number S71NS-JA0_00 **Revision** A **Amendment** 6 **Issue Date** September 22, 2005

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Some data sheets will contain a combination of products with different designations (Advance Information, Preliminary, or Full Production). This type of document will distinguish these products and their designations wherever necessary, typically on the first page, the ordering information page, and pages with DC Characteristics table and AC Erase and Program table (in the table notes). The disclaimer on the first page refers the reader to the notice on this page.

Full Production (No Designation on Document)

When a product has been in production for a period of time such that no changes or only nominal changes are expected, the Preliminary designation is removed from the data sheet. Nominal changes may include those affecting the number of ordering part numbers available, such as the addition or deletion of a speed option, temperature range, package type, or V_{IO} range. Changes may also include those needed to clarify a description or to correct a typographical error or incorrect specification. Spansion LLC applies the following conditions to documents in this category:

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S71NS128JA0/S71NS064JA0

Stacked Multi-Chip Product (MCP)
128 Megabit (8 M x 16-Bit) and 64 Megabit (4 M x 16-Bit), 110 nm CMOS 1.8 Volt-only Simultaneous Read/Write, Burst Mode Flash Memories with 16 Megabit (1M x 16-Bit) pSRAM

Data Sheet

ADVANCE INFORMATION

Distinctive Characteristics

- **Single 1.8 volt read, program and erase (1.7 to 1.95 volt)**
- **Multiplexed Data and Address for reduced I/O count**
  - A15–A0 multiplexed as DQ15–DQ0
  - Addresses are latched by AVD# control input when CE# low
- **Simultaneous Read/Write operation**
  - Data can be continuously read from one bank while executing erase/program functions in other bank
  - Zero latency between read and write operations
- **Read access times at 54 MHz (C_L=30 pF)**
  - Burst access times of 13.5 ns at industrial temperature range
  - Asynchronous random access times of 70 ns
  - Synchronous random access times of 87.5 ns
- **Burst length**
  - Continuous linear burst
  - 8/16/32 word linear burst with wrap around
  - 8/16/32 word linear burst without wrap around
- **Power dissipation (typical values, 8 bits switching, C_L = 30 pF)**
  - Burst Mode Read: 25 mA
  - Simultaneous Operation: 40 mA
  - Program/Erase: 15 mA
  - Standby mode: 9 µA
- **Sector Architecture**
  - Four 8 Kword sectors
  - Two hundred fifty-five (S29NS128J) or one hundred twenty-seven (S29NS064J) 32 Kword sectors
  - Four banks
- **Sector Protection**
  - Software command sector locking
  - All sectors locked when $V_{PP} = V_{IL}$
- **Handshaking feature**
  - Provides host system with minimum possible latency by monitoring RDY
- **Supports Common Flash Memory Interface (CFI)**
- **Software command set compatible with JEDEC 42.4 standards**
  - Backwards compatible with Am29F and Am29LV families
- **Manufactured on 110 nm process technology**
- **Minimum 100,000 erase cycle guarantee per sector**
- **Cycling Endurance: 1 million cycles per sector typical**
- **Data Retention: 20 years typical**
- **Embedded Algorithms**
  - Embedded Erase algorithm automatically preprograms and erases the entire chip or any combination of designated sectors
  - Embedded Program algorithm automatically writes and verifies data at specified addresses
- **Data# Polling and toggle bits**
  - Provides a software method of detecting program and erase operation completion
- **Erase Suspend/Resume**
  - Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation
- **Hardware reset input (RESET#)**
  - Hardware method to reset the device for reading array data
- **CMOS compatible inputs and outputs**
- **Package**
  - **48-ball Very Thin FBGA (S71NS128JA0)**
  - **44-ball Very Thin FBGA (S71NS064JA0)**

Publication Number S71NS-JA0_00 **Revision** A **Amendment** 6 **Issue Date** September 22, 2005

Contents

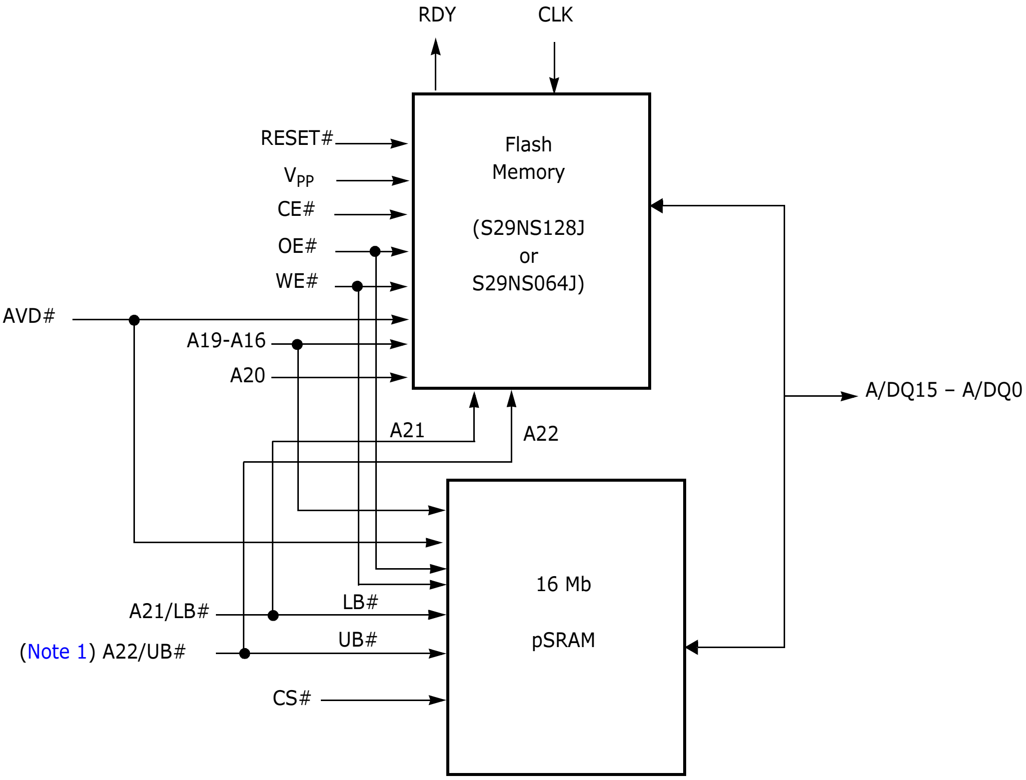
Tables

Figures

Product Selector Guide

	Part Number	**S71NS128JA0, S71NS064JA0**
	MCP Model Number	**01, 03, 11, 21, 23**
	Burst Frequency	**54 MHz**
Flash Memory	Flash Memory Device/Model Number	S29NS128J/00, S29NS064J/00
	Flash Speed Option	0L
	Max Initial Synchronous Access Time, ns (t_{IACC})	87.5
	Max Burst Access Time, ns (t_{BACC})	13.5
	Max Asynchronous Access Time, ns (t_{ACC})	70
	Max CE# Access Time, ns (t_{CE})	
	Max OE# Access Time, ns (t_{OE})	13.5
pSRAM	Max Access Time, ns (t_{ACC2})	90
	Max CE# Access Time, ns (t_{ACC3})	90
	Max OE# Access Time, ns (t_{OE})	50

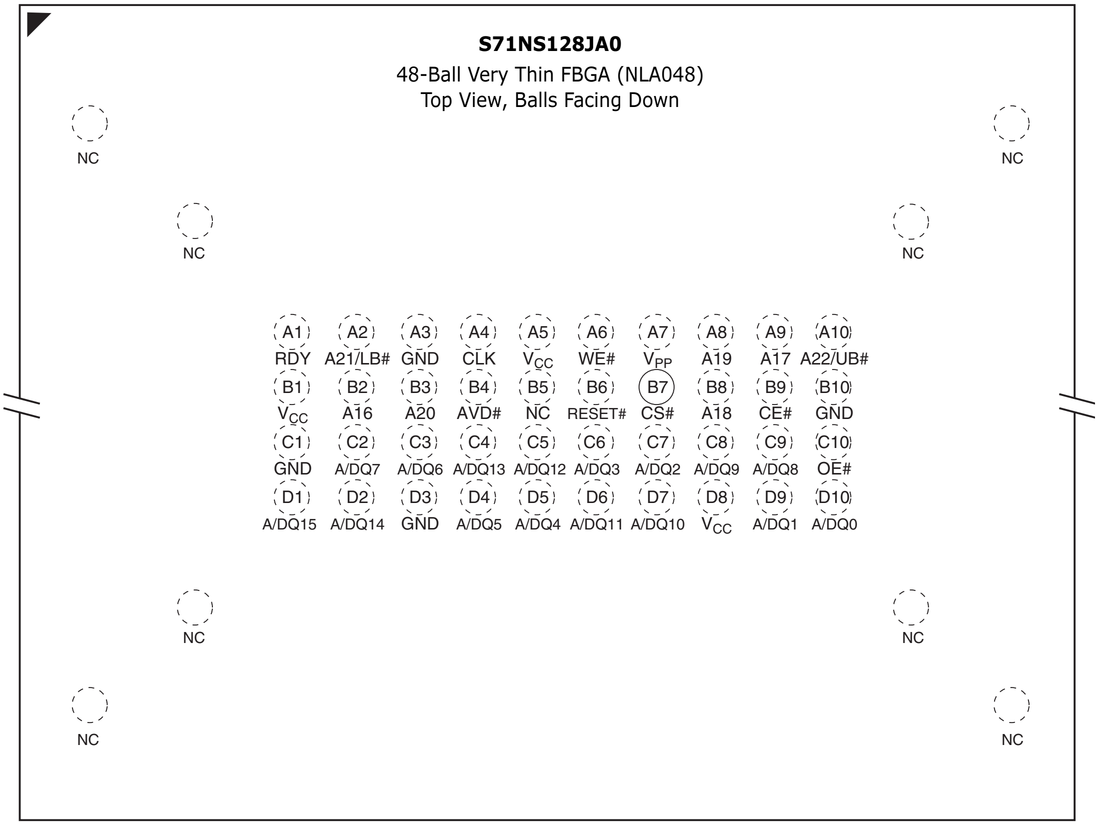
MCP Block Diagram



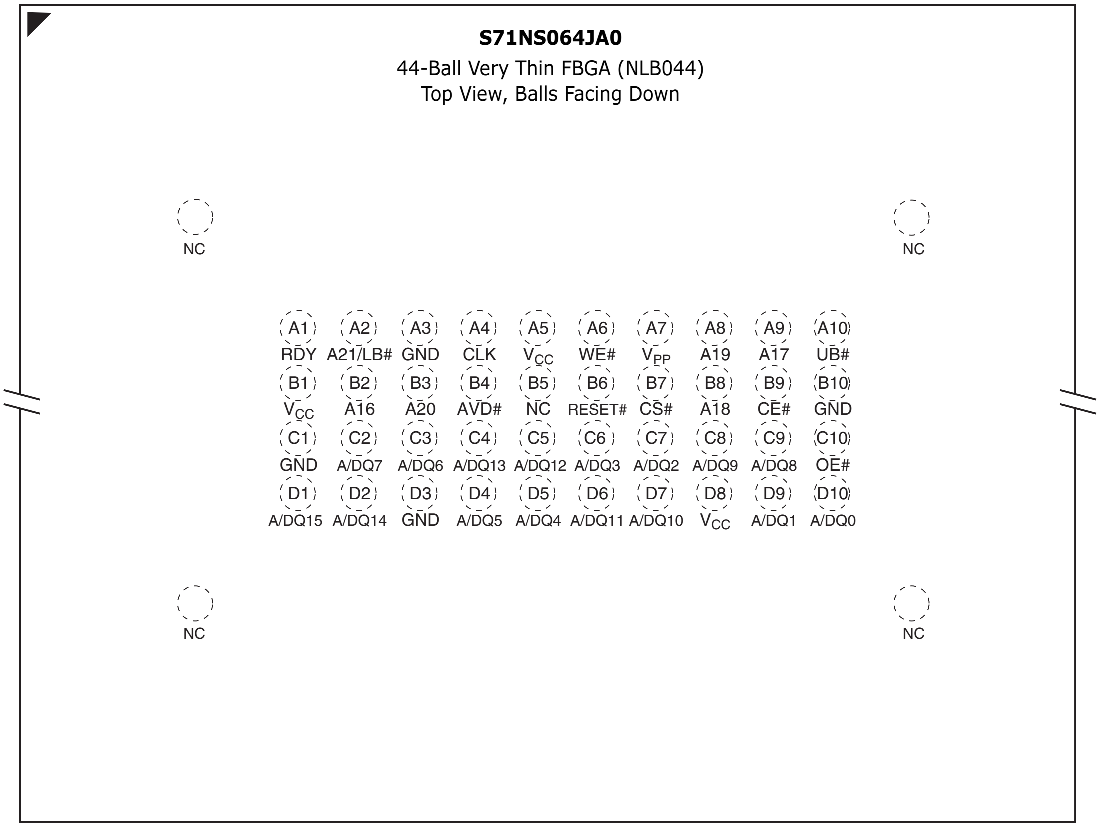
Notes:

1. *A22 available for 128 Mb Flash only*
2. *A15 – A0 are multiplexed with DQ15 – DQ0.*
3. *A_{MAX} indicates the highest order address bit.*

Connection Diagram



Connection Diagram



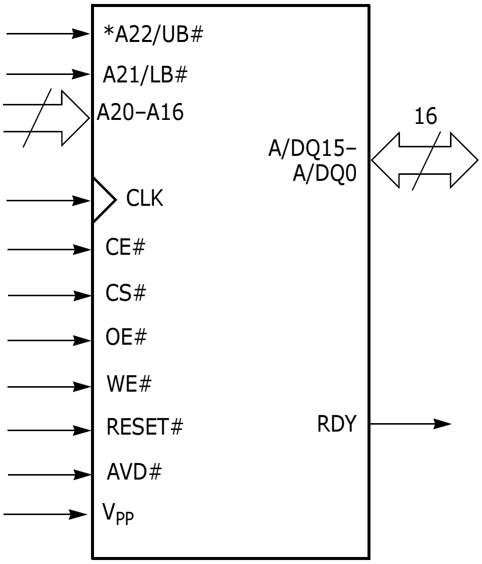
S71NS064JA0

44-Ball Very Thin FBGA (NLB044)
Top View, Balls Facing Down

Input/Output Descriptions

A22/UB# = Address Inputs, pSRAM Upper Byte Control (A22 available for 128 Mb Flash)
A21/LB# = Address Inputs, pSRAM Lower Byte Control
A20–A16 = Address Inputs
A/DQ15–A/DQ0 = Multiplexed Address/Data input/output
CS# = pSRAM Chip Select Input
CE# = Flash Chip Enable Input. Asynchronous relative to CLK for the Burst mode.
OE# = Output Enable Input. Asynchronous relative to CLK for the Burst mode.
WE# = Write Enable Input.
V_{CC} = Device Power Supply (1.7 V–1.95 V).
GND = Ground
NC = No Connect; not connected internally
RDY = Ready output; indicates the status of the Burst read. V_{OL}= data invalid.
CLK = Flash Clock input. The first rising edge of CLK in conjunction with AVD# low latches address input and activates burst mode operation. After the initial word is output, subsequent rising edges of CLK increment the internal address counter. CLK should remain low during asynchronous access.
AVD# = Address Valid input. Indicates to device that the valid address is present on the address inputs (address bits A15–A0 are multiplexed, address bits A22–A16 are address only).
V_{IL} = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched on rising edge of CLK.
V_{IH}= device ignores address inputs
RESET# = Hardware reset input. V_{IL}= device resets and returns to reading array data
V_{PP} = At 12 V, accelerates programming; automatically places device in unlock bypass mode. At V_{IL}, disables program and erase functions. Should be at V_{IH} for all other conditions.

Logic Symbol



*A22 available for 128Mb Flash only.

Ordering Information

The order number (Valid Combination) is formed by the following:

S71NS 128 J A0 BA W 01 0

PACKING TYPE

0 = Tray
2 = 7-inch Tape and Reel
3 = 13-inch Tape and Reel

ADDITIONAL ORDERING OPTIONS

01 = 54 MHz Flash, 90 ns, EMLSI pSRAM (E3)
03 = 54 MHz Flash, 90ns, EMLSI pSRAM (E4)
11 = 54 MHz Flash, 90 ns, Cypress pSRAM (C1)
21 = 54 MHz Flash, 90 ns, Micron pSRAM (M2)
23 = 54MHz Flash, 90 ns, Micron pSRAM (M3)

TEMPERATURE RANGE

W = Wireless (–25°C to +85°C)
For Industrial (–40°C to +85°C),
contact local sales office

PACKAGE TYPE

BA = Very Thin Fine-Pitch BGA
Lead (Pb)-Free Compliant Package
BF = Very Thin Fine-Pitch BGA
Lead (Pb)-Free Package
BJ = Very Thin Fine-Pitch BGA
Lead (Pb)-Free LF35 Package

pSRAM DENSITY

A0 = 16 Megabit (1M x 16-Bit)

FLASH PROCESS TECHNOLOGY

J = 110 nm Floating Gate Technology

FLASH DENSITY

128 = 128 Megabit (8 M x 16-Bit)
064 = 64 Megabit (4 M x 16-Bit)

DEVICE FAMILY

S71NS = Stacked Multi-Chip Product,
Simultaneous Read/Write, Burst Mode Flash Memory with Multiplexed I/O
1.8-Volt Operation, Top Boot Sectors, and pSRAM

Valid Combinations

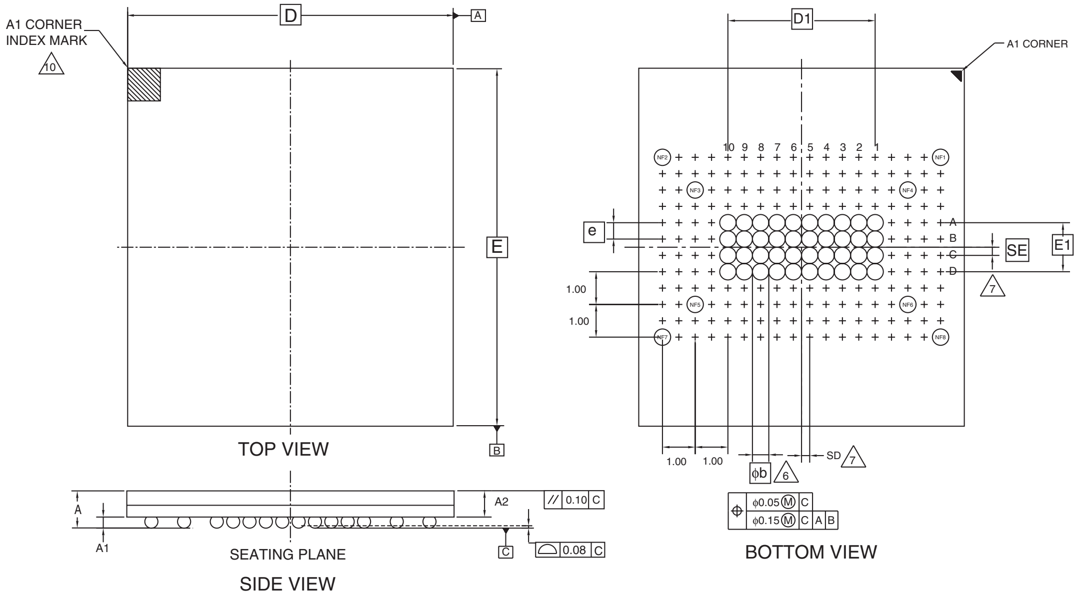
The following configurations are planned to be supported for this device. Consult the local sales office to confirm availability of specific valid combinations and to check on newly released combinations

Valid Combinations							
S71NS	128	J	A0	BA, BF, BJ	W	01, 03, 11, 21, 23	0, 2, 3
	064						

Note: *BGA package marking omits leading S and packing type designator from ordering part number.*

Physical Dimensions–S71NS128JA0

NLA048—48-Ball Very Thin Fine-Pitch Ball Grid Array (FBGA) 10 x 11 mm Package



PACKAGE	NLA 048			NOTE
JEDEC	N/A			
	9.95 mm x 10.95 mm NOM PACKAGE			
SYMBOL	MIN	NOM	MAX	
A	1.05	---	1.20	OVERALL THICKNESS
A1	0.20	---	---	BALL HEIGHT
A2	0.85	0.91	0.97	BODY THICKNESS
D	9.85	9.95	10.05	BODY SIZE
E	10.85	10.95	11.05	BODY SIZE
D1	4.50 BSC.			BALL FOOTPRINT
E1	1.50 BSC.			BALL FOOTPRINT
MD	10			ROW MATRIX SIZE D DIRECTION
ME	4			ROW MATRIX SIZE E DIRECTION
N	48			TOTAL BALL COUNT
φb	0.25	0.30	0.35	BALL DIAMETER
e	0.50 BSC.			BALL PITCH
SD / SE	0.25 BSC.			SOLDER BALL PLACEMENT
	---			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010 (EXCEPT AS NOTED).
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION.

   N IS THE TOTAL NUMBER OF SOLDER BALLS.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW PARALLEL TO THE D OR E DIMENSION, RESPECTIVELY, SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. NOT USED.
9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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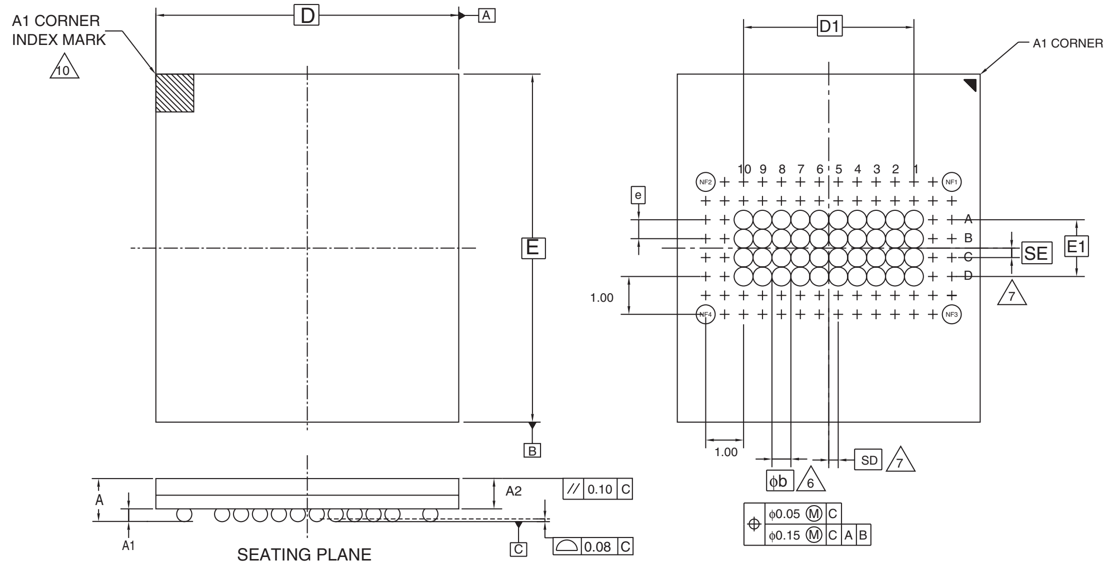
Note: *For reference only. BSC is an ANSI standard for Basic Space Centering*

Physical Dimensions–S71NS064JA0

NLB044—44-Ball Very Thin Fine-Pitch Ball Grid Array (FBGA) 9.2 x 8 mm Package



PACKAGE	NLB 044			NOTE
JEDEC	N/A			
	8.00 mm x 9.20 mm NOM PACKAGE			
SYMBOL	MIN	NOM	MAX	
A	1.05	---	1.20	OVERALL THICKNESS
A1	0.20	---	---	BALL HEIGHT
A2	0.85	0.91	0.97	BODY THICKNESS
D	7.90	8.00	8.10	BODY SIZE
E	9.10	9.20	9.30	BODY SIZE
D1	4.50 BSC.			BALL FOOTPRINT
E1	1.50 BSC.			BALL FOOTPRINT
MD	10			ROW MATRIX SIZE D DIRECTION
ME	4			ROW MATRIX SIZE E DIRECTION
N	44			TOTAL BALL COUNT
φb	0.25	0.30	0.35	BALL DIAMETER
e	0.50 BSC.			BALL PITCH
SD / SE	0.25 BSC.			SOLDER BALL PLACEMENT
	---			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010 (EXCEPT AS NOTED).
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION.

   N IS THE TOTAL NUMBER OF SOLDER BALLS.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW PARALLEL TO THE D OR E DIMENSION, RESPECTIVELY, SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. NOT USED.
9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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Note: *For reference only. BSC is an ANSI standard for Basic Space Centering*

Device History

Device/Model Number	Visual ID: Package Marking	Electrical ID: Extended Code (Hex)	Major Reasons(s) for Change
128+16 EMLSI			
S71NS128JA0BAW00	1ES	712Eh	ES, EMLSI2 (85ns die), 66MHz tCCS and tAVDH timing update
S71NS128JA0BAW01	1ES	711Eh	ES, EMLSI2 (85ns die), 54MHz tCCS and tAVDH timing update
S71NS128JA0BFW01	2E3ES	711Dh	ES, EMLSI3 (85ns die), 54MHz Fixed byte write operation
S71NS128JA0BFW01	2E3S	7111h	**Production release,** EMLSI3 (85ns die), 54MHz Fixed byte write operation
S71NS128JA0BAW02	3E4ES	712Ch	ES, EMLSI4 (70ns die), 54MHz New 70ns die to replace EOL 85ns die
S71NS128JA0BFW02			
S71NS128JA0BFW03	3E4S	7111h	**Production release**, EMLSI4 (70ns die), 54MHz New 70ns die to replace EOL 85ns die
128+16 Micron			
S71NS128JA0BAW21		711Dh	ES, Micron2 (85ns die), 54MHz
S71NS128JA0BFW21			
S71NS128JA0BAW21	3M2S	7111h	**Production release**, Micron2 (85ns die), 54MHz
S71NS128JA0BFW21			
S71NS128JA0BFW23	3M3ES	711Bh	ES, Micron3 (70ns die), 54MHz New 70ns die to replace EOL 85ns die
S71NS128JA0BFW23	3M3S	7111h	**Production release**, Micron3 (70ns die), 54MHz New 70ns die to replace EOL 85ns die
64+16 EMLSI			
S71NS064JA0BAW01	1E3ES	711Eh	ES, EMLSI3 (85ns die), 54MHz Fixed byte write operation
S71NS064JA0BFW01	1E3S	7111h	**Production release**, EMLSI3 (85ns die), 54MHz Fixed byte write operation
S71NS064JA0BAW02	2E4ES	712Dh	ES, EMLSI4 (70ns die), 54MHz New 70ns die to replace EOL 85ns die
S71NS064JA0BFW02			
S71NS064JA0BFW03	2E4S	7111h	**Production release**, EMLSI4 (70ns die), 54MHz New 70ns die to replace EOL 85ns die
64+16 Micron			
S71NS064JA0BAW21	1ES	711Eh	ES, Micron2 (85ns die), 54MHz
S71NS064JA0BFW21			
S71NS064JA0BAW21	2M2S	7111h	**Production release**, Micron2 (85ns die), 54MHz
S71NS064JA0BFW21			
S71NS064JA0BFW23	2M3ES	711Ch	ES, Micron3 (70ns die), 54MHz New 70ns die to replace EOL 85ns die
S71NS064JA0BFW23	2M3S	7111h	**Production release,** Micron3 (70ns die), 54MHz New 70ns die to replace EOL 85ns die

Note: *Underlined values are tentative as of the date of data sheet publication.*

Appendix A: Daisy Chain Information

Daisy Chain Part Number	Package Marking	Daisy Chain Connection	Spansion 128/16Mb MCP Part Number	Flash Description
Lead (Pb) - Free Compliant: S99DCNLA048MSA002	99DCNLA048MSA00	Substrate	S71NS128JA0	128-Mbit 110nm Flash 16-Mbit pSRAM
Lead (Pb) - Free: S99DCNLA048MSF002	99DCNLA048MSF00			

Component Type/Name	NLA048
Solder resist opening	0.25 ± 0.05 mm
Daisy Chain Connection Level	On Substrate
Lead-Free Compliant	Yes
Quantity per Reel	550 (300 units per reel by special request to factory)

C1 – D1	C6 – D6	A10 – B10	A5 – B5
C2 – D2	C7 – D7	A9 – B9	A4 – B4
C3 – D3	C8 – D8	A8 – B8	A3 – B3
C4 – D4	C9 – D9	A7 – B7	A2 – B2
C5 – D5	C10 – D10	A6 – B6	A1 – B1
On substrate			
NF1 – NF4		NF2 – NF5	
NF16 – NF19		NF17 – NF20	

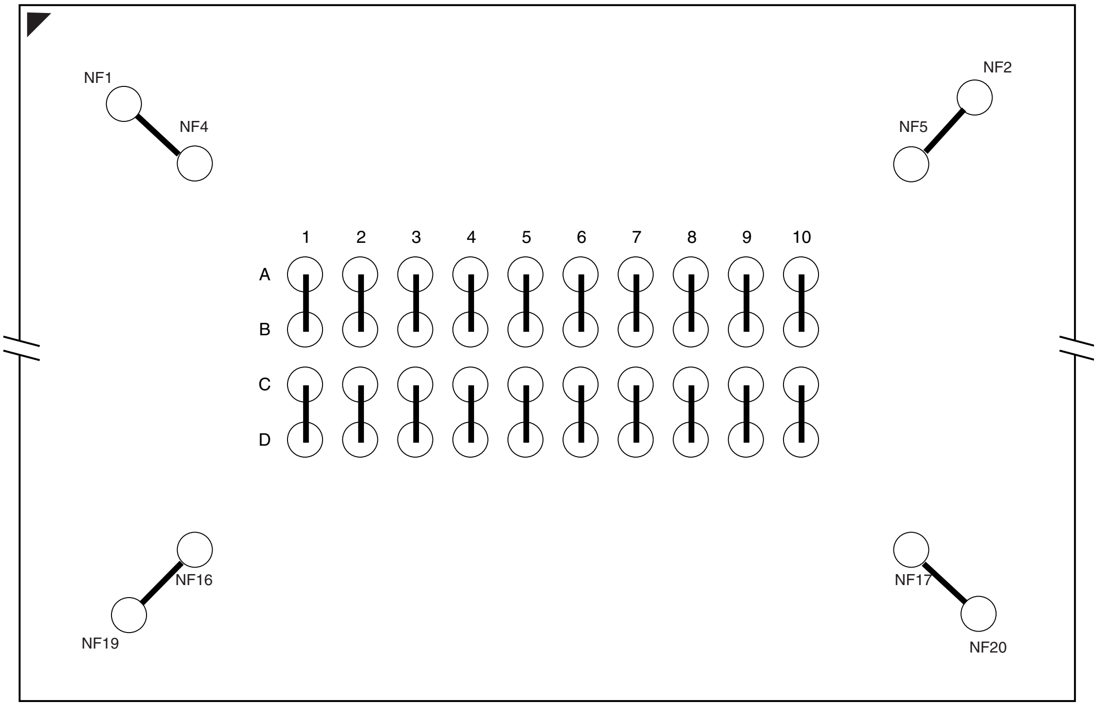


Figure 1 NLA048 Daisy Chain Layout (Top View, Balls Facing Down)

Appendix B: Daisy Chain Information

Daisy Chain Part Number	Package Marking	Daisy Chain Connection	Spansion 128/16Mb MCP Part Number	Flash Description
Lead (Pb) - Free Compliant: S99DCNLB044MSA002	99DCNLB044MSA00	Substrate Level	S71NS064JA0	64-Mbit 110nm Flash 16-Mbit pSRAM
Lead (Pb)- Free: S99DCNLB044MSF002	99DCNLB044MSF00			

Component Type/Name	NLB044
Solder resist opening	0.25 ± 0.05 mm
Daisy Chain Connection Level	On Substrate
Lead-Free Compliant	Yes
Quantity per Reel	600 (300 units per reel by special request to factory)

C1 – D1	C6 – D6	A10 – B10	A5 – B5
C2 – D2	C7 – D7	A9 – B9	A4 – B4
C3 – D3	C8 – D8	A8 – B8	A3 – B3
C4 – D4	C9 – D9	A7 – B7	A2 – B2
C5 – D5	C10 – D10	A6 – B6	A1 – B1
On substrate			
NF1 – NF3		NF2 – NF4	

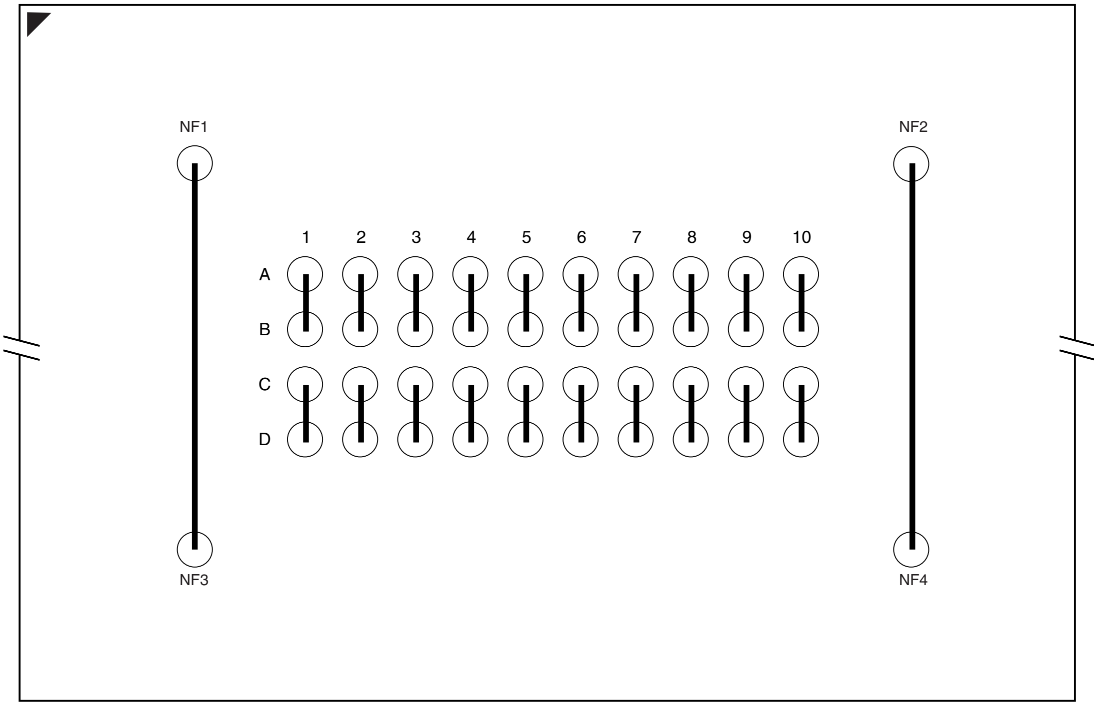


Figure 2 NLB044 Daisy Chain Layout (Top View, Balls Facing Down)

pSRAM Characteristics

pSRAM Device Bus Operations

CS#	OE#	WE#	LB#	UB#	AVD#	A[19-16]	A/DQ [15 – 0]	Mode	Power
H	X	X	X	X	X	X	HIGH-Z	Deselected	Standby
L	H	H	X	X	H	X	HIGH-Z	Output Disabled	Active
L	X	X	H	H	X	X	HIGH-Z	Output Disabled	Active
L	H	L	H	H	H	X	Data In	Configuration Register Write Access	Active
L	L	H	H	H	H	X	Data Out	Configuration Register Read Access	Active
L	H	H	H	H	L	Addr In	Addr In	Address Input	Active
L	L	H	L	H	H	X	Data Out	Lower Byte Read	Active
L	L	H	H	L	H	X	Data Out	Upper Byte Read	Active
L	L	H	L	L	H	X	Data Out	Word Read	Active
L	H	L	L	H	H	X	Data In	Lower Byte Write	Active
L	H	L	H	L	H	X	Data In	Upper Byte Write	Active
L	H	L	L	L	H	X	Data In	Word Write	Active

Legend: *L= Logic0, H= Logic1, X= Don't care*

pSRAM DC Characteristics

Symbol	Item	Test Conditions	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$V_{IN} = V_{SS}$ to V_{CC}	-1		1	µA
I_{LO}	Output Leakage Current	CS# = V_{IH} or OE# = V_{IH} or WE# = V_{IL}, $V_{IO} = V_{SS}$ to V_{CC}	-1		1	µA
I_{CC1}	Average Operating Current	Cycle Time = 1 µs, 100% duty, I_{IO} = 0 mA, CS# $\leq$ 0.2 V, $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$–0.2V			3	mA
I_{CC2}		Cycle Time = Min, I_{IO} = 0 mA, 100% duty, CS# = V_{IL}, $V_{IN} = V_{IH}$ or V_{IL}			25	mA
V_{OL}	Output Low Voltage	I_{OL} = 0.1 mA			0.1	V
V_{OH}	Output High Voltage	I_{OH} = -0.1 mA	$V_{CC}Q$–0.1 V			V
I_{SB1}	Standby Current (CMOS)	CS# $\geq V_{CC}$–0.2V, Other Inputs = 0~V_{CC}			60	µA

pSRAM AC Characteristics

Parameter List		Symbol	70 ns		90 ns		Units
			Min	Max	Min	Max	
Common	AVD# Low Pulse	t_{AVD}	15	1000	20		ns
	Address setup to AVD# rising edge	t_{AVDS}	15		20		ns
	Address hold from AVD# rising edge	t_{AVDH}	5		5		ns
	Chip enable setup to AVD# rising edge	t_{CSS}	7		10		ns
Read	AVD# low to Data Valid time	t_{ACC1}	70			90	ns
	Address access time	t_{ACC2}	70			90	ns
	Chip Enable to data output	t_{ACC3}	70			90	ns
	Address disabled to output enable	t_{ADOE}	0		0		ns
	Output enable to valid output	t_{OE}	25			50	ns
	UB#, LB# enable to data output	t_{UBLBA}	25			40	ns
	UB#, LB# enable to Low-Z output	t_{BLZ}	5		15		ns
	Output enable to Low-Z output	t_{OLZ}	5		15		ns
	Chip disable to High-Z output	t_{HZ}		15		20	ns
	UB#, LB# disable to High-Z output	t_{BHZ}		15		15	ns
	Output disable to High-Z output	t_{OHZ}		15		15	ns
Write	AVD# low to end of write	t_{ACW1}	70			90	ns
	Address valid to end of write	t_{ACW2}	70			90	ns
	Chip enable to end of write	t_{ACW3}	70			90	ns
	Write pulse low	t_{WRL}	45		70		ns
	UB#, LB# valid to end of write	t_{BW}	50		70		ns
	Data to write time overlap	t_{DW}	25		35		ns
	Data hold from write time	t_{DH}	0		0		ns

pSRAM Characteristics

pSRAM Device Operation

The access is performed in two stages. The first stage is address latching. The first stage takes place between points A and B in timing diagram. At this stage, the Chip Select (CS#) to the device is asserted. The random access is enabled either from the point the address becomes stable, the falling edge of the AVD# signal or from the falling edge of the last CS# signal.

The second stage is the read or write access. This takes place between points B and C in timing diagram. In case of read access, the multiplexed address/ data bus A/DQ[15-0] changes its direction. It is important to notice t_{OE} when it is dominant that the device gets into the read cycle since the address is available long before the device output is enabled.

pSRAM Read Access

The read access (See Figure 5 and Figure 6) is initiated by applying the address to the multiplexed address/data bus A/DQ[15-0] and address bus A[19-16]. When the address is stable, the device chip select (CS#) is set active low. At point A, the AVD# signal is taken low and the latch becomes transparent. This allows the address to be propagated to the memory array. The address is stable at the rising edge of the AVD# signal. The AVD# signal goes high at point B in which the address latch is completed. At this point the read cycle is entered. The OE# signal is set active low. This changes the direction of the bus. The status of control signals UB# and LB# is set according to the access. Data is read at point C.

pSRAM Write Access

The write access (Figure 7 and Figure 8) is initiated by applying the address to the multiplexed address/data bus A/DQ[15-0] and the address bus A[19-16]. When the address is stable, the device chip select (CS#) is asserted active low. At point A, the AVD# signal is taken low and the latch becomes transparent. This allows the address to be propagated to the memory array. The address is stable at the rising edge of the AVD# signal. The AVD# signal goes high at point B in which the address latch is completed. At this point, the second stage of the write process is entered. Data is input to the multiplexed address/data bus. The WE# signal is set low and control signals UB# and LB# are set according to the access.

Configuration Register Access

A configuration register is needed to control the different modes of the RAM. The configuration register consists of 16 bits and it can be accessed when LB# and UB# signals are de-asserted. The AVD# signal is not used during configuration access. Configuration registers read access is shown in Figure 3 and write accesses in Figure 4.

The configuration registers bits are specified in Table 1. Writing to bits 15 - 8, does not change the device operation in normal mode.

pSRAM Characteristics

Configuration Register Access (Continued)

Table 1 Configuration Register

Bit Number	Definition	Remarks
15 – 8	Don't use in normal mode	
7 – 4	Reserved for future use	
3 – 2	Reduced memory size	00 = Full array 01 = 1/2 array 10 = 1/4 array 11 = 1/8 array
1 – 0	Temperature	00 = Internal temperature sensing

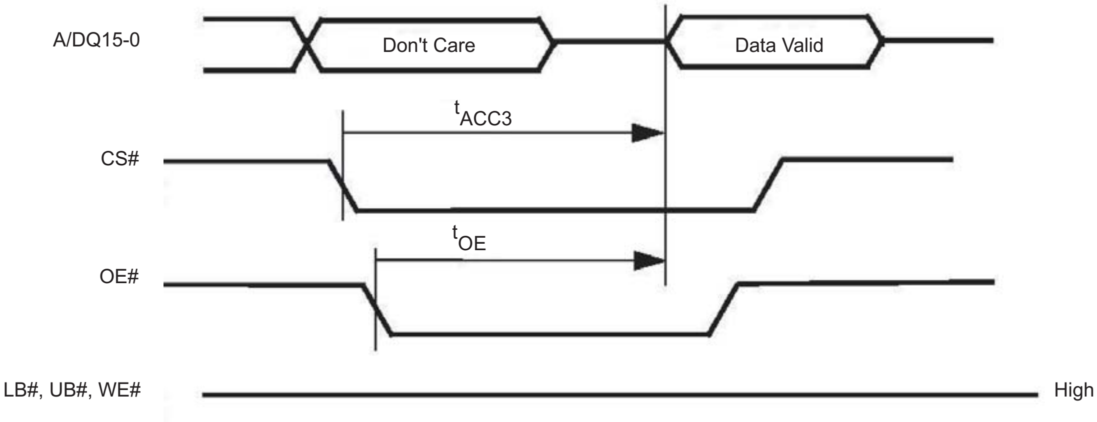


Figure 3 Configuration Register Read Access

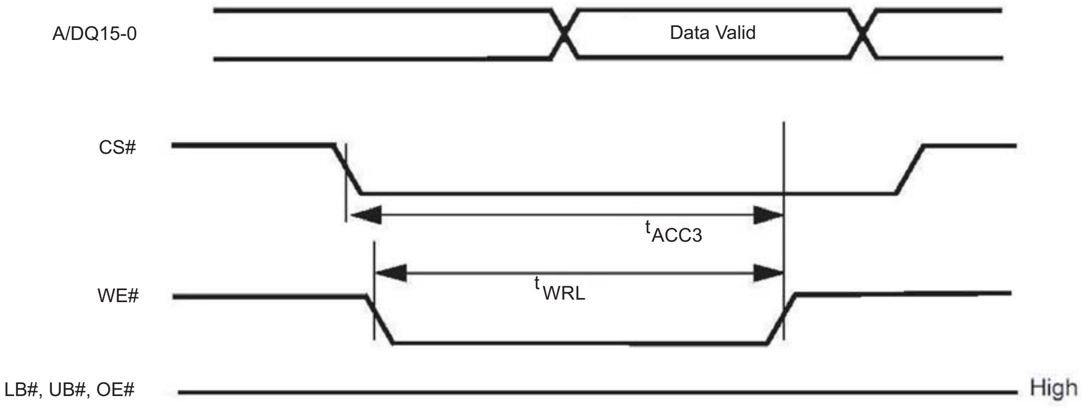


Figure 4 Configuration Register Write Access

pSRAM Characteristics

pSRAM Read Access Timing Diagrams

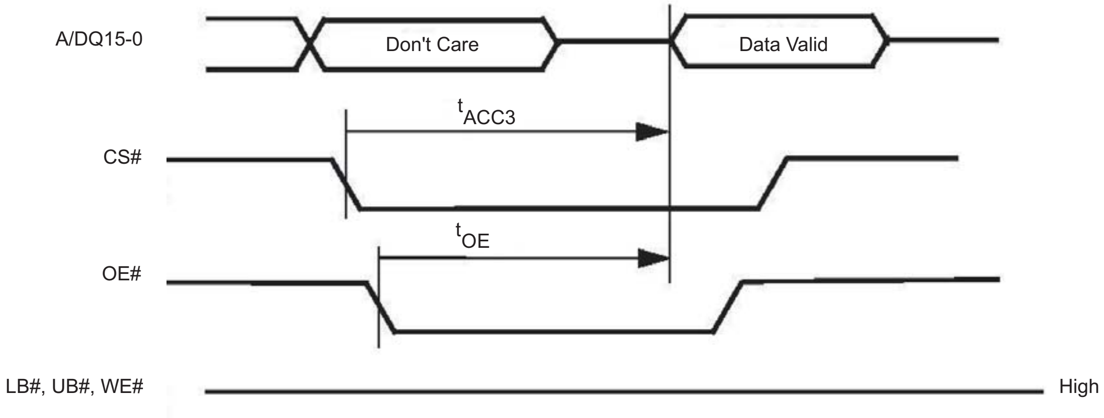
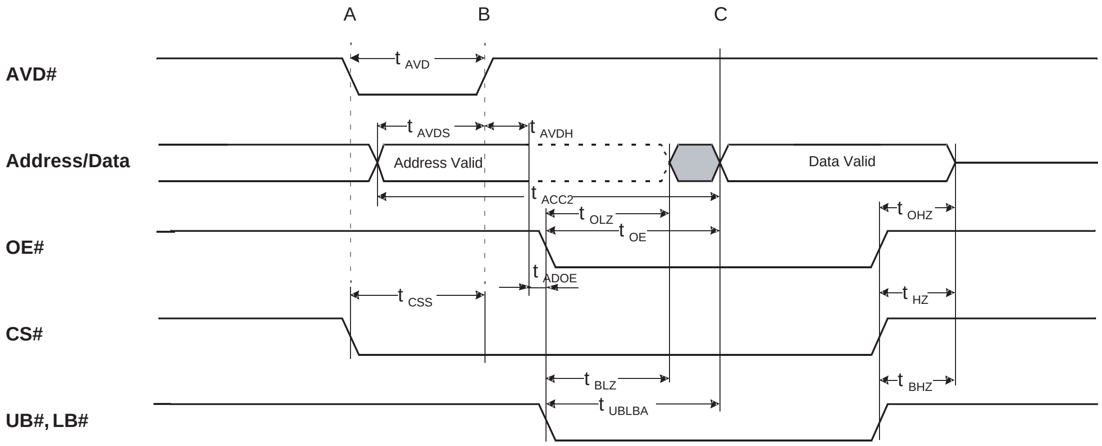


Figure 5 pSRAM Read Cycle 1 (WE# = V_{IH})



Notes:

1. *To have t_{OE} = t_{UBLBA} = 50 ns, time for the AVD# rising edge to OE# low and that for AVD# rising edge to UB#/LB# low must be over 30 ns at least.*
2. *If invalid address signals shorter than min. t_{ACC} are continuously repeated for over 4 µs, the device needs a normal read timing (t_{ACC}) or needs to sustain standby state for min. t_{ACC} at least once in every 4 µs.*

Figure 6 pSRAM Read Cycle 2 (WE# = V_{IH})

pSRAM Characteristics

pSRAM Write Access Timing Diagrams

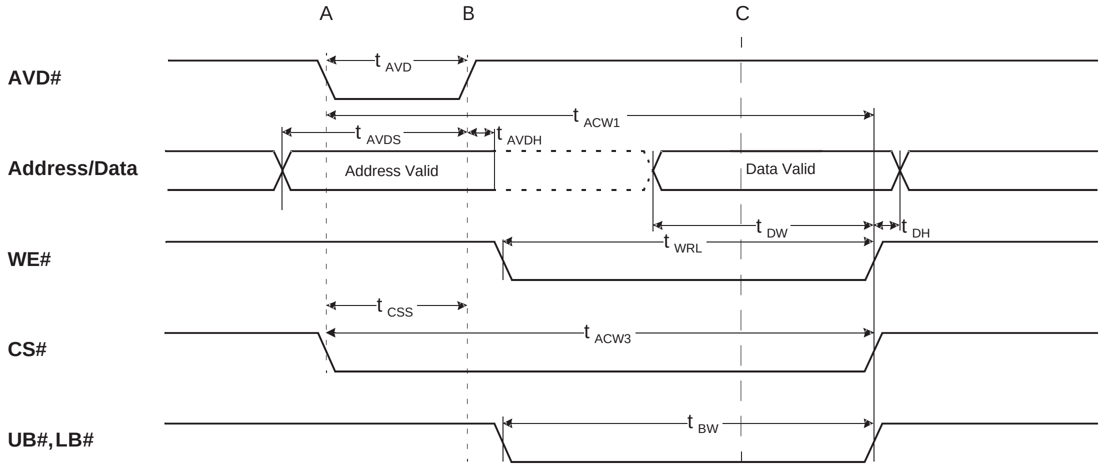
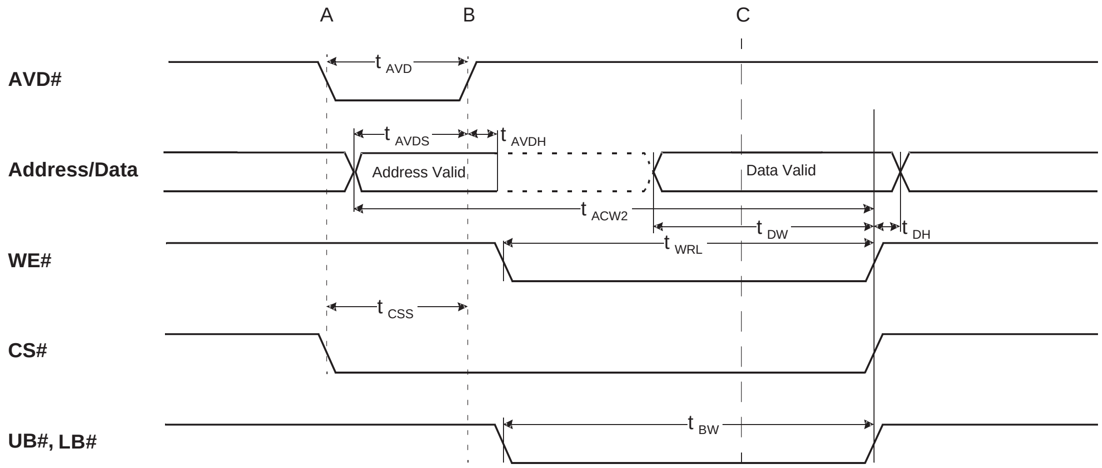


Figure 7 pSRAM Write Cycle 1 (OE# = V_{IH})



Note:
A write occurs during the 9overlap (t_{WRL}) of low CS#, low WE# and low UB# or LB#. A write begins at the last transition among low CS# and low WE# with asserting UB# or LB# low for single byte operation or simultaneously asserting UB# and LB# low for word operation. A write ends at the earliest transition among high CS# and high WE#. The t_{WRL} is measured from the beginning of write to the end of write.

Figure 8 pSRAM Write Cycle 2 (OE# = V_{IH})

Revision Summary

Revision A0 (December 8, 2003)

Initial Release.

Revision A1 (February 5, 2004)

Global: Converted datasheet to Preliminary to Advanced.

Product Selector Guide: Added additional MCP Model Numbers.

Ordering Information: Updated Ordering options to reflect new Model Numbers. Added new Valid Combinations and Package Markings to table.

Device History: Updated to reflect addition of Model Numbers.

pSRAM Device Bus Operations: Added two rows for Configuration Register Read/Write Access Mode.

Revision A2 (May 7, 2004)

Distinctive Characteristics: Added cycling endurance and data retention information.

Revision A3 (November 17, 2004)

Packing Type: Packing types added.

Revision A4 (March 21, 2005)

Product Selection Guide: Added MCP Model Numbers

pSRAM Characteristics: AC and DC characteristics updated

Ordering Information: updated

Device History: Updated

Revision A5 (August 3, 2005)

Product Selection Guide: Removed 66MHz ordering options

Ordering Information: Added ordering options for new EMLSI and Micron pSRAM die. Removed 66MHz ordering options.

Device History: Updated

Revision A6 (September 22, 2005)

Ordering Information

Added LF35 Package Type

Valid Combinations

Updated to include the new package type option

Colophon

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